C3M0016120U2

1200V 16mΩ Silicon Carbide Power MOSFET
N-Channel Enhancement Mode

Features

- Industry standard Top Side Cooled (TSC) Package
- High power dissipation capability
- Optimized package with separate driver source pin
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery (Q_{rr})
- Halogen free, RoHS compliant

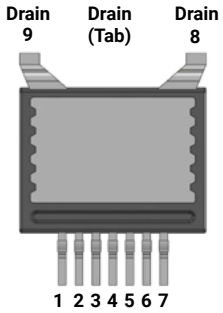
Benefits

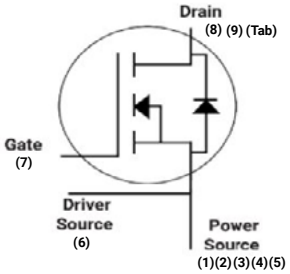
- Increase power density
- Reduce cooling requirements
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Increase system switching frequency

Typical Applications

- EV Chargers
- Solar/ESS
- Motor Control
- Industrial Power Supplies
- High Voltage DC/DC Converters

Package





Orderable Part Number	Package	Marking
C3M0016120U2-TR	U2	C3M0016120U2

Key Parameters

Parameter	Symbol	Min.	Typ.	Max	Unit	Conditions	Note
Drain - Source Voltage	V_{DS}			1200	v	T_C = 25°C	
Maximum Gate - Source Voltage	$V_{GS(max)}$	-8		+19		Transient	
Operational Gate-Source Voltage	$V_{GS\ op}$		-4/15			Static	Note 1
DC Continuous Drain Current	I_D			140	A	V_{GS} = 15 V, T_C = 25 °C, T_J ≤175 °C	Fig. 19 Note 2
				101		V_{GS} = 15 V, T_C = 100 °C, T_J ≤175 °C	
Pulsed Drain Current	I_{DM}			562		t_{Pmax} limited by T_{jmax} V_{GS} = 15V, T_C = 25 °C	Fig. 22
Power Dissipation	P_D			607	W	T_C = 25 ˚C, T_J = 175 °C	Fig. 20
Operating Junction and Storage Temperature	T_J, T_{stg}			-55 to +175	°C		
Solder Temperature	T_L			260		According to JEDEC J-STD-020	

Note (1): Recommended turn-on gate voltage is 15V with ±5% regulation tolerance, see Application Note PRD-04814 for additional details
Note (2): Verified by design

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Electrical Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	1200			V	V_{GS} = 0 V, I_D = 100 μA	
$V_{GS(th)}$	Gate Threshold Voltage	1.8	2.5	3.8	V	V_{DS} = V_{GS}, I_D = 22.08 mA	Fig. 11
			2.1			V_{DS} = V_{GS}, I_D = 22.08 mA, T_J = 175ºC	
I_{DSS}	Zero Gate Voltage Drain Current		1	50	μA	V_{DS} = 1200 V, V_{GS} = 0 V	
I_{GSS}	Gate-Source Leakage Current		10	250	nA	V_{GS} = 15 V, V_{DS} = 0 V	
$R_{DS(on)}$	Drain-Source On-State Resistance		16	22	mΩ	V_{GS} = 15 V, I_D = 80.3 A	Fig. 4, 5, 6
			29			V_{GS} = 15 V, I_D = 80.3 A, T_J = 175ºC	
g_{fs}	Transconductance		54		S	V_{DS}= 20 V, I_{DS}= 80.3 A	Fig. 7
			49			V_{DS}= 20 V, I_{DS}= 80.3 A, T_J = 175ºC	
C_{iss}	Input Capacitance		6922		pF	V_{GS} = 0 V, V_{DS} = 0V to 1000 V F = 100 kHz V_{AC} = 25 mV	Fig. 17, 18
C_{oss}	Output Capacitance		231				
C_{rss}	Reverse Transfer Capacitance		13				
E_{oss}	C_{oss} Stored Energy		127		μJ		Fig. 16
$C_{o(er)}$	Effective Output Capacitance (Energy Related)		268		pF	V_{GS} = 0 V, V_{DS} = 0... 800V	Note: 3
$C_{o(tr)}$	Effective Output Capacitance (Time Related)		404				
E_{ON}	Turn-On Switching Energy (MOSFET FWD)		1175		μJ	V_{DS}= 800 V, V_{GS}= -4 V/15 V, I_D= 80.3 A, $R_{G(ext)}$ = 2.5 Ω, L= 99 μH, T_J = 175ºC FWD = Internal Body Diode	Fig. 26, 28
E_{OFF}	Turn-Off Switching Energy (MOSFET FWD)		570				
$t_{d(on)}$	Turn-On Delay Time		18		ns	V_{DD} = 800 V, V_{GS} = -4 V/15 V I_D = 80.3 A, $R_{G(ext)}$ = 2.5 Ω, Timing relative to V_{DS} Inductive load	Fig. 27, 28
t_r	Rise Time		26				
$t_{d(off)}$	Turn-Off Delay Time		62				
t_f	Fall Time		14				
$R_{G(int)}$	Internal Gate Resistance		2.6		Ω	f = 1 MHz	
Q_{gs}	Gate to Source Charge		70		nC	V_{DS} = 800 V, V_{GS} = -4 V/15 V I_D = 80.3 A Per IEC60747-8-4 pg 21	Fig. 12
Q_{gd}	Gate to Drain Charge		65				
Q_g	Total Gate Charge		223				

Note (3): $C_{o(er)}$, a lumped capacitance that gives same stored energy as Coss while Vds is rising from 0 to 800V
$C_{o(tr)}$, a lumped capacitance that gives same charging time as Coss while Vds is rising from 0 to 800V

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Reverse Diode Characteristics (T_C = 25˚C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V_{SD}	Diode Forward Voltage	4.9		V	V_{GS} = -4 V, I_{SD} = 40.1 A, T_J = 25 °C	Fig. 8, 9, 10
		4.4			V_{GS} = -4 V, I_{SD} = 40.1 A, T_J = 175 °C	
I_S	Continuous Diode Forward Current		105	A	V_{GS} = -4 V, T_C = 25˚C	
I_{SM}	Diode pulse Current		562		V_{GS} = -4 V, pulse width t_P limited by T_{jmax}	
t_{rr}	Reverse Recovery time	25		ns	V_{GS} = -4 V, I_{SD} = 80.3 A, V_R = 800 V dif/dt = 7751 A/μs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	1905		nC		
I_{rrm}	Peak Reverse Recovery Current	117		A		
t_{rr}	Reverse Recovery time	43		ns	V_{GS} = -4 V, I_{SD} = 80.3 A, V_R = 800 V dif/dt = 2622 A/μs, T_J = 175 °C	
Q_{rr}	Reverse Recovery Charge	1402		nC		
I_{rrm}	Peak Reverse Recovery Current	50		A		

Thermal Characteristics

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
$R_{\theta JC}$	Thermal Resistance from Junction to Case	0.19	0.25	°C/W		Fig. 21

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Typical Performance

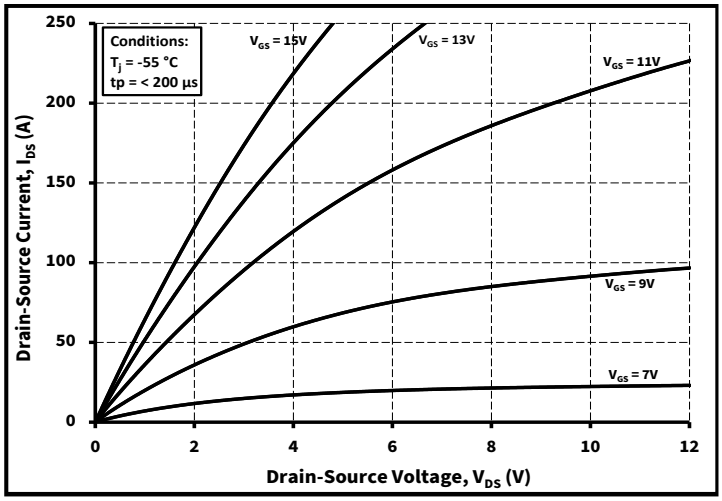

Figure 1. Output Characteristics T_J = -55 ºC

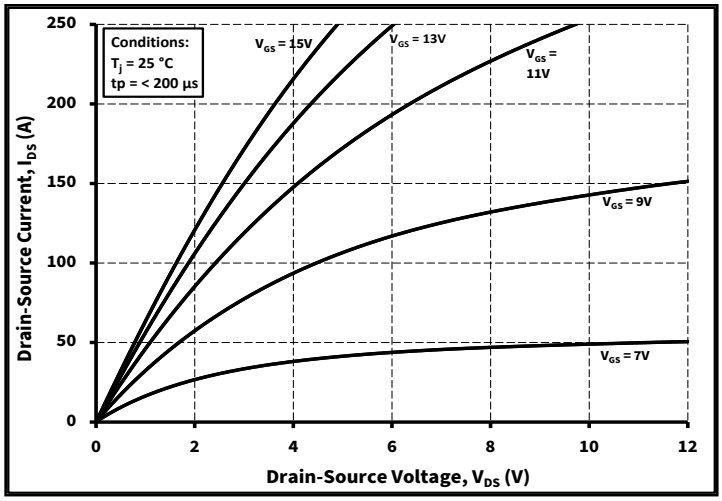

Figure 2. Output Characteristics T_J = 25 ºC

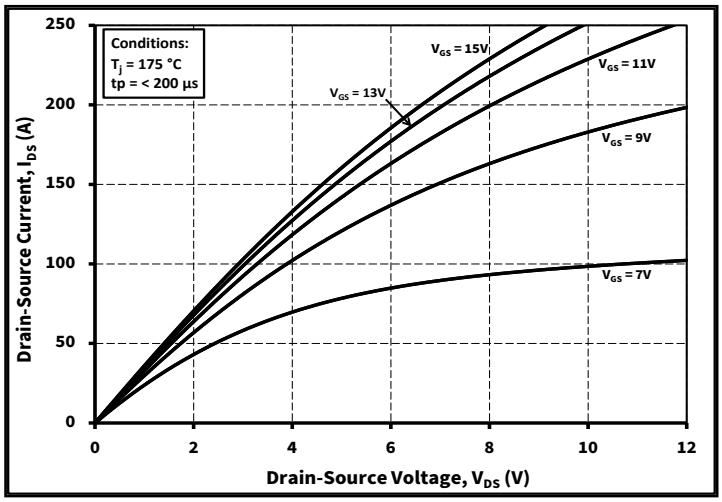

Figure 3. Output Characteristics T_J = 175 ºC

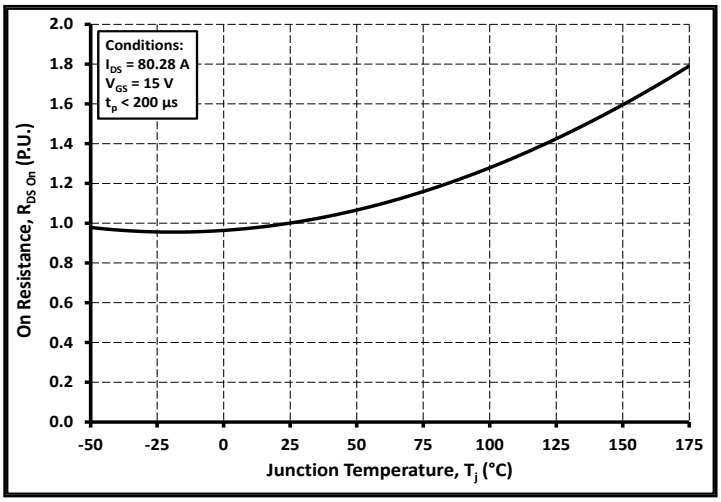

Figure 4. Normalized On-Resistance vs. Temperature

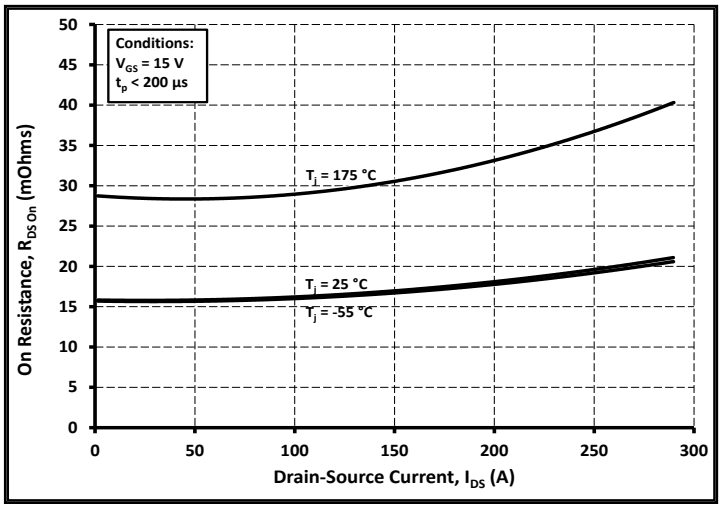

Figure 5. On-Resistance vs. Drain Current
For Various Temperatures

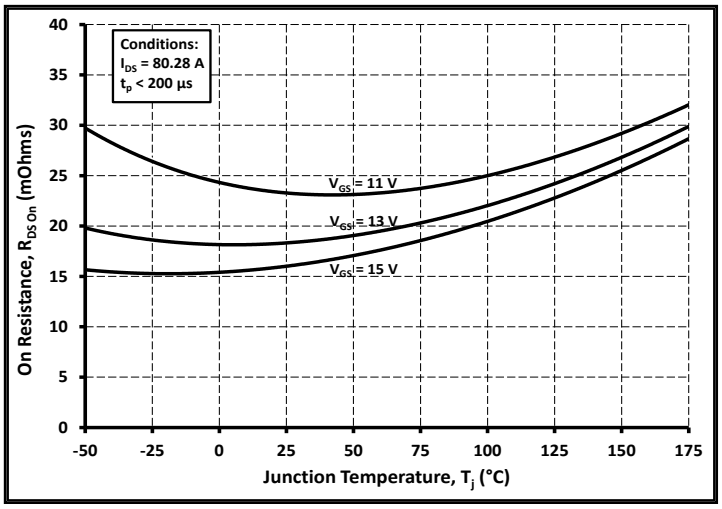

Figure 6. On-Resistance vs. Temperature
For Various Gate Voltage

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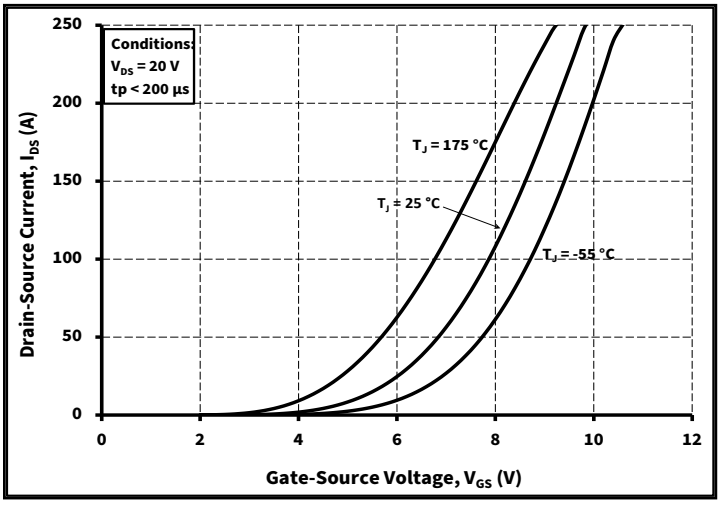

Figure 7. Transfer Characteristic for Various Junction Temperatures

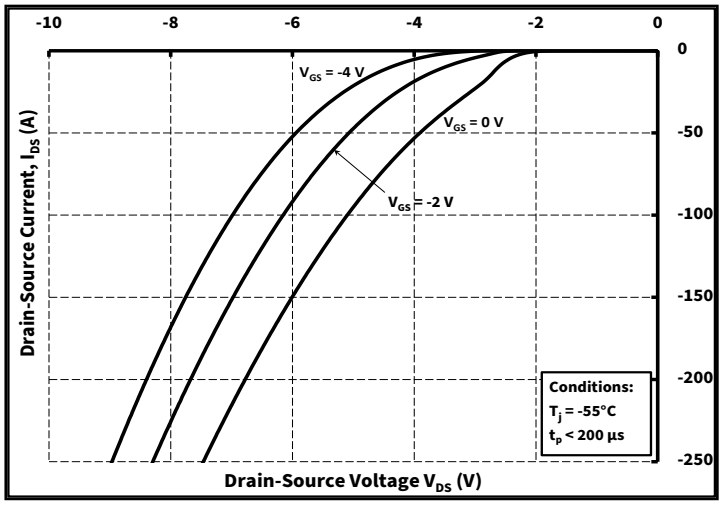

Figure 8. Body Diode Characteristic at -55 °C

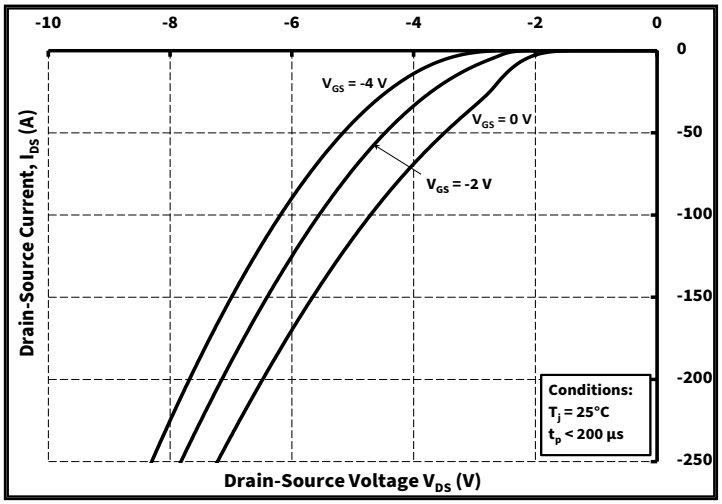

Figure 9. Body Diode Characteristic at 25 °C

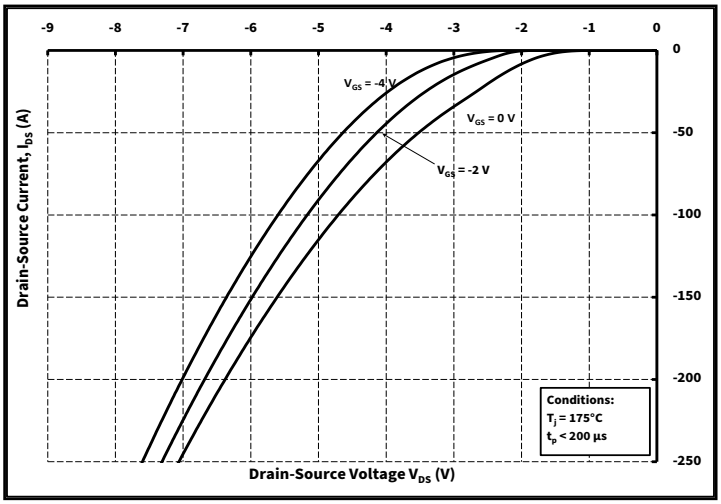

Figure 10. Body Diode Characteristic at 175 °C

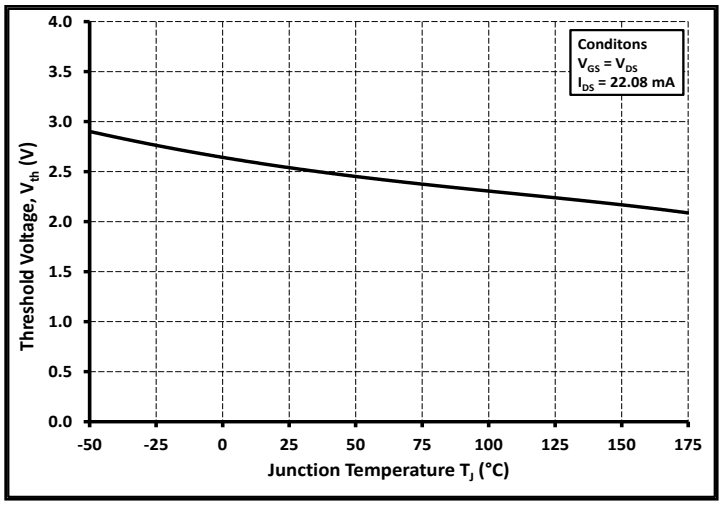

Figure 11. Threshold Voltage vs. Temperature

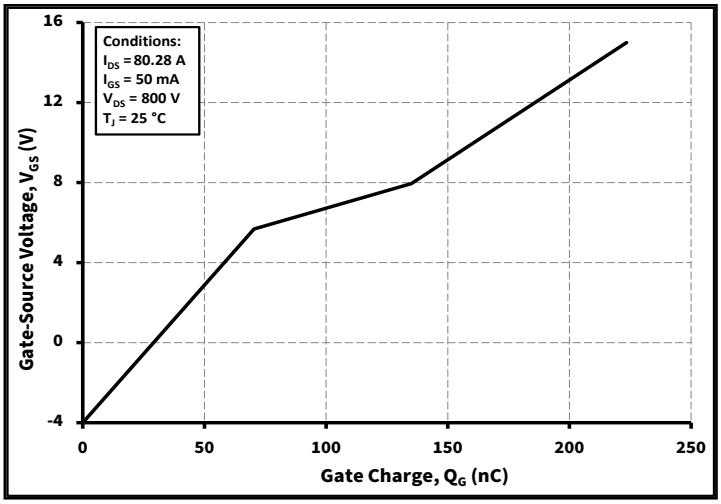

Figure 12. Gate Charge Characteristics

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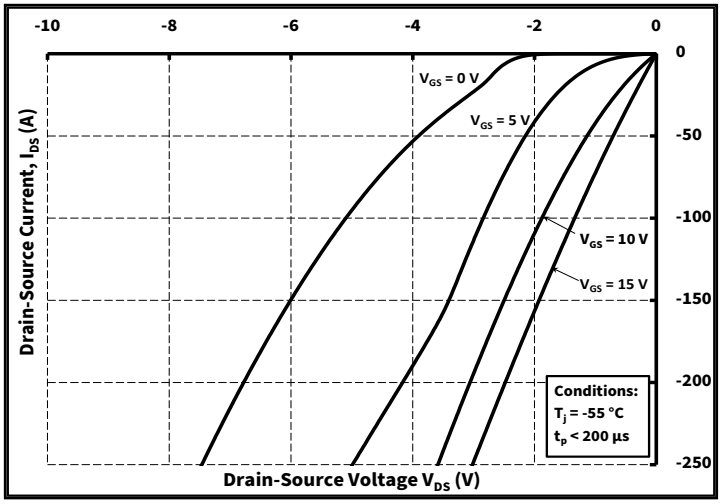

Figure 13. 3rd Quadrant Characteristic at -55 °C

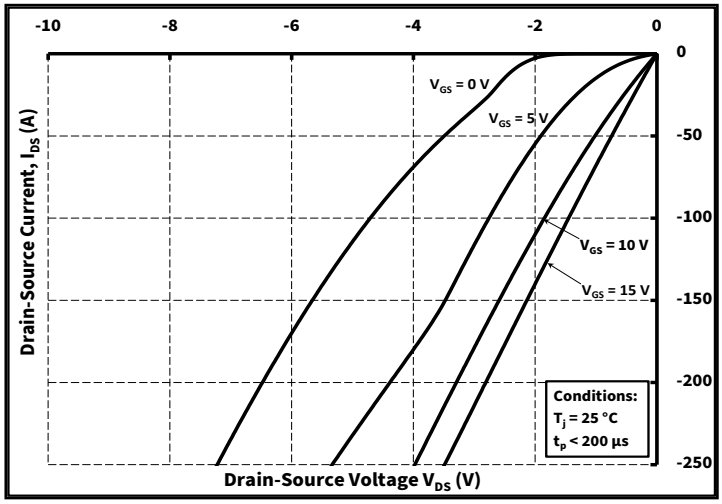

Figure 14. 3rd Quadrant Characteristic at 25 °C

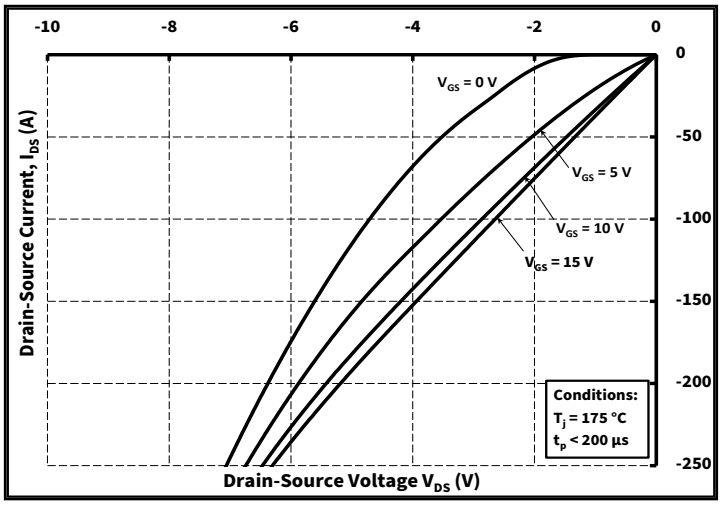

Figure 15. 3rd Quadrant Characteristic at 175 °C

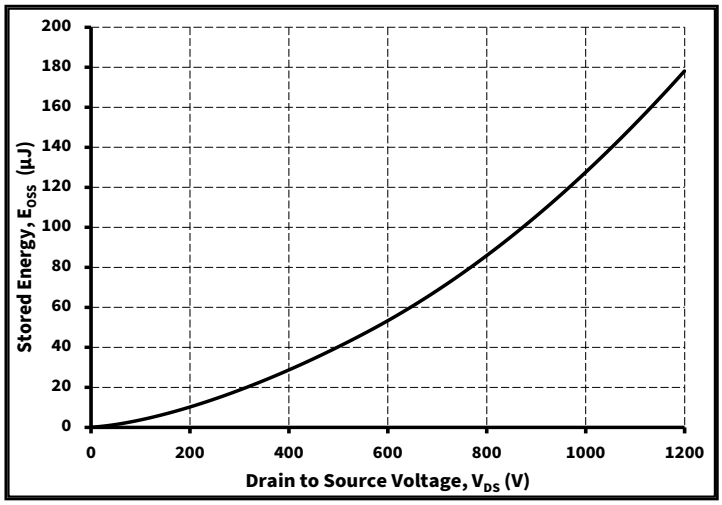

Figure 16. Output Capacitor Stored Energy

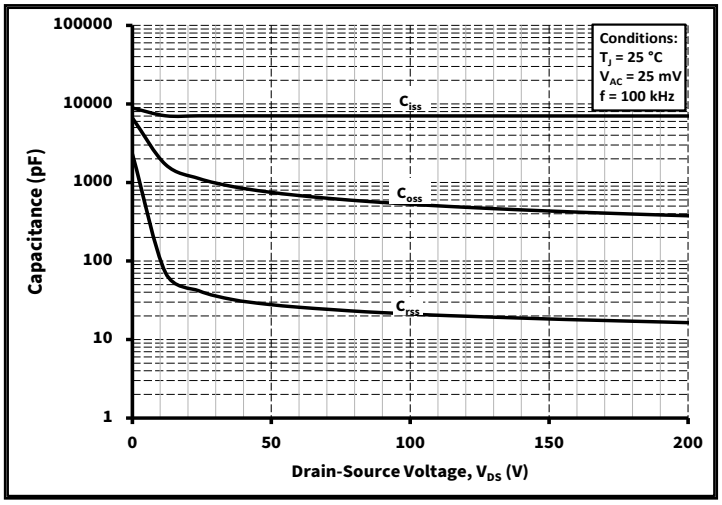

Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

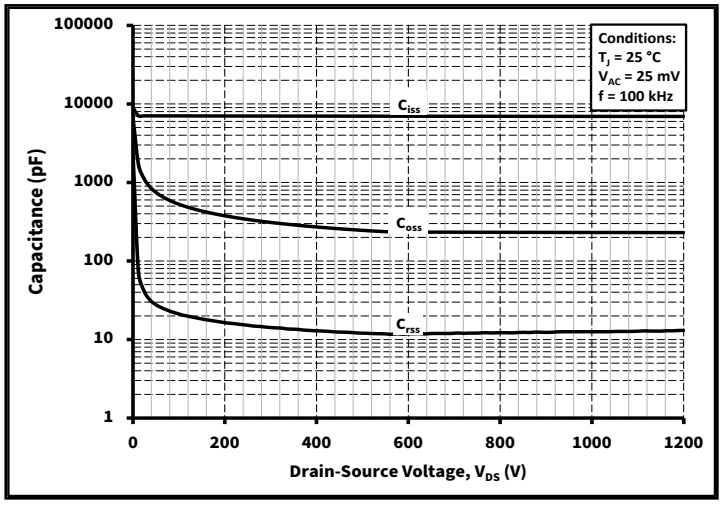

Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1200V)

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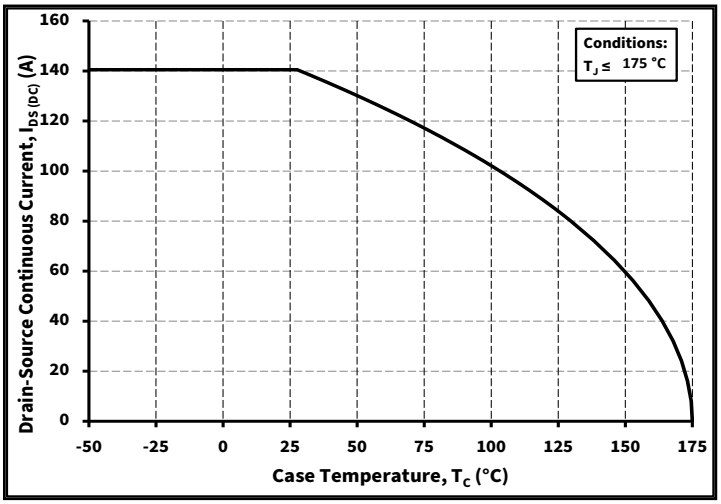

Figure 19. Continuous Drain Current Derating vs. Case Temperature

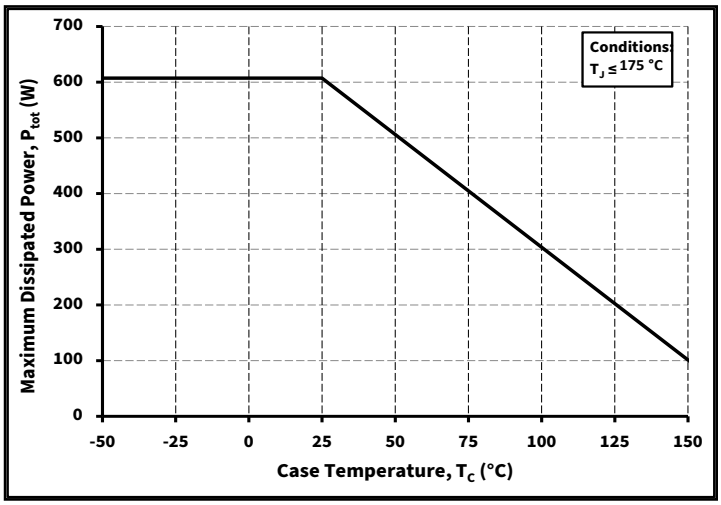

Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

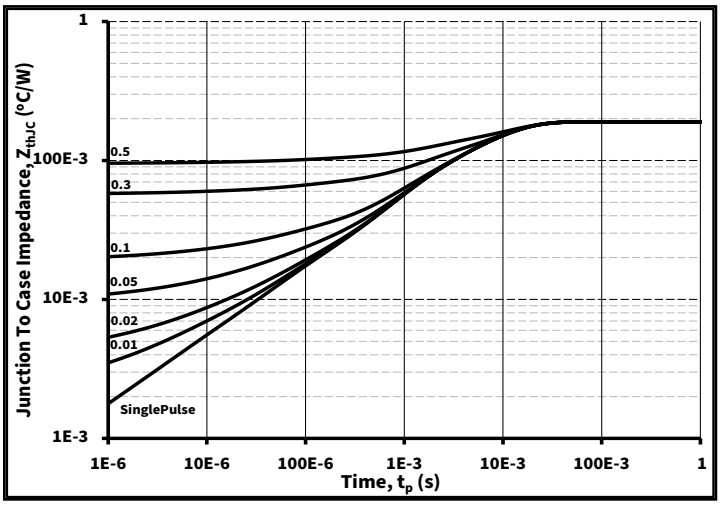

Figure 21. Transient Thermal Impedance (Junction - Case)

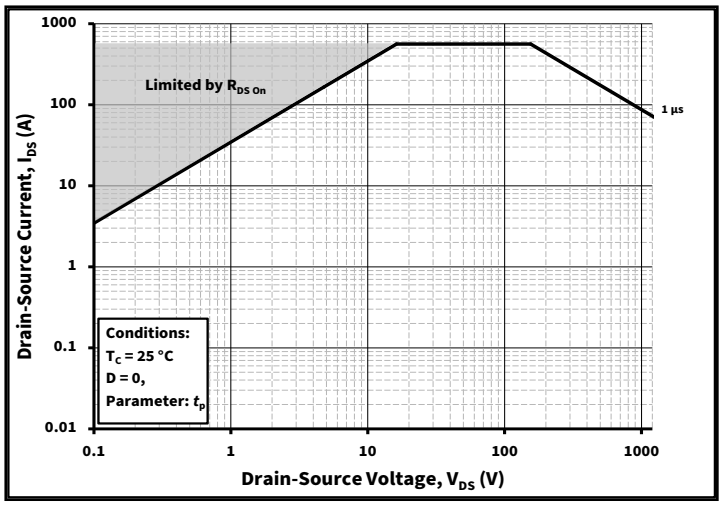

Figure 22. Safe Operating Area

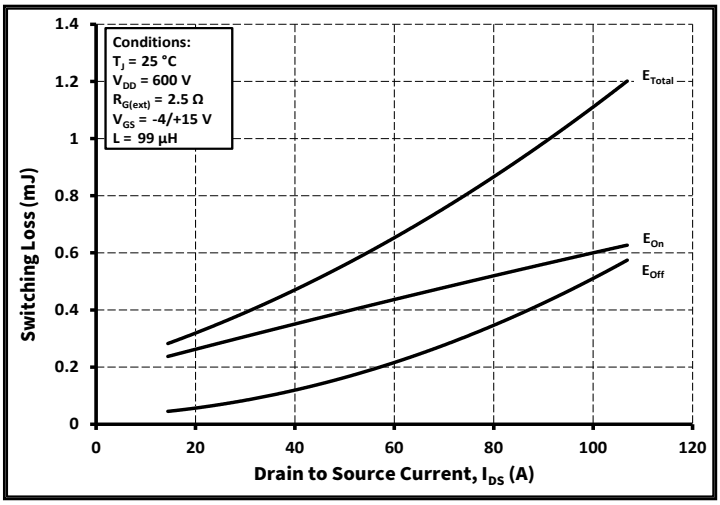

Figure 23. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 600V)

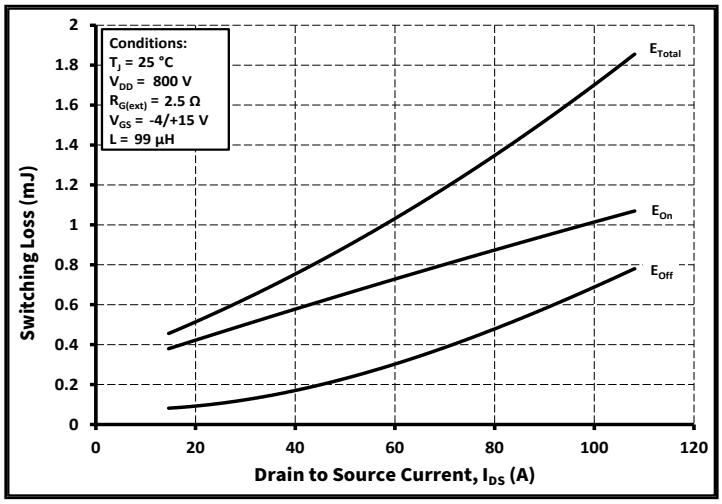

Figure 24. Clamped Inductive Switching Energy vs. Drain Current (V_{DD} = 800V)

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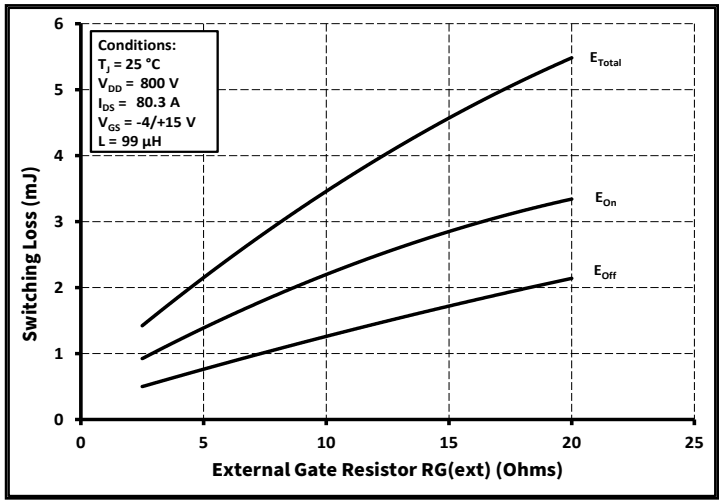

Figure 25. Clamped Inductive Switching Energy vs. $R_{G(ext)}$

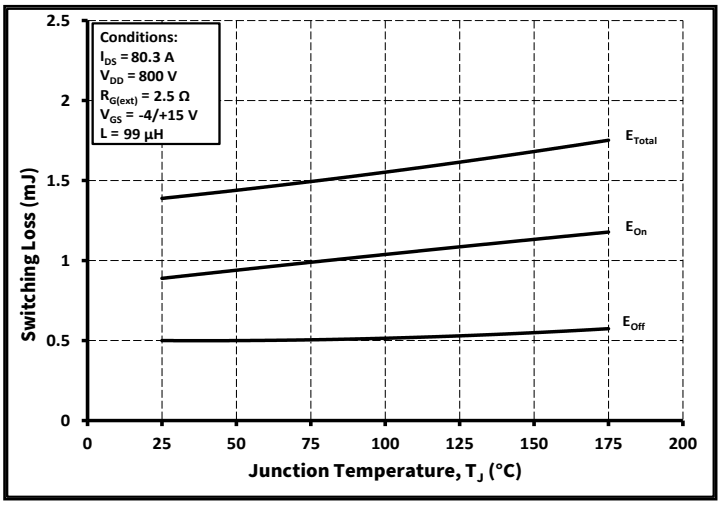

Figure 26. Clamped Inductive Switching Energy vs. Temperature

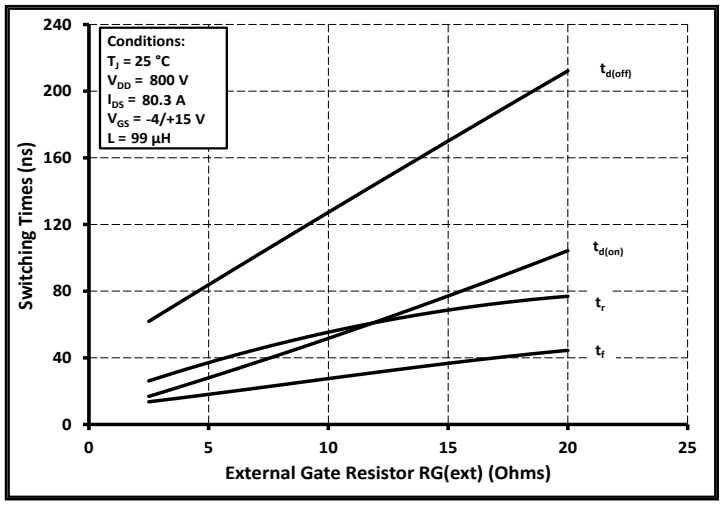

Figure 27. Switching Times vs. $R_{G(ext)}$

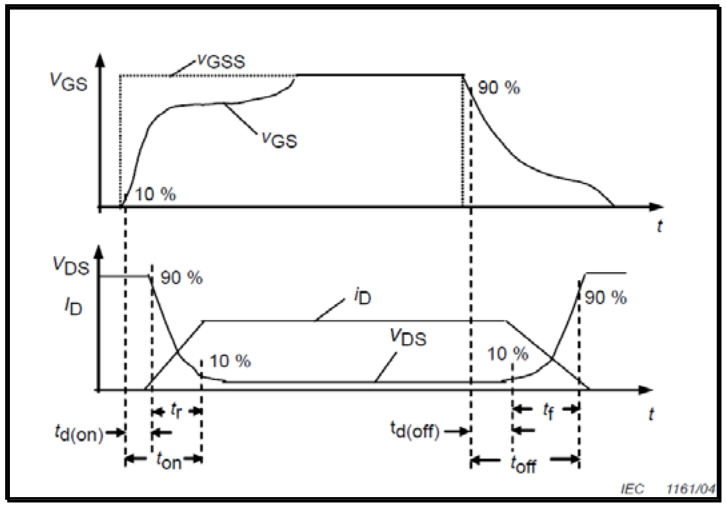

Figure 28. Switching Times Definition

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Test Circuit Schematic

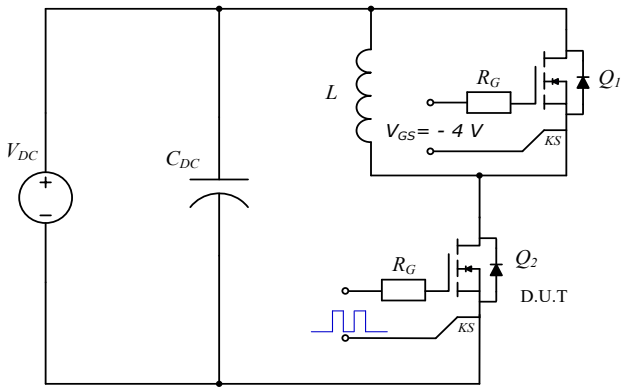

Figure 29. Clamped Inductive Switching Waveform Test Circuit

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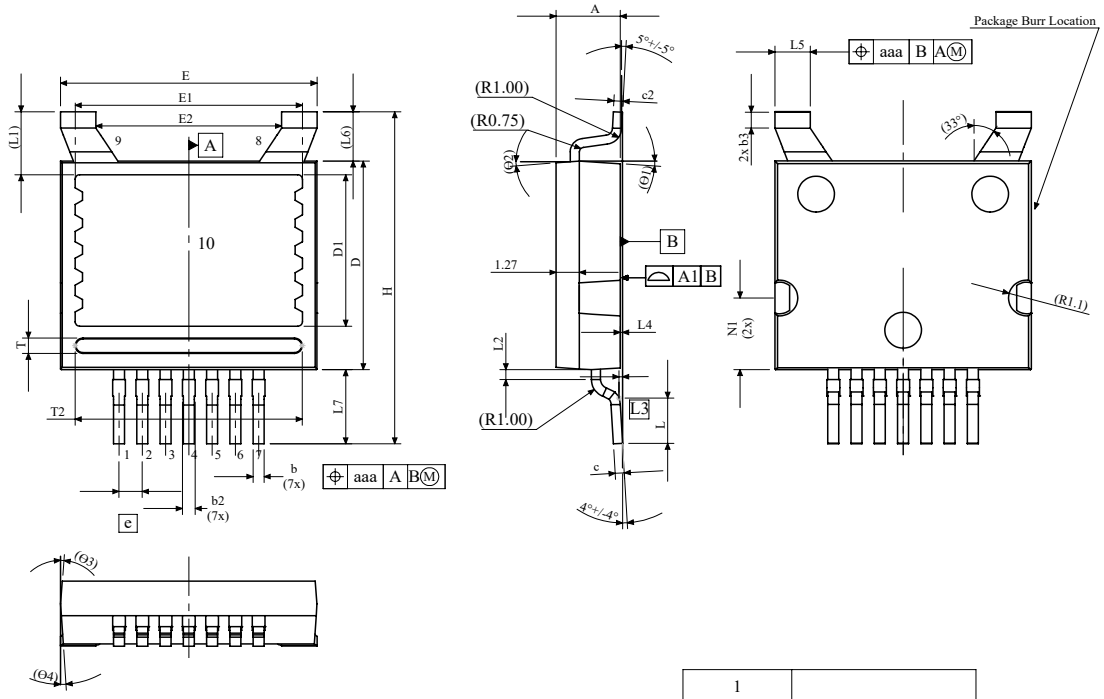
Package Dimensions



SYMBOL	MIN (mm)	MAX (mm)
A	3.40	3.60
A1	---	0.05
b	0.50	0.70
b2	0.50	1.00
b3	0.85	1.05
c	0.40	0.60
c2	0.40	0.60
D	11.55	11.75
D1	8.30	8.50
E	13.92	14.12
E1	12.22	12.42
E2	9.92	10.22
e	BSC 1.27	
H	18.00	19.00
L	2.47	2.67
L1	BSC 3.51	
L2	0.3	0.73
L3	BSC 0.26	
L4	0.09	0.2
L5	1.83	2.13
L6	BSC 2.75	
L7	4.03	4.23
T	0.75	0.95
T2	12.30	12.50
N1	3.90	4.10
Θ1	0°	8°
Θ2	0°	8°
Θ3	0°	8°
Θ4	0°	8°
aaa	---	0.10

1	SOURCE
2	
3	
4	
5	
6	DRIVER SOURCE
7	GATE
8	DRAIN
9	DRAIN
10	DRAIN

NOTE
1. ALL METAL SURFACES ARE TIN PLATED (MATTE), EXCEPT AREA OF CUT.
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
3. ALL DIMENSIONS ARE LISTED IN MILLIMETERS. ANGLES ARE IN DEGREES.
4. PACKAGE BURR FLASH SIZE (0.5 mm) IS NOT INCLUDED IN THE DIMENSIONS

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TITLE: PACKAGE OUTLINE DRAWING: U2PAK

REVISION NO. 02 | A4

Date: 12/13/24 | PRD-08764 | SCALE:3:1 | SHEET 1 OF 1

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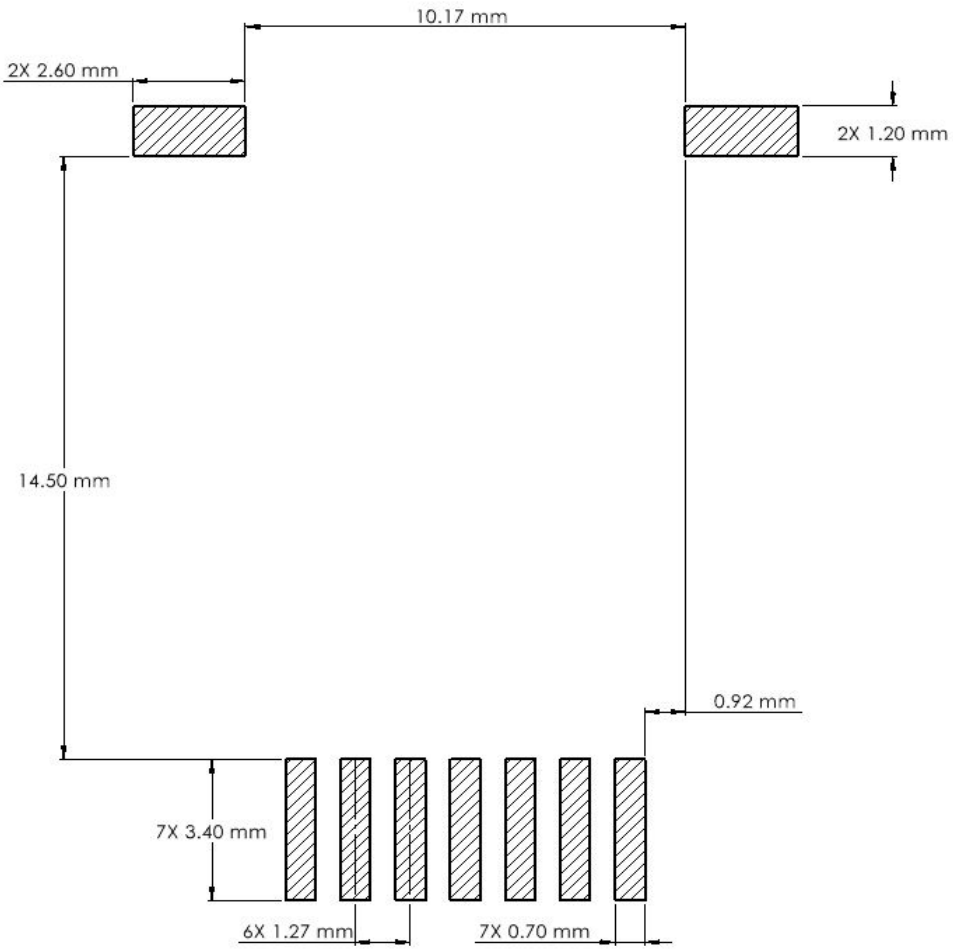
Recommended Solder Pad Layout

All dimensions in mm



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Revision history

Document Version	Date of release	Descriptiion of changes
1.0	November - 2025	Initial datasheet

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Contact info:

4600 Silicon Drive
Durham, NC 27703 USA
Tel: +1.919.313.5300
www.wolfspeed.com/power

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