MP2908A

4V-60V Input, Current Mode, Synchronous Step-Down Controller

The Future of Analog IC Technology

DESCRIPTION

The MP2908A is a high-voltage, synchronous step-down controller that directly steps down voltages from up to 60V. The MP2908A uses PWM current control architecture with accurate cycle-by-cycle current limiting and is capable of driving dual N-channel MOSFETs.

Advanced asynchronous mode (AAM) enables non-synchronous operation to optimize light-load efficiency.

The operating frequency of the MP2908A can be programmed by an external resistor or synchronized to an external clock for noise-sensitive applications. Full protection features include precision output over-voltage protection (OVP), output over-current protection (OCP), and thermal shutdown.

The MP2908A is available in TSSOP20-EP and QFN-20 (3mmx4mm) packages.

APPLICATIONS

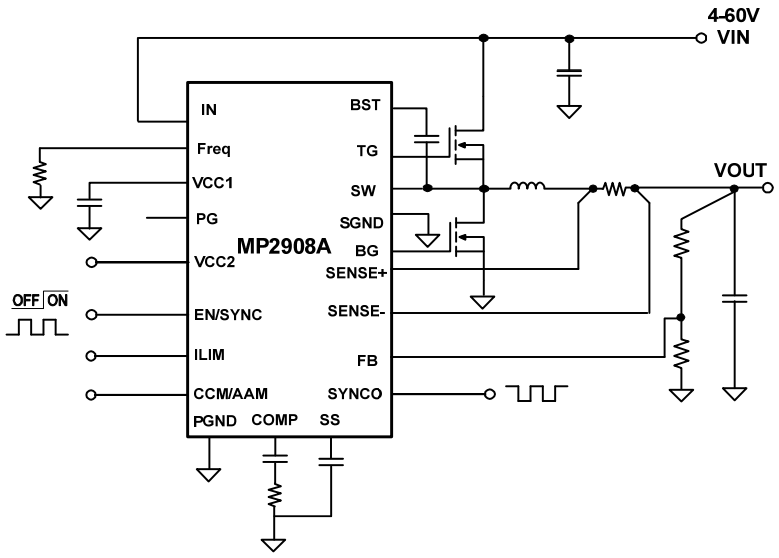
- Automotive
- Industrial Control Systems

FEATURES

- Wide 4V to 60V Operating Input Range
- Dual N-Channel MOSFET Driver
- 0.8V Voltage Reference with ±1.5% Accuracy Over Temperature
- Low Dropout Operation: Maximum Duty Cycle at 99.5%
- Programmable Frequency Range: 100kHz - 1000kHz
- External Sync Clock Range: 100kHz-1000kHz
- 180º Out-of-Phase SYNCO
- Programmable Soft Start
- Power Good Output Voltage Monitor
- Selectable Cycle-by-Cycle Current Limit
- Output Over-Voltage Protection (OVP)
- Over-Current Protection (OCP)
- Internal LDO with External Power Supply Option
- Programmable CCM, AAM Mode
- TSSOP20-EP and QFN-20 (3mmx4mm) Packages

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TYPICAL APPLICATION



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ORDERING INFORMATION

Part Number	Package	Top Marking
MP2908AGF*	TSSOP-20 EP	*See Below*
MP2908AGL**	QFN-20	*See Below*

* For Tape & Reel, add suffix –Z (e.g. MP2908AGF–Z)

* *For Tape & Reel, add suffix –Z (e.g. MP2908AGL–Z)

TOP MARKING (TSSOP-20 EP)

MPSYYWW
MP2908A
LLLLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP2908A: Product code of MP2908AGF
LLLLLLLLL: Lot number

TOP MARKING (QFN-20(3mm x4 mm))

MPYW
2908
ALLL

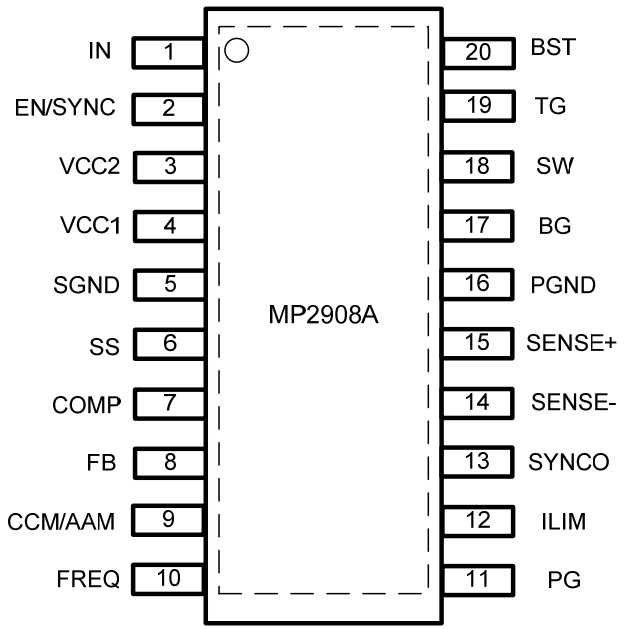
MP: MPS prefix:
YY: year code;
W: week code:
2908A: part number;
LLL: lot number;

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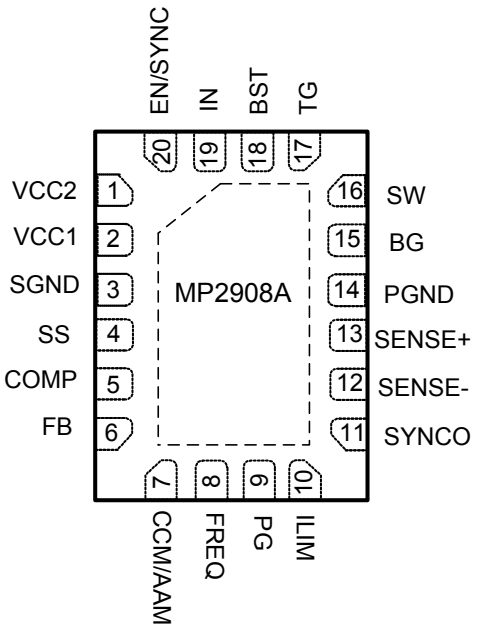
PACKAGE REFERENCE

TOP VIEW



TSSOP-20 EP

TOP VIEW



QFN-20 (3mmx4mm)

ABSOLUTE MAXIMUM RATINGS (1)

Input supply voltage (V_{IN}) 65V
BST supply voltage (V_{BST}) ..... V_{IN} + 6.5V
SW ..... -0.3V to 65V
BST - SW 6.5V
Supply voltage (VCC1) 6.5V
External supply voltage (VCC2) 15V
SENSE + / - 28V
Differential sense (SENSE+ to SENSE-) ..... -0.7V to +0.7V
TG ..... V_{SW} - 0.3V to V_{BST} + 0.3V
BG ..... -0.3V to VCC1 + 0.3V
All other pins ..... -0.3V to +6.5V
Continuous power dissipation (T_A = +25°C) (2)
TSSOP-20 EP 3.1W
QFN-20 (3mmx4mm) 2.6W
Junction temperature ..... 150°C
Lead temperature ..... 260°C
Storage temperature ..... -65°C to +175°C

Recommended Operating Conditions (3)

Supply voltage (V_{IN}) ..... 4V to 60V
Output voltage (V_{OUT}) ..... ≤24V
Supply voltage for (VCC2) ..... 4.5V to 12V
Operating junction temp. (T_J) ..... -40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSSOP-20 EP	40	8	°C/W
QFN-20 (3mmx4mm)	48	10	°C/W

NOTES:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

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ELECTRICAL CHARACTERISTICS

V_{IN} = 24V, T_J = +25°C, EN = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Input Supply						
V_{IN} UVLO threshold (rising)	IN_{UV_RISING}			4.5	5	V
V_{IN} UVLO threshold (falling)	$IN_{UV_FALLING}$			3.7	3.95	V
V_{IN} UVLO hysteresis	IN_{UV_HYS}			800		mV
V_{IN} supply current with VCC2 bias	I_{Q_VCC2}	VCC2 = 12V, external bias		25	40	µA
V_{IN} supply current without VCC2 bias	I_Q	VCC2 = 0, V_{FB} = 0.84V, V_{AAM} = 5V, SENSE+ = SENSE- = 0.3V		750	1000	µA
V_{IN} AAM current	I_{Q_AAM}	V_{AAM}=0.6V, V_{FB}=0.84V, SENSE+ = SENSE- = 0.3V		250	350	µA
V_{IN} shutdown current	I_{SHDN}	V_{EN} = 0V		0.5	1.5	µA
V_{CC} Regulator						
VCC1 regulator output voltage from V_{IN}	$VCC1_{VIN}$	VIN > 6V		5		V
VCC1 regulator load regulation from V_{IN}		Load = 0 to 50mA, VCC2 floating or connects to GND		1	3	%
VCC1 regulator output voltage from VCC2	$VCC1_{VCC2}$	VCC2 > 6V		5		V
VCC1 regulator load regulation from VCC2		Load = 0 to 50mA, VCC2 = 12V		1	3	%
VCC2 UVLO threshold (rising)	$VCC2_{RISING}$			4.7	4.92	V
VCC2 UVLO threshold (falling)	$VCC2_{FALLING}$			4.45		V
VCC2 threshold hysteresis	$VCC2_{HYS}$			250		mV
VCC2 supply current	I_{VCC2}	V_{AAM} = 5V, V_{FB} = 0.84V, VCC2 = 12V		800		µA
		V_{AAM} = 0.6V, V_{FB} = 0.84V, VCC2 = 12V		200		µA
Feedback (FB)						
Feedback voltage	V_{FB}	4V ≤ V_{IN} ≤ 60V	0.788	0.800	0.812	V
Feedback current	I_{FB}	V_{FB} = 0.8V		10		nA
Enable (EN)						
Enable threshold (rising)	V_{EN_RISING}		1.16	1.22	1.28	V
Enable threshold (falling)	$V_{EN_FALLING}$		1.03	1.09	1.15	V
Enable threshold hysteresis	V_{EN_TH}			130		mV
EN input current	I_{EN}	V_{EN} = 2V		2		µA
Enable turn-off delay	T_{OFF}		10	15		µs

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = +25°C, EN = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Oscillator and Sync						
Operating frequency	F_{SW}	R_{Freq} = 65kΩ	240	300	360	kHz
Foldback operating frequency	$F_{SW_FOLDBACK}$	V_{FB}=0.1V		50%		F_{SW}
Maximum programmable frequency	F_{SWH}		1000			kHz
Minimum programmable frequency	F_{SWL}				100	kHz
Sync/EN frequency range	F_{SYNC}		100		1000	kHz
Sync/EN voltage rising threshold	V_{SYNC_RISING}		2			V
Sync/EN voltage falling threshold	$V_{SYNC_FALLING}$				0.35	V
Current Sense						
Current sense common mode voltage range	$V_{SENSE+/-}$		0		24	V
Current limit sense voltage	V_{ILIMIT}	I_{LIM} = GND, V_{SENSE+} = 3.3V	15	25	35	mV
		I_{LIM} = VCC1, V_{SENSE+} = 3.3V	40	50	60	mV
		I_{LIM} = FLOAT, V_{SENSE+} = 3.3V	65	75	85	mV
Reverse current limit sense voltage	V_{REV_ILIMIT}	I_{LIM} = GND, V_{SENSE+} = 3.3V		8		mV
		I_{LIM} = VCC1, V_{SENSE+} = 3.3V		17		
		I_{LIM} = FLOAT, V_{SENSE+} = 3.3V		24		
Valley current limit	V_{VAL_ILIMIT}	I_{LIM} = GND, V_{SENSE+} = 3.3V		22.5		mV
		I_{LIM} = VCC1, V_{SENSE+} = 3.3V		47.5		
		I_{LIM} = FLOAT, V_{SENSE+} = 3.3V		72.5		
Input current of sensor	I_{SENSE}	$V_{SENSE+/-(CM)}$ = 0V		-45		µA
		$V_{SENSE+/-(CM)}$ = 3.3V		115		µA
		$V_{SENSE+/-(CM)}$ > 5V		150		µA
Soft Start (SS)						
Soft-start source current	I_{SS}	SS = 0.5V	2	4	6	µA
Error Amplifier						
Error amp transconductance(5)	G_m	ΔV = 5mV		500		µS
Error amp open loop DC gain(5)	A_O			70		dB
Error amp sink/source current	I_{EA}	FB = 0.7/0.9V		±30		µA
Protection						
Over-voltage threshold	V_{OV}		110%	115%	120%	V_{FB}
Over-voltage hysteresis	V_{OV_HYS}			10%		V_{FB}
Thermal shutdown(6)				170		°C
Thermal shutdown hysteresis(6)				20		°C

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ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = 24V, T_J = +25°C, EN = 2V, V_{ILIMIT} = 75mV, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Gate Driver						
TG pull-up resistor	R_{TG_PULLUP}			2		Ω
TG pull-down resistor	R_{TG_PULLDN}			1		Ω
BG pull-up resistor	R_{BG_PULLUP}			3		Ω
BG pull-down resistor	R_{BG_PULLDN}			1		Ω
Dead time	T_{Dead}	C_{Load} = 3.3nF		60		ns
TG maximum duty cycle	D_{max}	V_{FB} = 0.7V	98	99.5		%
TG minimum on time(6)	$T_{ON_MIN_TG}$			92		ns
BG minimum on time	$T_{ON_MIN_BG}$			175	250	ns
Power Good						
Power good low	V_{PG_Low}	I_{load} = 4mA		0.1	0.3	V
PG rising threshold	PG_{Vth_RSING}	V_{OUT} rising	85%	90%	96.5%	V_{FB}
		V_{OUT} falling	101%	107%	112.5%	
PG falling threshold	$PG_{Vth_FALLING}$	V_{OUT} falling	81%	87%	92.5%	V_{FB}
		V_{OUT} rising	105%	110%	116.5%	
PG threshold hysteresis	PG_{Vth_HYS}			3%		V_{FB}
Power good leakage	I_{PG_LK}	PG = 5V			2	μA
Power good delay	T_{PG_delay}			25		μs
AAM/CCM						
AAM output current	I_{AAM}	R_{Freq} = 65 kΩ		9.2		μA
CCM required AAM threshold voltage	V_{CCM_TH}		2.3			V

NOTES:

5) Guaranteed by design, not tested.

6) Derived from bench characterization, not tested in production.

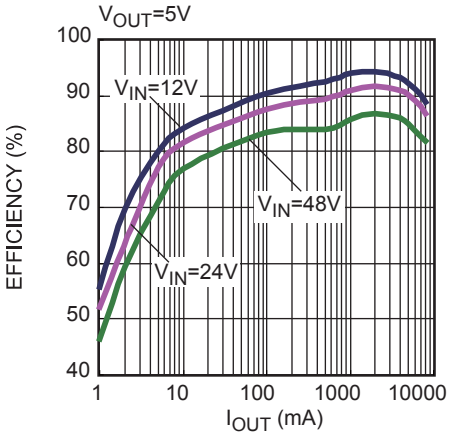
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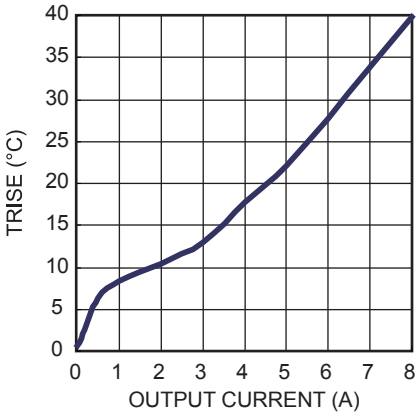
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, T_A = +25°C

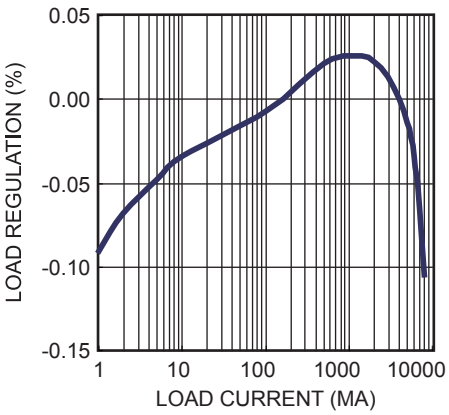
Efficiency vs. Load Current



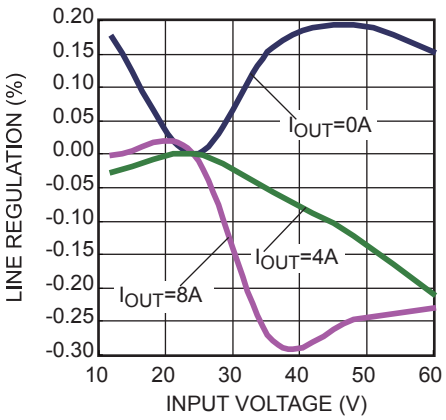
IC Thermal Rise



Load Regulation



Line Regulation



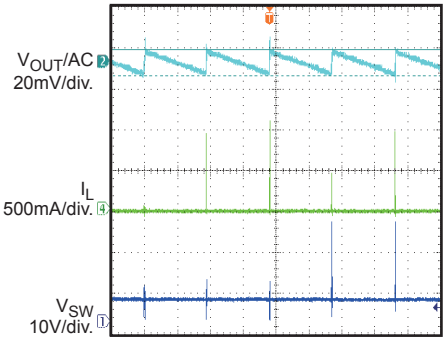
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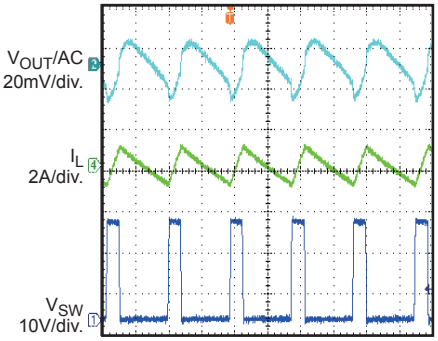
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, T_A = +25°C

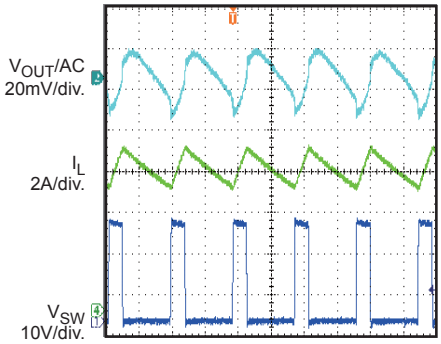
Steady State
I_{OUT}=0, AAM Mode



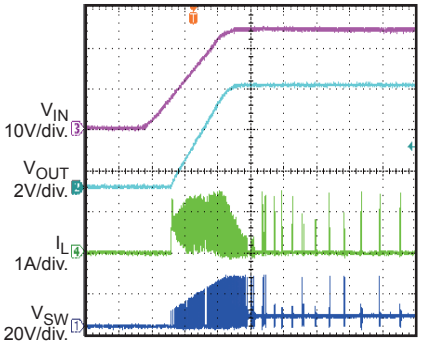
Steady State
I_{OUT}=0, Forced CCM Mode



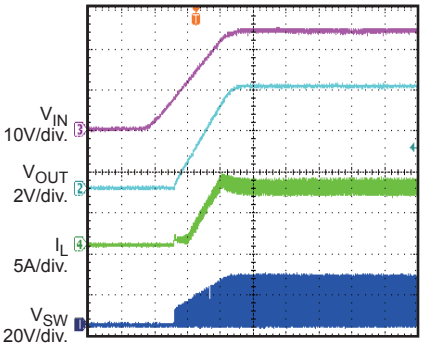
Steady State
I_{OUT}=7A



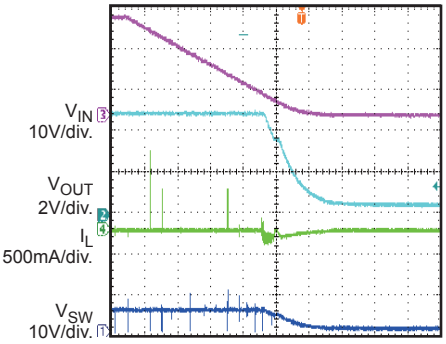
Start-Up Through VIN
I_{OUT}=0



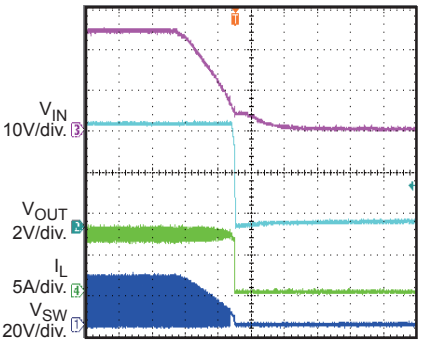
Start-Up Through VIN
I_{OUT}=7A



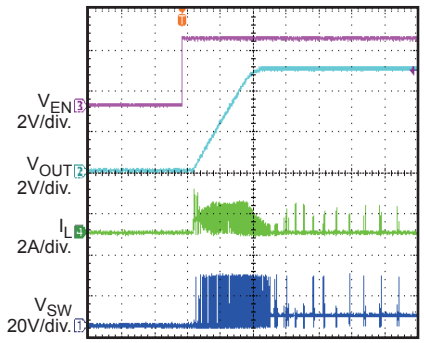
Shutdown Through VIN
I_{OUT}=0



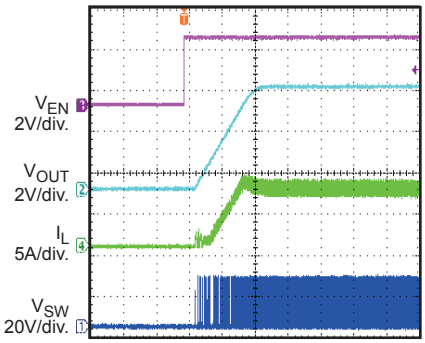
Shutdown Through VIN
I_{OUT}=7A



Start-Up Through EN
I_{OUT}=0



Start-Up Through EN
I_{OUT}=7A



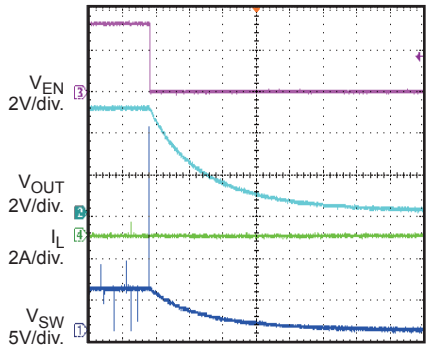
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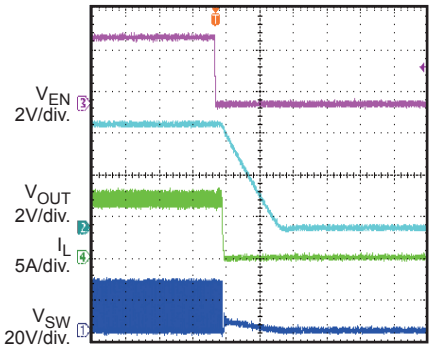
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

V_{IN} = 24V, V_{OUT} = 5V, L = 4.7µH, T_A = +25°C

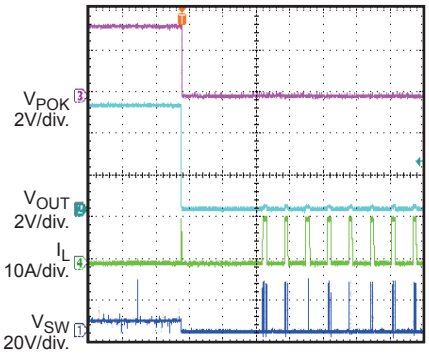
Shutdown Through EN
I_{OUT}=0



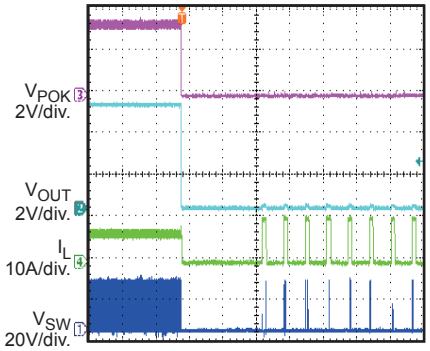
Shutdown Through EN
I_{OUT}=7A



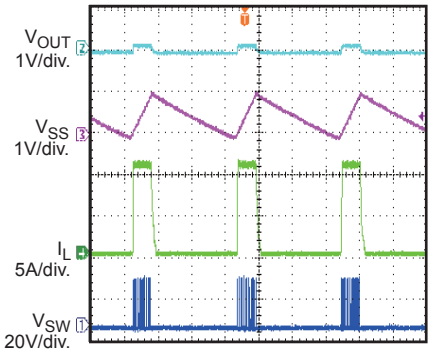
SCP Entry
I_{OUT}=0 to short circuit



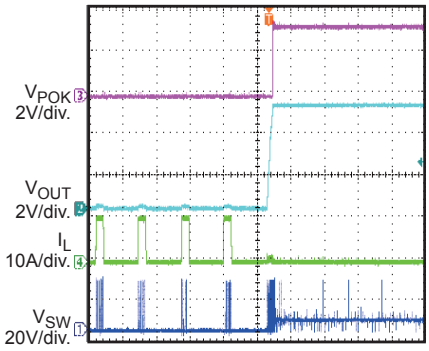
SCP Entry
I_{OUT}=7A to short circuit



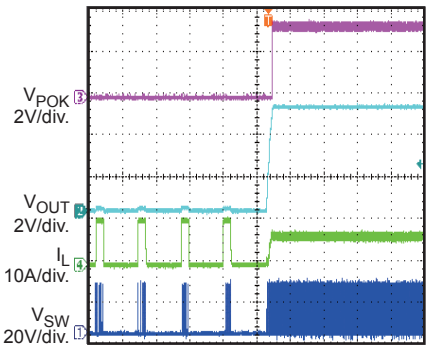
SCP Steady State



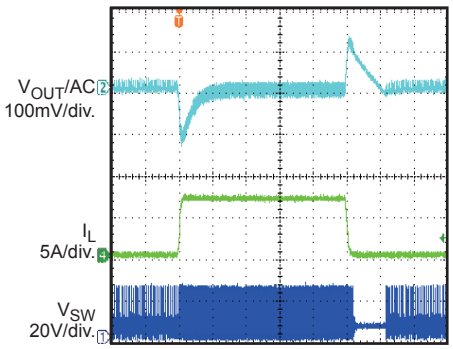
SCP Recovery
short circuit to I_{OUT}=0



SCP Recovery
short circuit to I_{OUT}=7A



Load Transient
I_{OUT}=0.2A<->7A, 1.6A/µs



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PIN FUNCTIONS

TSSOP Pin #	QFN20 Pin #	Name	Description
1	19	IN	**Input supply.** The MP2908A operates on a 4V to 60V input range. A ceramic capacitor is needed to prevent large voltage spikes at the input.
2	20	EN/SYNC	**Enable input.** The threshold is 1.22V with 140mV of hysteresis and is used to implement an input under-voltage lockout (UVLO) function externally. If an external sync clock is applied to EN/SYNC, the internal clock follows the sync frequency.
3	1	VCC2	**External power supply for the internal VCC1 regulator.** VCC2 disables the power from V_{IN} as long as VCC2 is higher than 4.5V. Do not connect a power supply greater than 12V to VCC2. Connecting VCC2 to an external power supply reduces power dissipation and increases efficiency.
4	2	VCC1	**Internal bias supply.** Decouple VCC1 with a ceramic capacitor 1μF or greater. The capacitance should be no more than 4.7μF.
5	3	SGND	**Low-noise ground reference.** SGND should be connected to the V_{OUT} side of the output capacitors.
6	4	SS	**Soft-start control input.** SS is used to program the soft-start period with an external capacitor between SS and SGND.
7	5	COMP	**COMP is used to compensate the regulation control loop.** Connect an RC network from COMP to GND to compensate for the regulation control loop.
8	6	FB	**Feedback.** FB is the input to the error amplifier. An external resistive divider connected between the output and GND is compared to the internal +0.8V reference to set the regulation voltage.
9	7	CCM/AAM	**Continuous conduction mode/advanced asynchronous mode.** Floating CCM/AAM or connecting CCM/AAM to VCC1 sets the part to operate in CCM. Connecting an appropriate external resistor from CCM/AAM to GND (so AAM is at a low level) sets the part to operate in AAM. The AAM voltage should be no less than 480mV.
10	8	FREQ	**Connect a resistor between FREQ and GND to set the switching frequency.**
11	9	PG	**Power good output.** The output of PG is an open drain.
12	10	ILIM	**Sense voltage limit set.** The voltage at ILIM sets the nominal sense voltage at the maximum output current. There are three fixed options: float, VCC1, and GND.
13	11	SYNCO	**SYNCO outputs an out-of-phase 180ºclock when the part works in CCM for dual-channel operation.**
14	12	SENSE-	**Negative input for the current sense.** The sensed inductor current limit threshold is determined by the status of ILIM.
15	13	SENSE+	**Positive input for the current sense.** The sensed inductor current limit threshold is determined by the status of ILIM.
16	14	PGND	**High-current ground reference for the internal low-side switch driver and the VCC1 regulator circuit.** Connect PGND directly to the negative terminal of the VCC1 decoupling capacitor.

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PIN FUNCTIONS *(continued)*

TSSOP Pin #	QFN20 Pin #	Name	Description
17	15	BG	**Bottom gate driver output.** Connect BG to the gate of the synchronous N-channel MOSFET.
18	16	SW	**Switch node.** SW is the reference for the V_{BST} supply and high-current returns for the bootstrapped switch.
19	17	TG	**Top gate drive.** TG drives the gate of the top N-channel synchronous MOSFET. The TG driver draws power from the BST capacitor and returns to SW, providing a true floating drive to the top N-channel MOSFET.
20	18	BST	**Bootstrap.** BST is the positive power supply for the internal, floating, high-side MOSFET driver. Connect a bypass capacitor between BST and SW. A diode from VCC1 to BST charges the BST capacitor when the low-side switch is off.

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TIME SEQUENCE

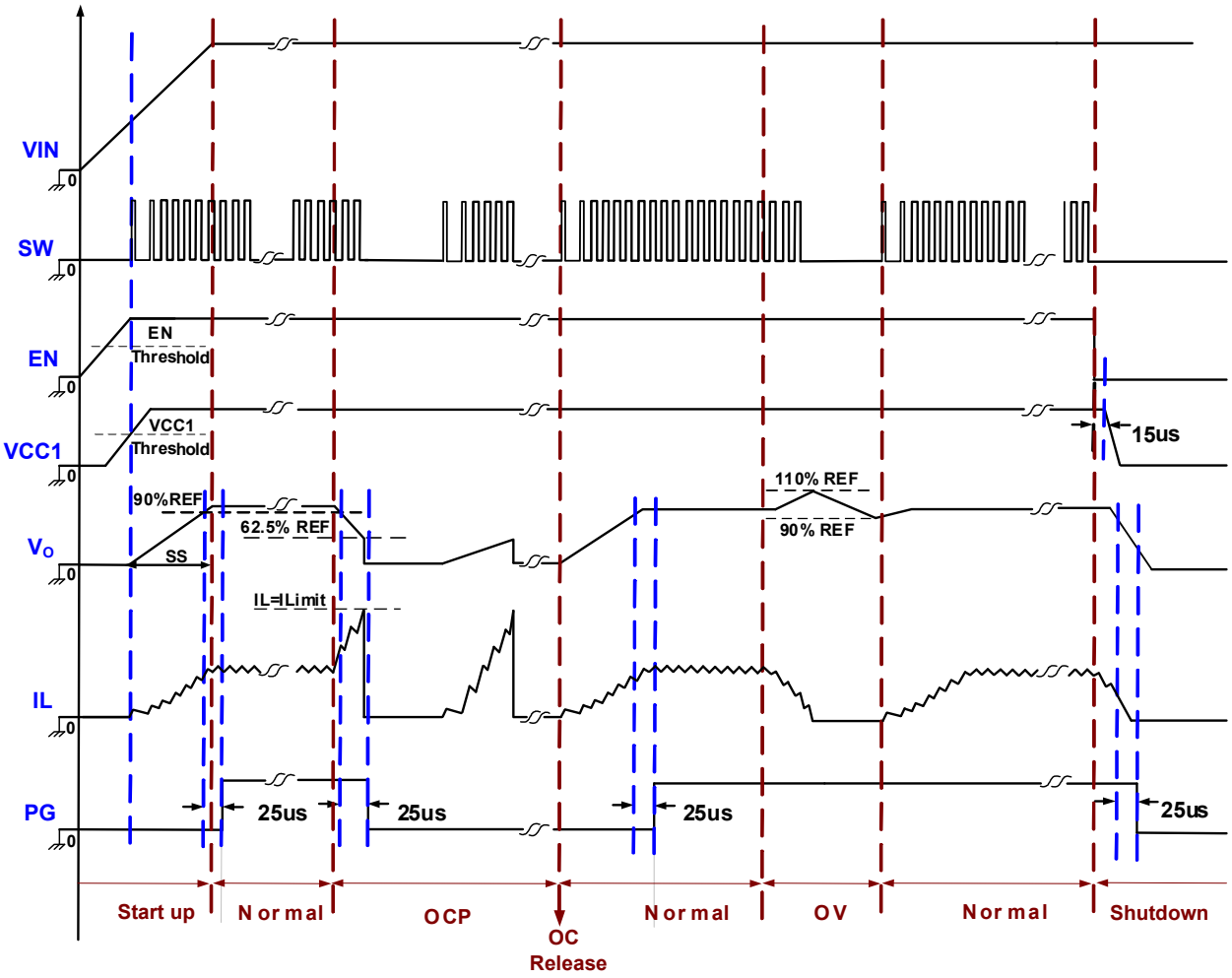


Figure 1: Time Sequence

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OPERATION

The MP2908A is a high-performance, step-down, synchronous DC/DC controller IC with a wide input voltage range. It implements current mode and switching frequency programmable control architecture to regulate the output voltage with external N-channel MOSFETs.

The MP2908A senses the voltage at FB; the difference between the FB voltage and an internal 0.8V reference is amplified to generate an error voltage on COMP. This is used as a threshold for the current sense comparator with a slope compensation ramp.

Under normal load conditions, the controller operates in full PWM mode (see Figure 2). At the beginning of each oscillator cycle, the top gate driver is enabled. The top gate turns on for a period determined by the duty cycle. When the top gate turns off, the bottom gate turns on after a dead time and remains on until the next clock cycle begins.

There is an optional power-save mode for light-load or no-load conditions.

Advanced Asynchronous Mode (AAM)

The MP2908A employs AAM functionality to optimize efficiency during light-load or no-load conditions (see Figure 2). It is enabled when CCM/AAM is at a low level by connecting an appropriate resistor to GND to ensure that V_{AAM} is no less than 480mV. See Equation (1):

$$V_{AAM}\,(mV) = I_{AAM}\,(\mu A) \times R_{AAM}\,(k\Omega) \qquad (1)$$

Where I_{AAM} is the CCM/AAM output current.

The CCM/AAM output current (I_{AAM}) is shown in Equation (2). AAM is disabled when CCM/AAM is floating or connected to VCC1.

$$I_{AAM}\,(\mu A) = 600\,(mV) / R_{FREQ}\,(k\Omega) \qquad (2)$$

If AAM is enabled, the MP2908A first enters non-synchronous operation as long as the inductor current approaches zero at light-load. If the load decreases further to make the COMP voltage drop below the CCM/AAM voltage (V_{AAM}), the MP2908A enters AAM. In AAM, the internal clock resets whenever V_{COMP} crosses over V_{AAM}; the crossover time is the benchmark for the next clock cycle. When the load increases and the DC value of V_{COMP} is higher than V_{AAM}, the operation mode is DCM or CCM, which has a constant switching frequency.

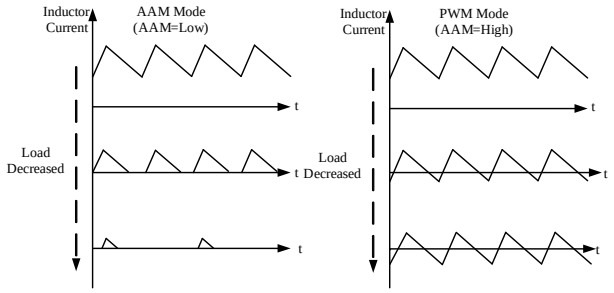


Figure 2: AAM and PWM

Floating Driver and Bootstrap Charging

The floating top gate driver is powered by an external bootstrap capacitor (C_{BST}), which is normally refreshed when the high-side MOSFET (HS-FET) turns off. This floating driver has its own UVLO protection. This UVLO's rising threshold is 3.05V with a hysteresis of 170mV.

If the BST voltage is lower than the bootstrap UVLO, the MP2908A enters constant-off-time mode to ensure that the BST cap is high enough to drive the HS-FET.

VCC1 Regulator and VCC2 Power Supply

Both the top and bottom MOSFET drivers and most of the internal circuitries are powered by the VCC1 regulator. An internal, low, dropout linear regulator supplies VCC1 power from VIN. Connect a ceramic capacitor 4.7μF or smaller from VCC1 to GND.

If VCC2 is left open or connected to a voltage less than 4.5V, an internal 5V regulator supplies power to VCC1 from V_{IN}. If VCC2 is greater than 4.5V, the internal regulator that supplies power to VCC1 from VCC2 is triggered.

If VCC2 is greater than 4.5V but less than 5V, the 5V regulator is in dropout, and VCC1 is approximately equal to VCC2. Using the VCC2 power supply allows the VCC1 power to be derived from a high-efficiency external source, such as one of the MP2908A's switching regulator outputs.

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Error Amplifier

The error amplifier compares the FB voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two input voltages. This output current is then used to charge or discharge the external compensation network to form the COMP voltage, which is used to control the power MOSFET current. Adjusting the compensation network from COMP to GND optimizes the control loop for good stability or fast transient response.

Current Limit Function

There are three fixed current limit options: 25mV, when ILIM is connected to GND; 50mV, when ILIM is connected to VCC1; and 75mV, when ILIM is floating.

When the peak value of the inductor current exceeds the set current limit threshold, the output voltage begins dropping until FB is 37.5% below the reference. The MP2908A enters hiccup mode to restart the part periodically. The frequency is lowered when FB is below 0.4V. This protection mode is especially useful when the output is dead-shorted to ground. The average short-circuit current is reduced greatly to alleviate thermal issues. The MP2908A exits hiccup mode once the over-current condition is removed.

Low Dropout Operation

In low dropout mode, the MP2908A is designed to operate in a HS fully on mode as long as the voltage difference across BST - SW is greater than 3.05V, improving dropout. When the voltage from BST to SW drops below 3.05V, an under-voltage lockout (UVLO) circuit turns off the high-side MOSFET (HS-FET). At the same time, the low-side MOSFET (LS-FET) turns on to refresh the charge on the BST capacitor. After the BST capacitor voltage is re-charged, the HS-FET turns on again to regulate the output. Since the supply current sourced from the BST capacitor is low, the HS-FET can remain on for more switching cycles than are required to refresh the BST capacitor, increasing the effective duty cycle of the switching regulator. The low dropout operation makes the MP2908A suitable for automotive cold-crank.

Power Good (PG) Function

The MP2908A includes an open-drain power good output that indicates whether the regulator's output is within ±10% of its nominal value. When the output voltage falls outside of this range, the PG output is pulled low. It should be connected to a voltage source no more than 5V through a resistor (e.g., 100kΩ). The PG delay time is 25μs.

Soft Start (SS)

The soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts, the internal circuitry generates a soft-start voltage that ramps up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF, so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

An external capacitor connected from SS to SGND is charged from an internal 4μA current source, producing a ramped voltage. The soft-start time (t_{SS}) is set by the external SS capacitor and can be calculated by Equation (3):

$$t_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(\mu A)} \quad (3)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (0.8V), and I_{SS} is the 4μA SS charge current. There is no internal SS capacitor. SS is reset when a fault protection other than OVP occurs.

Output Over-Voltage Protection (OVP)

The output over-voltage is monitored by the FB voltage. If the FB voltage is typically 10% higher than the reference, the MP2908A enters discharge mode: the HS-FET turns off, and the LS-FET turns on. The LS-FET remains on until the reverse current limit is triggered. The LS-FET then turns off, and the inductor current increases to 0. The LS-FET is turned on again after ZCD is triggered. The MP2908A works in discharge mode until the over-voltage condition is cleared.

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EN/SYNC Control

The MP2908A has a dedicated enable (EN/SYNC) control. It uses a bandgap-generated precision threshold of 1.22V. By pulling it high or low, the IC can be enabled or disabled. To disable the part, EN/SYNC must be pulled low for at least 15μs.

Tie EN/SYNC to VIN through a resistor divider R5 and R6 to program the VIN start-up threshold (see Figure 3). The EN/SYNC threshold is 1.09V (falling edge), so the V_{IN} UVLO threshold is 1.09V x (1+ R5/R6).

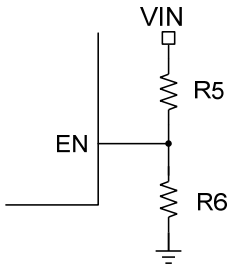


Figure 3: EN Resistor Divider

Synchronize

The MP2908A can be synchronized to an external clock ranging from 100kHz up to 1000kHz through EN/SYNC. The internal clock rising edge is synchronized to the external clock rising edge. The pulse width (both on and off) of the external clock signal should be no less than 100ns.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient input supply voltages. The MP2908A UVLO rising threshold is about 4.5V while its falling threshold is a consistent 3.7V.

Thermal Protection

Thermal protection prevents damage to the IC from excessive temperatures. The die temperature is monitored internally until the thermal limit is reached. When the silicon die temperature is higher than 170°C, the entire chip shuts down. When the temperature is below its lower threshold (typically 20°C), the chip is enabled again.

Start-Up and Shutdown

If both VIN and EN/SYNC are higher than their respective thresholds, the chip starts up. The reference block starts first, generating stable reference voltages and currents. The internal regulator is then enabled. The regulator provides a stable supply for the remaining circuitry.

Three events can shut down the chip: EN low, VIN low, and thermal shutdown. During the shutdown procedure, the signal path is blocked first to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subjected to this shutdown command.

Pre-Bias Start-Up

If SS is less than FB at start-up, the output has a pre-bias voltage and neither TG nor BG is turned on until SS is greater than FB.

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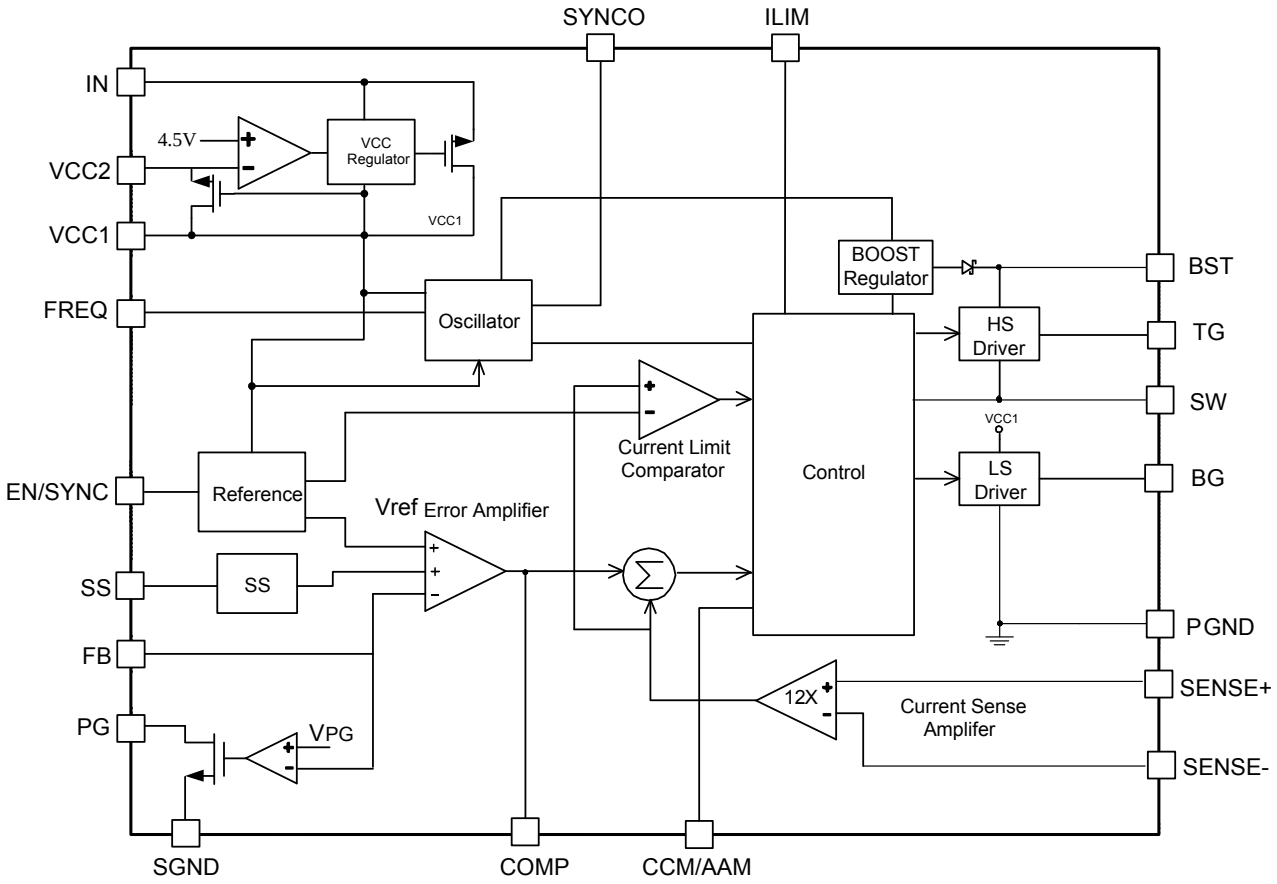


Figure 4: Block Diagram

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APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see Figure 5).

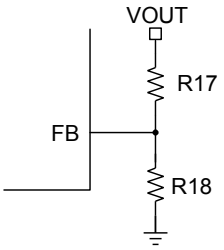


Figure 5: External Resistor Divider

If R17 is known, then R18 can be calculated with Equation (4):

$$R_{18} = \frac{R_{17}}{\frac{V_{OUT}}{0.8V} - 1} \quad (4)$$

Table 1 lists the recommended feedback resistor values for common output voltages.

Table 1: Resistor Selection for Common Output Voltages (needs callout)

V_{OUT} (V)	R17 (kΩ)	R18 (kΩ)
3.3	37.4 (1%)	12 (1%)
5	63.4 (1%)	12 (1%)
12	169 (1%)	12 (1%)

Setting Current Sensing

The MP2908A has three fixed current limit options: 25mV, when ILIM is connected to GND; 50mV, when ILIM is connected to VCC1; and 75mV, when ILIM is floating.

The current sense resistor (R_{SENSE}) monitors the inductor current. Its value is chosen based on the current limit threshold. The relationship between the peak inductor current (I_{pk}) and R_{SENSE} can be calculated with Equation (5):

$$R_{SENSE} = \frac{V_{ILIMIT}}{Ipk} \quad (5)$$

The typical values for R_{SENSE} are in the range of 10mΩ to 50mΩ.

Programmable Switching Frequency

Consider different variables when choosing the switching frequency. A high frequency increases switching losses and gate charge losses while a low frequency requires more inductance and capacitance, resulting in larger real estate and higher cost. It is a trade off between power loss and passive component size. In noise-sensitive applications, the switching frequency should be out of a sensitive frequency band.

The MP2908A's frequency can be programmed from 100kHz to 1000kHz with a resistor from FREQ to SGND (see Table 2). The value of R_{FREQ} for a given operating frequency can be calculated with Equation (6):

$$R_{FREQ}(k\Omega) = \frac{20000}{f_s(kHz)} - 1 \quad (6)$$

To get f_S = 500kHz, set R_{FREQ} to 39kΩ.

Table 2: Frequency vs. Resistor

Resistor (kΩ)	Frequency (kHz)
65	300
39	500
19	1000

V_{CC} Regulator Connection

VCC1 can be powered from both VIN and VCC2. If connecting VCC2 to an external power supply to improve the overall efficiency, VCC2 should be larger than 4.5V but smaller than 12V (see Figure 6).

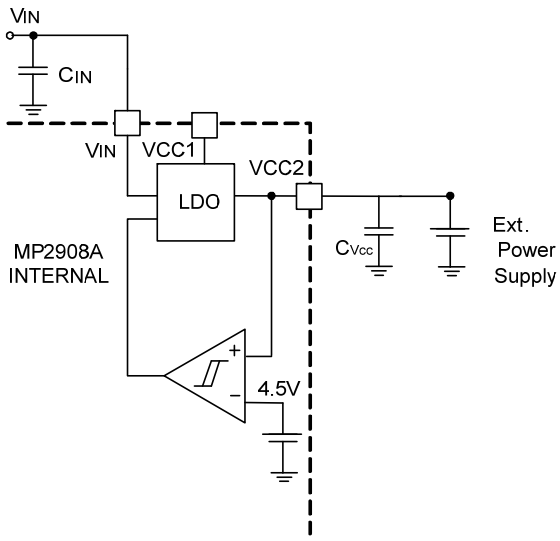


Figure 6: Internal Circuitry of VCC2

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If V_{OUT} is higher than 4.5V but less than 12V, VCC2 can be connected to V_{OUT} directly (see Figure 7).

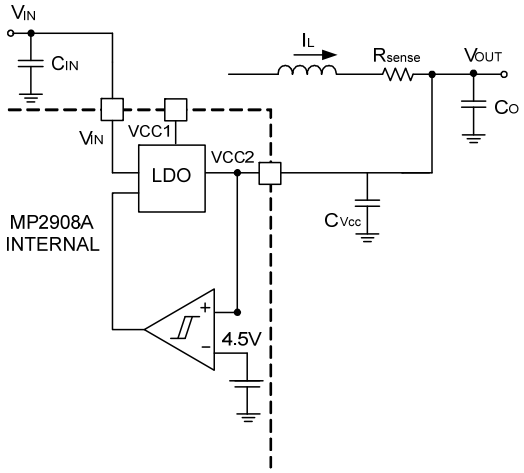


Figure 7: Configuration of VCC2 Connecting to V_{OUT}

Selecting the Inductor

An inductor with a DC current rating at least 25% higher than the maximum load current is recommended for most applications. A larger value inductor results in less ripple current and a lower output ripple voltage. However, the larger value inductor also has a larger physical size, higher series resistance, and lower saturation current. Choose the inductor ripple current approximately 30% of the maximum load current. The inductance value can be then be calculated with Equation (7):

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_S} \quad (7)$$

Where V_{OUT} is the output voltage, V_{IN} is the input voltage, f_S is the 300kHz switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

The maximum inductor peak current can be calculated with Equation (8):

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2} \quad (8)$$

Where I_{LOAD} is the load current.

Input Capacitor Selection

Since the input capacitor absorbs the input switching current, it requires an adequate ripple current rating. The selection of the input capacitor is based mainly on its maximum ripple current capability. The RMS value of the ripple current flowing through the input capacitor can be calculated with Equation (9):

$$I_{RMS} = I_{LOAD} \sqrt{\frac{V_{OUT}}{V_{IN}} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)} \quad (9)$$

The worst-case condition occurs at $V_{IN} = 2V_{OUT}$, shown in Equation (10):

$$I_{RMS} = I_{LOAD}/2 \quad (10)$$

The input capacitor must be capable of handling this ripple current.

Output Capacitor Selection

The output capacitor keeps the output voltage The output capacitor impedance should be low at the switching frequency. The output voltage ripple can be estimated with Equation (11):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C_O}\right) \quad (11)$$

Where C_O is the output capacitance value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

For tantalum or electrolytic capacitor application, the ESR dominates the impedance at the switching frequency. Formula 11 can then be approximated with Equation (12):

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR} \quad (12)$$

Compensation Components

The MP2908A employs current-mode control for easy compensation and fast transient response. COMP is the output of the internal error amplifier and controls system stability and transient response. A series capacitor-resistor combination sets a pole-zero combination to control the control system's characteristics. The DC gain of the voltage feedback loop can be calculated with Equation (13):

$$A_{VDC} = R_{LOAD} \times G_{CS} \times A_O \times \frac{V_{FB}}{V_{OUT}} \quad (13)$$

Where A_O is the error-amplifier voltage gain 3000V/V, G_{CS} is the current-sense transconductance $1/(12xR_{SENSE})$ (A/V), and R_{LOAD} is the load resistor value.

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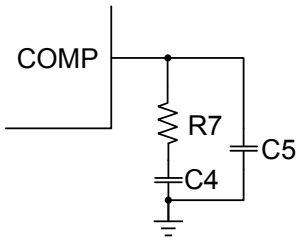


Figure 8: Compensation Network

The system has two important poles: one from the compensation capacitor (C4) and the output resistor of the error amplifier and the other from the output capacitor and the load resistor (see Figure 8). These poles can be calculated with Equation (14) and Equation (15):

$$f_{P1} = \frac{G_m}{2\pi \times C4 \times A_O} \quad (14)$$

$$f_{P2} = \frac{1}{2\pi \times Co \times R_{LOAD}} \quad (15)$$

Where G_m is the error-amplifier transconductance 500μA/V, and Co is the output capacitor.

The system has one important zero due to the compensation capacitor and the compensation resistor (R7), and can be calculated with Equation (16):

$$f_{Z1} = \frac{1}{2\pi \times C4 \times R7} \quad (16)$$

The system may have another significant zero if the output capacitor has a large capacitance or a high ESR value, and can be calculated with Equation (17):

$$f_{ESR} = \frac{1}{2\pi \times Co \times R_{ESR}} \quad (17)$$

In this case, a third pole set by the compensation capacitor (C5) and the compensation resistor can compensate for the effect of the ESR zero. This pole is calculated with Equation (18):

$$f_{P3} = \frac{1}{2\pi \times C5 \times R7} \quad (18)$$

The goal of the compensation design is to shape the converter transfer function for a desired loop gain. The system crossover frequency where the feedback loop has unity gain is important, since lower crossover frequencies result in slower line and load transient responses, and higher crossover frequencies lead to system instability. Set the crossover frequency to ~0.1×f_{SW}.

Follow the steps below to design the compensation:

1. Choose R7 to set the desired crossover frequency with Equation (19):

$$R7 = \frac{2\pi \times Co \times f_C}{G_m \times G_{CS}} \times \frac{V_{OUT}}{V_{FB}} \quad (19)$$

Where f_C is the desired crossover frequency.

2. Choose C4 to achieve the desired phase margin. For applications with typical inductor values, set the compensation zero (f_{Z1}) < 0.25 x f_C to provide a sufficient phase margin. C4 is then calculated with Equation (20):

$$C4 > \frac{4}{2\pi \times R7 \times f_C} \quad (20)$$

3. C5 is required if the ESR zero of the output capacitor is located at <0.5×f_{SW}, or Equation (21) is valid:

$$\frac{1}{2\pi \times Co \times R_{ESR}} < \frac{f_{SW}}{2} \quad (21)$$

If this is the case, use C5 to set the pole (f_{P3}) at the location of the ESR zero. Determine C5 with Equation (22):

$$C5 = \frac{Co \times R_{ESR}}{R7} \quad (22)$$

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TYPICAL APPLICATION CIRCUITS

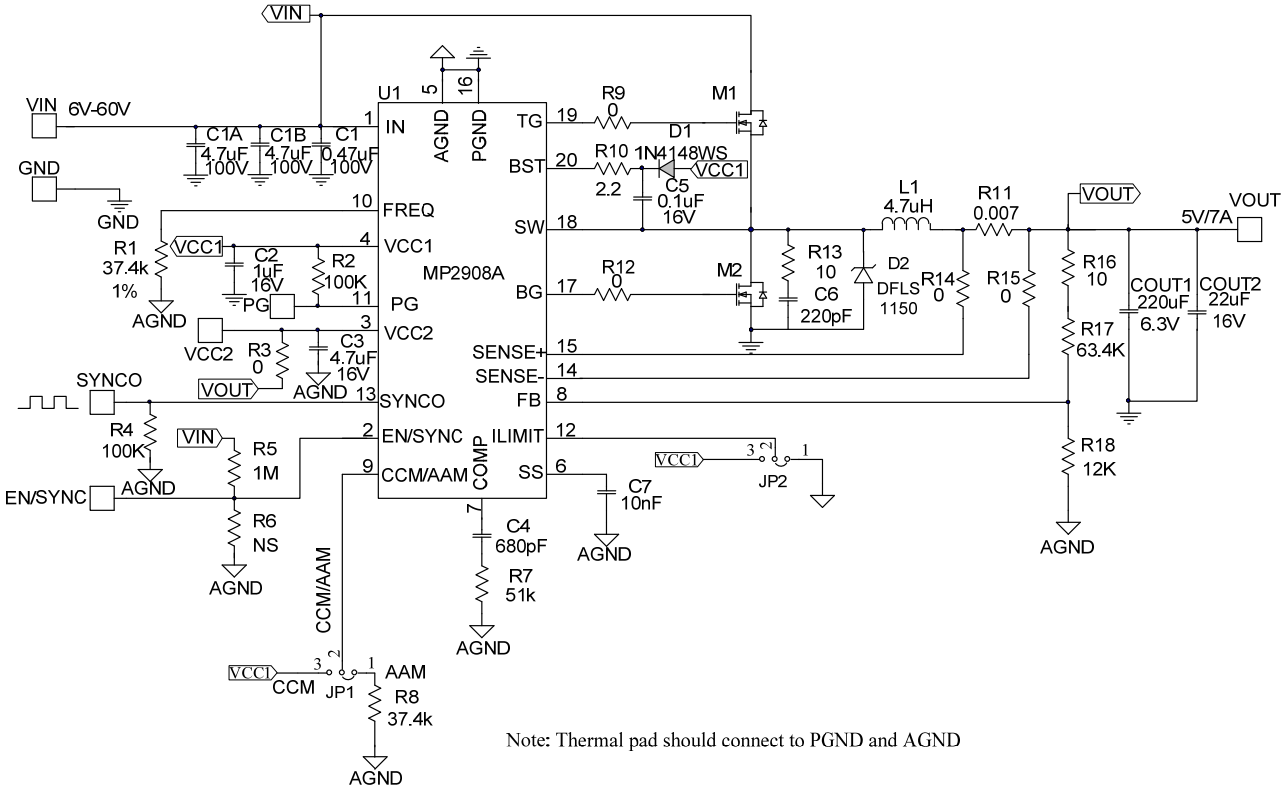


Figure 9: Application Circuit for 5V Output

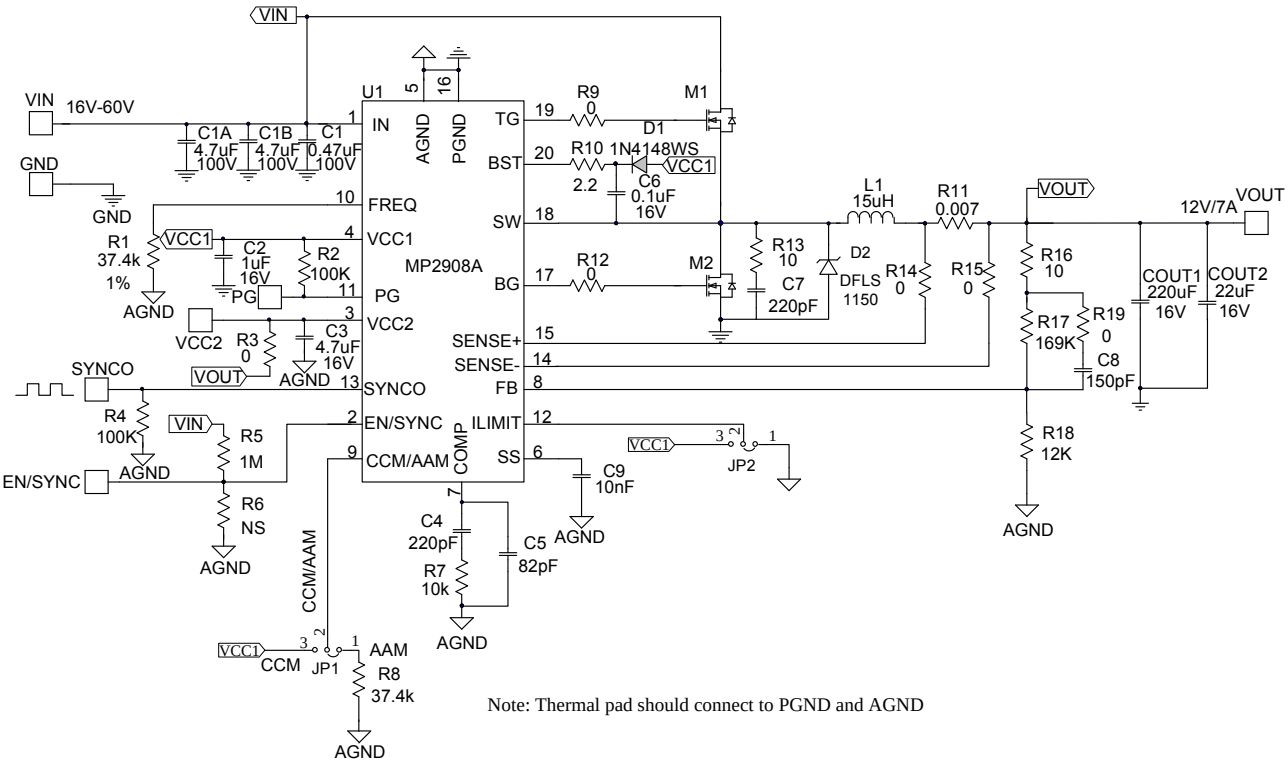


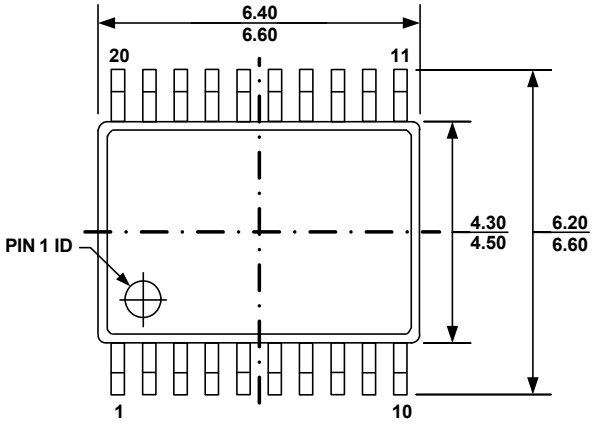
Figure 10: Application Circuit for 12V Output

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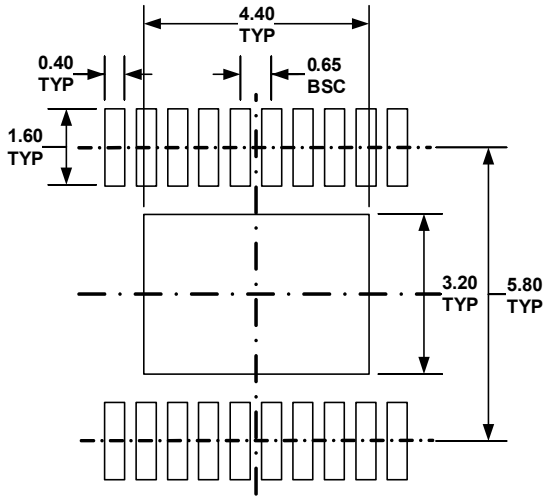
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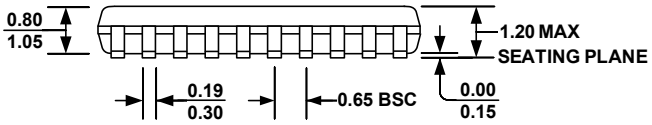
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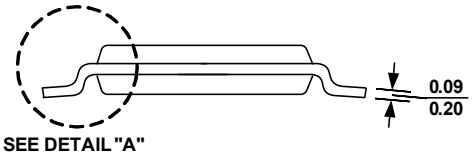
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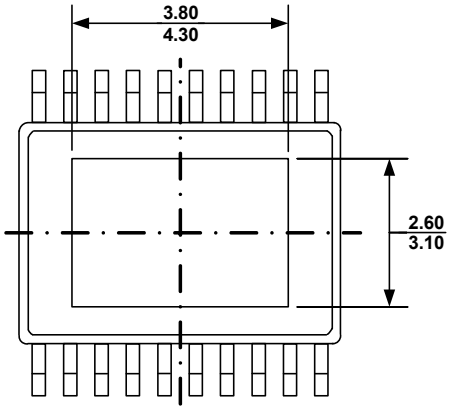
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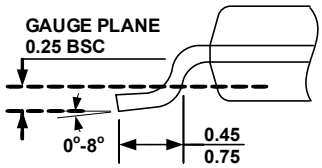
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

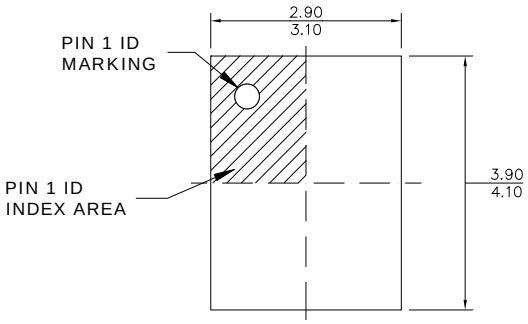
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1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE

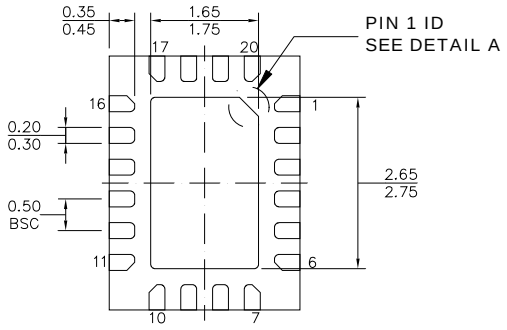
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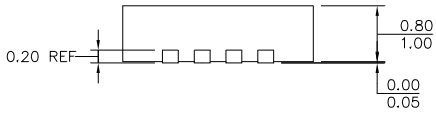
QFN-20 (3mmx4mm)



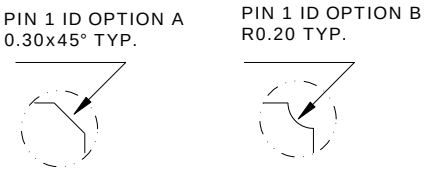
TOP VIEW



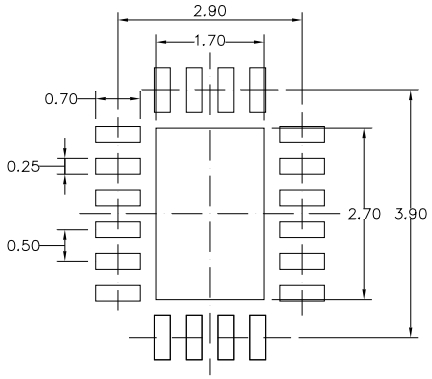
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH.
3) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
4) JEDEC REFERENCE IS MO-220.
5) DRAWING IS NOT TO SCALE.

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