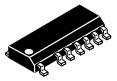
Current-Mode Controller, Fixed Frequency, for Two-Switch Forward Converter

NCL30125



SOIC−16
CASE 751DU

The NCL30125 is a fixed−frequency current−mode controller featuring the Dynamic Self−Supply (DSS). This function greatly simplifies the design of the auxiliary supply and the V_{CC} capacitor by activating the internal startup current source to supply the controller during start−up, transients, latch, stand−by etc.

With a supply range up to 35 V, the controller hosts an adjustable switching frequency with jittering function operated in peak current mode control. When the power on the secondary side drops drastically, the part enters skip cycle while limiting the peak current that insures the output voltage regulation and excellent efficiency in light load condition.

It features a timer−based fault detection that ensures the detection of overload and a brown−out protection against low input voltages.

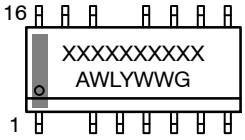
Features

- Integrated High−side Driver
- Adjustable Switching Frequency Up to 300 kHz
- Peak Current−mode Control
- Skip Mode to Maximize Performance in Light Load Conditions
- High−voltage Current Source with DSS
- Brown−out (BO) Detection
- Internal Slope Compensation
- Adjustable Soft−start Duration
- Frequency Jittering
- 15 ms Timer−based Short−circuit Protection with Auto−recovery or Latched Operation
- Auto−recovery or Latched OVP on V_{CC}
- Latched OVP/OTP Input for Improved Robustness
- 35−V V_{cc} Operation
- +0.9 A / −1.2 A Peak Source/Sink Drive Capability
- Internal Thermal Shutdown
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

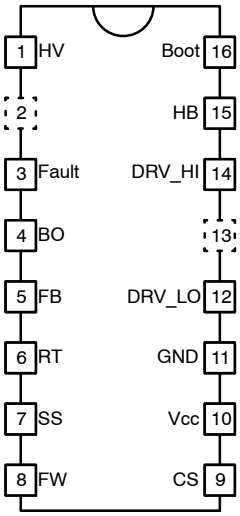
- Power Supplies for PC Silver Boxes, Games Adapter
- Two−Switch Forward Converter
- Dc−to−Dc Application Capability

MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

PIN CONNECTION



ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 34 of this data sheet.

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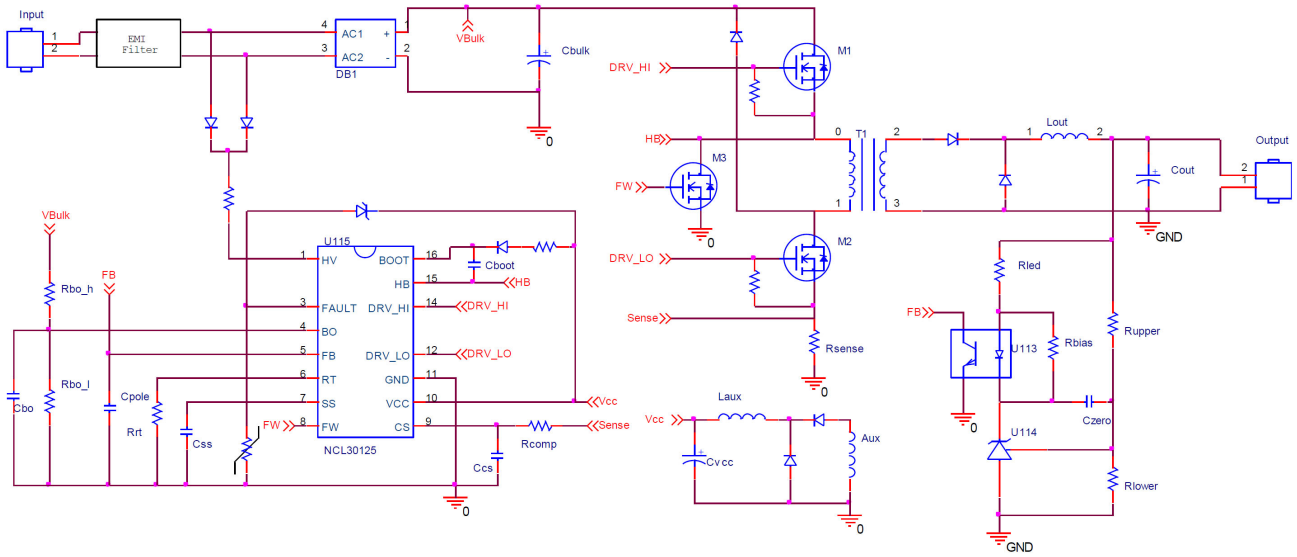


Figure 1. Two−Switch Forward Application Schematic

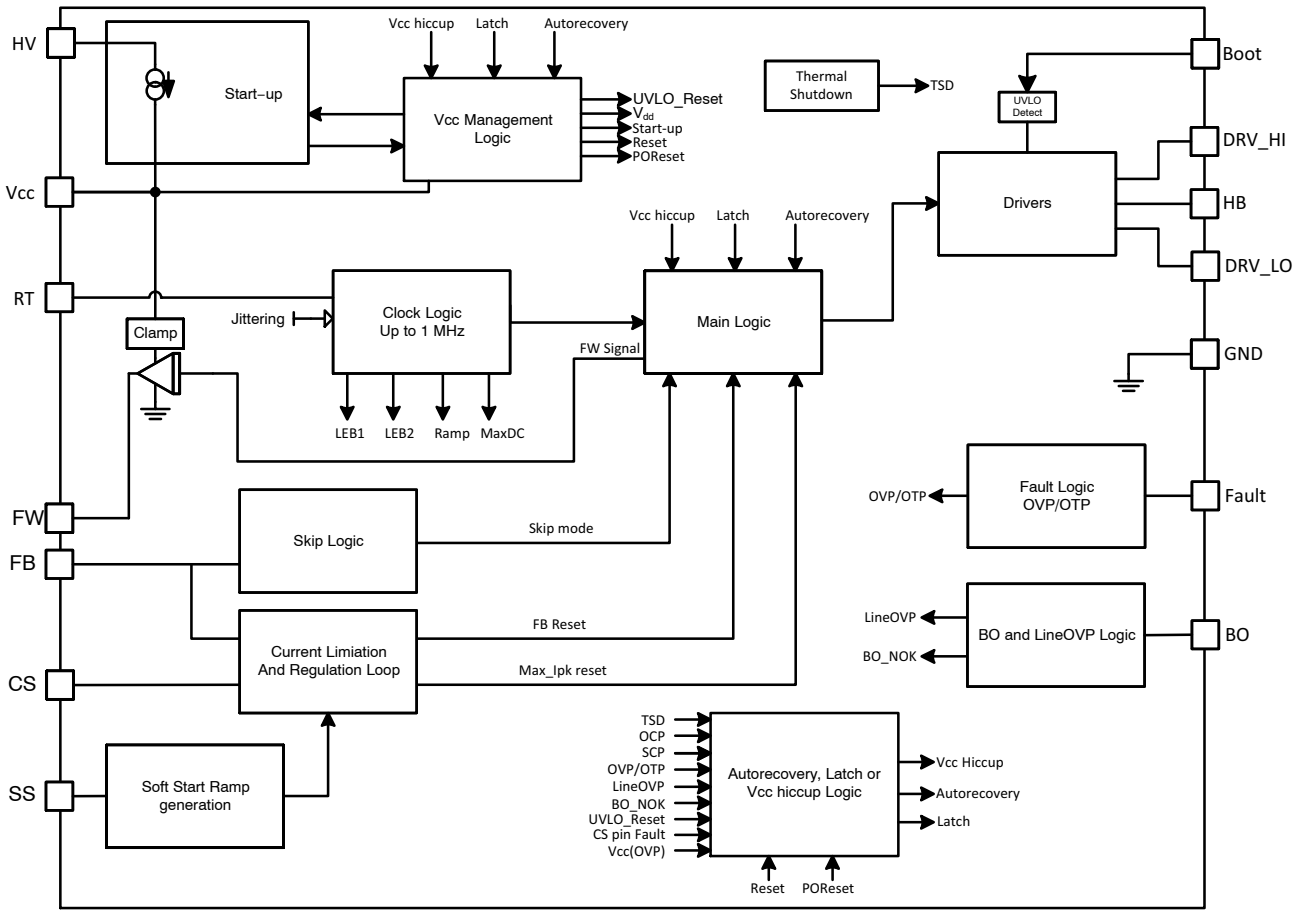


Figure 2. Simplified Block Diagram

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PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	HV	Connected to the rectified ac line, this pin powers the internal current source to deliver a startup current.
2	NC	Non−connected for improved creepage
3	Fault	The controller enters fault mode if the voltage of this pin is pulled above or below the fault thresholds. A precise pull up current source allows direct interface with an NTC thermistor. Fault detection triggers a latch
4	BO	This pin monitors the input voltage to offer a Brown−out protection
5	FB	Hooking an optocoupler collector to this pin will allow regulation
6	RT	A resistor connected to ground fixes the switching frequency
7	SS	A capacitor connected to ground selects the soft−start duration
8	FW	The driver's output used to refresh the bootstrap capacitor during startup or skip mode
9	CS	This pin monitors the primary peak current but also used to select the ramp compensation amplitude. When CS pin is brought above 0.75 V, the part detects the 2nd OCP level
10	V_{cc}	This pin is connected to an external auxiliary voltage. An OVP comparator monitors this pin and offers a means to stop the converter in fault conditions
11	GND	The controller ground
12	DRV_LO	The driver's output to an external low−side MOSFET gate
13	NC	Non−connected for improved creepage
14	DRV_HI	The driver's output to an external high−side MOSFET gate
15	HB	Connects to the half−bridge output
16	Boot	The floating V_{cc} supply for the upper stage

OPTIONS

Device	OCP Protection	SCP Protection	V_{cc} OVP Protection	Fault OTP/OVP protection (Pin 3)	FW (Pin 8) in normal operation
NCL30125A2	Latched	Latched	Autorecovery	Latched	Enabled
NCL30125B2	Autorecovery	Autorecovery	Autorecovery	Latched	Enabled

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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply voltage, V_{cc} pin, continuous voltage	V_{cc}	−0.3 to 35	V
Maximum voltage on low power pins FB, BO, CS, RT, SS and Fault		−0.3 to 5.5	V
FW Driver Output Voltage (Pin 8) (Note 3)	V_{FW}	−0.3 to V_{cc} + 0.3	V
Low Side Driver Output Voltage (Pin 11)	V_{DRV_LO}	−0.3 to V_{cc} + 0.3	V
High Side Driver Output Voltage (Pin 16)	V_{DRV_HI}	V_{HB} − 0.3 to V_{BOOT} + 0.3	V
High Side Offset Voltage (Pin 15)	V_{HB}	V_{Boot} − 20 to V_{Boot} + 0.3	V
High Side Boot Voltage (Pin 16) T_J = −40°C to +125°C	V_{BOOT}	−0.3 to 620	V
High Side Floating Supply Voltage (Pin 15 and 16)	$V_{boot} - V_{HB}$	−0.3 to 20.0	V
High Voltage Pin Voltage	HV	−0.3 to 700	V
Thermal Resistance Junction−to−Air Single layer PCB 50 mm^2, 2 Oz Cu Printed Circuit Copper Clad	$R_{\theta J-A}$	163	°C/W
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−60 to 150	°C
ESD Capability, Human Body Model − All pins except HV (Note 4)	ESD_{HBM}	3	kV
Charged Device Model ESD capability per JEDEC JESD22−C101E	ESD_{CDM}	1	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and/or APPLICATION INFORMATION for Safe Operating parameters.
2. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
3. Maximum current flowing into pin 8 in high state must be limited to 10 mA.
4. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Charged Device Model tested per JEDEC standard: JESD22, Method C101E
   Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78, except pin 8 (FW) in high state. Maximum current flowing into pin 8 in high state must be limited to 10 mA.
5. Values based on copper area of 25 mm^2 of 2 oz copper thickness and FR4 PCB substrate.

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ELECTRICAL CHARACTERISTICS

For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C; V_{HV} = 100 V, V_{CC} = 12 V unless otherwise noted. (Notes 6, 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
STARTUP SECTION						
Minimum voltage for current source operation	I_{HV} = 6 mA, V_{CC} = $V_{CC(on)}$ − 0.5 V	$V_{HV(min)}$	–	30	60	V
Current delivered by the internal HV current source	V_{CC} = 0 V	I_{start1}	0.2	0.5	0.8	mA
Current delivered by the internal HV current source	V_{CC} = $V_{CC(on)}$ − 0.5 V	I_{start2}	8.0	11.0	14.0	mA
Current delivered by the internal HV current source for lower HV pin voltage	V_{CC} = $V_{CC(on)}$ − 0.5 V, V_{HV} = 35 V	I_{start3}	3.0	10.0	14.0	mA
HV pin leakage current	V_{HV} = 600 V	I_{leak1}	–	1.5	10.0	μA
SUPPLY SECTION						
Startup Threshold HV current source stop threshold	V_{cc} increasing	$V_{cc(on)}$	15.0	16.0	17.0	V
HV current source restart threshold	V_{cc} decreasing	$V_{cc(min)}$	9.0	10.0	11.0	V
Minimum Operating Voltage	V_{cc} decreasing	$V_{cc(off)}$	8.0	8.8	9.4	V
Internal Latch / Logic Reset Level		$V_{cc(reset)}$	–	8.55	–	V
Hysteresis above $V_{cc(off)}$ for fast hiccup in latch mode		$V_{cc(hyst)}$	0.1	0.25	0.5	V
Hysteresis below $V_{cc(off)}$ before Latch reset		$V_{cc(reset_hyst)}$	0.1	0.4	0.7	V
V_{CC} level for I_{start1} to I_{start2} transition		$V_{cc(inhibit)}$	0.5	1.0	1.5	V
Internal IC consumption	V_{FB}=2.0 V , f_{sw}=100 kHz and C_L = 0	$I_{CC(steady1)}$	–	1.8	2.2	mA
Internal IC consumption	V_{FB}=2.0 V , f_{sw}=100 kHz and C_L = 1 nF	$I_{CC(steady2)}$	–	2.8	3.3	mA
Internal IC consumption in Skip cycle	V_{CC} = 12 V, V_{FB} = V_{skip} − 50 mV	$I_{CC(stb)}$	–	780	–	μA
Internal IC consumption in fault mode (after a fault when V_{cc} decreasing to $V_{cc(off)}$)	Autorecovery or latch mode	$I_{CC(fault)}$	–	740	–	μA
Internal IC consumption before start−up	V_{cc} < $V_{cc(reset)}$ + $V_{cc(hyst)}$ and FB pin unloaded	$I_{CC(start1)}$	–	100	190	μA
Internal IC consumption before start−up	V_{cc} = 9.5 V and FB pin unloaded	$I_{CC(start2)}$	–	800	950	μA
Internal IC consumption before start−up	$V_{cc(min)}$ < V_{cc} < $V_{cc(on)}$ and FB pin unloaded	$I_{CC(start3)}$	–	1.05	1.7	mA
BOOTSTRAP SECTION						
Startup voltage on the floating section		$V_{Boot(on)}$	8.1	8.5	9.1	V
Cutoff voltage on the floating section	Minimum operating voltage	$V_{Boot(off)}$	7.5	7.9	8.5	V
Upper driver consumption	No DRV pulses	$I_{Boot(STB)}$	–	75	130	μA
Upper driver consumption	C_L = 0 nF between Pins 14 & 16 f_{sw}= 100 kHz, HB connected to GND	I_{Boot1}	–	0.19	0.35	mA
Upper driver consumption	C_L = 1 nF between Pins 14 & 16 f_{sw}= 100 kHz, HB connected to GND	I_{Boot2}	–	1.6	2.0	mA
Minimum Internal delay from ONIPP ends to 1st DRV pulse	Note: SS ramp start with the 1st DRV pulse	$t_{boot(start)}$	180	200	220	μs
FW OUTPUT						
Delay to turn on the FW signal	Duration between the DRV falling edge and the FW pin rising edge	t_{delay1}	480	550	630	ns
Delay to turn off the FW signal	Duration between the FW pin falling edge and the DRV rising edge	t_{delay2}	120	150	185	ns

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ELECTRICAL CHARACTERISTICS (continued)

For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C; V_{HV} = 100 V, V_{CC} = 12 V unless otherwise noted. (Notes 6, 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
FW OUTPUT						
Peak source current	FW high state, V_{FW} = 0 V V_{cc} = $V_{cc(off)}$ + 0.2 V, C_L = 1 nF (Note 8)	$I_{source(FW)}$	–	100	–	mA
Peak sink current	FW low state, V_{FW} = V_{cc} V_{cc} = $V_{cc(off)}$ + 0.2 V, C_L = 1 nF (Note 8)	$I_{sink(FW)}$	–	200	–	mA
Source resistance		$R_{OH(FW)}$	–	33	–	Ω
Sink resistance		$R_{OL(FW)}$	–	11.0	–	Ω
High State Voltage (Low V_{CC} level)	V_{cc} = $V_{CC(off)}$ + 0.2 V, R_{FW} = 33 kΩ FW high state	$V_{FW(low)}$	7.6	–	–	V
High State Voltage (High V_{CC} level)	V_{cc} = $V_{cc(OVP)}$ − 0.2 V, FW high state and unloaded	$V_{FW(clamp)}$	11.0	12.7	16.0	V
DRIVE OUTPUTS						
Rise Time (10−90%)	V_{DRV} from 10 to 90% V_{cc} = $V_{cc(off)}$ + 0.2 V, C_L = 1 nF	t_r	–	13	22	ns
Fall Time (90−10%)	V_{DRV} from 90 to 10% V_{cc} = $V_{cc(off)}$ + 0.2 V , C_L = 1 nF	t_f	–	13	22	ns
Source resistance		R_{OH}	–	2.6	–	Ω
Sink resistance		R_{OL}	–	2.1	–	Ω
Peak source current	DRV high state, V_{DRV} = 0 V V_{cc} = $V_{cc(off)}$ + 0.2 V, C_L = 1 nF (Note 8)	I_{source}	–	0.9	–	A
Peak sink current	DRV low state, V_{DRV} = V_{cc} V_{cc} = $V_{cc(off)}$ + 0.2 V, C_L = 1 nF (Note 8)	I_{sink}	–	1.2	–	A
High State Voltage (Low V_{CC} level)	V_{cc} = $V_{CC(off)}$ + 0.2 V, R_{DRV} = 33 kΩ DRV high state	$V_{DRV(low)}$	8.8	–	–	V
High State Voltage (High V_{CC} level)	V_{cc} = $V_{cc(OVP)}$ − 0.2 V, DRV_LO high state and unloaded	$V_{DRV(clamp)}$	11.0	13.5	16.0	V
CURRENT COMPARATOR						
Maximum Internal Current Setpoint		V_{ILimit}	0.470	0.500	0.530	V
Short Current Protection Threshold		$V_{CS(stop)}$	0.69	0.75	0.81	V
Leading Edge Blanking Duration	R_{RT} = 200 kΩ R_{RT} = 100 kΩ R_{RT} = 32 kΩ (Note 9)	t_{LEB1}	– – –	300 285 200	– – –	ns
Abnormal Overcurrent Fault Blanking Duration for $V_{CS(stop)}$	R_{RT} = 200 kΩ R_{RT} = 100 kΩ R_{RT} = 32 kΩ (Note 9)	t_{LEB2}	– – –	100 90 50	– – –	ns
Propagation delay from V_{ILimit} to DRV off−state	C_{DRV} = 0 nF	t_{delay}	–	40	80	ns
Number of clock cycles before fault confirmation		t_{count}	–	4	–	
Pull−up Current Source on CS pin for Open detection	Before start−up only	I_{CS}	–	60	–	μA
CS pin Open detection	CS pin open	$V_{CS(open)}$	–	0.75	–	V

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ELECTRICAL CHARACTERISTICS (continued)

For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C; V_{HV} = 100 V, V_{CC} = 12 V unless otherwise noted. (Notes 6, 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
INTERNAL OSCILLATOR						
Oscillation Frequency	R_{RT} = 200 kΩ R_{RT} = 100 kΩ R_{RT} = 32 kΩ	f_{OSC}	46 92 275	51 100 300	58 108 325	kHz
Maximum allowed switching frequency for A2 and B2 versions		F_{max}	–	300	–	kHz
Maximum duty−cycle	R_{RT} = 100 kΩ	D_{max}	43.0	45.0	48.0	%
Maximum duty−cycle	R_{RT} = 32 kΩ	D_{max}	40.8	42.5	46.0	%
Frequency jittering	In percentage of f_{OSC}	f_{jitter}	–	±5	–	%
Swing frequency		f_{swing}	–	300	–	Hz
FEEDBACK SECTION						
FB internal pull−up resistor		R_{FB}	–	11.6	–	kΩ
Equivalent ac resistor from FB to GND	(Note 8)	R_{eq}	–	10	–	kΩ
Internal pull−up voltage on FB pin	FB open	$V_{FB(ref)}$	4.0	4.3	–	V
V_{FB} to Current Setpoint Division Ratio		K_{FB}	–	4	–	
INTERNAL RAMP COMPENSATION						
Internal Ramp Compensation Voltage	(Note 8)	V_{ramp}	–	3.5	–	V
Internal Ramp Compensation resistance to CS pin	(Note 8)	R_{ramp}	–	26.5	–	kΩ
SOFT START						
Soft−start pull−up current source	SS pin = GND	I_{SS}	4.5	5.2	6.0	μA
Soft start completion voltage threshold		V_{SS}	1.8	2.0	2.2	V
SKIP SECTION						
Skip threshold		V_{skip}	–	0.3	–	V
Skip threshold Hysteresis		$V_{skip(HYS)}$	–	50	–	mV
BROWN−OUT (BO)						
Brown−out function is disabled below this level (Before the 1st DRV pulse only)		$V_{BO(en)}$	80	100	120	mV
Pull−down Current Source on BO pin for Open detection		$I_{BO(en)}$	–	400	–	nA
Brown−out level at which the controller starts pulsing	V_{BO} increasing	$V_{BO(on)}$	0.76	0.80	0.84	V
Brown−out level at which the controller stops pulsing	V_{BO} decreasing	$V_{BO(off)}$	0.66	0.70	0.74	V
Brown−out filter duration		t_{BO}	40	50	60	ms
Brown−out input bias current	V_{BO} = 2.5 V	$I_{BO(bias)}$	–	–	50	nA
Line OVP level at which the controller stops pulsing	V_{BO} increasing	$V_{LineOVP(on)}$	2.6	2.9	3.2	V
Line OVP level at which the controller resumes operation	V_{BO} decreasing	$V_{LineOVP(off)}$	2.3	2.6	2.9	V
Blanking time for Line OVP detection		$t_{LineOVP(blank)}$	–	20	–	μs
FAULT INPUT (OTP/OVP)						
Overvoltage protection threshold	V_{Fault} increasing	$V_{Fault(OVP)}$	2.43	2.5	2.57	V
Overtemperature protection threshold	V_{Fault} decreasing, T_J = 110 °C	$V_{Fault(OTP)}$	0.36	0.40	0.44	V

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ELECTRICAL CHARACTERISTICS (continued)

For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C; V_{HV} = 100 V, V_{CC} = 12 V unless otherwise noted. (Notes 6, 7)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
FAULT INPUT (OTP/OVP)						
NTC biasing current	V_{Fault} = 0 V	I_{OTP}	40	50	60	μA
OTP resistance threshold	External NTC resistance is going down T_J = 110 °C	R_{OTP}	7.6	8.0	8.4	kΩ
Blanking time for OTP input during startup		$t_{OTP(blank)}$	7.3	8.0	8.7	ms
NTC biasing current during start−up only	V_{Fault} = 0 V − During $t_{OTP(blank)}$ only	$I_{OTP(boost)}$	80	100	120	μA
Fault clamping voltage	I_{fault} = 0 mA (V_{Fault} = open)	$V_{Fault(clamp)0}$	1.0	1.2	1.4	V
Fault clamping voltage	I_{fault} = 1 mA	$V_{Fault(clamp)1}$	1.8	2.4	3.0	V
Fault filter time		$t_{Fault(filter)}$	−	10	−	μs
Number of clock cycles before latch confirmation (after elapsing $t_{Fault(filter)}$)		$t_{latch(count)}$	−	4	−	
OVERCURRENT PROTECTION (OCP)						
Internal OCP timer duration		t_{OCP}	12	15	18	ms
Autorecovery timer		$t_{autorec}$	0.85	1	1.35	s
V_{CC} OVERVOLTAGE (VCC OVP)						
Over Voltage Protection on V_{CC} pin	V_{cc} increasing	$V_{cc(OVP)}$	24.0	25.9	27.0	V
Over Voltage Protection on V_{CC} pin Hysteresis	V_{cc} decreasing	$V_{cc(OVP_hyst)}$	−	0.8	−	V
Blanking before OVP on V_{CC} confirmation		$t_{OVP(blank)}$	−	10	−	μs
THERMAL SHUTDOWN (TSD)						
Temperature shutdown	T_J increasing − (Note 8)	T_{SHDN}	135	150	165	°C
Temperature shutdown hysteresis	T_J decreasing − (Note 8)	$T_{SHDN(hyst)}$	−	20	−	°C

6. Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
7. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
8. Guaranteed by design.
9. The LEB duration does not include the propagation delay.

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TYPICAL CHARACTERISTICS

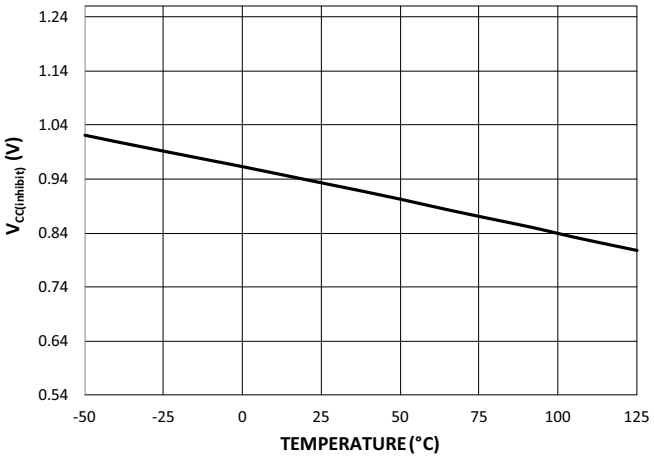


Figure 3. $V_{cc(inhibit)}$ vs. Junction Temperature

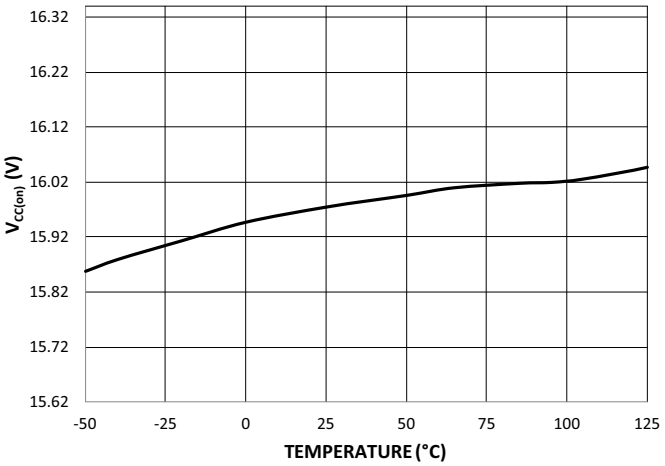


Figure 4. $V_{cc(on)}$ vs. Junction Temperature

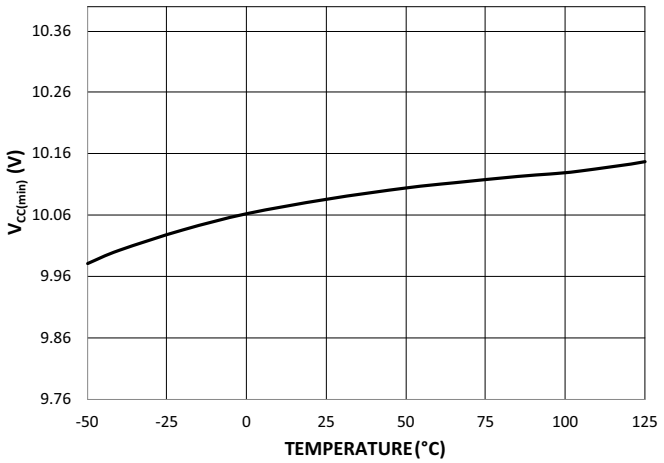


Figure 5. $V_{cc(min)}$ vs. Junction Temperature

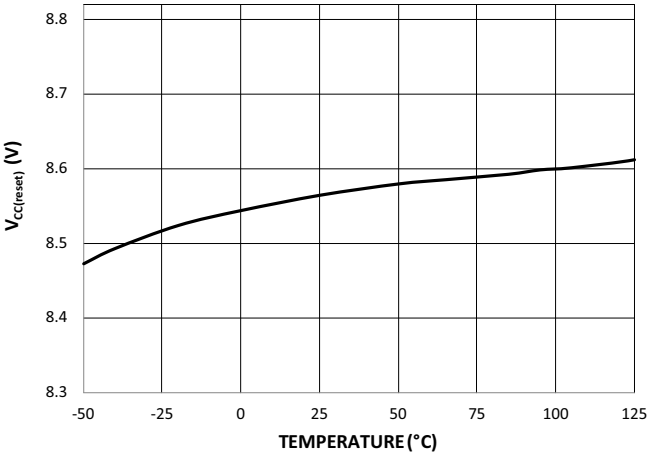


Figure 6. $V_{cc(reset)}$ vs. Junction Temperature

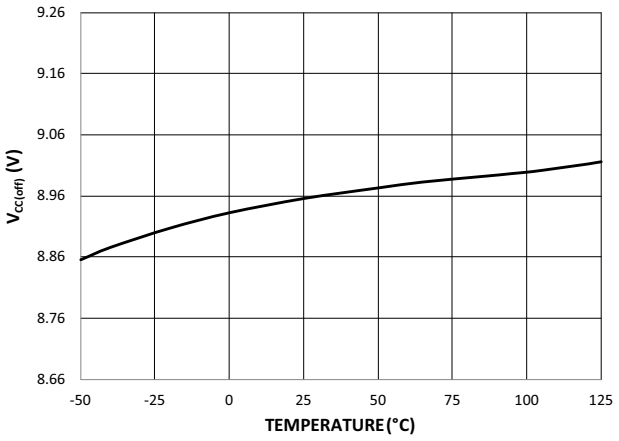


Figure 7. $V_{cc(off)}$ vs. Junction Temperature

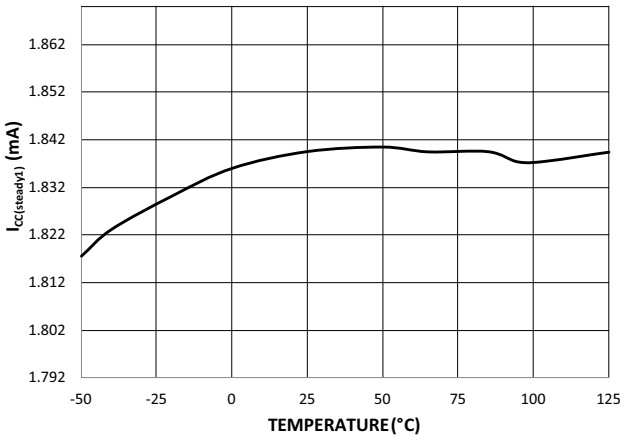


Figure 8. $I_{CC(steady1)}$ vs. Junction Temperature

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TYPICAL CHARACTERISTICS

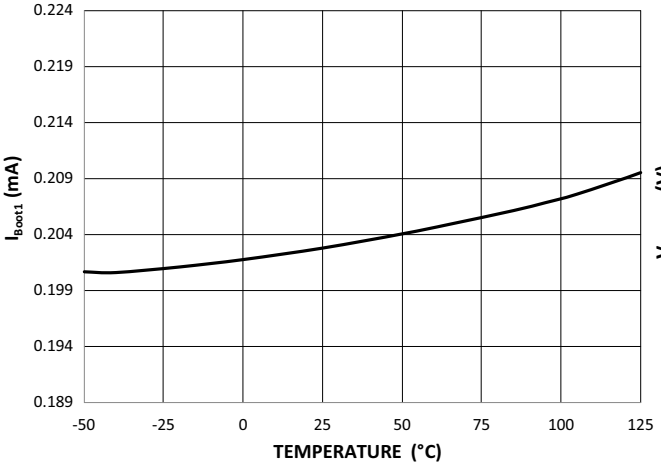


Figure 9. I_{Boot1} vs. Junction Temperature

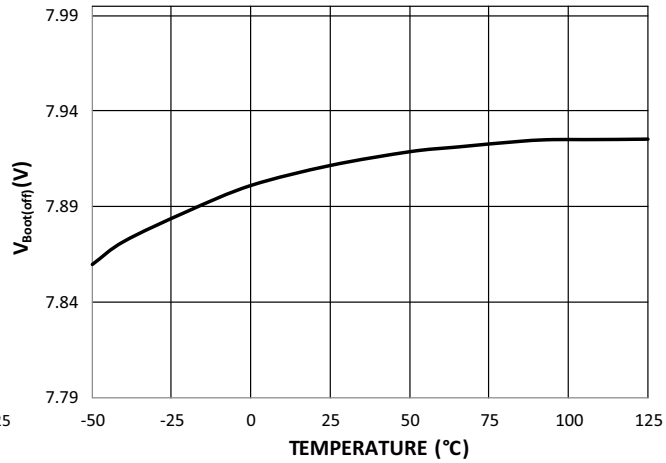


Figure 10. $V_{Boot(off)}$ vs. Junction Temperature

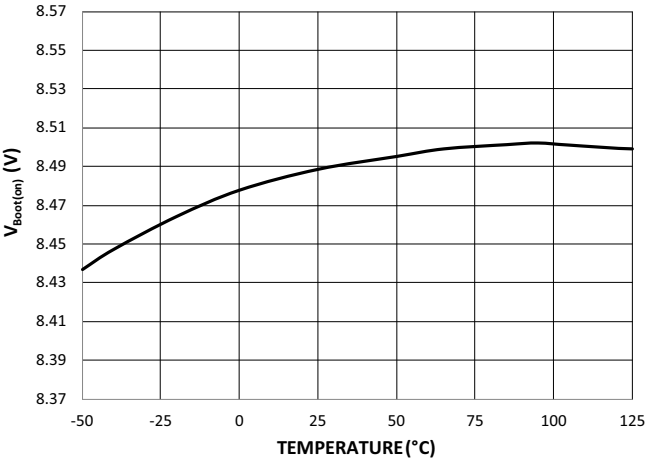


Figure 11. $V_{Boot(off)}$ vs. Junction Temperature

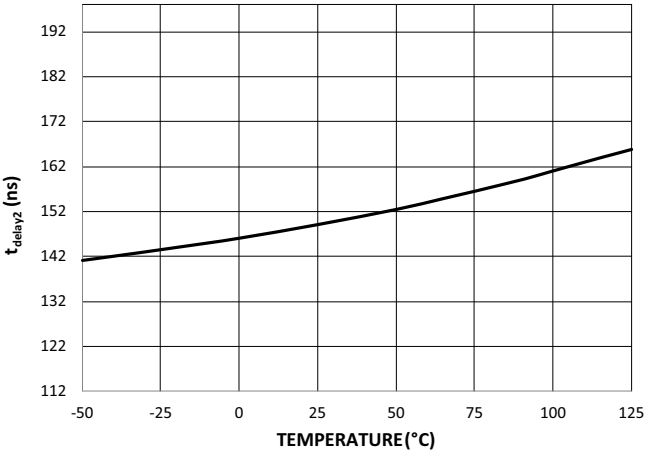


Figure 12. t_{delay2} vs. Supply Voltage

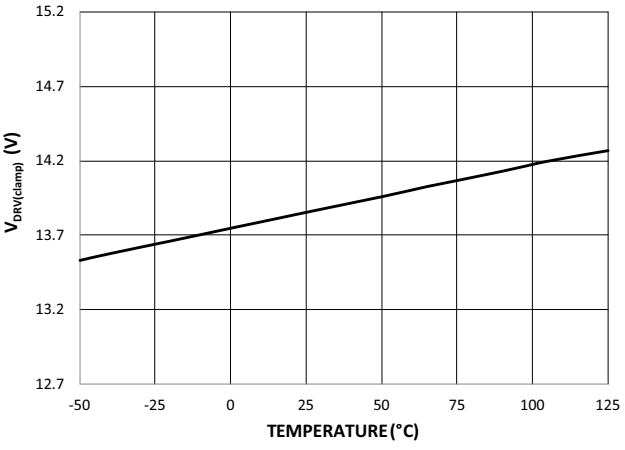


Figure 13. $V_{DRV(clamp)}$ vs. Junction Temperature

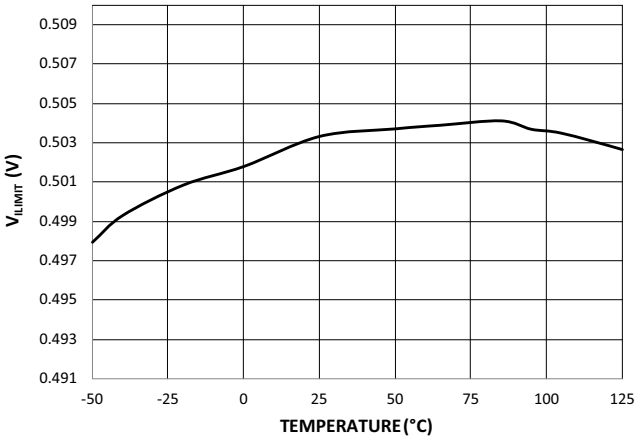


Figure 14. V_{ILIMIT} vs. Junction Temperature

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TYPICAL CHARACTERISTICS

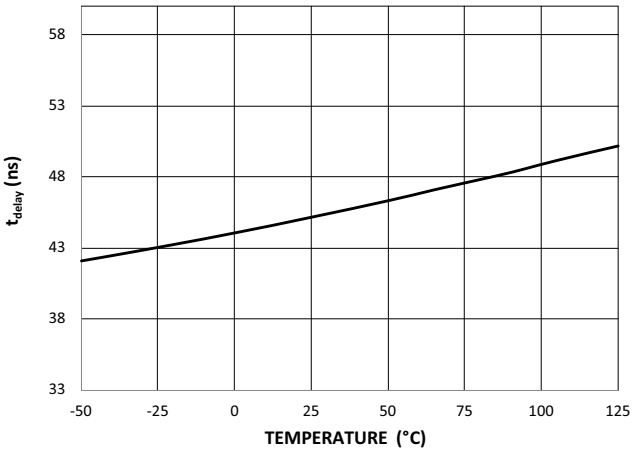


Figure 15. t_{delay} vs. Junction Temperature

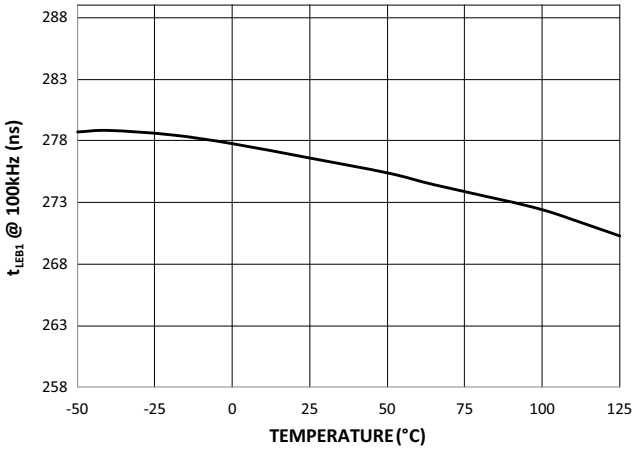


Figure 16. t_{LEB1} @ 100 kHz vs. Junction Temperature

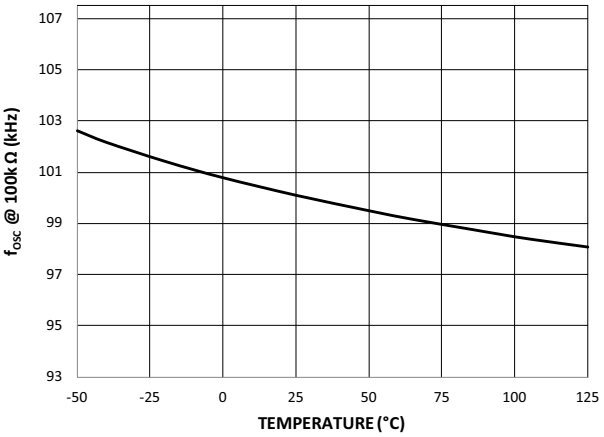


Figure 17. f_{OSC} @ 100 kΩ vs. Junction Temperature

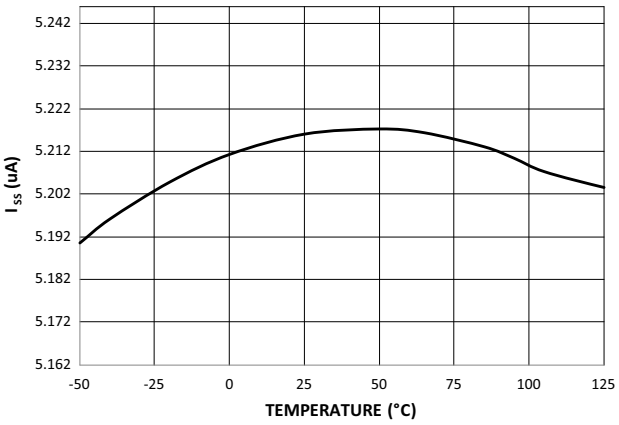


Figure 18. I_{SS} vs. Junction Temperature

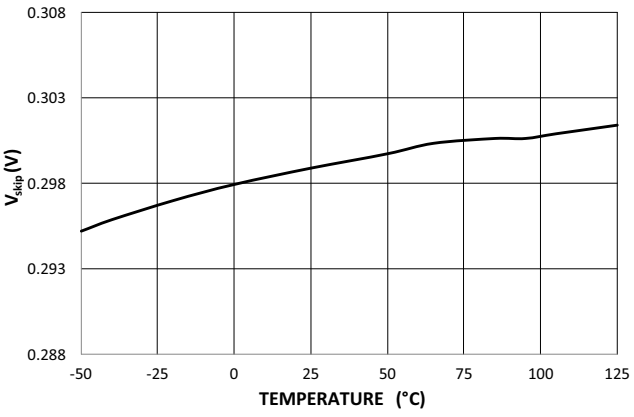


Figure 19. V_{skip} vs. Junction Temperature

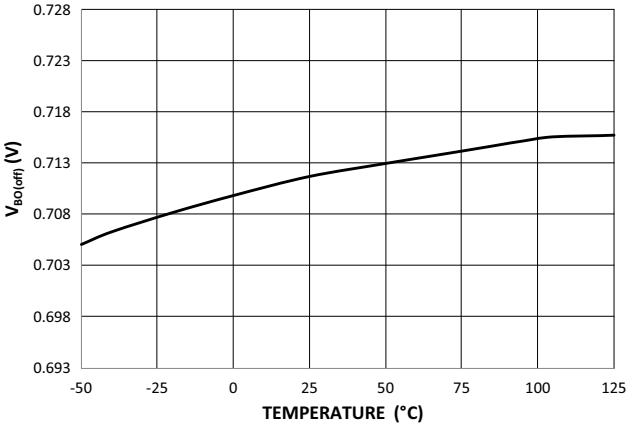


Figure 20. $V_{BO(off)}$ vs. Junction Temperature

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TYPICAL CHARACTERISTICS

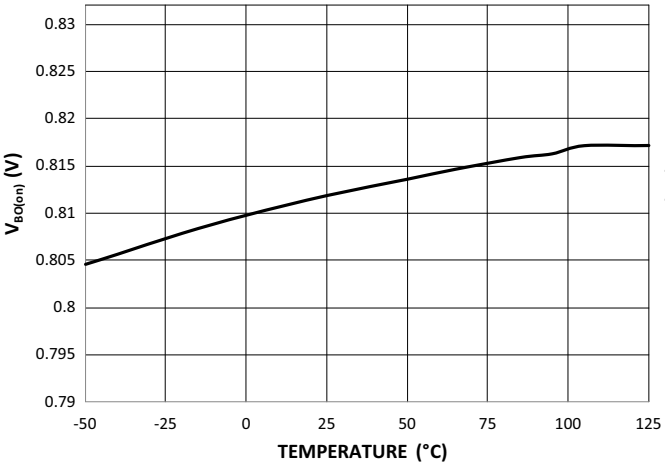


Figure 21. $V_{BO(on)}$ vs. Junction Temperature

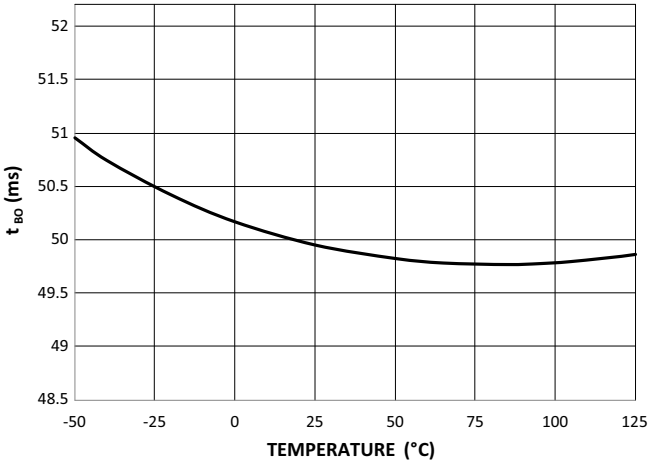


Figure 22. t_{BO} vs. Junction Temperature

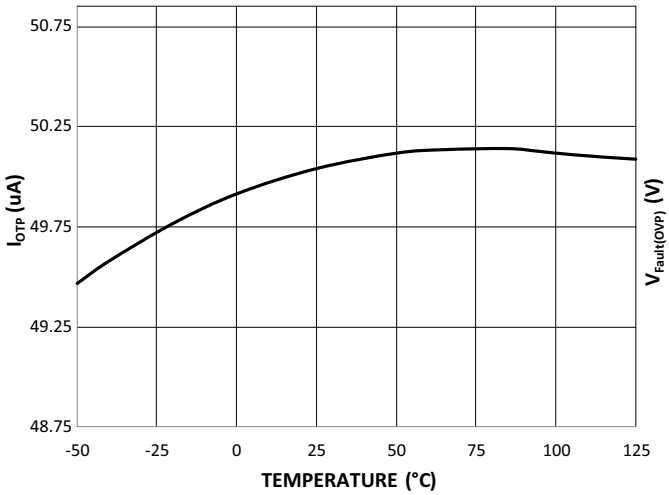


Figure 23. I_{OTP} vs. Junction Temperature

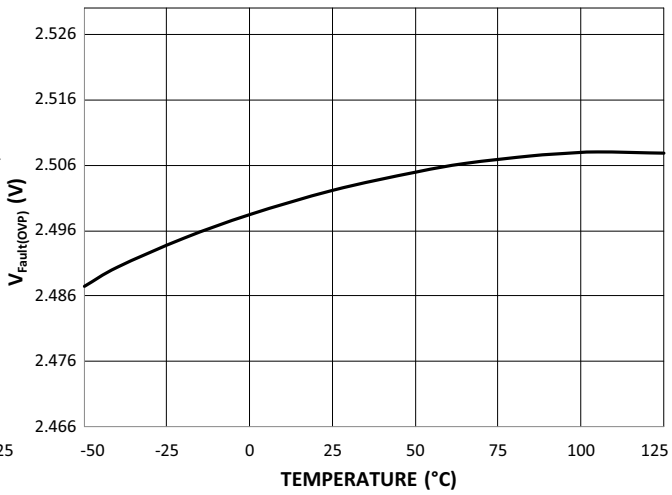


Figure 24. $V_{Fault(OVP)}$ vs. Junction Temperature

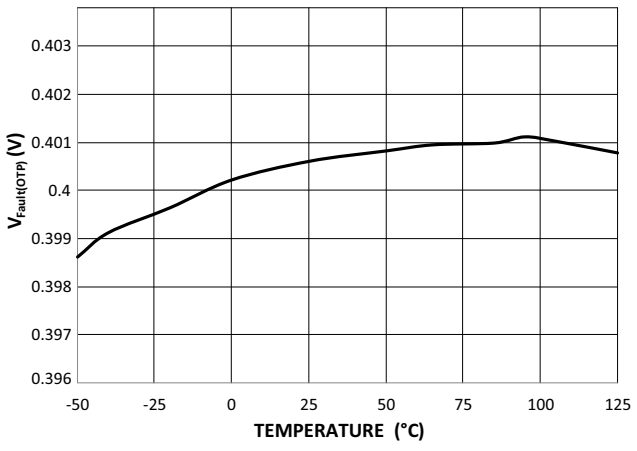


Figure 25. $V_{Fault(OTP)}$ vs. Junction Temperature

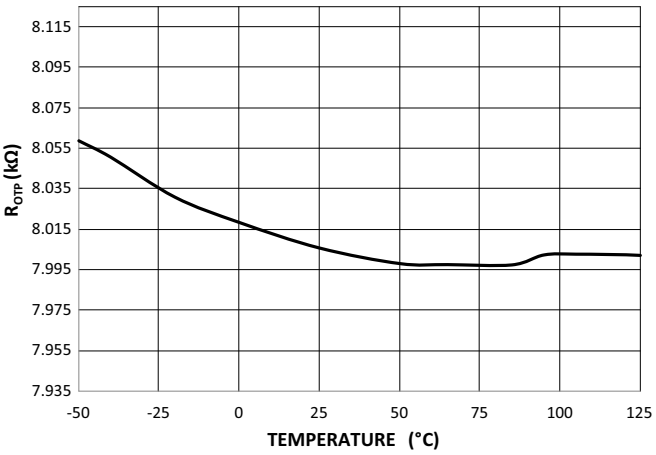


Figure 26. R_{OTP} vs. Junction Temperature

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TYPICAL CHARACTERISTICS

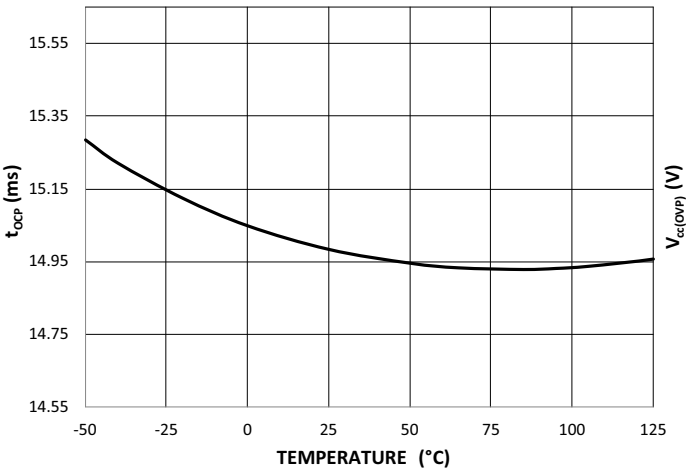


Figure 27. t_{OCP} vs. Junction Temperature

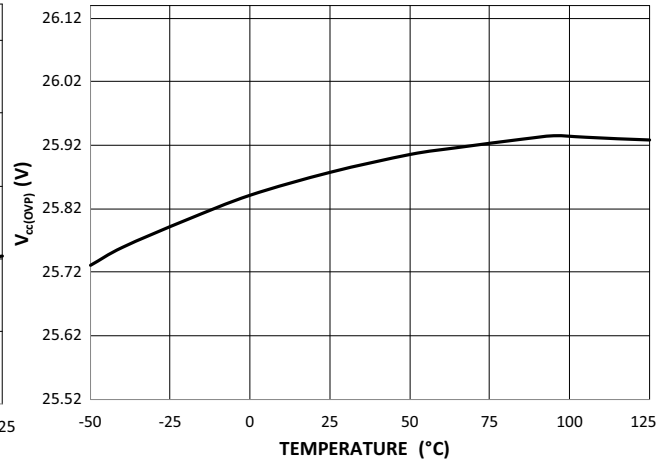


Figure 28. $V_{CC(OVP)}$ vs. Junction Temperature

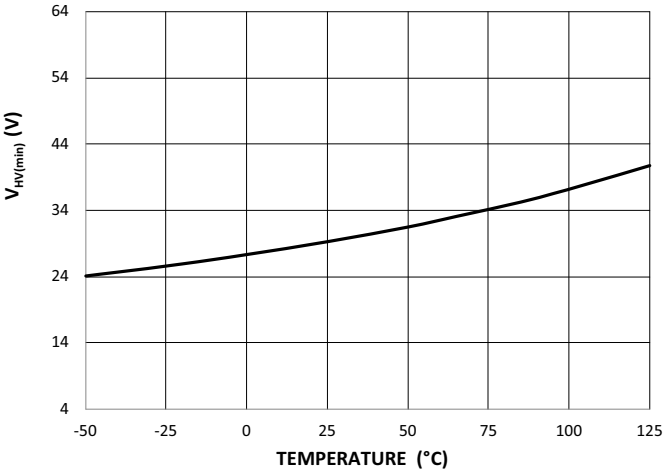


Figure 29. $V_{HV(min)}$ vs. Junction Temperature

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DEFINITIONS

General

The NCL30125 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate for two−switch forward application with integrated high side driver. The NCL30125 packs all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a brown−out protection or HV startup current source.

Current−mode Operation with Internal Ramp Compensation

Implementing peak current mode control operating at fixed switching frequency, the NCL30125 offers an internal ramp compensation signal that can easily by summed up to the sensed current. The controller can thus prevents the appearance of sub−harmonic oscillations

Adjustable Switching Frequency

A resistor to ground precisely sets the switching frequency between 50 kHz and a maximum of 300 kHz.

Internal Brown−Out Protection

A portion of the input mains (or the rectified bulk rail) is brought to the BO pin via a resistive network. When the voltage on this pin is too low, the part stops pulsing. No re−start attempt is made until the controller senses that the voltage is back within its normal range. When the brown−out comparator senses the voltage is acceptable, it sends a general reset to the controller (latched states are released) and authorizes re−start. Please note that a re−start is always synchronized with a $V_{cc(on)}$ transition event for a clean start−up sequence. If V_{cc} is naturally above $V_{cc(on)}$ when the BO circuit recovers, re−start is immediate. An external transistor pulling down the BO pin to ground during operation will shut−off the controller after the end of the BO timer.

High−Voltage Start−up with DSS

Low standby power results cannot be obtained with the classical resistive start−up network. In this part, a high−voltage current−source provides the necessary current at start−up and turns off afterwards. The dynamic Self−Supply (DSS) restarting the start−up current source to supply the controller if the V_{cc} voltage transiently drops

EMI Jittering

An internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. Since the bulk capacitor ripple brings a natural jittering at low line, the jittering modulation is enabled only at high line.

Adjustable Soft−start

A soft−start precludes the main power switch from being stressed upon start−up. In this controller, the soft−start is externally adjusted with a capacitor. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup or BO event.

Skip Cycle Feature

When the power supply loads are decreasing to a low level, the duty cycle also decreases to the minimum value the controller can offer. If the output loads disappear, the converter runs at the minimum duty cycle fixed by the leading edge blanking duration and propagation delay. It often delivers too much energy to the secondary side and it trips the voltage supervisor. To avoid this problem, when the FB pin drops below the internal skip threshold, zero duty cycle is imposed.

Fault Input

The NCL30125 includes a dedicated fault input accessible via the Fault pin. It can be used to sense an overvoltage condition on the adapter and latch off the controller by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 2.5 V. The controller is also disabled if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP)}$, typically 0.4 V. The lower threshold is normally used for detecting an overtemperature fault (by the means of an NTC).

OVP Protection on V_{cc}

It is sometimes interesting to implement a circuit protection by sensing the V_{cc} level. This is what this controller does by monitoring its V_{cc} pin. When the voltage on this pin exceeds $V_{cc(OVP)}$ threshold, the pulses are immediately stopped and the part enters in autorecovery mode.

Short−circuit/Overload protection

Short−circuit and especially overload protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.5 V maximum peak current limit is activated, an error flag is asserted and a time period starts, thanks to the OCP timer. When the fault is validated, all pulses are stopped and the controller enters an auto−recovery burst mode, with a soft−start sequence at the beginning of each cycle. An internal timer keeps the pulses off for 1 s typically which, associated to the pulsing re−try period, ensures a duty−cycle in fault mode less than 10%, independent from the line level. As soon as the fault disappears, the SMPS resumes operation. Please note that B version is auto−recovery as we just described, A version does not and latch off in case of a short−circuit.

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HV Current Source Pin

The NCL30125 HV circuitry provides two features:

- Start−up current source to charge the V_{cc} capacitor at start−up
- Dynamic Self−Supply to maintain the V_{cc} voltage above $V_{cc(off)}$ threshold

The Figure 30 shows the typical schematic around the HV pin. The pin can also be connected to the bulk capacitor.

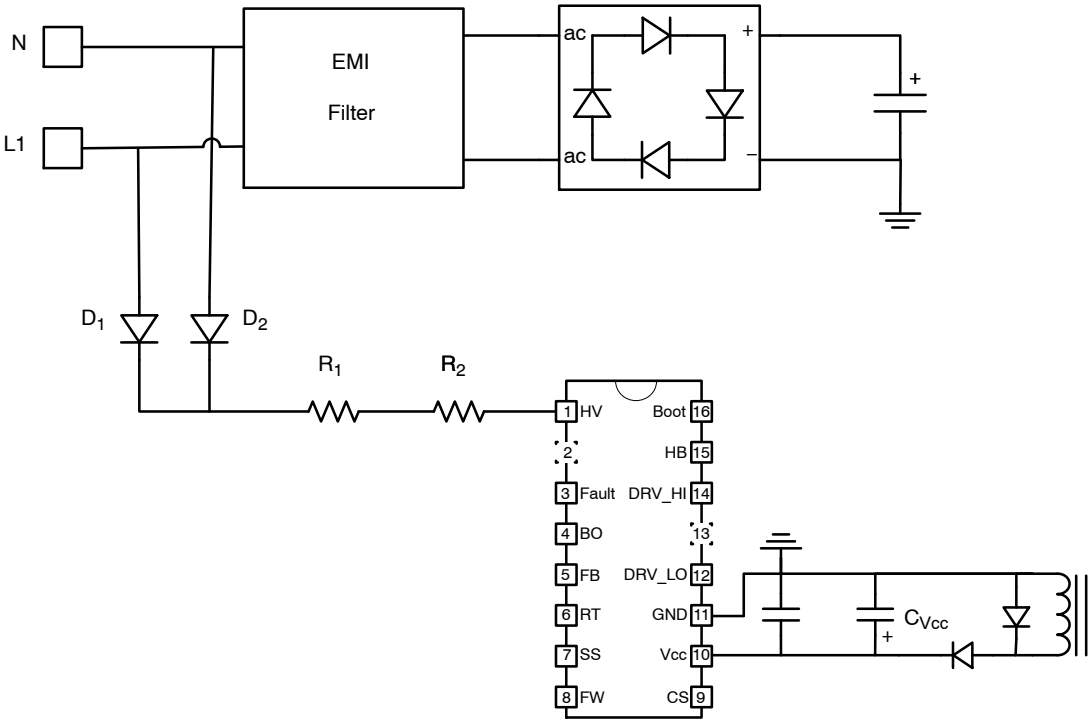


Figure 30. Two Diodes Route the Full−wave Rectified Mains to the HV Pin

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Start−up Sequence

The start−up time of a power supply largely depends on the time necessary to charge the V_{cc} capacitor to the controller V_{cc} start−up threshold ($V_{cc(on)}$ which is 16 V typically). The NCL30125 high−voltage current−source provides the necessary current for a prompt start−up and turns off afterwards. The delivered current (I_{start1}) is reduced to less than 0.5 mA when the V_{cc} voltage is below $V_{cc(inhibit)}$ (1.0 V typically). This feature reduces the die stress if the V_{cc} pin happens to be accidentally grounded. When V_{cc} exceeds $V_{cc(inhibit)}$, a 11−mA current (I_{start2}) is provided that charges the V_{cc} capacitor.

The V_{cc} charging time is then the total of the three following durations:

- Charge from 0 V to $V_{cc(inhibit)}$:

$$t_{start1} = \frac{V_{cc(inhibit)} C_{V_{cc}}}{I_{start1} - I_{CC(start1)}} \quad \text{(eq. 1)}$$

- Charge from $V_{cc(inhibit)}$ to $V_{cc(min)}$:

$$t_{start2} = \frac{(V_{cc(min)} - V_{cc(inhibit)}) C_{V_{cc}}}{I_{start2} - I_{CC(start2)}} \quad \text{(eq. 2)}$$

- Charge from $V_{cc(min)}$ to $V_{cc(on)}$:

$$t_{start3} = \frac{(V_{cc(on)} - V_{cc(min)}) C_{V_{cc}}}{I_{start2} - I_{CC(start3)}} \quad \text{(eq. 3)}$$

Assuming a 47−μF V_{cc} capacitor is selected and replacing I_{start1}, I_{start2}, $I_{CC(start1)}$, $I_{CC(start2)}$, $I_{CC(start3)}$, $V_{cc(inhibit)}$ and $V_{cc(on)}$ by their typical values, it comes:

$$t_{start1} = \frac{1.0 \times 47\,\mu}{500\,\mu - 100\,\mu} = 118\ \text{ms} \quad \text{(eq. 4)}$$

$$t_{start2} = \frac{(10 - 1.0) \times 47\,\mu}{11\,\text{m} - 800\,\mu} = 41\ \text{ms}$$

$$t_{start3} = \frac{(16 - 10) \times 47\,\mu}{11\,\text{m} - 1.05\,\text{m}} = 28\ \text{ms}$$

$$t_{start} = t_{start1} + t_{start2} + t_{start3} = 187\ \text{ms}$$

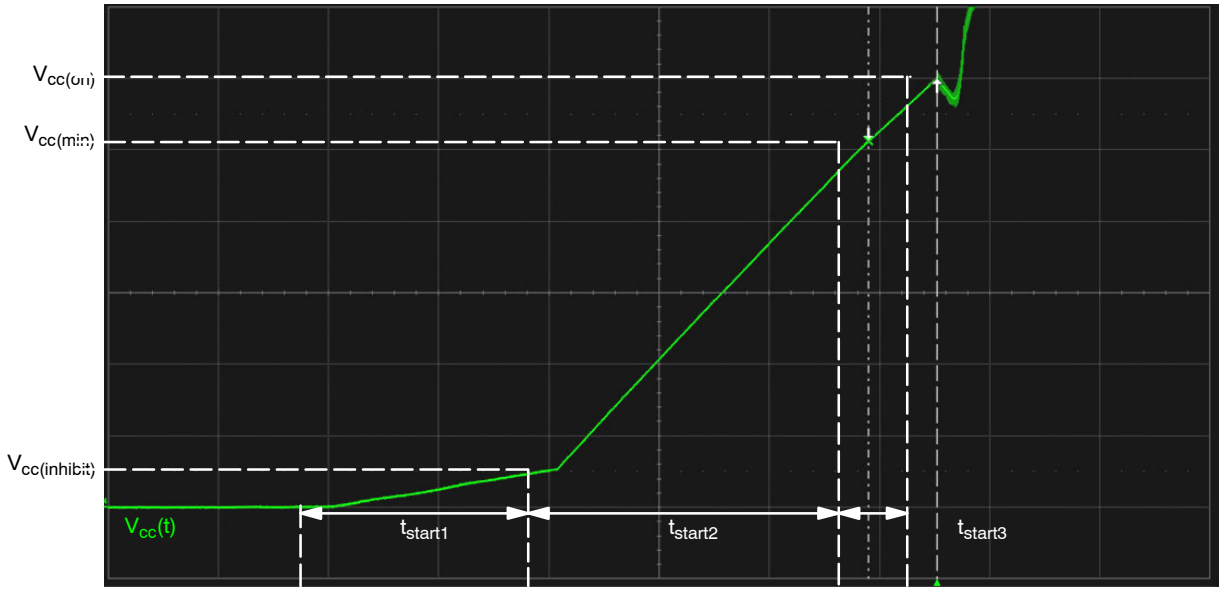


Figure 31. The V_{cc} at Start−up is Made of Two Segments Given the Short−circuit Protection Implemented on the HV Source

If the V_{cc} capacitor is first dimensioned to supply the controller for the traditional 5 to 50 ms until the auxiliary winding takes over, no−load standby requirements usually cause it to be larger. The HV start−up current source is then a key feature since it allows keeping short start−up times with large V_{cc} capacitors (the total start−up sequence duration is often required to be less than 1 s).

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Soft Start

At start−up, in order to limit the stress on the MOSFET, the primary peak current is limited by an internal ramp. As illustrated by the Figure 32, the rising voltage on the SS pin voltage divided by 4 controls the peak current sensed on the CS pin as long as the SS pin voltage is below the FB pin voltage. The driver latch is reset as soon as the CS pin voltage becomes higher than the SS pin voltage divided by 4.

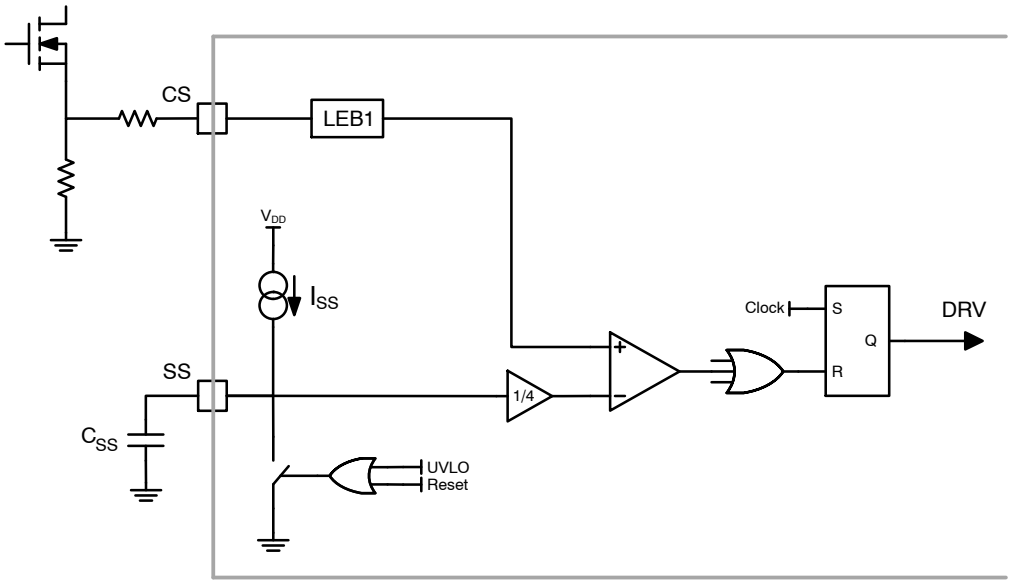


Figure 32. Soft Start Simplified Schematic

The soft start ramp slope is defined by the internal current source and the external capacitor connected to the SS pin. It is a capacitor charged at constant current. The maximum primary peak current is 0.5 V so the primary peak current can be defined by the soft start block from 0 V to 2.0 V (V_{Ilimit} x K_{FB}). The needed capacitance for defined soft start duration is:

$$C_{SS} = \frac{I_{SS} T_{SS}}{2.0\ V} \qquad \text{(eq. 5)}$$

An example is shown in Figure 33.

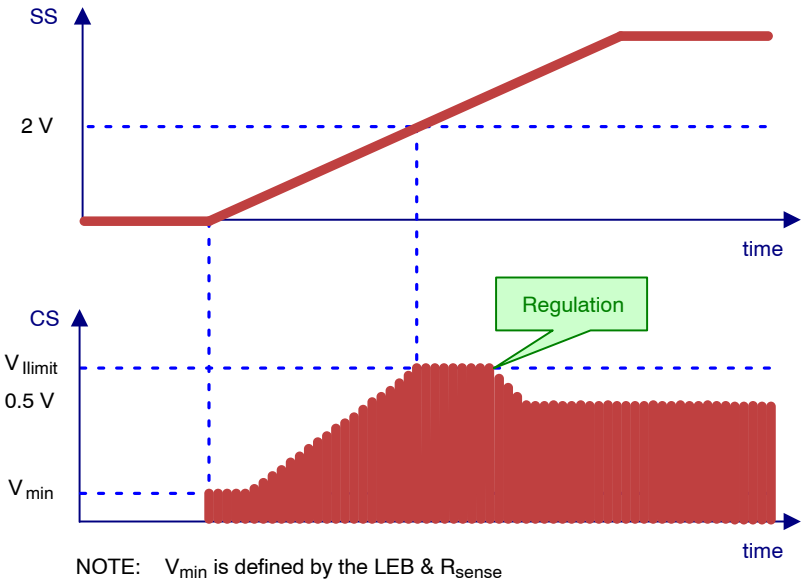


Figure 33. Typical Soft start sequence

Please note that the soft start capacitor is internally grounded after a fault detection (OCP, UVLO etc) or during a BO event. The next restart will be started with the soft start ramp up.

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Brown−out Circuitry

Power supplies are always designed to operate with a specific bulk voltage range. Operation below minimum bulk voltage level would result in current and temperature overstress of the converter power stage. The NCL30125 controller features a Brown−Out (BO) input in order to precisely adjust the bulk voltage turn−on and turn−off levels. When the BO pin voltage exceeds $V_{BO(on)}$, the input is considered sufficient. On the contrary, if V_{BO} remains below $V_{BO(off)}$ for 50 ms, the circuit detects a brown−out situation and stops pulsing until the input level goes back to normal and resumes the operation via a new soft start sequence. The internal circuitry is shown in Figure 34.

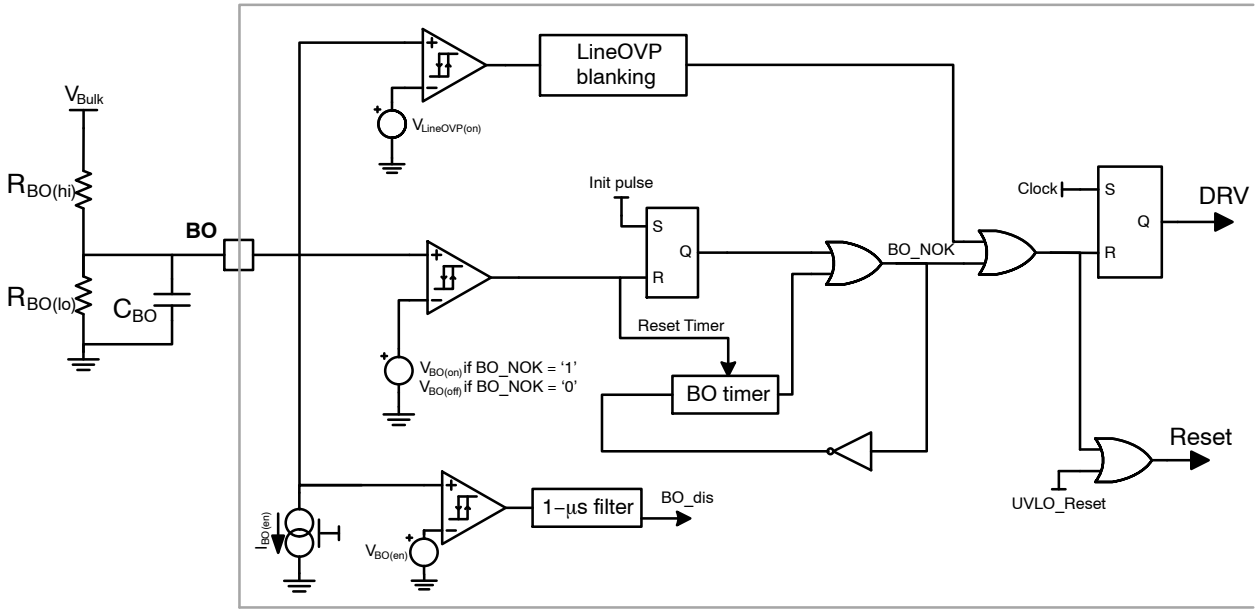


Figure 34. Simplified BO Pin Schematic

To ensure a clean re−start, the controller waits the next $V_{cc(on)}$ event to initiate a new start−up sequence. This ensures a fully−charged V_{cc} capacitor when the controller pulses again. From the above schematic, the calculation of the resistor is straightforward. We have connected the resistor to the bulk capacitor. Choose a bridge current compatible with the power consumption you can accept. If we chose 40 µA, the pull−down resistor $R_{BO(lo)}$ calculation is simple:

$$R_{BO(lo)} = \frac{V_{BO(on)}}{I_{bridge}} = \frac{0.8}{40\ \mu} = 20\ k\Omega \qquad \text{(eq. 6)}$$

Now suppose we want a typical turn−on voltage $V_{turn(on)}$ of 80 V_{rms}. From the two above equations, we can calculate the value of the upper resistive string:

$$R_{BO(hi)} = \frac{V_{turn(on)}\sqrt{2} - V_{BO(on)}}{I_{bridge}} = \frac{80\sqrt{2} - 0.8}{40\ \mu} = 6.2\ M\Omega \qquad \text{(eq. 7)}$$

The hysteresis on the internal reference source is 100 mV typically. The ratio of the two voltages is 1.14. With the upper resistive network, the turn−off voltage can then easily be derived:

$$V_{turn(off)} = \frac{V_{turn(on)}}{1.14} = \frac{80}{1.14} = 70\ V \qquad \text{(eq. 8)}$$

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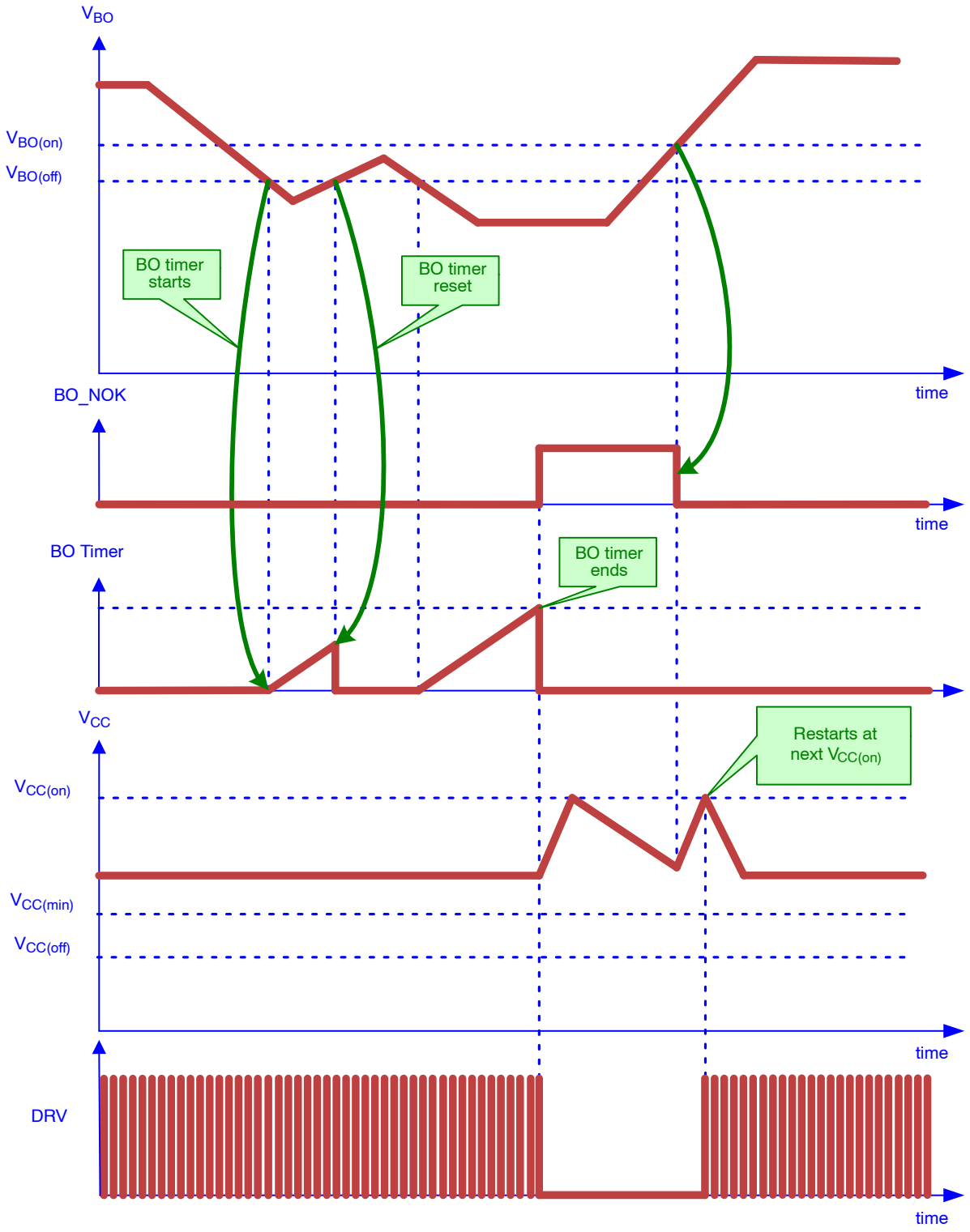


Figure 35. BO Event during Normal Operation

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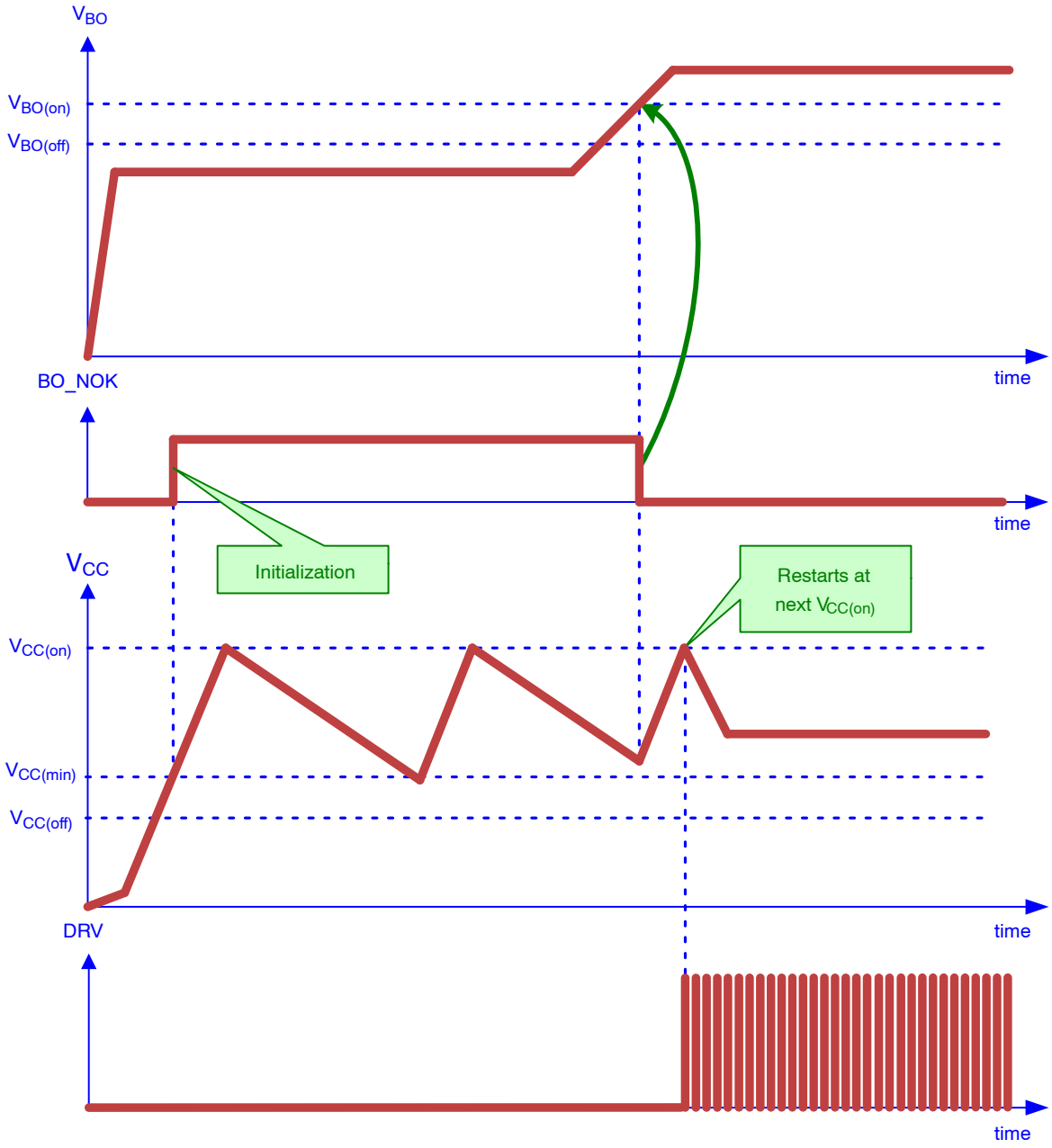


Figure 36. BO Event before Start−Up

The IC also includes over−voltage protection. If the voltage on BO pin exceed $V_{LineOVP(on)}$, the controller stops pulsing after the 20 ms blanking time and until the voltage on BO pin drops down under $V_{LineOVP(off)}$ (Figure 37).

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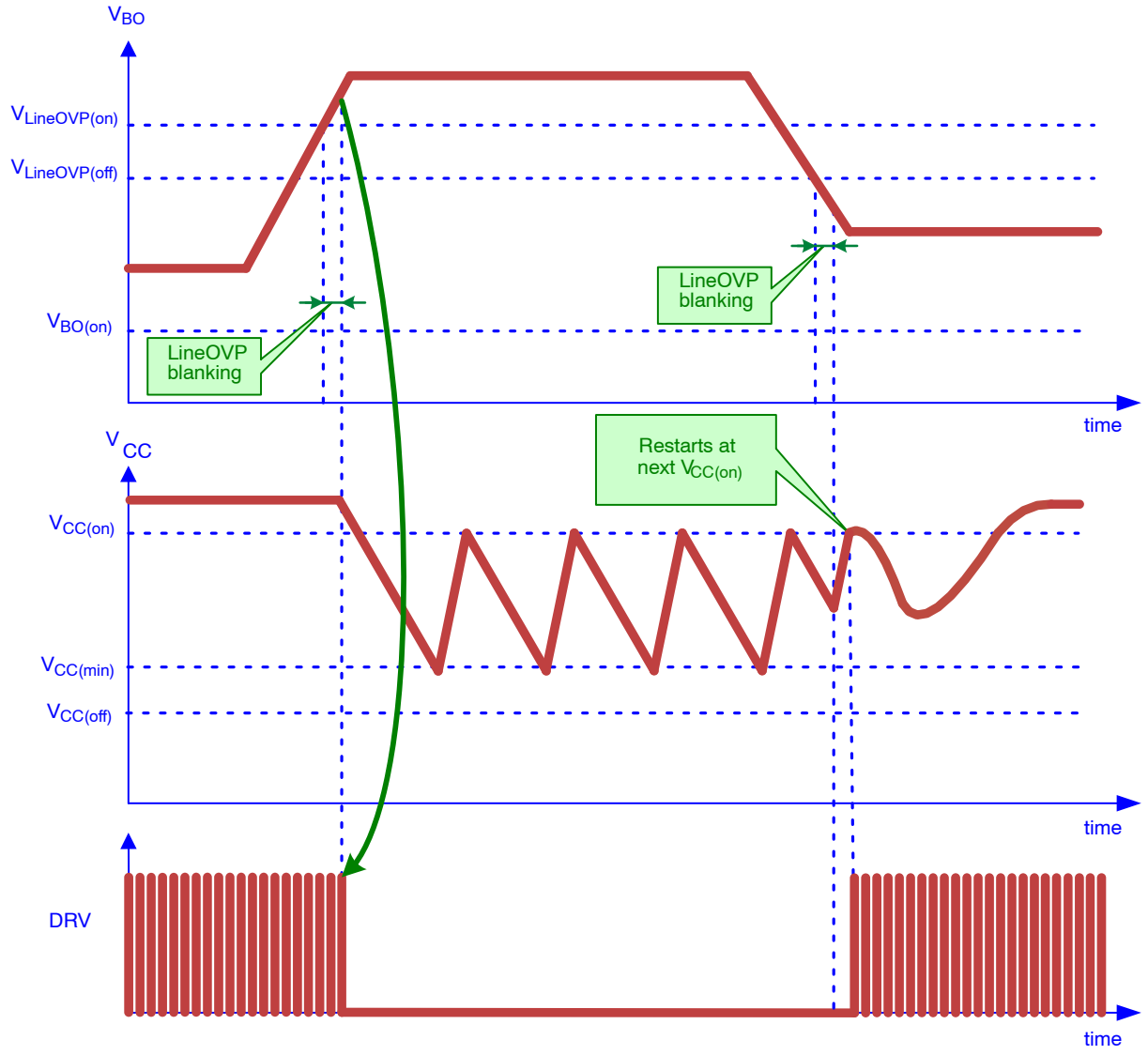


Figure 37. Brown−out Input Functionality with Line OVP Function

There is the possibility to disable the BO protection if this function is not needed. To implement this feature, the BO pin voltage is checked when V_{cc} crosses $V_{cc(min)}$ threshold during the first start−up sequence or after a $V_{cc(reset)}$ event. If the BO voltage is still below $V_{BO(en)}$, the BO function is disabled. Please note that all functions linked to the BO pin will be disabled too.

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Ramp Compensation

The NCL30125 includes an internal ramp compensation signal. This is the buffered oscillator clock delivered only during the on time. Its amplitude is around 3.5 V at the maximum duty−cycle. Ramp compensation is a known means used to cure sub harmonic oscillations in Continuous Conduction Mode (CCM) operated current−mode converters. These oscillations take place at half the switching frequency and occur only during CCM with a duty−cycle close or greater than 50%. To lower the current loop gain, one usually injects between 50% and 100% of the inductor downslope. Figure 38 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the off time.

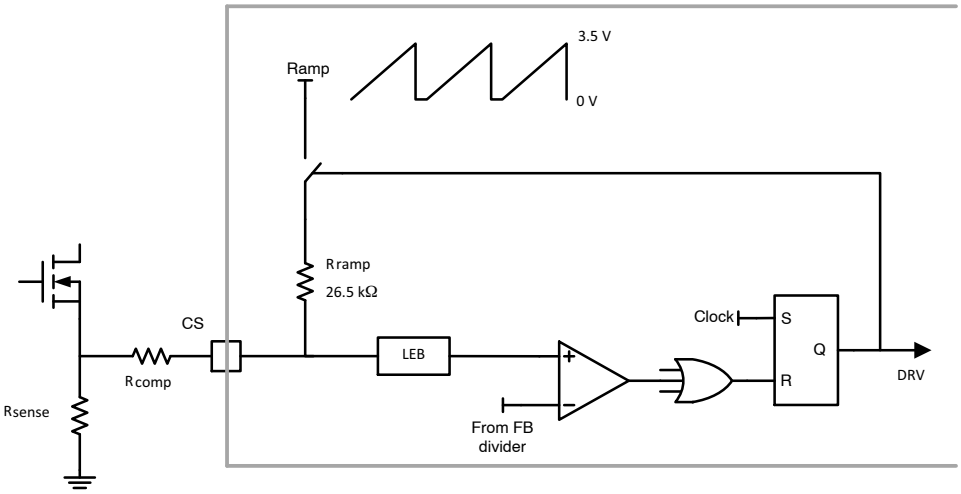


Figure 38. Ramp Compensation Setup

In the NCL30125 controller, the oscillator ramp features a 3.5 V swing reached at a 48% duty−ratio. If the clock operates at a 100 kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp(pk)}}{D_{max} T_{sw}} = \frac{3.5}{0.48 \times 10\ \mu} = 729\ mV/\mu s \qquad \text{(eq. 9)}$$

In a two−switch forward application, the secondary−side downslope is seen on primary side:

$$S_p = \frac{(V_{out} + V_f)}{L_{out}} \times \frac{N_s}{N_p} \qquad \text{(eq. 10)}$$

where:

- V_{out} is output voltage level
- V_f the freewheel diode forward drop
- L_{out}, the secondary inductor value
- N_s/N_p the transformer turns ratio
- R_{sense}: the sense resistor on the primary side

A particularity of the forward converter is the natural slope compensation created by the transformer magnetizing inductance. The natural ramp is extracted from the following equation:

$$S_{natural} = \frac{V_{bulk}}{L_{mag}} \qquad \text{(eq. 11)}$$

The above natural ramp brings a natural compensation:

$$\delta_{natural} = \frac{S_{natural}}{S_p} \qquad \text{(eq. 12)}$$

If the natural ramp compensation ($\delta_{natural}$) is higher than the needed ramp compensation (δ_{comp}) defined by the designer, the power supply does not need additional ramp compensation. If not, the natural compensation has to be subtracted to the compensation brought by the controller in order to avoid over compensation.

$$\delta_{comp(final)} = \delta_{comp} - \delta_{natural} \qquad \text{(eq. 13)}$$

The required amount of ramp compensation, $\delta_{comp(final)}$, will help to define the needed ramp injection:

$$S_{inj} = \delta_{comp(final)} \times S_p \qquad \text{(eq. 14)}$$

Our internal compensation being of 729 mV/µs, the divider ratio (Ratio) between R_{comp} and the internal 26.5 kΩ resistor is:

$$Ratio = \frac{S_{inj}}{S_{ramp}} \qquad \text{(eq. 15)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp}.Ratio \qquad \text{(eq. 16)}$$

A resistor of the above value will be inserted from the sense resistor to the current sense pin. We recommend adding a small capacitor of 100 pF, from the current sense pin to the controller ground for an improved immunity to the noise. Please make sure both components are located very close to the controller.

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Autorecovery Overload Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than its programmed value (15 ms typical), the driving pulses are stopped and 1−s autorecovery timer starts. If V_{cc} voltage is below $V_{cc(min)}$, HV current source is activated to build up the voltage to $V_{cc(on)}$. On the contrary, if V_{cc} voltage is above $V_{cc(min)}$, HV current source is not activated, V_{cc} falls down as the auxiliary pulses are missing and the controller waits that $V_{cc(min)}$ is crossed to enable the start−up current source. Until autorecovery timer is not elapsed, the controller purposely ignores the re−start when V_{cc} crosses $V_{cc(on)}$ and waits the end of the timer. By lowering the duty ratio in fault condition, it naturally reduces the average input power and the rms current in the output cable. Illustration of such principle appears in Figure 39. The soft−start is activated upon re−start attempt. Please note that the OCP timer is also activated by the maximum duty cycle protection. This maxDC is affected by the t_{delay1} parameter when the FW is activated during the normal operation. Higher the switching frequency is, lower will be the maximum duty cycle. Please refer to the parametric table.

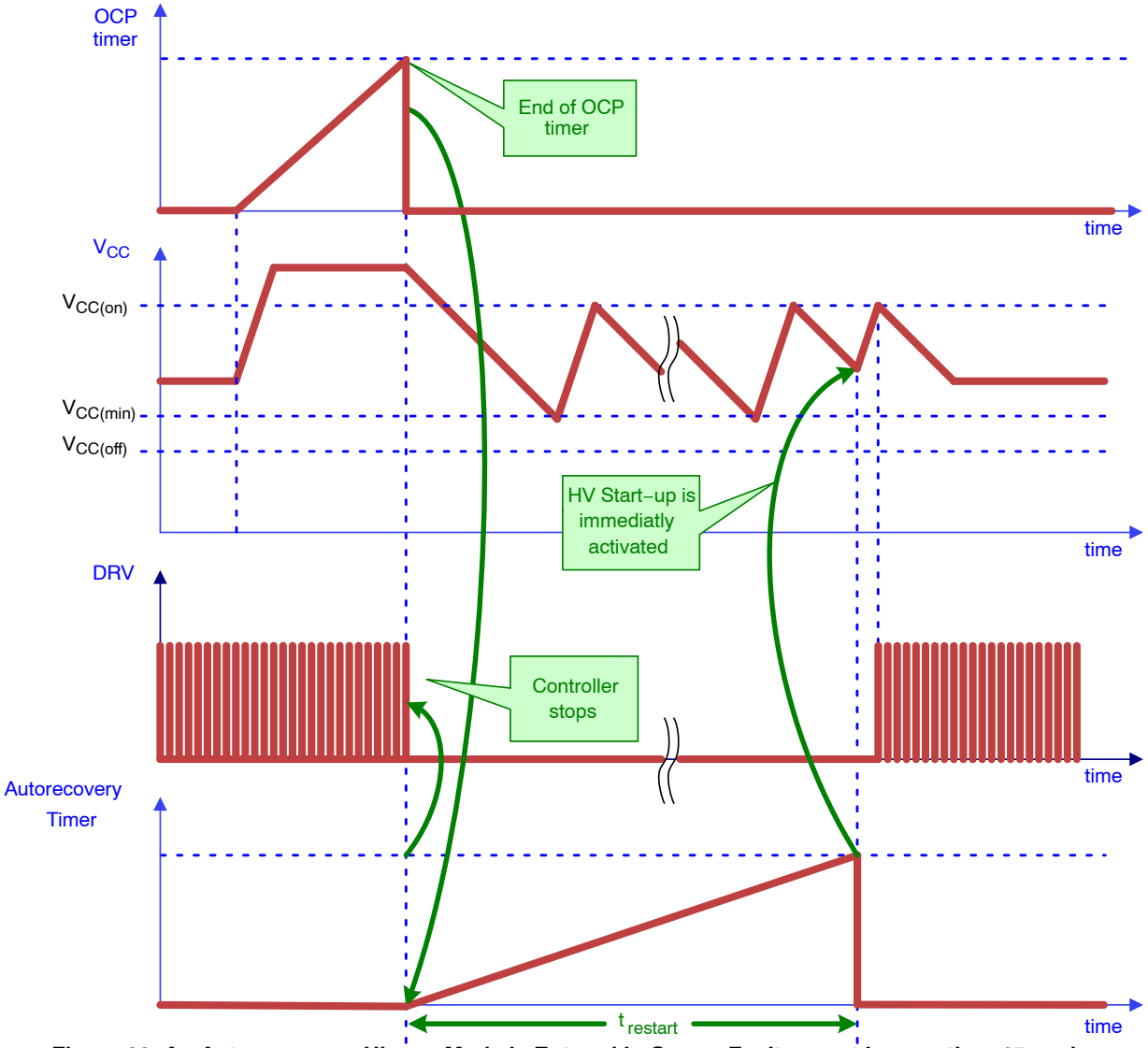


Figure 39. An Auto−recovery Hiccup Mode is Entered in Case a Faulty event Longer than 15 ms is Acknowledged by the Controller

The hiccup is operating regardless of the brown−out level. However, when the internal comparator toggles indicating that the controller recovers from a brown−out situation (the input line was ok, then too low and back again to normal), the hiccup is interrupted and the controller re−starts to the next available $V_{cc(on)}$. Figure 40 displays the resulting waveform: the controller is protecting the converter against an overload. The mains suddenly went down, and then back again at a normal level. Right at this moment, the hiccup logic receives a reset signal and ignores the next hiccup to immediately initiate a re−start signal.

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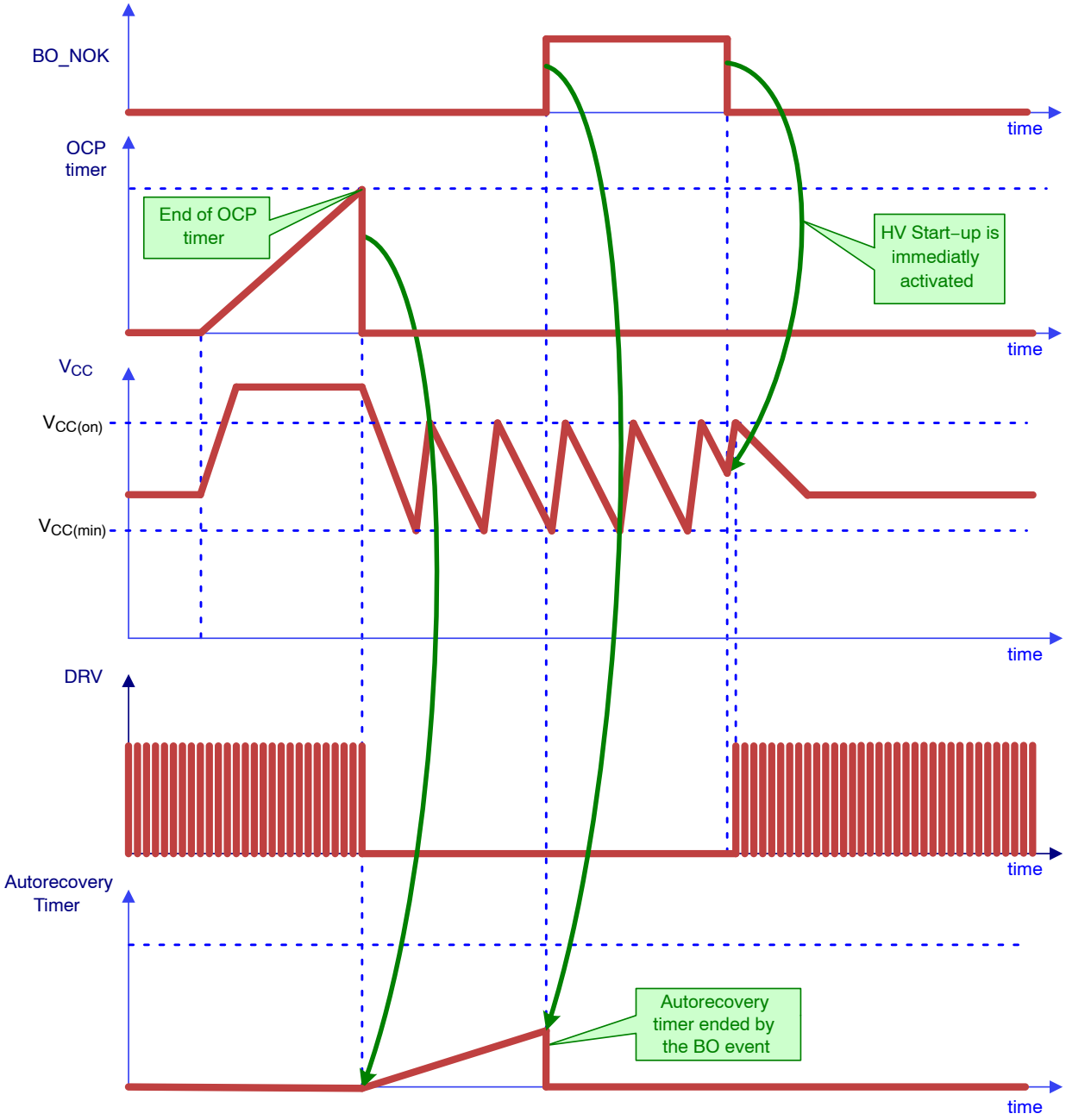


Figure 40. The BO Event Reset the Autorecovery Timer or the Latch State (Latching off OCP Protection)

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Latch Overload Protection

In some applications, the controller must be fully latched in case of an output short circuit presence. In that case, you would select a controller with an OCP latched option. When the error flag is asserted, meaning the controller is asked to deliver its full peak current, the controller latches off after the elapse of fault timer – i.e. the pulses are immediately stopped and V_{cc} hiccups between two voltage levels, given by a $V_{cc(off)}$ level and added hysteresis $V_{cc(hyst)}$. The device cannot recover operation until V_{cc} drops below $V_{cc(reset)}$ or brownout recovery signal is applied or Line OVP protection. Practically, the power supply must be unplugged to be reset ($V_{cc} < V_{cc(reset)}$). The Figure 41 and Figure 42 depict the controller behavior in these cases.

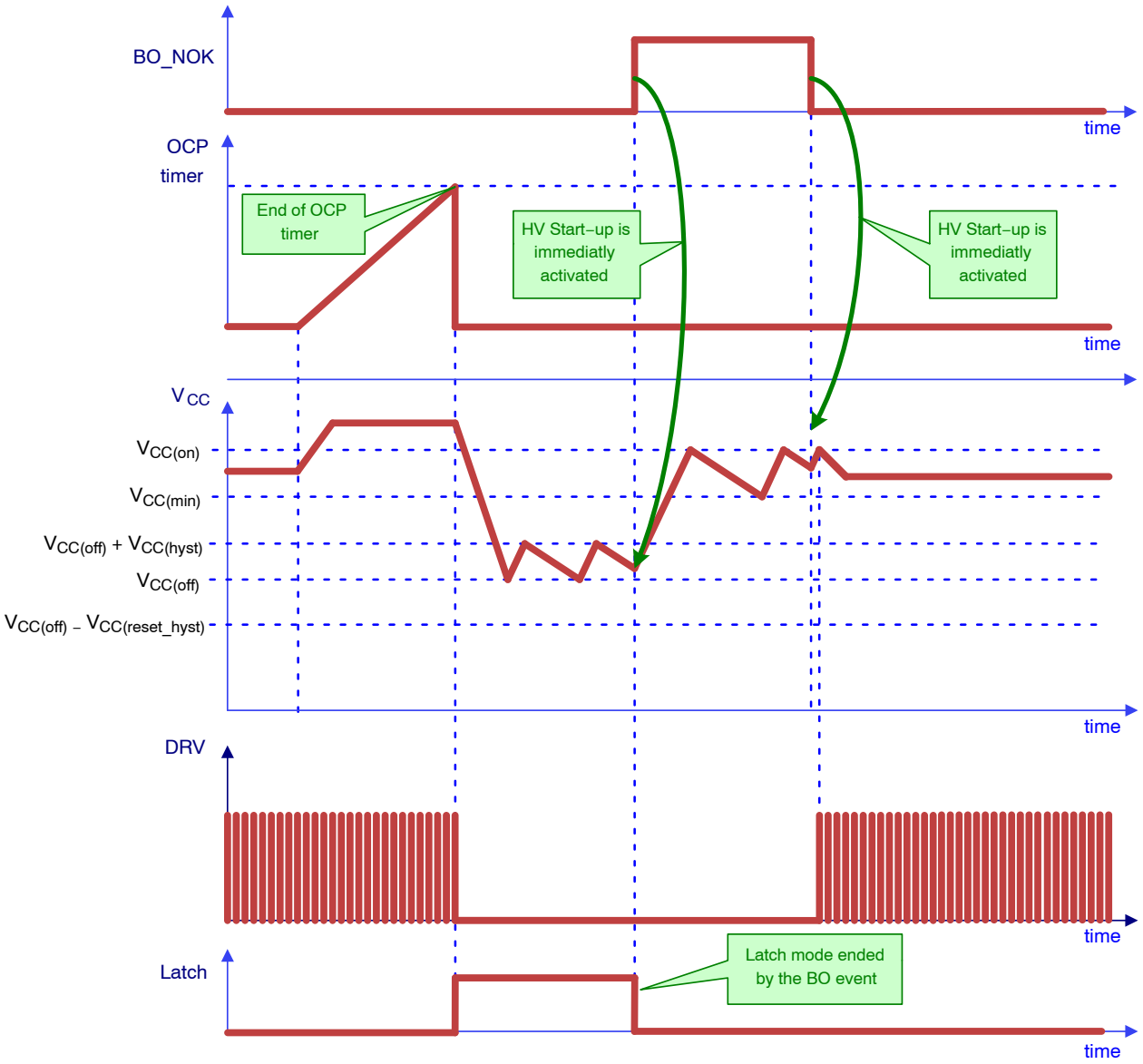


Figure 41. BO Event Reset the Latch Mode Operation Activated by the OCP Protection

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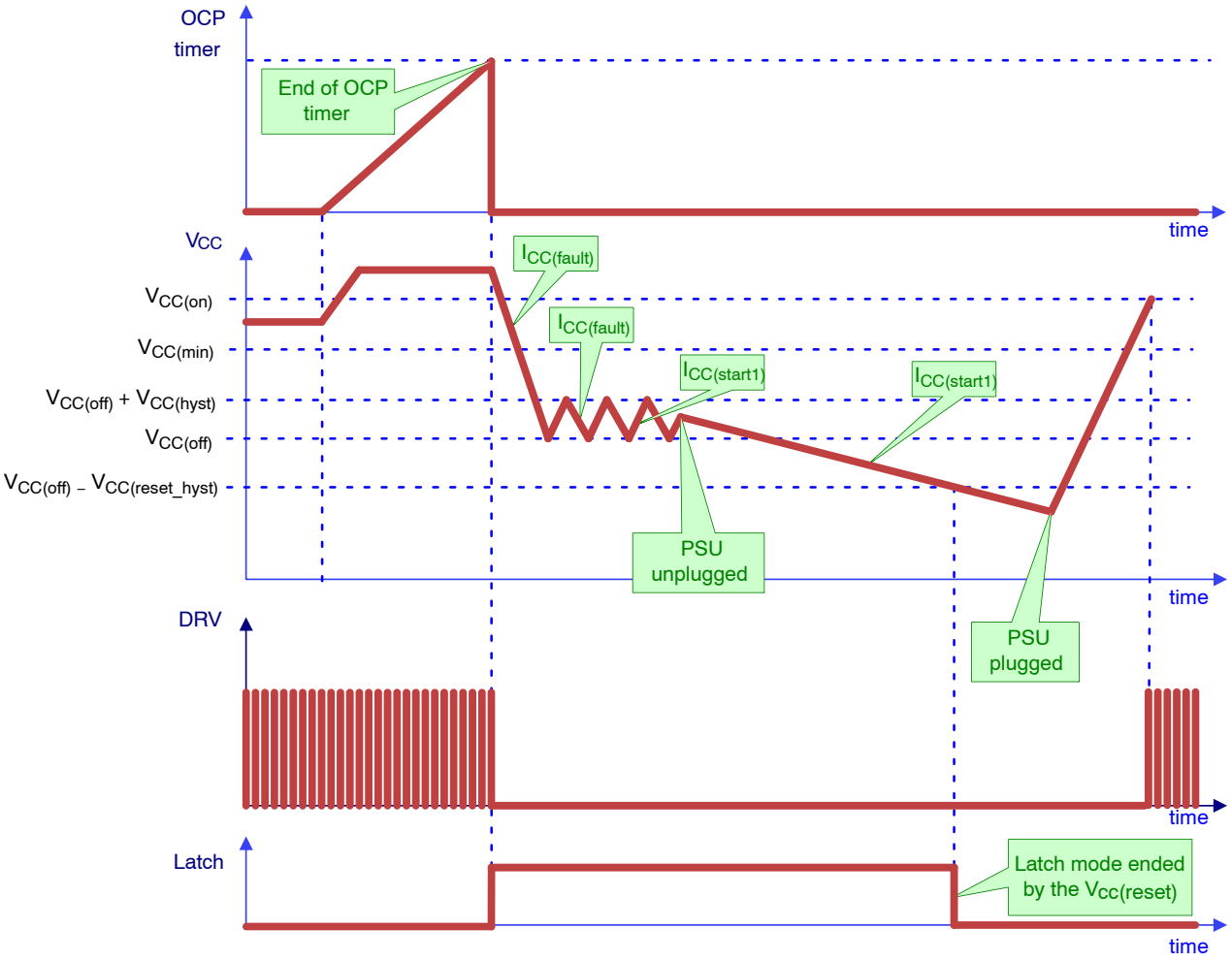


Figure 42. The Latch Mode Operation, Activated by the OCP Protection, is Reset by Low Vcc Voltage

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A 2nd Over−Current Comparator for Abnormal Over−Current Protection

A severe fault like a winding short−circuit can cause the switch current to increase very rapidly during the on−time. The current sense signal significantly exceeds V_{ILimit} . But, because the current sense signal is blanked by the LEB circuit during the switch turn on, the power switch current can become huge causing system damage.

The NCL30125 protects against this fault by adding an additional comparator for Abnormal Over−current Fault detection. The current sense signal is blanked with a shorter LEB duration, t_{LEB2}, before applying it to the 2nd Over−Current Comparator. The voltage threshold of the comparator, $V_{CS(stop)}$, typically 0.75 V, is set 50 % higher than V_{ILimit}, to avoid interference with normal operation. Four consecutive Abnormal Over−Current faults cause the controller to enter latch mode. The count to 4 provides noise immunity during surge testing. The counter is reset each time a DRV pulse occurs without activating the Fault Overcurrent Comparator.

Please note that like timer−based short−circuit protection, some versions are latching off and others are auto−recovery.

Fault Input

The NCL30125 includes a dedicated fault input accessible via the Fault pin. Figure 43 shows the architecture of the Fault input. The controller can be latching off by pulling up the pin above the upper fault threshold, $V_{Fault(OVP)}$, typically 2.5 V. An active clamp prevents the Fault pin voltage from reaching the $V_{Fault(OVP)}$ if the pin is left open. To reach the upper threshold, the external pull−up current has to be higher than the pull−down capability of the clamp (typically 1.5 mA). This OVP function is typically used to detect a V_{cc} or auxiliary winding overvoltage by means of a Zener diode generally in series with a small resistor (see Figure 43).

Neglecting the resistor voltage drop, the OVP threshold is then:

$$V_{AUX(OVP)} = V_Z + V_{Fault(OVP)} \qquad \text{(eq. 17)}$$

where V_Z is the Zener diode voltage.

The controller can also be latched off if the Fault pin voltage, V_{Fault}, is pulled below the lower fault threshold, $V_{Fault(OTP)}$, typically 0.4 V. This capability is normally used for detecting an overtemperature fault by means of an NTC thermistor. A pull up current source I_{OTP}, (typically 50 μA) generates a voltage drop across the thermistor. The resistance of the NTC thermistor decreases at higher temperatures resulting in a lower voltage across the thermistor. The controller detects a fault once the thermistor voltage drops below $V_{Fault(OTP)}$.

The circuit detects an overtemperature situation when:

$$R_{NTC} I_{OTP} = V_{Fault(OTP)} \qquad \text{(eq. 18)}$$

Hence, the OTP protection trips when

$$R_{NTC} = \frac{V_{Fault(OTP)}}{I_{OTP}} \qquad \text{(eq. 19)}$$

The controller bias current is reduced during power up by disabling most of the circuit blocks including I_{OTP}. This current source is enabled once V_{cc} reaches $V_{cc(min)}$. A bypass capacitor is usually connected between the Fault and GND pins. It will take some time for V_{Fault} to reach its steady state value once I_{OTP} is enabled. Therefore, the lower fault comparator (i.e. overtemperature detection) is ignored during $t_{OTP(blank)}$ duration. In addition, in order to speed up this fault pin capacitor, OTP current is doubled during the same period.

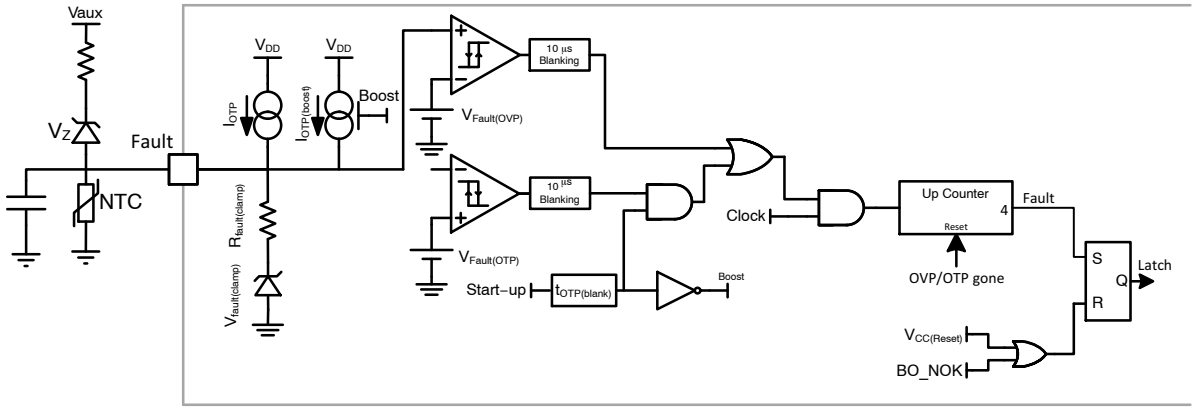


Figure 43. Fault Detection Schematic

As a matter of fact, the controller operates normally while the Fault pin voltage is maintained within the upper and lower fault thresholds. Upper and lower fault detectors have blanking delays to prevent noise from triggering them. Both OVP and OTP comparator outputs are validated only if its high−state duration lasts a minimum of 10 μs. Below this value, the event is ignored. Then, a counter ensures that OVP/OTP events occurred for 4 successive drive clock pulses before actually latching the part.

When the part is latched−off, the drive is immediately turned off and V_{cc} goes in endless hiccup mode. The power supply needs to be un−plugged to reset the part as a result of a BO_NOK (BO fault condition) if Brown−Out feature is enabled or Line OVP otherwise $V_{cc(Reset)}$.

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Over voltage protection on V_{cc} pin

The NCL30125 hosts a dedicated comparator on the V_{cc} pin. When the voltage on this pin exceeds $V_{cc(OVP)}$ for more than 20 μs, a signal is sent to the internal latch and the controller immediately stops the driving pulses while remaining in a lockout state. This OVP on V_{cc} pin activates the autorecovery mode. This technique offers a simple and cheap means to protect the converter against optocoupler.

Protecting from a failure of the current sensing

A 60 μA (typically) pull−up current source, I_{CS}, pulls up the CS pin to disable the controller at start−up if the pin is left open.

In addition, the maximum duty cycle (48% typically) avoids that the MOSFET stays permanently ON if the switch current cannot reach the current setpoint when for instance, the input voltage is low or if the CS pin is grounded. In this case, the 15−ms OCP timer is activated. If the timer elapses, the controller enters in auto−recovery or endless hiccup mode depending on the controller option.

Driver

The NCL30125 maximum supply voltage, $V_{cc(max)}$, is 35 V. Typical high−voltage MOSFETs have a maximum gate−source voltage rating of 20 V. The DRV_LO pin incorporates an active voltage clamp to limit the gate voltage on the external MOSFETs. The DRV voltage clamp, $V_{DRV(high)}$ is typically 13.5 V with a maximum limit of 16 V.

The High Side Driver Using the Bootstrap Technique

The driver features a traditional bootstrap circuitry, requiring an external high voltage diode with resistor in series for the capacitor refueling path. This technique is normally used in half−bridge application. Indeed, compared to the two−switch forward topology, the low−side driver is turned on in opposition compared to the high−side driver. This operation is useful to refresh the bootstrap capacitor but the two−switch forward topology is less friendly. To be able to use the bootstrap technique, an external switch is added to refresh the capacitor during startup or in skip mode. In normal operation, the MOSFET body diode will replaced the freewheel diode. The current capability of this additional switch is adjusted to handle the magnetization current during the off time. Please note that the freewheel diode connected between the HB node and the ground is not needed anymore. Figure 44 shows the internal architecture of the drivers section. The device incorporates an upper UVLO circuitry that makes sure enough V_{GS} voltage is available for the upper side MOSFET.

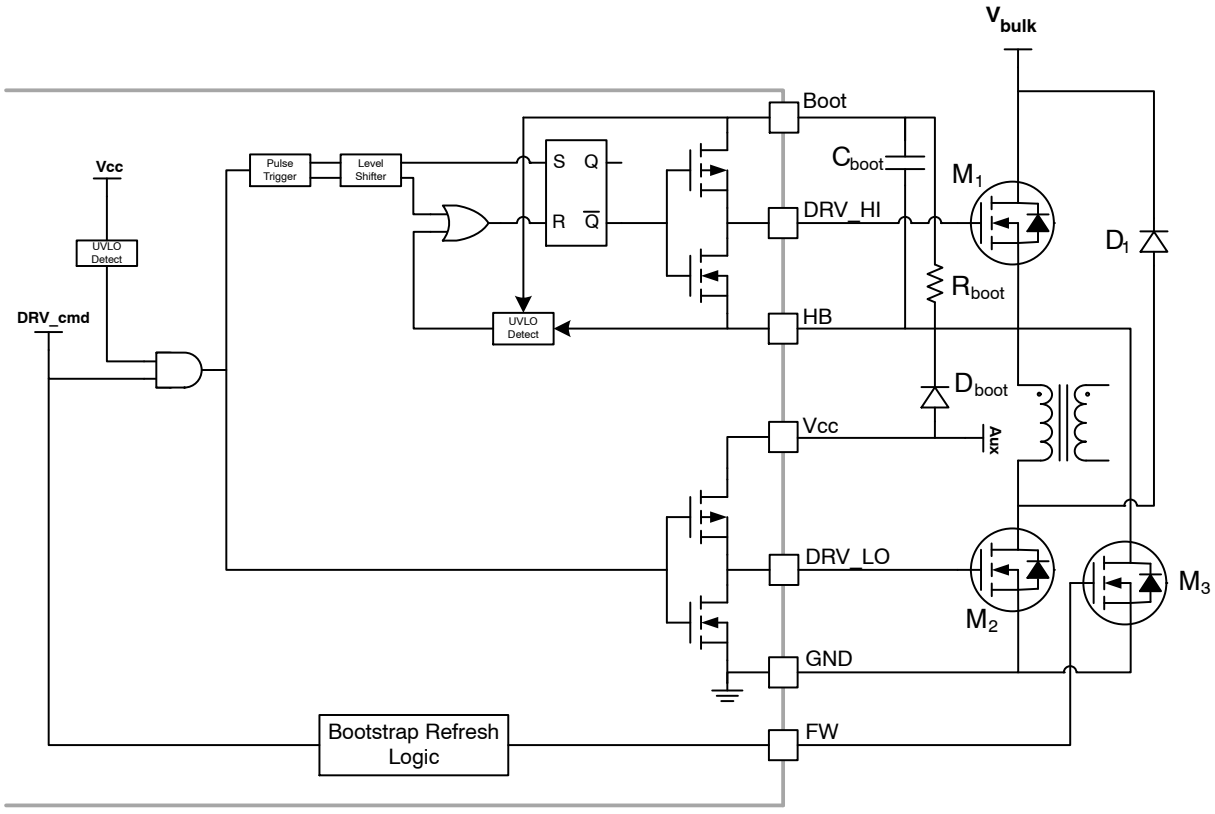


Figure 44. Internal Drive stage with Bootstrap Capacitor Refresh Switch

In order to charge the bootstrap capacitor voltage to the V_{cc} threshold during the startup sequence, the purposed circuit will activate the external switch during $t_{boot(start)}$ timer to charge the capacitor to the V_{cc} voltage and then generate the first driver pulse with soft start as depicted in Figure 45.

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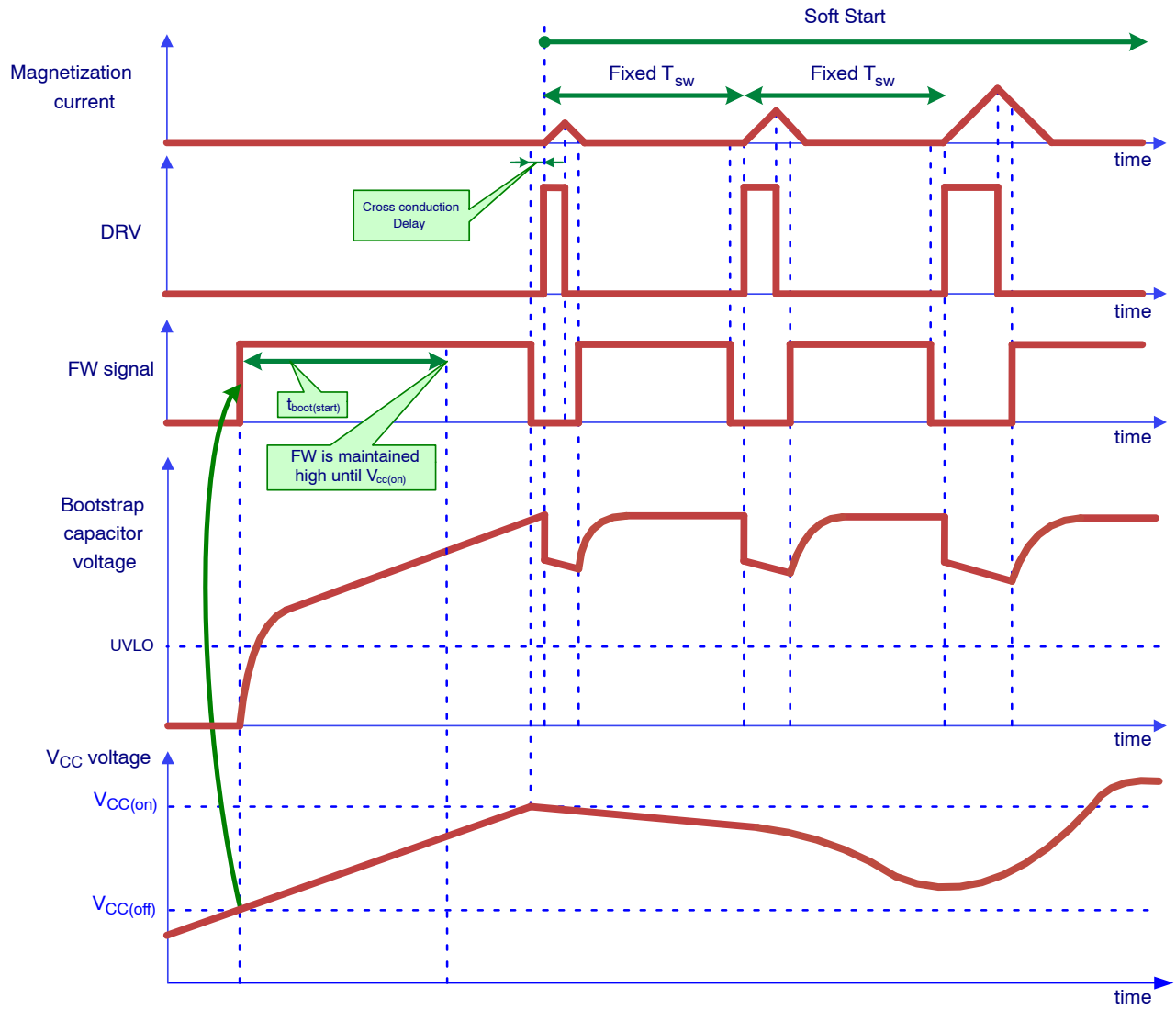


Figure 45. Bootstrap Switch Activated during Startup Sequence

In normal operation, at the nominal switching frequency, the bootstrap capacitor voltage is charged during the demagnetization on the primary side. When the magnetizing current circulates in the freewheel diode and the M_3 MOSFET body diode (both power MOSFETs M_1 and M_2 are off), the HB pin drops to $-V_f$ that create a path to refuel the capacitor. However, when the core is fully reset, both diodes stop conducting and the HB node turns to a high−impedance state. The capacitor is no more refreshed. For this reason, the FW pin is maintained on during the off time. In skip cycle mode, the dead time between the core reset and the next off time cycle where the capacitor is refreshed again can be long, the high side driver UVLO protection will be trigged. To avoid this unexpected behavior, the M_3 switch will be turned on during the skip mode to perform the bootstrap capacitor refresh during large off time duration, the Figure 46 illustrates the controller behavior in normal operation and during the skip mode.

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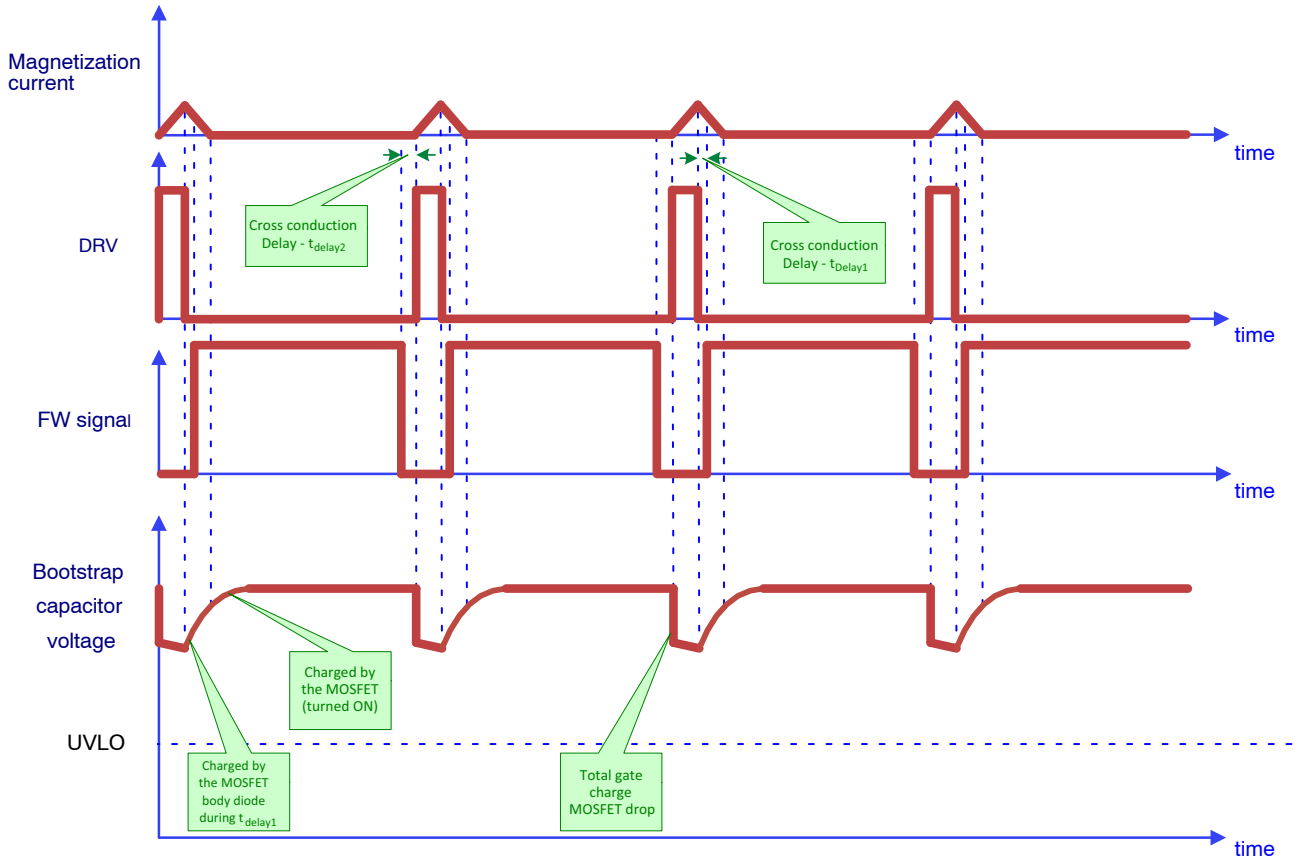


Figure 46. Bootstrap Refresh in Normal Operation

As shown in the two previous waveforms, the bootstrap capacitor voltage is not constant so the capacitor must be calculated to avoid UVLO protection activation. We can identify three phases on the bootstrap voltage. The first one, when the MOSFETS are turned on, is due to the total gate charge Q_G of the upper MOSFET. The energy is transferred from the capacitor to the MOSFET. The second phase is during the on time duration. The negative slope is introduced by the driver current consumption I_{DRV} (internal bias) and also the external pull down resistor R_{PD} connected between the gate and the source of the upper−side transistor Q_{DC}. The last portion is related to the charge sequence when the power MOSFETS are turned off.

The total gate charge taken from the bootstrap capacitor during the on time is:

$$Q_{total} = Q_G + Q_{DC} = Q_G + D_{max}T_{SW}\left(\frac{V_{cc} + V_f}{R_{PD}} + I_{DRV}\right) \quad \text{(eq. 20)}$$

According to the V_{cc} voltage and the high−side driver UVLO threshold, C_{boot} can be calculated by including some design margin:

$$C_{boot} \geq \frac{Q_G + D_{max}T_{SW}\left(\frac{V_{CC}+V_f}{R_{PD}} + I_{DRV}\right)}{\Delta V} \quad \text{(eq. 21)}$$

where:

– $\Delta V = V_{CC} - V_f - UVLO - Margin$

– R_{PD} is the gate−source pull down resistor.

Please note that the maximum voltage between V_{Boot} and V_{HB} is 20 V. If the bootstrap capacitor is supplied by the V_{cc} voltage through a diode and $V_{cc} > 20$ V, a network has to be inserted to protection the high−side driver.

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Skip Mode

The NCL30125 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 5 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for lower peak current. When this setpoint reaches a determined level, the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so–called skip cycle mode, also named controlled burst operation. Because this operation takes place at low peak currents, you will not hear any acoustic noise in your transformer.

When the IC enters the skip cycle mode, the peak current cannot go below $V_{skip}/4$.

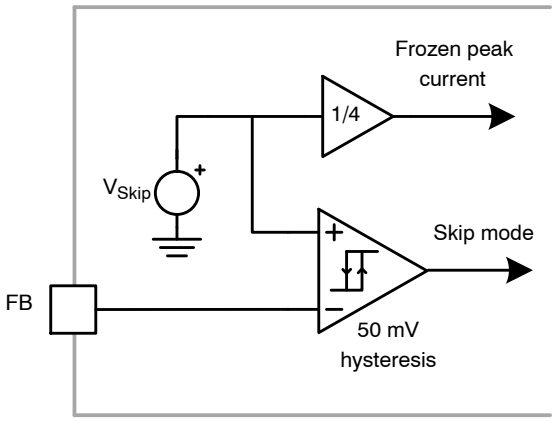


Figure 47. Skip Mode and Frozen Peak Current

Adjustable Switching Frequency

The controller operates at fixed switching frequency where the duty ratio is adjusted according to the power demand. The switching frequency can be selected by playing on the resistor connected on the RT pin. The switching frequency range goes from 50 kHz to 300 kHz to give more design flexibility. The curve in the Figure 48 gives an idea of the needed resistor according to the selected switching frequency.

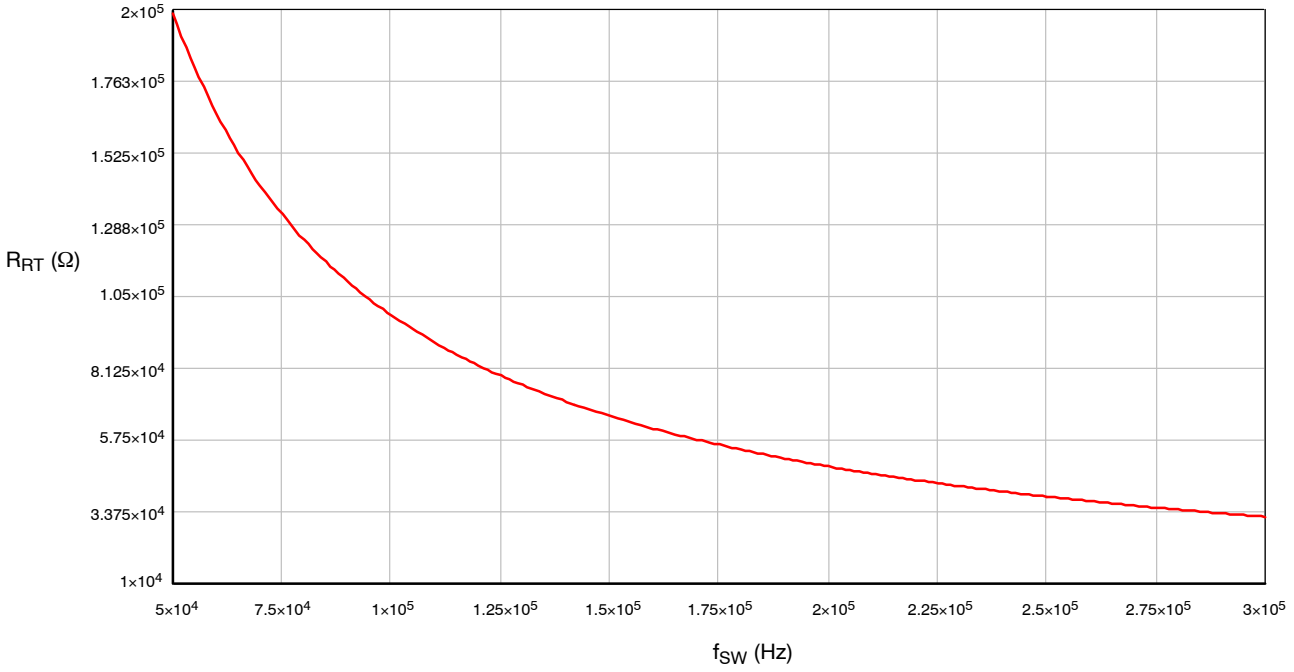


Figure 48. Switching Frequency versus RT Pin Resistance

The RT resistance can be calculated more precisely by using the following equation:

$$R_{RT} = \left(\frac{1}{f_{SW}} - 120\ ns\right) \times 10^{10} \qquad \text{(eq. 22)}$$

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Adaptive Leading Edge Blanking

The leading edge blanking (LEB) used on CS pin at the MOSFET turn on is present to blank the parasitic peak voltage and avoid false primary peak current. Normally, the time is fixed around 300 ns. However, due to the RT pin, the switching frequency range is large, from 50 kHz to 300 kHz. With 1 µs period, the classical 300 ns LEB cannot be used. For this reason, the NCL30125 introduced an adaptive LEB duration according to the switching frequency set on the RT pin. The blanking duration is 300 ns for 50−kHz frequency and it is linearly reduced as shown in the Figure 49.

$$LEB1 = -3.33.10^{-13} f_{SW} + 316.6.10^{-9} \quad \text{(eq. 23)}$$

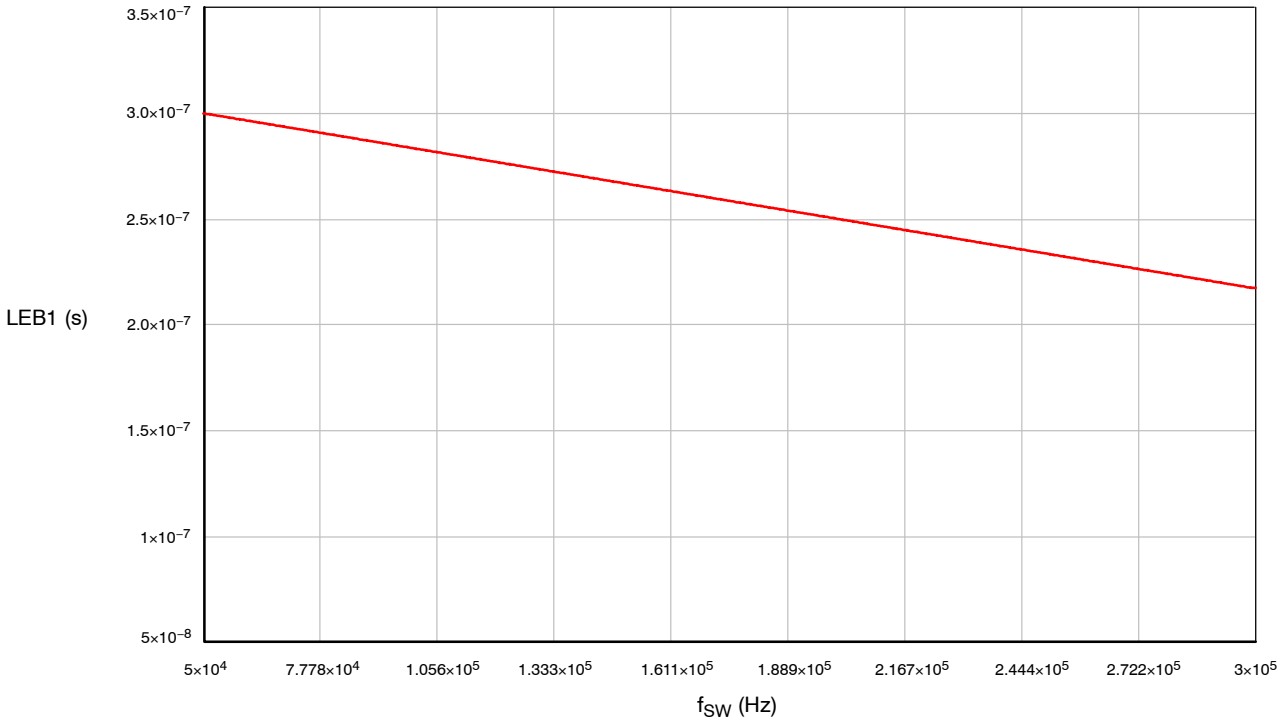


Figure 49. Leading Edge Blanking (LEB1) versus Switching Frequency (f_{SW})

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The same principle is used for the LEB2. This LEB is only used for the 2nd Over−Current Comparator ($V_{CS(stop)}$). The blanking duration LEB2 is now 100 ns for 50 kHz frequency and it is linearly reduced. The curve in the Figure 50 depicts the LEB2 evolution according to the switching frequency.

$$LEB2 = -1.44.10^{-13} f_{SW} + 107.2.10^{-9} \quad \text{(eq. 24)}$$

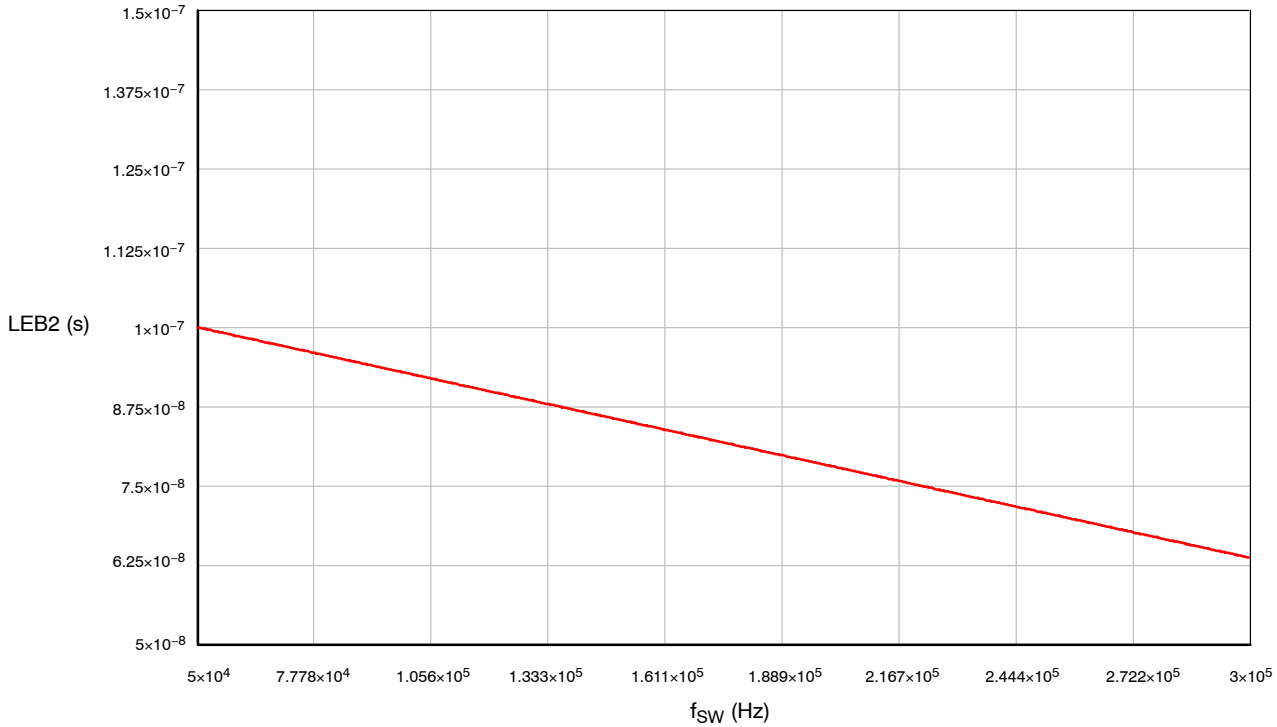


Figure 50. Leading Edge Blanking (LEB2) versus Switching Frequency (fsw)

Thermal Shutdown

An internal thermal shutdown circuit monitors the junction temperature of the IC. The controller is disabled if the junction temperature exceeds the thermal shutdown threshold, T_{SHDN}, typically 150°C. A continuous V_{cc} hiccup is initiated after a thermal shutdown fault is detected. The controller restarts at the next $V_{cc(on)}$ once the IC temperature drops below below T_{SHDN} by the thermal shutdown hysteresis, $T_{SHDN(HYS)}$, typically 20°C.

The thermal shutdown is also cleared if V_{cc} drops below $V_{cc(reset)}$ or a brown−out fault is detected. A new power up sequences commences at the next $V_{cc(on)}$ once all the faults are removed.

Layout Guideline

In order to avoid noise around the controller and unexpected behavior, we recommend to take care about the layout. The first thing is to identify the high−current paths and make sure the area they encompass is kept as small as possible. When both power MOSFETs are turned on, current is delibered by the bulk capacitor and crosses the high−side MOSFET, the transformer primary inductance, the power low side MOSFET and finally, the sense resistance before returning to the bulk negative connection. Another loop will be around the auxiliary winding to refuels the auxiliary capacitor. Finally, the MOSFETs drives draw currents from the auxiliary capacitor that enter the IC via its V_{cc} pin before reaching the gate via the DRV_LO pin. The current returns to ground trough the sense resistance. At turn off, the gate stored energy is depleted by a current that now enters the IC DRV_LO pin and circulates to ground to flow, again, in the sense resistance. Same path is visible on the high side driver.

All decoupling components as well as other small low−current devices (timing capacitors, feedback decoupling…) must be placed as close as possible to the main control IC. Failure to respect this rule will 1) affect the converter stability 2) degrade its susceptibility to external events such as input surges or ESD zaps.

Keep noisy (from power loop or auxiliary signal) and quiet grounds separated. The optocoupler emitter must absolutely return to the IC ground. Do not connect it to an intermediate point. Keep the optocoupler collector close to its return ground and make sure these two lines are away from noisy sources (MOSFETs, transformer). Don't cross noisy tracks. A small capacitor connected between FB and GND pins will not only place the high−frequency pole you need for compensation but it will also locally filter the noise picked up by the feedback and return lines. As mentioned above, the capacitor has to be placed as close as possible to the pin controller.

The 3rd MOSFET used to refresh the bootstrap capacitor has to be placed as closed as possible to the high side driver in order to avoid large noise peak current. Short connection should be used between the HB pin and the drain and between IC GND and source pin.

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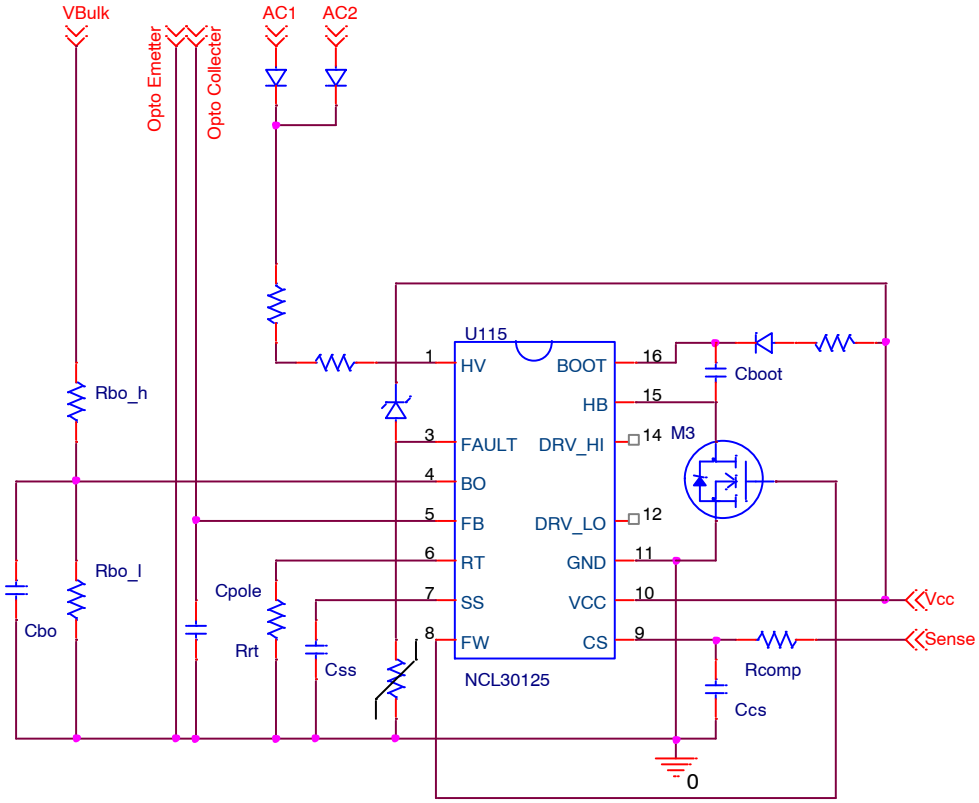


Figure 51. Typical Schematic with Components that Should be Placed Close to the IC

ORDERING INFORMATION

Device	OCP	FW in Normal Operation	Marking	Package	Shipping†
NCL30125A2DR2G	Latched	Enabled	30125A2	SOIC – 16 (Pb – Free)	2500 / Tape & Reel
NCL30125B2DR2G	Autorecovery	Enabled	30125B2		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

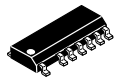
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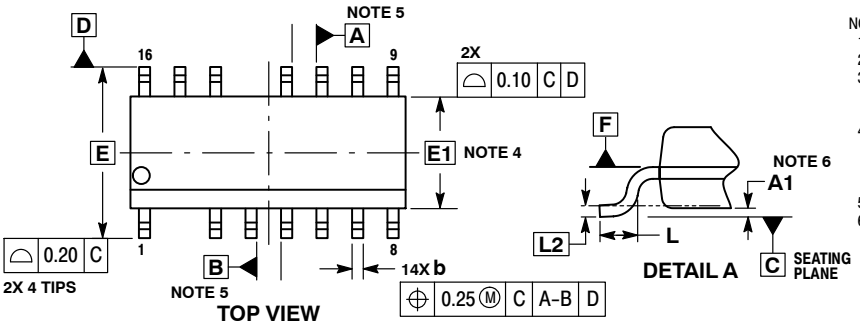
SOIC−16 NB MISSING PINS 2 AND 13

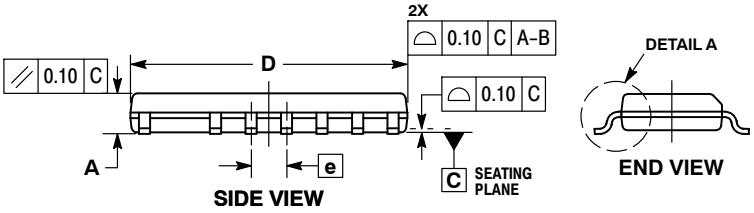
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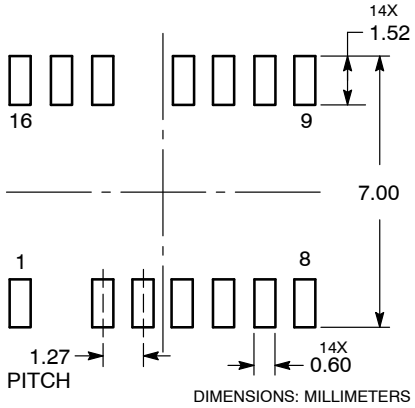




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DIMENSIONS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

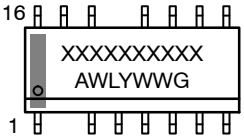
	MILLIMETERS	
DIM	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.35	0.49
c	0.17	0.25
D	9.80	10.00
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
L2	0.203 BSC	

RECOMMENDED SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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