# 74LVC1G74

## Single D-type flip-flop with set and reset; positive edge trigger

Rev. 18 — 22 September 2025 Product data sheet

## 1. General description

The 74LVC1G74 is a single positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using $I_{OFF}$. The $I_{OFF}$ circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

## 2. Features and benefits

- Wide supply voltage range from 1.65 V to 5.5 V
- Overvoltage tolerant inputs to 5.5 V
- High noise immunity
- ±24 mA output drive ($V_{CC}$ = 3.0 V)
- CMOS low power consumption
- Direct interface with TTL levels
- $I_{OFF}$ circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

# 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC1G74DP | -40 °C to +125 °C | TSSOP8 | plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm | SOT505-2 |
| 74LVC1G74DC | -40 °C to +125 °C | VSSOP8 | plastic very thin shrink small outline package; 8 leads; body width 2.3 mm | SOT765-1 |
| 74LVC1G74GT | -40 °C to +125 °C | XSON8 | plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm | SOT833-1 |
| 74LVC1G74GN | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm | SOT1116 |
| 74LVC1G74GS | -40 °C to +125 °C | XSON8 | extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm | SOT1203 |

# 4. Marking

**Table 2. Marking codes**

| Type number | Marking code [1] |
|---|---|
| 74LVC1G74DP | V74 |
| 74LVC1G74DC | V74 |
| 74LVC1G74GT | V74 |
| 74LVC1G74GN | Y4 |
| 74LVC1G74GS | Y4 |

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

# 5. Functional diagram

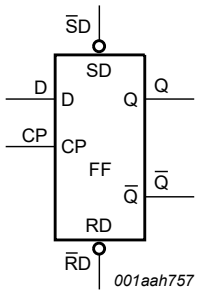



**Fig. 1. Logic symbol**

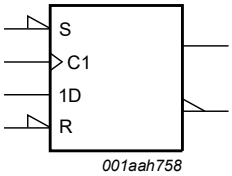



**Fig. 2. IEC logic symbol**

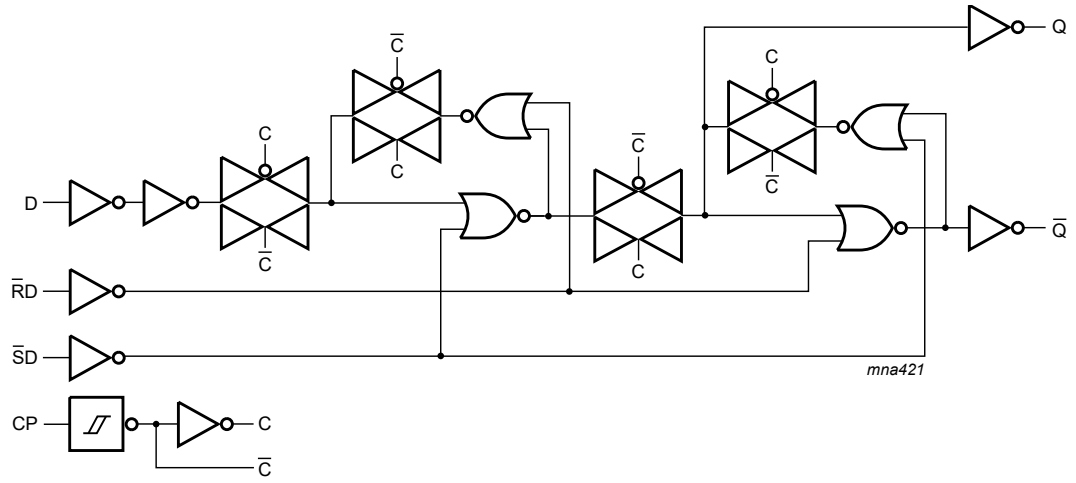
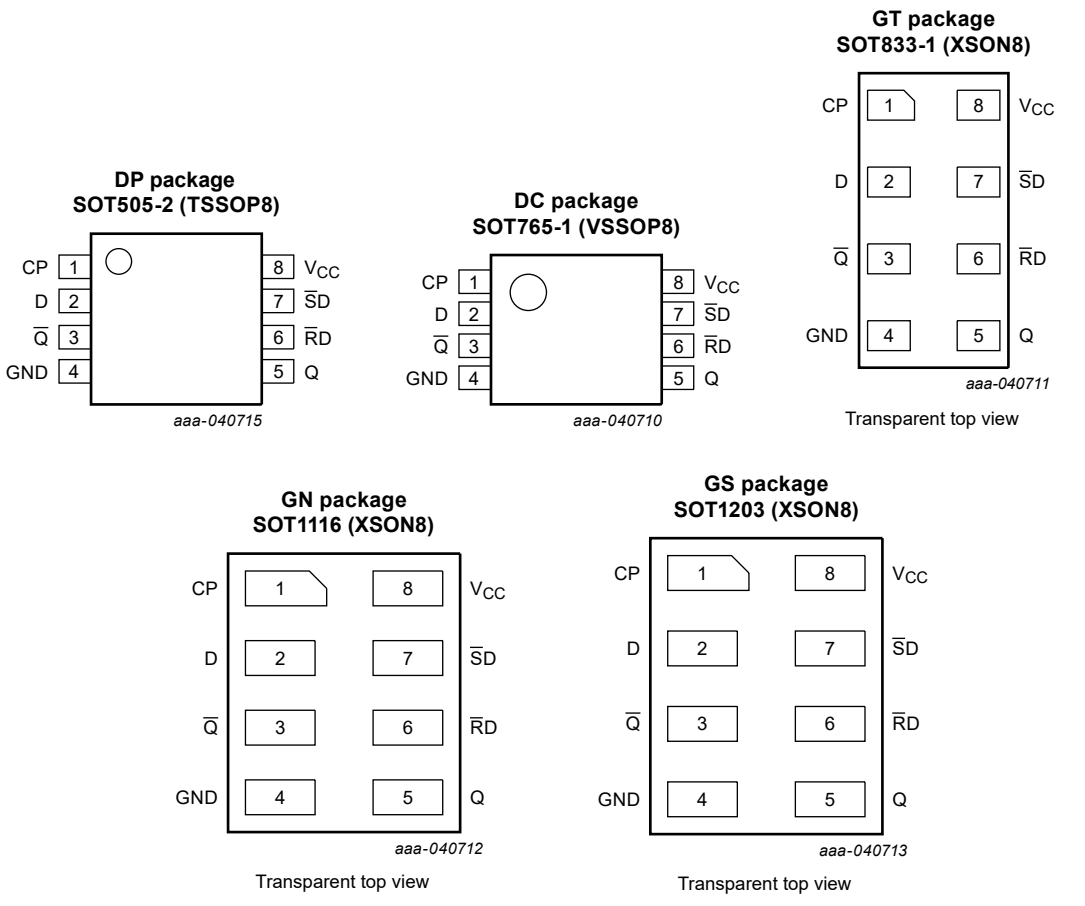



Fig. 3. Logic diagram

# 6. Pinning information

## 6.1. Pinning



### 6.2. Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| CP | 1 | clock input (LOW-to-HIGH, edge-triggered) |
| D | 2 | data input |
| $\overline{Q}$ | 3 | complement output |
| GND | 4 | ground (0 V) |
| Q | 5 | true output |
| $\overline{RD}$ | 6 | asynchronous reset-direct input (active LOW) |
| $\overline{SD}$ | 7 | asynchronous set-direct input (active LOW) |
| $V_{CC}$ | 8 | supply voltage |

## 7. Functional description

**Table 4. Function table for asynchronous operation**

*H = HIGH voltage level; L = LOW voltage level; X = don't care.*

| Input | | | | Output | |
|---|---|---|---|---|---|
| **$\overline{SD}$** | **$\overline{RD}$** | **CP** | **D** | **Q** | **$\overline{Q}$** |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | L | X | Q | $\overline{Q}$ |

**Table 5. Function table for synchronous operation**

*H = HIGH voltage level; L = LOW voltage level; ↑ = LOW-to-HIGH CP transition;*
*$Q_{n+1}$ = state after the next LOW-to-HIGH CP transition.*

| Input | | | | Output | |
|---|---|---|---|---|---|
| **$\overline{SD}$** | **$\overline{RD}$** | **CP** | **D** | **$Q_{n+1}$** | **$\overline{Q}_{n+1}$** |
| H | H | ↑ | L | L | H |
| H | H | ↑ | H | H | L |

# 8. Limiting values

**Table 6. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | -0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | -50 | - | mA |
| $V_I$ | input voltage | [1] | -0.5 | +6.5 | V |
| $I_{OK}$ | output clamping current | $V_O > V_{CC}$ or $V_O < 0$ V | - | ±50 | mA |
| $V_O$ | output voltage | Active mode [1] | -0.5 | $V_{CC}$ + 0.5 | V |
| | | Power-down mode; $V_{CC}$ = 0 V [1] | -0.5 | +6.5 | V |
| $I_O$ | output current | $V_O$ = 0 V to $V_{CC}$ | - | ±50 | mA |
| $I_{CC}$ | supply current | | - | 100 | mA |
| $I_{GND}$ | ground current | | -100 | - | mA |
| $P_{tot}$ | total power dissipation | $T_{amb}$ = -40 °C to +125 °C [2] | - | 250 | mW |
| $T_{stg}$ | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT505-2 (TSSOP8) package: $P_{tot}$ derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: $P_{tot}$ derates linearly with 4.9 mW/K above 99 °C.
For SOT833-1 (XSON8) package: $P_{tot}$ derates linearly with 3.1 mW/K above 68 °C.
For SOT1116 (XSON8) package: $P_{tot}$ derates linearly with 4.2 mW/K above 90 °C.
For SOT1203 (XSON8) package: $P_{tot}$ derates linearly with 3.6 mW/K above 81 °C.

# 9. Recommended operating conditions

**Table 7. Operating conditions**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 1.65 | 5.5 | V |
| $V_I$ | input voltage | | 0 | 5.5 | V |
| $V_O$ | output voltage | Active mode | 0 | $V_{CC}$ | V |
| | | Power-down mode; $V_{CC}$ = 0 V | 0 | 5.5 | V |
| $T_{amb}$ | ambient temperature | | -40 | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC}$ = 1.65 V to 2.7 V | - | 20 | ns/V |
| | | $V_{CC}$ = 2.7 V to 5.5 V | - | 10 | ns/V |

# 10. Static characteristics

**Table 8. Static characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | $T_{amb}$ = -40 °C to +85 °C | | | $T_{amb}$ = -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | 0.65$V_{CC}$ | - | - | 0.65$V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.7$V_{CC}$ | - | - | 0.7$V_{CC}$ | - | V |

| Symbol | Parameter | Conditions | $T_{amb}$ = -40 °C to +85 °C | | | $T_{amb}$ = -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | - | - | $0.35V_{CC}$ | - | $0.35V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 2.7 V to 3.6 V | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | $0.3V_{CC}$ | - | $0.3V_{CC}$ | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = -100 µA; $V_{CC}$ = 1.65 V to 5.5 V | $V_{CC}$ - 0.1 | - | - | $V_{CC}$ - 0.1 | - | V |
| | | $I_O$ = -4 mA; $V_{CC}$ = 1.65 V | 1.2 | 1.54 | - | 0.95 | - | V |
| | | $I_O$ = -8 mA; $V_{CC}$ = 2.3 V | 1.9 | 2.15 | - | 1.7 | - | V |
| | | $I_O$ = -12 mA; $V_{CC}$ = 2.7 V | 2.2 | 2.50 | - | 1.9 | - | V |
| | | $I_O$ = -24 mA; $V_{CC}$ = 3.0 V | 2.3 | 2.62 | - | 2.0 | - | V |
| | | $I_O$ = -32 mA; $V_{CC}$ = 4.5 V | 3.8 | 4.11 | - | 3.4 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_I$ = $V_{IH}$ or $V_{IL}$ | | | | | | |
| | | $I_O$ = 100 µA; $V_{CC}$ = 1.65 V to 5.5 V | - | - | 0.10 | - | 0.10 | V |
| | | $I_O$ = 4 mA; $V_{CC}$ = 1.65 V | - | 0.07 | 0.45 | - | 0.70 | V |
| | | $I_O$ = 8 mA; $V_{CC}$ = 2.3 V | - | 0.12 | 0.30 | - | 0.45 | V |
| | | $I_O$ = 12 mA; $V_{CC}$ = 2.7 V | - | 0.17 | 0.40 | - | 0.60 | V |
| | | $I_O$ = 24 mA; $V_{CC}$ = 3.0 V | - | 0.33 | 0.55 | - | 0.80 | V |
| | | $I_O$ = 32 mA; $V_{CC}$ = 4.5 V | - | 0.39 | 0.55 | - | 0.80 | V |
| $I_I$ | input leakage current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | - | ±0.1 | ±1 | - | ±1 | µA |
| $I_{OFF}$ | power-off leakage current | $V_I$ or $V_O$ = 5.5 V; $V_{CC}$ = 0 V | - | ±0.1 | ±2 | - | ±2 | µA |
| $I_{CC}$ | supply current | $V_I$ = 5.5 V or GND; $V_{CC}$ = 1.65 V to 5.5 V; $I_O$ = 0 A | - | 0.1 | 4 | - | 4 | µA |
| $\Delta I_{CC}$ | additional supply current | per pin; $V_I$ = $V_{CC}$ - 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 2.3 V to 5.5 V | - | 5 | 500 | - | 500 | µA |
| $C_I$ | input capacitance | | - | 4.0 | - | - | - | pF |

[1] All typical values are measured at $T_{amb}$ = 25 °C.

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.*

| Symbol | Parameter | Conditions | $T_{amb}$ = -40 °C to +85 °C | | | $T_{amb}$ = -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | CP to Q, $\overline{Q}$; see Fig. 4 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | 6.0 | 13.4 | 1.5 | 13.4 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.5 | 7.1 | 1.0 | 7.1 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 3.5 | 7.1 | 1.0 | 7.1 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.5 | 5.9 | 1.0 | 5.9 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | 2.5 | 4.1 | 1.0 | 4.1 | ns |
| | | $\overline{SD}$ to Q, $\overline{Q}$; see Fig. 5 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | 6.0 | 12.9 | 1.5 | 12.9 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.0 | 5.9 | 1.0 | 5.9 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | 2.5 | 4.1 | 1.0 | 4.1 | ns |
| | | $\overline{RD}$ to Q, $\overline{Q}$; see Fig. 5 [2] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | 5.0 | 12.9 | 1.5 | 12.9 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 3.5 | 7.0 | 1.0 | 7.0 | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 3.0 | 5.9 | 1.0 | 5.9 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | 2.5 | 4.1 | 1.0 | 4.1 | ns |
| $t_W$ | pulse width | CP HIGH or LOW; see Fig. 4 | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 6.2 | - | - | 6.2 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC}$ = 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.7 | 1.3 | - | 2.7 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | ns |
| | | $\overline{SD}$ and $\overline{RD}$ LOW; see Fig. 5 | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 6.2 | - | - | 6.2 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC}$ = 2.7 V | 2.7 | - | - | 2.7 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 2.7 | 1.6 | - | 2.7 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | ns |
| $t_{rec}$ | recovery time | $\overline{SD}$ or $\overline{RD}$; see Fig. 5 | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.9 | - | - | 1.9 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.4 | - | - | 1.4 | - | ns |
| | | $V_{CC}$ = 2.7 V | 1.3 | - | - | 1.3 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | +1.2 | -3.0 | - | +1.2 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | - | - | 1.0 | - | ns |

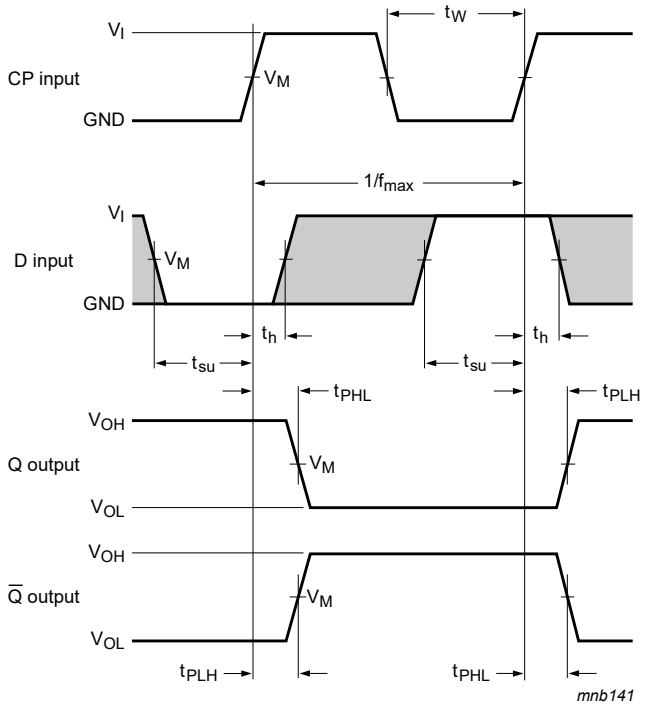
| Symbol | Parameter | Conditions | $T_{amb}$ = -40 °C to +85 °C | | | $T_{amb}$ = -40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ [1] | Max | Min | Max | |
| $t_{su}$ | set-up time | D to CP; see Fig. 4 | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.9 | - | - | 2.9 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | ns |
| | | $V_{CC}$ = 2.7 V | 1.7 | - | - | 1.7 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.3 | 0.5 | - | 1.3 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.1 | - | - | 1.1 | - | ns |
| $t_h$ | hold time | D to CP; see Fig. 4 | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.5 | - | - | 1.5 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | - | - | 1.0 | - | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | - | - | 1.0 | - | ns |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 1.0 | 0.6 | - | 1.0 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 1.0 | - | - | 1.0 | - | ns |
| $f_{max}$ | maximum frequency | CP; see Fig. 4 | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 80 | - | - | 80 | - | MHz |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 175 | - | - | 175 | - | MHz |
| | | $V_{CC}$ = 2.7 V | 175 | - | - | 175 | - | MHz |
| | | $V_{CC}$ = 3.0 V to 3.6 V | 175 | 280 | - | 175 | - | MHz |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 200 | - | - | 200 | - | MHz |
| $C_{PD}$ | power dissipation capacitance | $V_I$ = GND to $V_{CC}$; $V_{CC}$ = 3.3 V [3] | - | 15 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C and $V_{CC}$ = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

[3] $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW). $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz;
$C_L$ = output load capacitance in pF; $V_{CC}$ = supply voltage in V;
N = number of inputs switching; $\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

## 11.1. Waveforms and test circuit

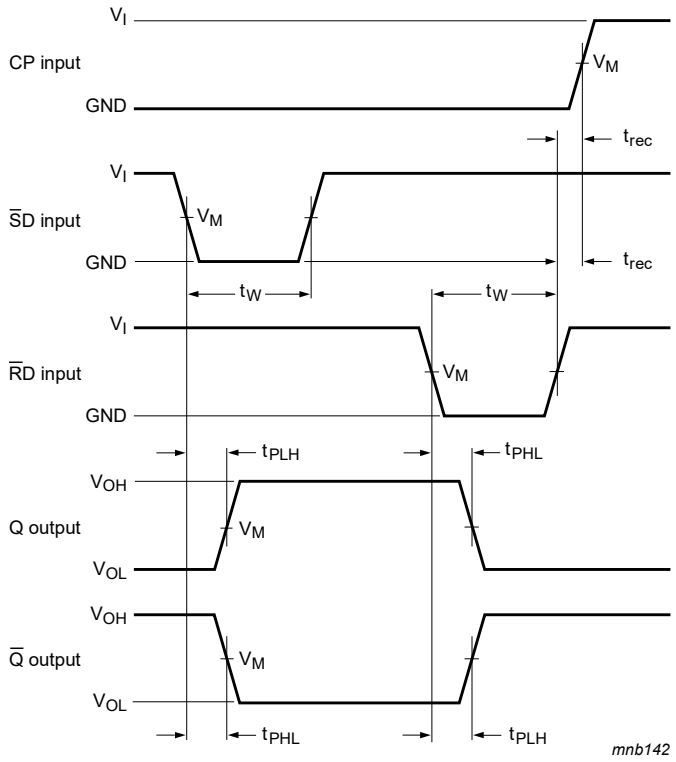



Measurement points are given in Table 10.

The shaded areas indicate when the input is permitted to change for predictable output performance.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 4. The clock input (CP) to output (Q, $\overline{Q}$) propagation delays and pulse width, D to CP set-up, CP to D hold times and the maximum frequency**



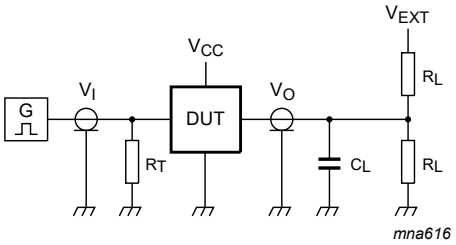

Measurement points are given in Table 10.

$V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig. 5. The set ($\overline{SD}$) and reset ($\overline{RD}$) input to output (Q, $\overline{Q}$) propagation delays, pulse widths and the $\overline{RD}$ to CP recovery time**

**Table 10. Measurement points**

| Supply voltage | Input | Output |
|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ |
| 1.65 V to 1.95 V | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |
| 2.3 V to 2.7 V | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |
| 2.7 V | 1.5 V | 1.5 V |
| 3.0 V to 3.6 V | 1.5 V | 1.5 V |
| 4.5 V to 5.5 V | 0.5 × $V_{CC}$ | 0.5 × $V_{CC}$ |




Test data is given in Table 11.

Definitions for test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to the output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = External voltage for measuring switching times.

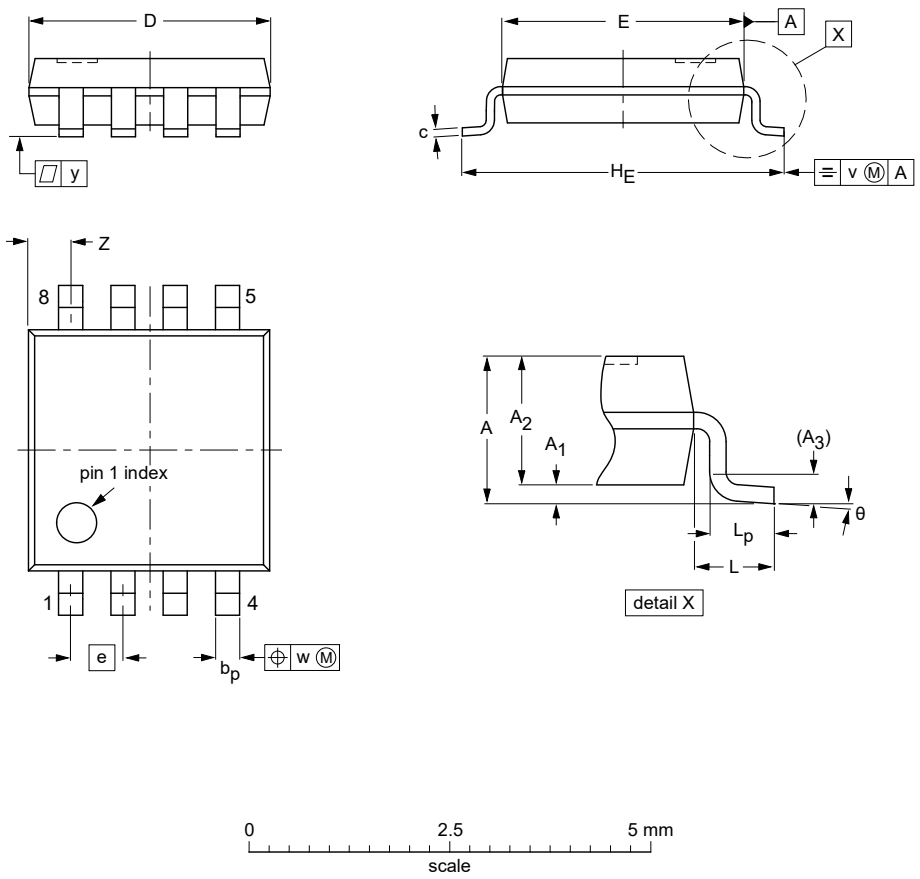
**Fig. 6. Test circuit for measuring switching times**

**Table 11. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 1 kΩ | open | GND | 2 × $V_{CC}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 30 pF | 500 Ω | open | GND | 2 × $V_{CC}$ |
| 2.7 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 3.0 V to 3.6 V | 2.7 V | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 6 V |
| 4.5 V to 5.5 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | 2 × $V_{CC}$ |

## 12. Package outline

**TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.00 | 0.95<br>0.75 | 0.25 | 0.38<br>0.22 | 0.18<br>0.08 | 3.1<br>2.9 | 3.1<br>2.9 | 0.65 | 4.1<br>3.9 | 0.5 | 0.47<br>0.33 | 0.2 | 0.13 | 0.1 | 0.70<br>0.35 | 8°<br>0° |

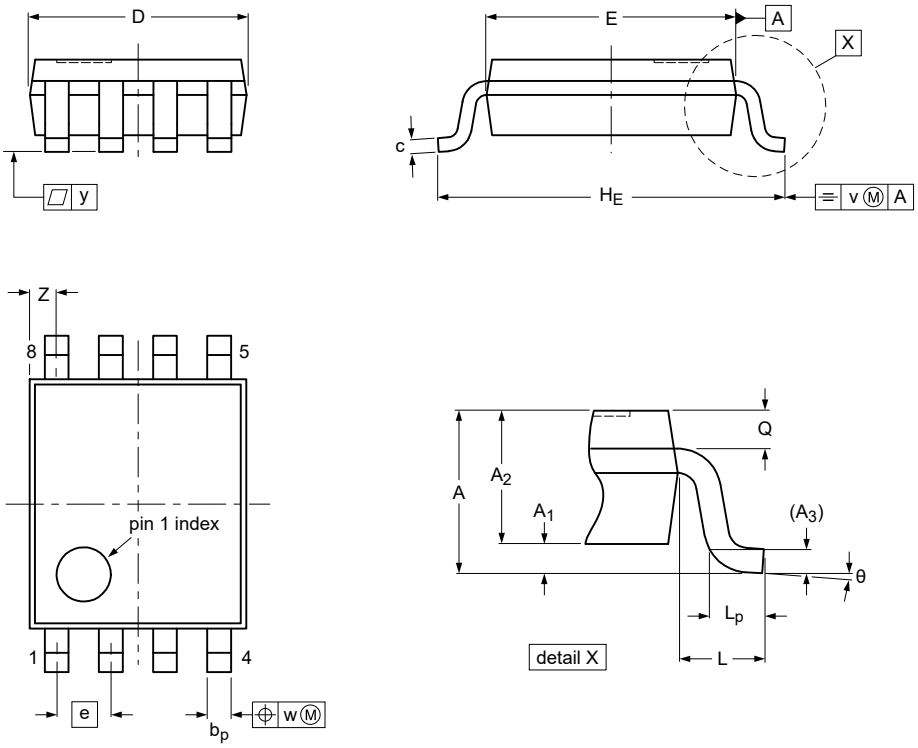
**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT505-2 | | - - - | | | | 02-01-16 |

**Fig. 7. Package outline SOT505-2 (TSSOP8)**

**VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm** **SOT765-1**




Dimensions (mm are the original dimensions)

| Unit | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| max | | 0.15 | 0.85 | | 0.27 | 0.23 | 2.1 | 2.4 | | 3.2 | | 0.40 | 0.21 | | | | 0.4 | 8° |
| mm nom | 1 | | | 0.12 | | | | | 0.5 | | 0.4 | | | 0.2 | 0.08 | 0.1 | | |
| min | | 0.00 | 0.60 | | 0.17 | 0.08 | 1.9 | 2.2 | | 3.0 | | 0.15 | 0.19 | | | | 0.1 | 0° |

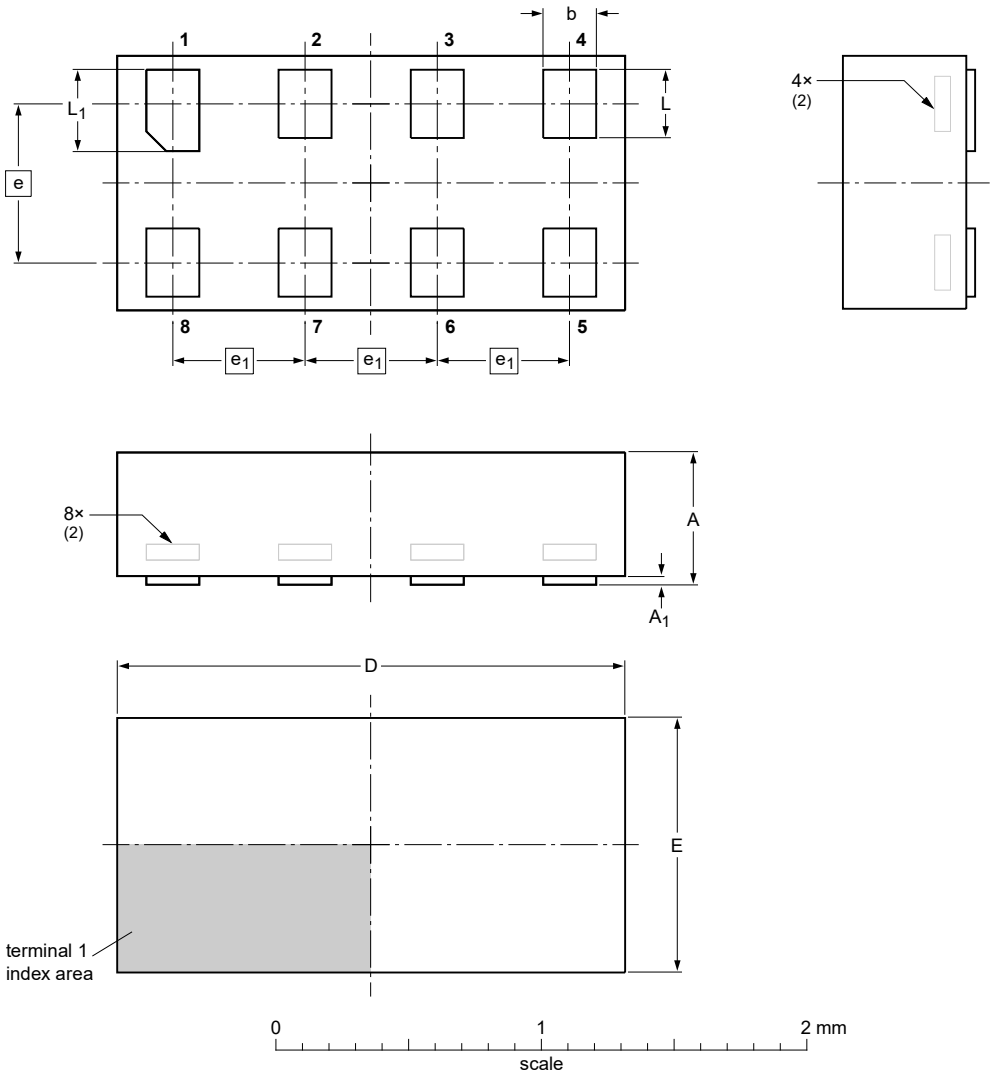
Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

*sot765-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT765-1 | | MO-187 | | | | ~~07-06-02~~ 16-05-31 |

**Fig. 8. Package outline SOT765-1 (VSSOP8)**

**XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm** **SOT833-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max | $A_1$ max | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.25<br>0.17 | 2.0<br>1.9 | 1.05<br>0.95 | 0.6 | 0.5 | 0.35<br>0.27 | 0.40<br>0.32 |

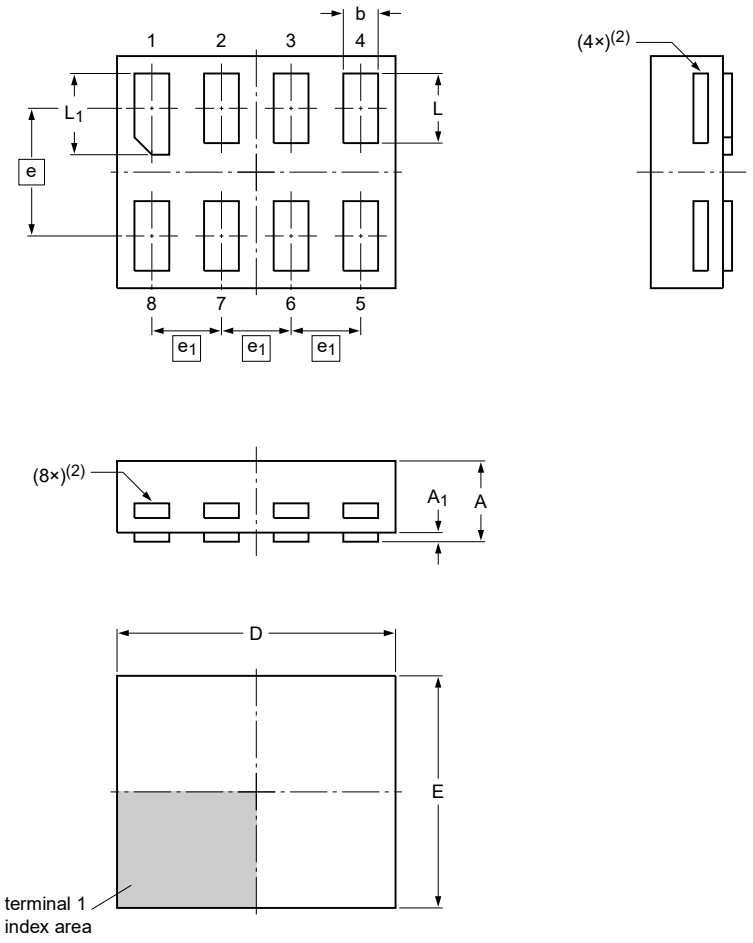
**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT833-1 | - - - | MO-252 | - - - | | | ~~07-11-14~~<br>07-12-07 |

**Fig. 9. Package outline SOT833-1 (XSON8)**

**XSON8: extremely thin small outline package; no leads;**
**8 terminals; body 1.2 x 1.0 x 0.35 mm** **SOT1116**




Dimensions

| Unit | | A(1) | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.35 | 0.04 | 0.20 | 1.25 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.15 | 1.20 | 1.00 | 0.55 | 0.3 | 0.30 | 0.35 |
| | min | | | 0.12 | 1.15 | 0.95 | | | 0.27 | 0.32 |

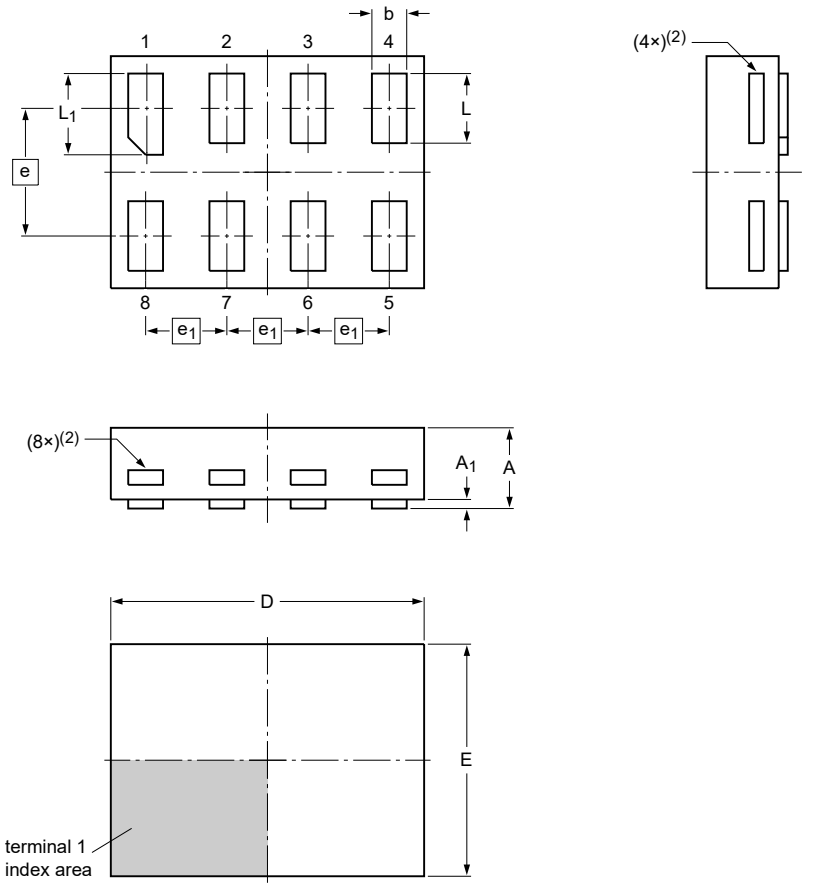
Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

*sot1116_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1116 | | | | | | ~~10-04-02~~ 10-04-07 |

**Fig. 10. Package outline SOT1116 (XSON8)**

**XSON8: extremely thin small outline package; no leads; 8 terminals; body 1.35 x 1.0 x 0.35 mm** **SOT1203**




Dimensions

| Unit | | A(1) | $A_1$ | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 0.35 | 0.04 | 0.20 | 1.40 | 1.05 | | | 0.35 | 0.40 |
| | nom | | | 0.15 | 1.35 | 1.00 | 0.55 | 0.35 | 0.30 | 0.35 |
| | min | | | 0.12 | 1.30 | 0.95 | | | 0.27 | 0.32 |

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

*sot1203_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1203 | | | | | | ~~10-04-02~~ 10-04-06 |

**Fig. 11. Package outline SOT1203 (XSON8)**

# 13. Abbreviations

**Table 12. Abbreviations**

| Acronym | Description |
|---|---|
| ANSI | American National Standards Institute |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| ESDA | ElectroStatic Discharge Association |
| HBM | Human Body Model |
| JEDEC | Joint Electron Device Engineering Council |
| TTL | Transistor-Transistor Logic |

# 14. Revision history

**Table 13. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC1G74 v.18 | 20250922 | Product data sheet | - | 74LVC1G74 v.17 |
| Modifications: | • Updates made to Table 4. | | | |
| 74LVC1G74 v.17 | 20240809 | Product data sheet | - | 74LVC1G74 v.16 |
| Modifications: | • Type number 74LVC1G74GF (SOT1089/XSON8) removed. | | | |
| 74LVC1G74 v.16 | 20230818 | Product data sheet | - | 74LVC1G74 v.15 |
| Modifications: | • Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74LVC1G74 v.15 | 20210920 | Product data sheet | - | 74LVC1G74 v.14 |
| Modifications: | • Section 1 and Section 2 updated.<br>• Type number 74LVC1G74GM (SOT902-2/XQFN8) removed.<br>• Section 8: $P_{tot}$ total power dissipation and derating values updated. | | | |
| 74LVC1G74 v.14 | 20181227 | Product data sheet | - | 74LVC1G74 v.13 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate.<br>• Type number 74LVC1G74GD (SOT996-2) removed. | | | |
| 74LVC1G74 v.13 | 20161205 | Product data sheet | - | 74LVC1G74 v.12 |
| Modifications: | • Table 8: The maximum limits for leakage current and supply current have changed. | | | |
| 74LVC1G74 v.12 | 20130402 | Product data sheet | - | 74LVC1G74 v.11 |
| Modifications: | • For type number 74LVC1G74GD XSON8U has changed to XSON8. | | | |
| 74LVC1G74 v.11 | 20120604 | Product data sheet | - | 74LVC1G74 v.10 |
| Modifications: | • For type number 74LVC1G74GM the SOT code has changed to SOT902-2. | | | |
| 74LVC1G74 v.10 | 20111202 | Product data sheet | - | 74LVC1G74 v.9 |
| Modifications: | • Legal pages updated. | | | |
| 74LVC1G74 v.9 | 20100805 | Product data sheet | - | 74LVC1G74 v.8 |
| 74LVC1G74 v.8 | 20091203 | Product data sheet | - | 74LVC1G74 v.7 |
| 74LVC1G74 v.7 | 20080626 | Product data sheet | - | 74LVC1G74 v.6 |
| 74LVC1G74 v.6 | 20080219 | Product data sheet | - | 74LVC1G74 v.5 |

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC1G74 v.5 | 20070809 | Product data sheet | - | 74LVC1G74 v.4 |
| 74LVC1G74 v.4 | 20061207 | Product data sheet | - | 74LVC1G74 v.3 |

# 15. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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**Date of release: 22 September 2025**