

16-Mbit (2M words × 8 bits) Static RAM with Error-Correcting Code (ECC)

Features

- Ultra-low standby power
 - Typical standby current: 1.5 μ A
 - Maximum standby current: 8 μ A
- High speed: 45 ns
- Embedded error-correcting code (ECC) for single-bit error correction
- Wide voltage range: 2.2 V to 3.6 V
- 1.0 V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- ERR pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-ball VFBGA package

Functional Description

CY62168G30 and CY62168GE30 are high-performance CMOS low-power (MoBL) SRAM devices with embedded ECC. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY62168GE30 device includes an error indication pin that signals a single-bit error-detection and correction event during a read cycle.

Devices with a single chip enable input are accessed by asserting the chip enable input (CE) LOW. Dual chip enable devices are accessed by asserting both chip enable inputs – CE₁ as LOW and CE₂ as HIGH.

Write to the device by taking Chip Enable 1 ($\overline{CE_1}$) LOW and Chip Enable 2 (CE₂) HIGH and the Write Enable (WE) input LOW. Data on the eight I/O pins (I/O₀ through I/O₇) is then written into the location specified on the address pins (A₀ through A₂₀).

Read from the device by taking Chip Enable 1 ($\overline{CE_1}$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE₂) HIGH while forcing Write Enable (WE) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input and output pins (I/O₀ through I/O₇) are placed in a high impedance state when the device is deselected ($\overline{CE_1}$ HIGH or CE₂ LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE_1}$ LOW and CE₂ HIGH and WE LOW). See the [Truth Table – CY62168G/CY62168GE on page 13](#) for a complete description of read and write modes.

On CY62168GE30 devices, the detection and correction of a single bit error in the accessed location is indicated by the assertion of the ERR output (ERR = HIGH)^[1].

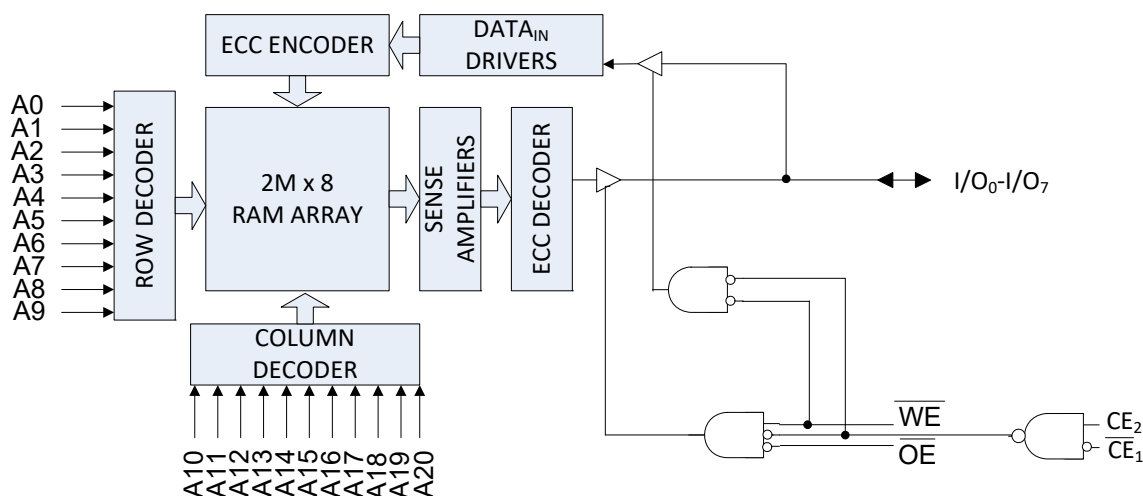
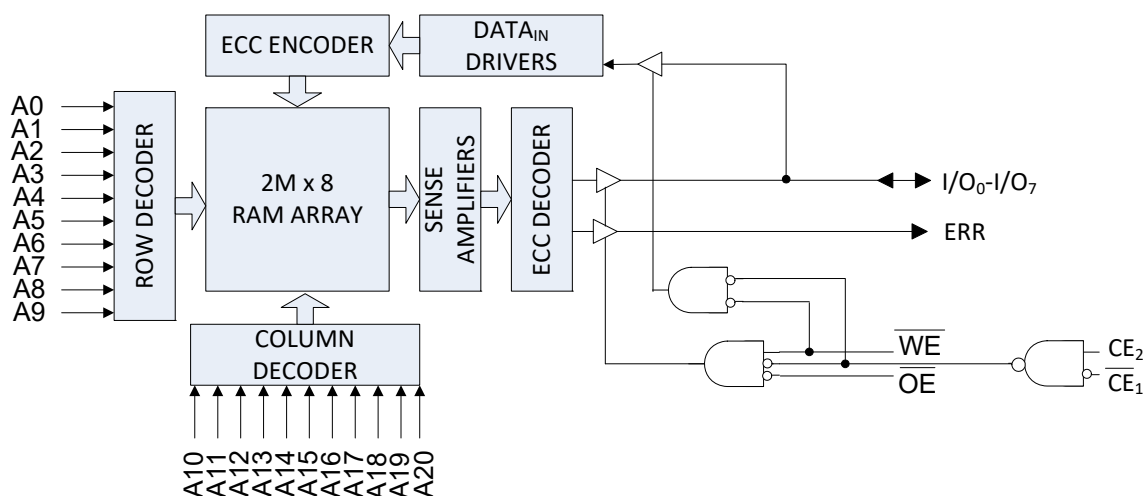
The CY62168G30 and CY62168GE30 devices are available in a Pb-free 48-pin VFBGA package. The logic block diagrams are on page 2.

Product Portfolio

Product	Features and Options (see Pin Configurations section)	Range	V _{CC} Range (V)	Speed (ns)	Power Dissipation			
					Operating I _{CC} , (mA)		Standby, I _{SB2} (μA)	
					f = f _{max}			
					Typ ^[2]	Max	Typ ^[2]	Max
CY62168G(E)30 ^[3, 4]	Single or dual Chip Enables Optional ERR pin	Industrial	2.2 V–3.6 V	45	29	35	1.5	8

Notes

1. This device does not support automatic write-back on error detection.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = 3 V (for V_{CC} range of 2.2 V–3.6 V), T_A = 25 °C.
3. This device offers improved I_{CC}, I_{SB1} and I_{SB2} specifications compared to the previous revision with same marketing part number.
4. For previous version of this device, kindly refer [here](#). Further details about improvement and comparison between old and new versions can be found in the [PCN193805](#).

Logic Block Diagram – CY62168G30

Logic Block Diagram – CY62168GE30


Contents

Pin Configurations	4	Ordering Information	14
Maximum Ratings	5	Ordering Code Definitions	14
Operating Range	5	Package Diagrams	15
DC Electrical Characteristics	5	Acronyms	16
Capacitance	6	Document Conventions	16
Thermal Resistance	6	Units of Measure	16
AC Test Loads and Waveforms	6	Document History Page	17
Data Retention Characteristics	7	Sales, Solutions, and Legal Information	18
Data Retention Waveform	7	Worldwide Sales and Design Support	18
Switching Characteristics	8	Products	18
Switching Waveforms	9	PSoC® Solutions	18
Truth Table – CY62168G/CY62168GE	13	Cypress Developer Community	18
ERR Output – CY62168GE	13	Technical Support	18

Pin Configurations

Figure 1. 48-ball VFBGA (6 × 8 × 1 mm) pinout ^[5]
CY62168G30

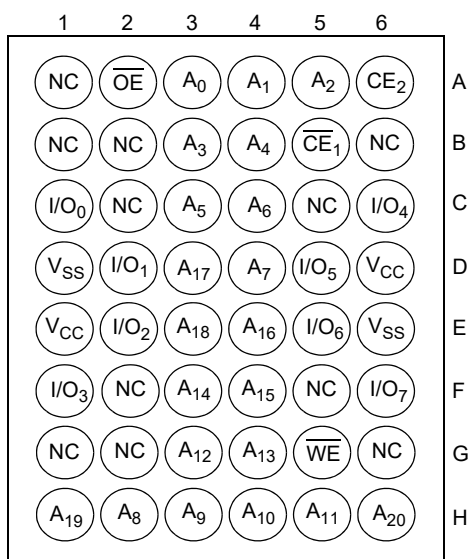
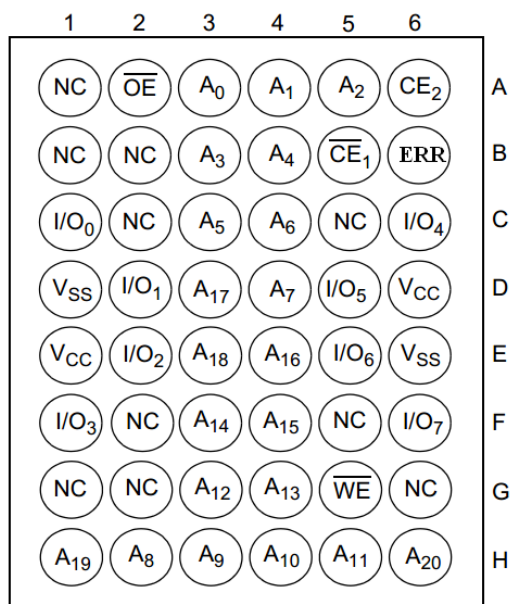


Figure 2. 48-ball VFBGA (6 × 8 × 1 mm) pinout ^[5, 6]
CY62168GE30



Notes

- NC pins are not connected internally to the die and are typically used for address expansion to a higher-density device. Refer to the respective datasheets for pin configuration.
- ERR is an Output pin. If not used, this pin should be left floating.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to + 150 °C

Ambient temperature
with power applied -55 °C to + 125 °C

Supply voltage to ground potential -0.5 V to 6 V

DC voltage applied to outputs
in High Z state^[7] -0.5 V to $V_{CC} + 0.5$ V

DC input voltage^[7] -0.5 V to $V_{CC} + 0.5$ V

Output current into outputs (LOW) 20 mA

Static discharge voltage
(MIL-STD-883, Method 3015) >2001 V

Latch-up current >140 mA

Operating Range

Grade	Ambient Temperature	V_{CC} ^[8]
Industrial	-40 °C to +85 °C	2.2 V to 3.6 V,

DC Electrical Characteristics

Over the operating range of -40 °C to 85 °C

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ ^[9]	Max	
V_{OH}	Output HIGH voltage	2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OH} = -0.1 \text{ mA}$	2.0	—	V
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OH} = -1.0 \text{ mA}$	2.4	—	V
V_{OL}	Output LOW voltage	2.2 V to 2.7 V	$V_{CC} = \text{Min}, I_{OL} = 0.1 \text{ mA}$	—	0.4	V
		2.7 V to 3.6 V	$V_{CC} = \text{Min}, I_{OL} = 2.1 \text{ mA}$	—	0.4	V
V_{IH}	Input HIGH voltage	2.2 V to 2.7 V	—	1.8	$V_{CC} + 0.3$	V
		2.7 V to 3.6 V	—	2.0	$V_{CC} + 0.3$	V
V_{IL}	Input LOW voltage ^[10]	2.2 V to 2.7 V	—	-0.3	0.6	V
		2.7 V to 3.6 V	—	-0.3	0.8	V
I_{IX}	Input leakage current	$GND \leq V_{IN} \leq V_{CC}$	-1.0	—	+1.0	μA
I_{OZ}	Output leakage current	$GND \leq V_{OUT} \leq V_{CC}$, Output disabled	-1.0	—	+1.0	μA
I_{CC} ^[11, 12]	V_{CC} operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, \text{CMOS levels}$	—	29.0	35.0	mA
		$f = 22.22 \text{ MHz (45 ns)}$	—	7.0	9.0	mA
I_{SB1} ^[11, 12, 13]	Automatic power down current – CMOS inputs; $V_{CC} = 2.2$ to 3.6 V	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}, V_{IN} \leq 0.2 \text{ V}, f = f_{\text{max}}$ (address and data only), $f = 0$ ($\overline{OE}$, and $\overline{WE}$), $V_{CC} = V_{CC(\text{max})}$	—	1.5	8.0	μA
		$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}, V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}, f = 0, V_{CC} = V_{CC(\text{max})}$	—	1.5	3.0 ^[15]	μA
I_{SB2} ^[11, 12, 14]	Automatic power down current – CMOS inputs; $V_{CC} = 2.2$ to 3.6 V	25 °C ^[15]	—	—	3.5 ^[15]	μA
		40 °C ^[15]	—	—	6.5 ^[15]	μA
		70 °C ^[15]	—	—	8.0	μA
		85 °C	—	—	8.0	μA

Notes

- $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.
- Full Device AC operation assumes a 100 μs ramp time from 0 to $V_{CC(\text{min})}$ and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3 \text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), $T_A = 25 \text{ °C}$.
- $V_{IL(\text{min})} = -2.0 \text{ V}$ and $V_{IH(\text{max})} = V_{CC} + 2 \text{ V}$ for pulse durations of less than 20 ns.
- This device offers improved I_{CC} , I_{SB1} and I_{SB2} specifications compared to the previous revision with same marketing part number.
- For previous version of this device, kindly refer [here](#). Further details about improvement and comparison between old and new versions can be found in the [PCN193805](#).
- This parameter is guaranteed by design and is not tested.
- Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
- The I_{SB2} limits at 25 °C, 40 °C, 70 °C and typical limit at 85 °C are guaranteed by design and not 100% tested.

Capacitance

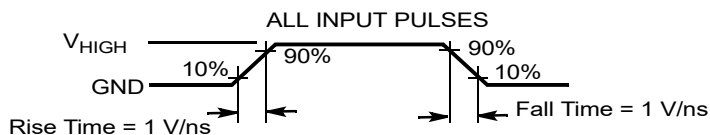
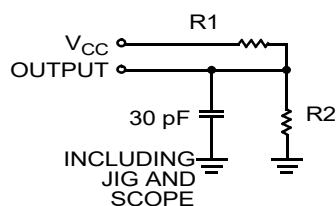
Parameter ^[16]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	$T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = V_{CC(\text{typ})}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

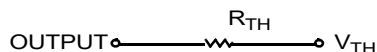
Parameter ^[16]	Description	Test Conditions	48-ball VFBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3×4.5 inch, four-layer printed circuit board	31.50	$^\circ\text{C/W}$
Θ_{JC}	Thermal resistance (junction to case)		15.75	$^\circ\text{C/W}$

AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms



Equivalent to: THÉVENIN EQUIVALENT



Parameters	1.8 V	2.5 V	3.0 V	5.0 V	Unit
R1	13500	16667	1103	1800	Ω
R2	10800	15385	1554	990	Ω
R_{TH}	6000	8000	645	639	Ω
V_{TH}	0.8	1.2	1.75	1.77	V
V_{HIGH}	1.8	2.5	3.0	5.0	V

Note

16. Tested initially and after any design or process changes that may affect these parameters.

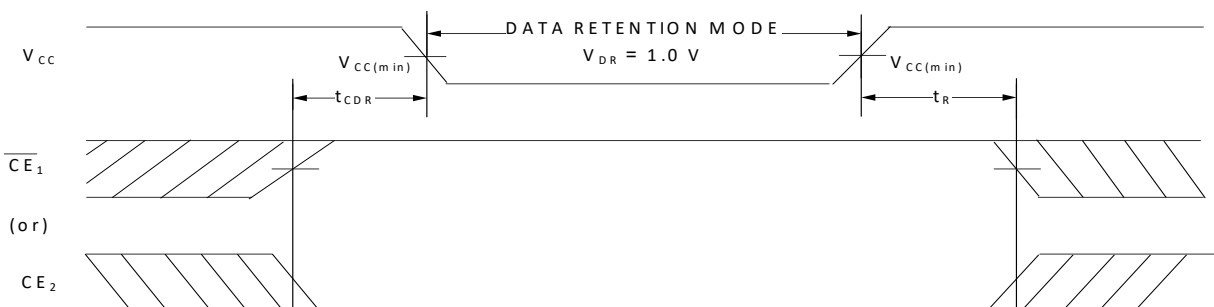
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ ^[17]	Max	Unit
V_{DR}	V_{CC} for data retention		1.0	–	–	V
I_{CCDR} ^[18, 19, 20, 21]	Data retention current	$1.2\text{ V} \leq V_{CC} \leq 2.2\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	16.0	μA
		$2.2\text{ V} < V_{CC} \leq 3.6\text{ V}$ or $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$	–	–	8.0	μA
t_{CDR} ^[22]	Chip deselect to data retention time		0	–	–	–
t_R ^[22, 23]	Operation recovery time		45/55	–	–	ns

Data Retention Waveform

Figure 4. Data Retention Waveform



Notes

17. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = 3\text{ V}$ (for V_{CC} range of 2.2 V–3.6 V), $T_A = 25^\circ\text{C}$.
18. Chip enables ($\overline{CE}_1$ and CE_2) must be tied to CMOS levels to meet the $I_{SB1}/I_{SB2}/I_{CCDR}$ spec. Other inputs can be left floating.
19. I_{CCDR} is guaranteed only after device is first powered up to $V_{CC(min)}$ and brought down to V_{DR} .
20. This device offers improved I_{CC} , I_{SB1} and I_{SB2} specifications compared to the previous revision with same marketing part number.
21. For previous version of this device, kindly refer [here](#). Further details about improvement and comparison between old and new versions can be found in the [PCN193805](#).
22. These parameters are guaranteed by design.
23. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)} \geq 100\text{ }\mu\text{s}$.

Switching Characteristics

Parameter ^[24, 25]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	45.0	–	ns
t _{AA}	Address to data valid / Address to ERR valid	–	45.0	ns
t _{OHA}	Data hold from address change / ERR hold from address change	10.0	–	ns
t _{ACE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to data valid / $\overline{CE}$ LOW to ERR valid	–	45.0	ns
t _{DOE}	$\overline{OE}$ LOW to data valid / $\overline{OE}$ LOW to ERR valid	–	22.0	ns
t _{LZOE}	$\overline{OE}$ LOW to Low Z ^[25, 26]	5.0	–	ns
t _{HZOE}	$\overline{OE}$ HIGH to High Z ^[25, 26, 27]	–	18.0	ns
t _{LZCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to Low Z ^[25, 26]	10.0	–	ns
t _{HZCE}	$\overline{CE}_1$ HIGH and CE ₂ LOW to High Z ^[25, 26, 27]	–	18.0	ns
t _{PU} ^[28]	$\overline{CE}_1$ LOW and CE ₂ HIGH to power-up	0	–	ns
t _{PD} ^[28]	$\overline{CE}_1$ HIGH and CE ₂ LOW to power-down	–	45.0	ns
Write Cycle ^[29, 30]				
t _{WC}	Write cycle time	45.0	–	ns
t _{SCE}	$\overline{CE}_1$ LOW and CE ₂ HIGH to write end	35.0	–	ns
t _{AW}	Address setup to write end	35.0	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{WE}$ pulse width	35.0	–	ns
t _{SD}	Data setup to write end	25.0	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	$\overline{WE}$ LOW to High Z ^[25, 27, 26]	–	18.0	ns
t _{LZWE}	$\overline{WE}$ HIGH to Low Z ^[25, 26]	10.0	–	ns

Notes

24. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for $V_{CC} \geq 3$ V) and $V_{CC}/2$ (for $V_{CC} < 3$ V), and input pulse levels of 0 to 3 V (for $V_{CC} \geq 3$ V) and 0 to V_{CC} (for $V_{CC} < 3$ V). Test conditions for the read cycle use output loading shown in AC Test Loads and Waveforms section, unless specified otherwise.

25. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.

26. Tested initially and after any design or process changes that may affect these parameters.

27. t_{HZOE} , t_{HZCE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

28. These parameters are guaranteed by design and are not tested.

29. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

30. The minimum write cycle pulse width for write cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ Low) should be equal to the sum of t_{HZWE} and t_{SD} .

Switching Waveforms

Figure 5. Read Cycle No. 1 of CY62168G (Address Transition Controlled)^[31, 32]

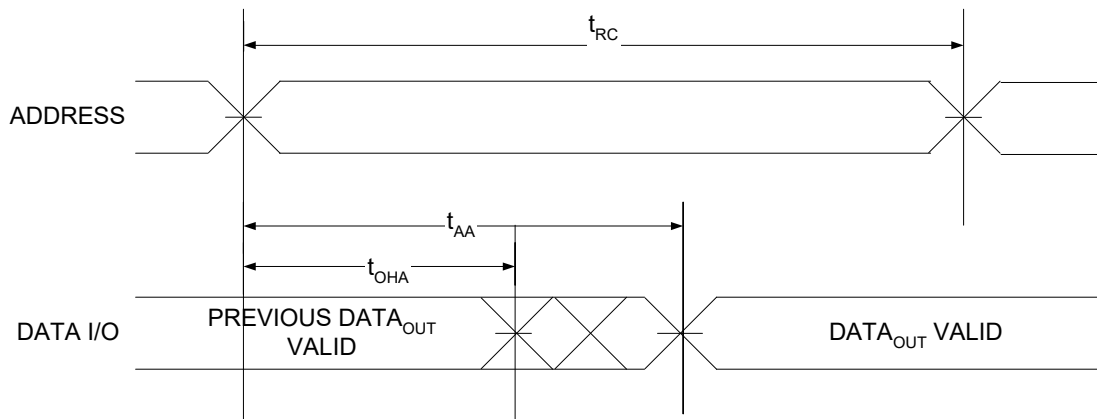
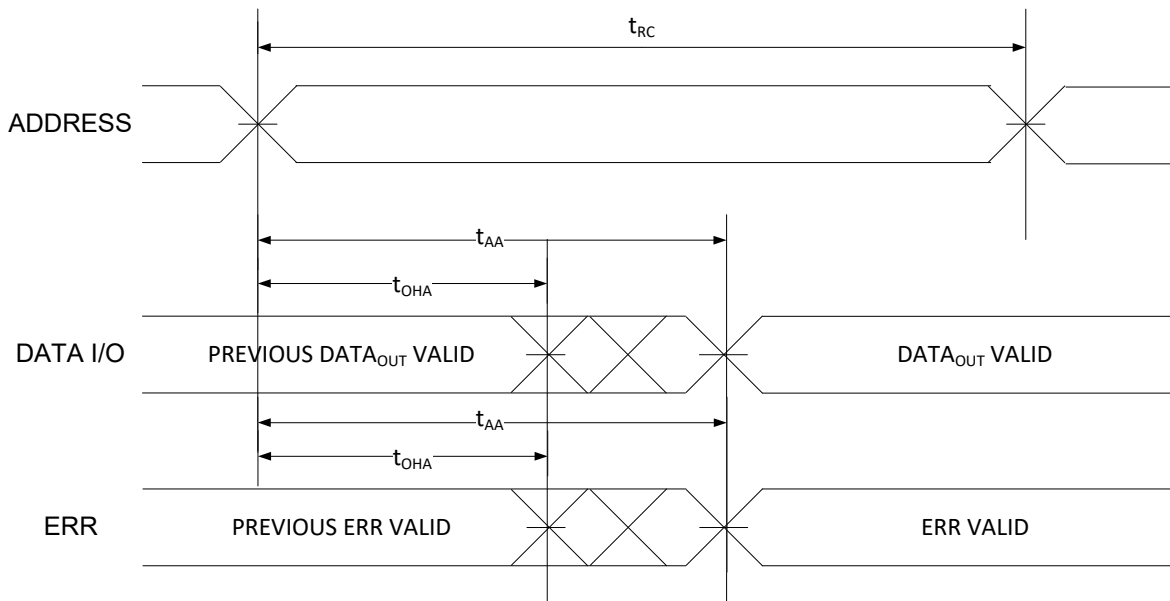
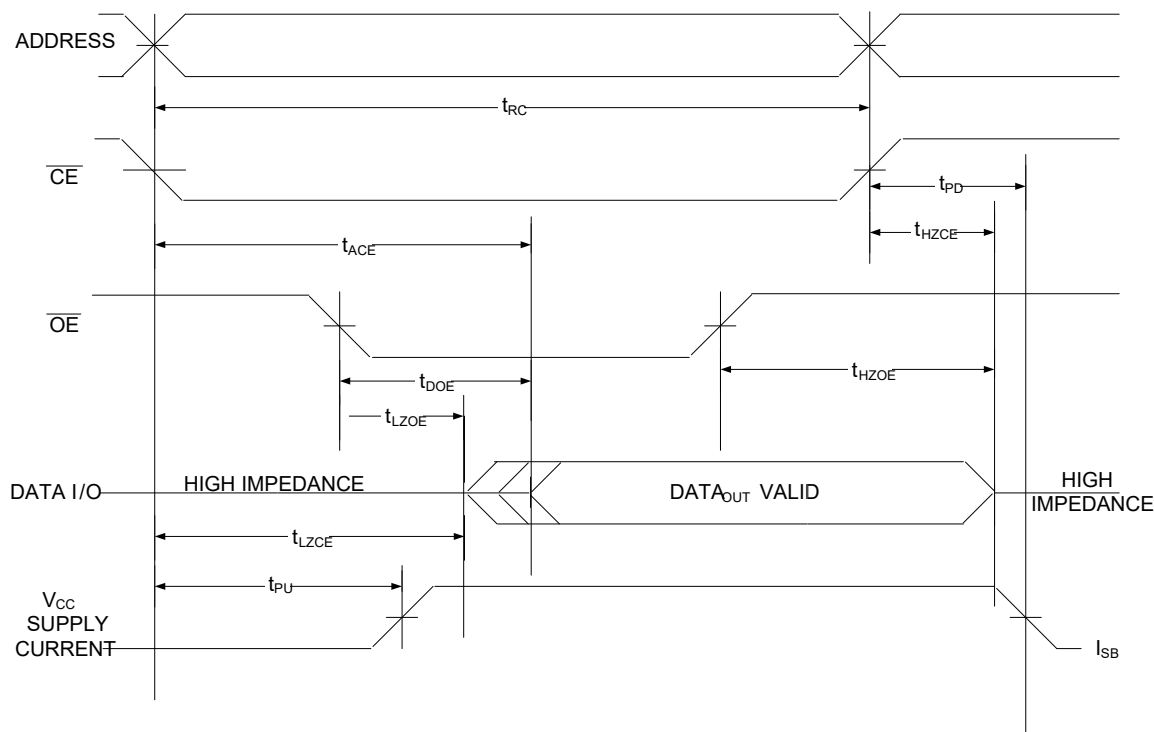


Figure 6. Read Cycle No. 1 of CY62168GE (Address Transition Controlled)^[31, 32]



Notes

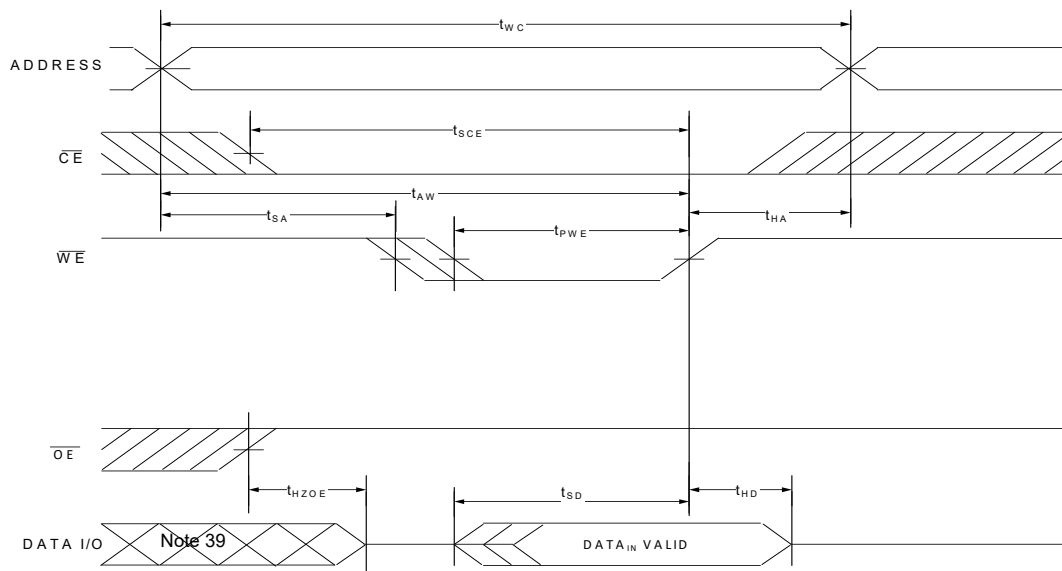
31. The device is continuously selected. $\overline{OE} = V_{IL}$, $\overline{CE} = V_{IL}$.
 32. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)
Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [33, 34, 35]

Notes

33. $\overline{WE}$ is HIGH for read cycle.

34. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2 . When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

35. Address valid prior to or coincident with $\overline{CE}$ LOW transition.

Switching Waveforms (continued)
Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled) [36, 37, 38]

Notes

36. For all dual chip enable devices, $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2 . When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

37. The internal write time of the memory is defined by the overlap of $\overline{WE} = V_{IL}$, $\overline{CE}_1 = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.

38. Data I/O is in the high-impedance state if $\overline{CE} = V_{IH}$ or $\overline{OE} = V_{IH}$.

39. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 9. Write Cycle No. 2 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ Low)^[40, 41, 42, 43]

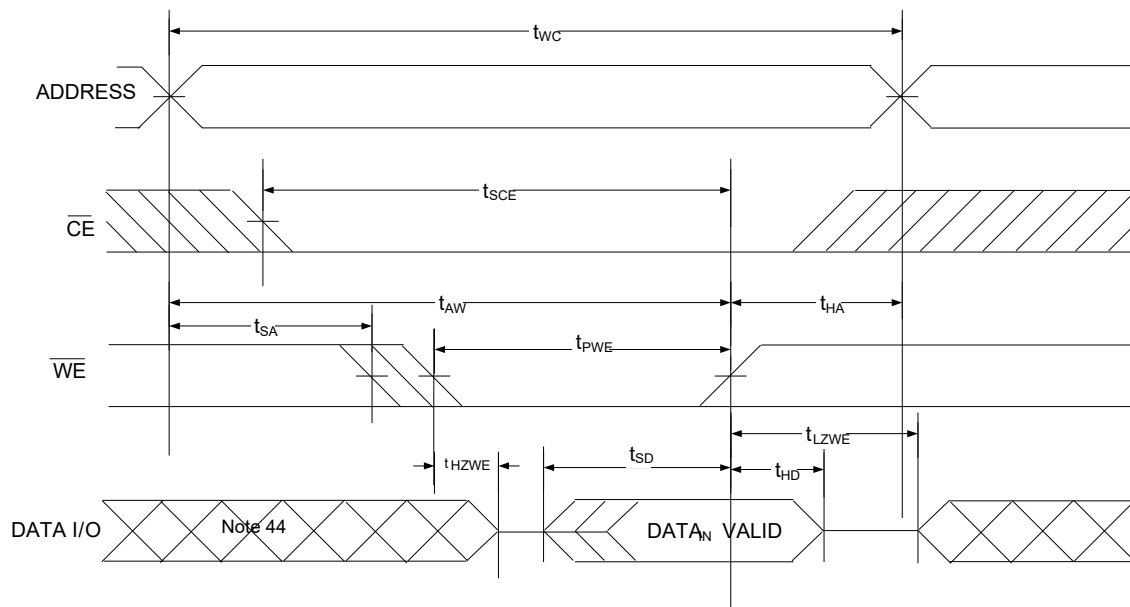
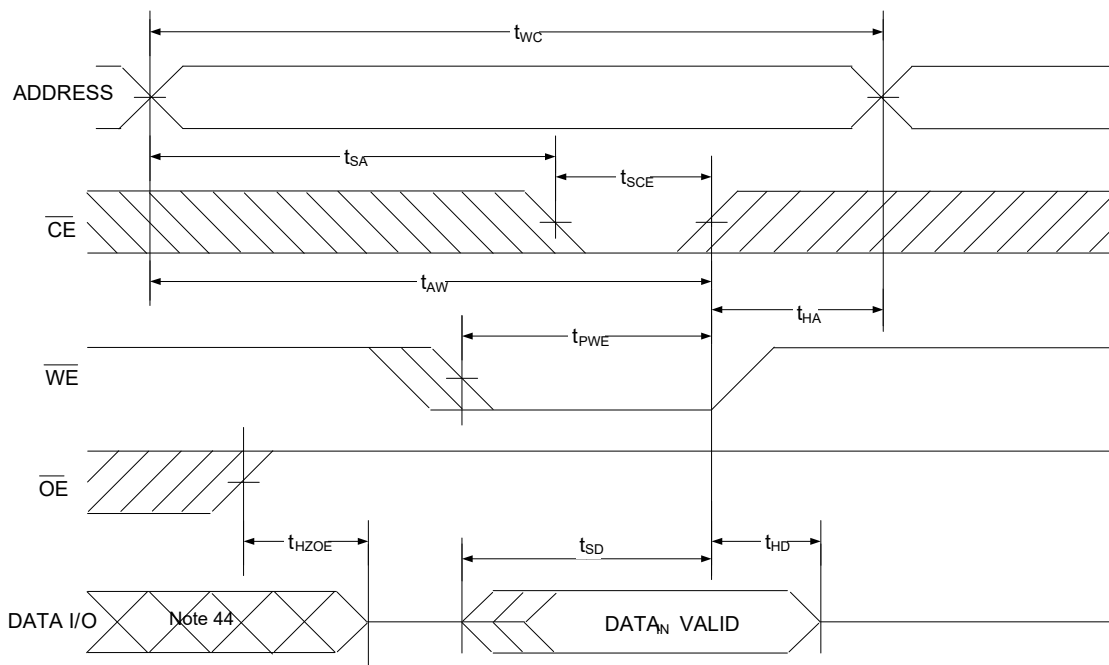


Figure 10. Write Cycle No. 3 ($\overline{\text{CE}}$ Controlled)^[40, 41, 42]



Notes

40. For all dual chip enable devices, $\overline{\text{CE}}$ is the logical combination of $\overline{\text{CE}}_1$ and CE_2 . When $\overline{\text{CE}}_1$ is LOW and CE_2 is HIGH, $\overline{\text{CE}}$ is LOW; when $\overline{\text{CE}}_1$ is HIGH or CE_2 is LOW, $\overline{\text{CE}}$ is HIGH.
41. The internal write time of the memory is defined by the overlap of $\overline{\text{WE}} = V_{IL}$, $\overline{\text{CE}}_1 = V_{IL}$, and $\text{CE}_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing must refer to the edge of the signal that terminates the write.
42. Data I/O is in high impedance state if $\overline{\text{CE}} = V_{IH}$ or $\overline{\text{OE}} = V_{IH}$.
43. The minimum write cycle pulse width should be equal to the sum of the t_{HZWE} and t_{SD} .
44. During this period I/O are in the output state. Do not apply input signals.

Truth Table – CY62168G/CY62168GE

$\overline{CE}_1$	CE_2	$\overline{WE}$	$\overline{OE}$	I/Os	Mode	Power
H	X ^[45]	X ^[45]	X ^[45]	High Z	Deselect / Power down	Standby (I_{SB2})
X ^[45]	L	X ^[45]	X ^[45]	High Z	Deselect / Power down	Standby (I_{SB2})
L	H	H	L	Data Out (I/O_0 – I/O_7)	Read	Active (I_{CC})
L	H	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	X	Data In (I/O_0 – I/O_7)	Write	Active (I_{CC})

ERR Output – CY62168GE

Output ^[46]	Mode
0	Read Operation, no single-bit error in the stored data.
1	Read Operation, single-bit error detected and corrected.
High Z	Device deselected / Outputs disabled / Write Operation.

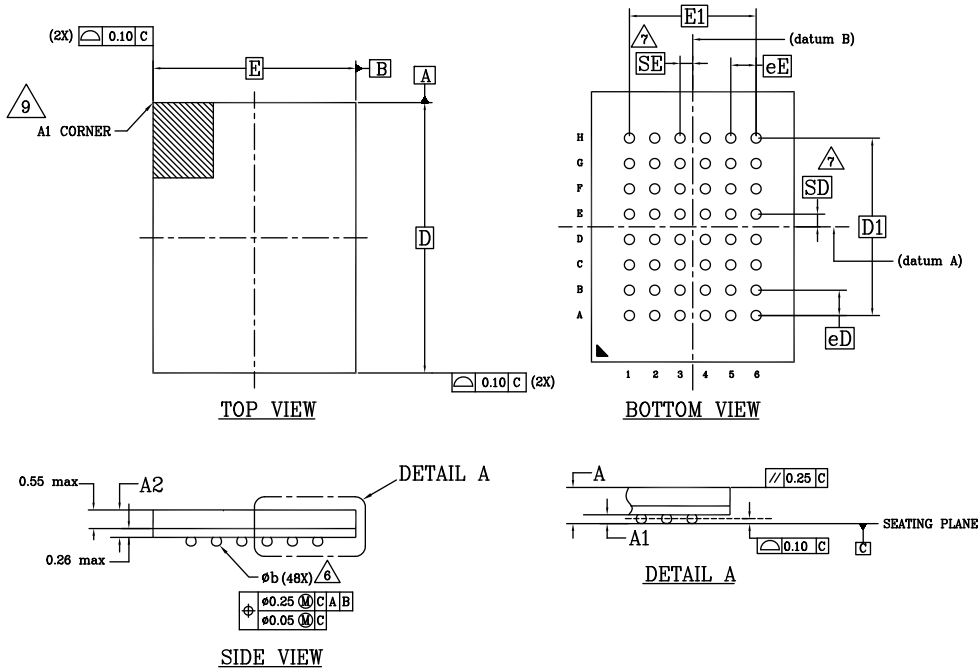
Note

45. The 'X' (Don't care) state for the chip enables refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

46. ERR is an Output pin. If not used, this pin should be left floating.

Package Diagrams

Figure 11. 48-ball VFBGA (6 × 8 × 1.0 mm) Package Outline, 51-85150



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1,00
A1	0,16	-	-
A2	-	-	0,81
D	8,00 BSC		
E	6,00 BSC		
D1	5,25 BSC		
E1	3,75 BSC		
MD	8		
ME	6		
n	48		
Ø b	0,25	0,30	0,35
eE	0,75 BSC		
eD	0,75 BSC		
SD	0,375 BSC		
SE	0,375 BSC		

NOTES:

- DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-2009.
- ALL DIMENSIONS ARE IN MILLIMETERS.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
- Ø b REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW
"SD" OR "SE" = 0.
WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW,
"SD" = eD/2 AND "SE" = eE/2.
- "*" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK METALIZED MARK, INDENTATION OR OTHER MEANS.

51-85150 *I

Acronyms

Acronym	Description
CE	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
OE	Output Enable
SRAM	Static Random Access Memory
VFBGA	Very Fine-Pitch Ball Grid Array
WE	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
μs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62168G30/CY62168GE30 MoBL, 16-Mbit (2M words × 8 bits) Static RAM with Error-Correcting Code (ECC) Document Number: 002-28440			
Rev.	ECN No.	Submission Date	Description of Change
**	6676291	09/23/2019	New data sheet.
*A	6834967	03/20/2020	Updated Product Portfolio : Updated Note 3. Updated DC Electrical Characteristics : Updated Note 11. Updated Data Retention Characteristics : Updated Note 20. Updated to new template.

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Code Examples](#) | [Projects](#) | [Video](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

© Cypress Semiconductor Corporation, 2019–2020. This document is the property of Cypress Semiconductor Corporation and its subsidiaries ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.