Sensitive Gate Silicon Controlled Rectifiers

Reverse Blocking Thyristors

2N5060 Series

Annular PNPN devices designed for high volume consumer applications such as relay and lamp drivers, small motor controls, gate drivers for larger thyristors, and sensing and detection circuits. Supplied in an inexpensive plastic TO−92/TO-226AA package which is readily adaptable for use in automatic insertion equipment.

Features

- Sensitive Gate Trigger Current − 200 μA Maximum
- Low Reverse and Forward Blocking Current − 50 μA Maximum, T_C = 110°C
- Low Holding Current − 5 mA Maximum
- Passivated Surface for Reliability and Uniformity
- These are Pb−Free Devices

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Peak Repetitive Off−State Voltage (Note 1) (T_J = −40 to 110°C, Sine Wave, 50 to 60 Hz, R_{GK} = 1 kΩ) 2N5060 2N5061 2N5062 2N5064	V_{DRM}, V_{RRM}	 30 60 100 200	V
On-State Current RMS (180° Conduction Angles; T_C = 80°C)	$I_{T(RMS)}$	0.8	A
*Average On-State Current (180° Conduction Angles) (T_C = 67°C) (T_C = 102°C)	$I_{T(AV)}$	 0.51 0.255	A
*Peak Non-repetitive Surge Current, T_A = 25°C (1/2 cycle, Sine Wave, 60 Hz)	I_{TSM}	10	A
Circuit Fusing Considerations (t = 8.3 ms)	I^2t	0.4	A^2s
*Average On-State Current (180° Conduction Angles) (T_C = 67°C) (T_C = 102°C)	$I_{T(AV)}$	 0.51 0.255	A
*Forward Peak Gate Power (Pulse Width ≤ 1.0 μsec; T_A = 25°C)	P_{GM}	0.1	W
*Forward Average Gate Power (T_A = 25°C, t = 8.3 ms)	$P_{G(AV)}$	0.01	W
*Forward Peak Gate Current (Pulse Width ≤ 1.0 μsec; T_A = 25°C)	I_{GM}	1.0	A
*Reverse Peak Gate Voltage (Pulse Width ≤ 1.0 μsec; T_A = 25°C)	V_{RGM}	5.0	V
*Operating Junction Temperature Range	T_J	−40 to +110	°C
*Storage Temperature Range	T_{stg}	−40 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

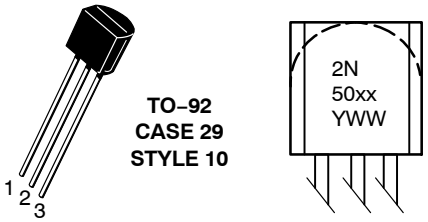
1. V_{DRM} and V_{RRM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

*Indicates JEDEC Registered Data.

SILICON CONTROLLED RECTIFIERS
0.8 A RMS, 30 − 200 V



MARKING DIAGRAM



TO−92
CASE 29
STYLE 10

50xx = Specific Device Code
Y = Year
WW = Work Week

PIN ASSIGNMENT	
1	Cathode
2	Gate
3	Anode

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

© Semiconductor Components Industries, LLC, 2011

Downloaded from Arrow.com.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
*Thermal Resistance, Junction−to−Case (Note 2)	$R_{\theta JC}$	75	°C/W
Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	200	°C/W

2. This measurement is made with the case mounted “flat side down” on a heatsink and held in position by means of a metal clamp over the curved surface.

*Indicates JEDEC Registered Data.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
*Peak Repetitive Forward or Reverse Blocking Current (Note 3)		I_{DRM}, I_{RRM}				
(V_{AK} = Rated V_{DRM} or V_{RRM})	T_C = 25°C		–	–	10	μA
	T_C = 110°C		–	–	50	μA
ON CHARACTERISTICS						
*Peak Forward On−State Voltage (Note 4)		V_{TM}	–	–	1.7	V
(I_{TM} = 1.2 A peak @ T_A = 25°C)						
Gate Trigger Current (Continuous DC) (Note 5)		I_{GT}				μA
*(V_{AK} = 7.0 Vdc, R_L = 100 Ω)	T_C = 25°C		–	–	200	
	T_C = −40°C		–	–	350	
Gate Trigger Voltage (Continuous DC) (Note 5)	T_C = 25°C	V_{GT}	–	–	0.8	V
*(V_{AK} = 7.0 Vdc, R_L = 100 Ω)	T_C = −40°C		–	–	1.2	
*Gate Non−Trigger Voltage		V_{GD}				V
(V_{AK} = Rated V_{DRM}, R_L = 100 Ω) T_C = 110°C			0.1	–	–	
Holding Current (Note 3)	T_C = 25°C	I_H	–	–	5.0	mA
*(V_{AK} = 7.0 Vdc, initiating current = 20 mA)	T_C = −40°C		–	–	10	
Turn-On Time						μs
Delay Time		t_d	–	3.0	–	
Rise Time		t_r	–	0.2	–	
(I_{GT} = 1.0 mA, V_D = Rated V_{DRM}, Forward Current = 1.0 A, di/dt = 6.0 A/μs						
Turn-Off Time		t_q				μs
(Forward Current = 1.0 A pulse, Pulse Width = 50 μs, 0.1% Duty Cycle, di/dt = 6.0 A/μs, dv/dt = 20 V/μs, I_{GT} = 1 mA)	2N5060, 2N5061		–	10	–	
	2N5062, 2N5064		–	30	–	
DYNAMIC CHARACTERISTICS						
Critical Rate of Rise of Off−State Voltage		dv/dt	–	30	–	V/μs
(Rated V_{DRM}, Exponential, R_{GK} = 1 kΩ)						

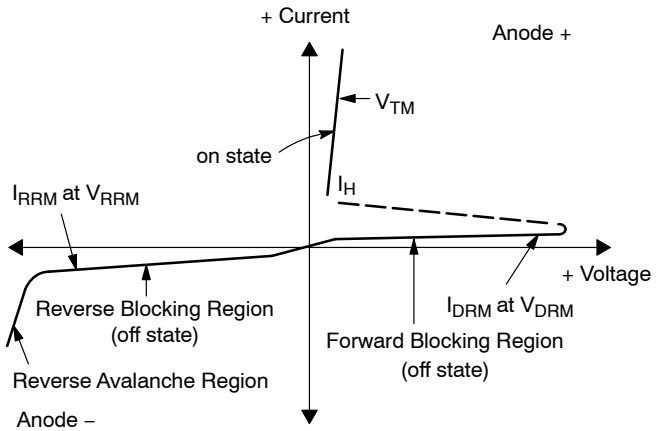
*Indicates JEDEC Registered Data.

3. R_{GK} = 1000 Ω is included in measurement.
4. Forward current applied for 1 ms maximum duration, duty cycle ≤ 1%.
5. R_{GK} current is not included in measurement.

Downloaded from Arrow.com.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Off State Forward Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Off State Reverse Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Peak on State Voltage
I_H	Holding Current



CURRENT DERATING

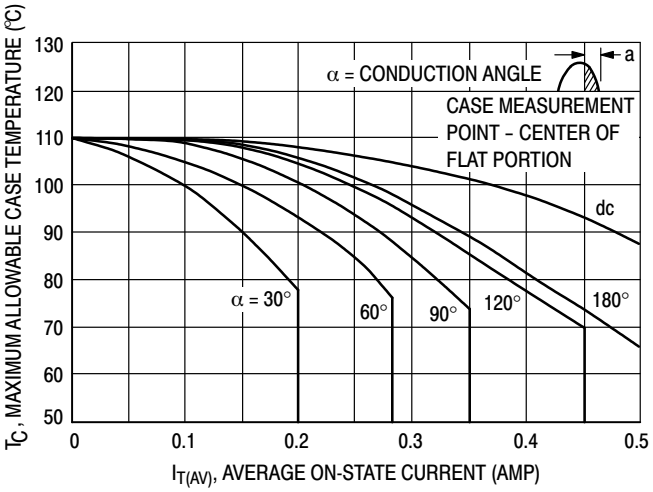


Figure 1. Maximum Case Temperature

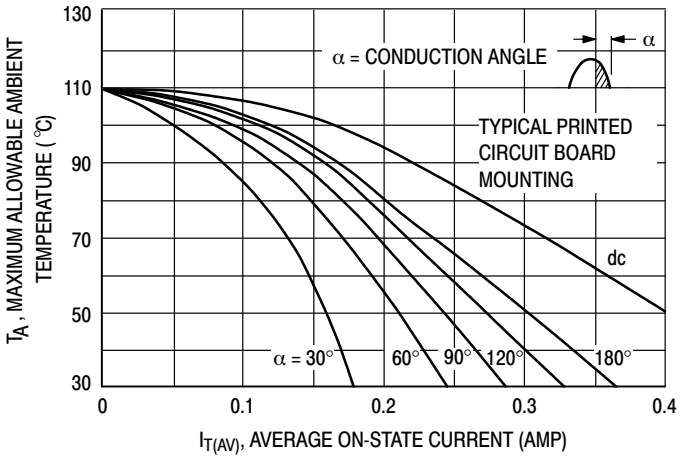


Figure 2. Maximum Ambient Temperature

Downloaded from Arrow.com.

CURRENT DERATING

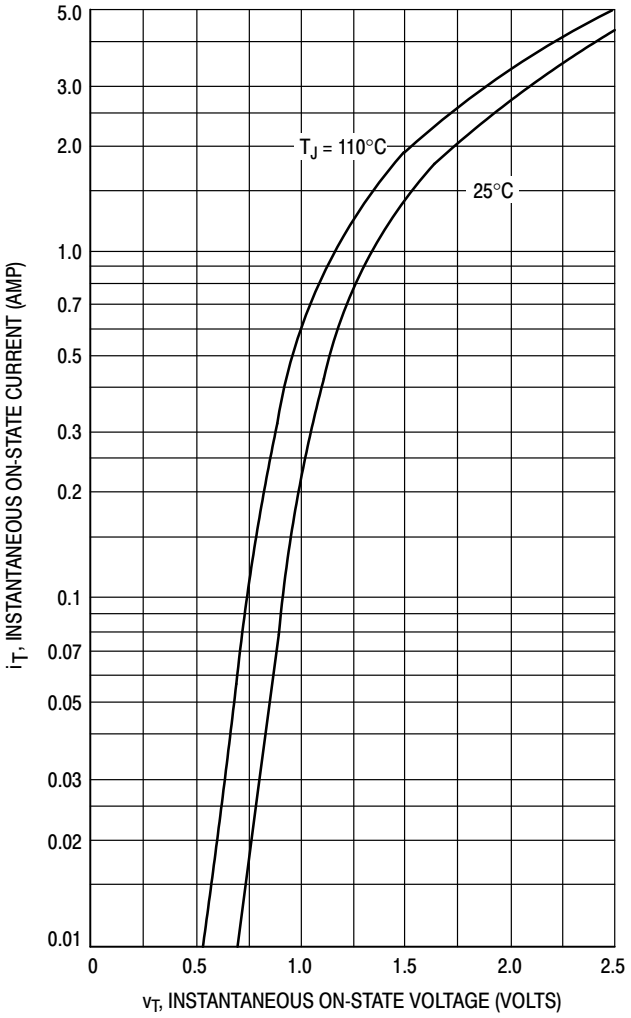


Figure 3. Typical Forward Voltage

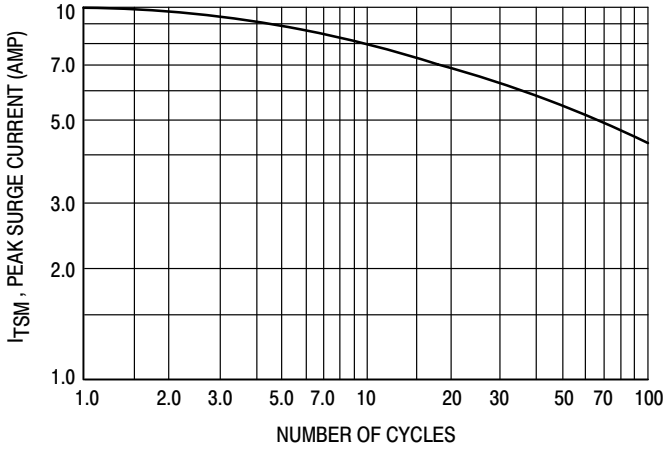


Figure 4. Maximum Non−Repetitive Surge Current

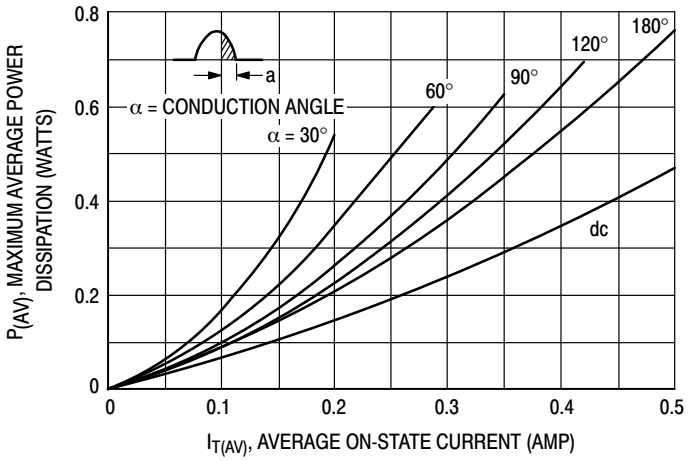


Figure 5. Power Dissipation

Downloaded from Arrow.com.

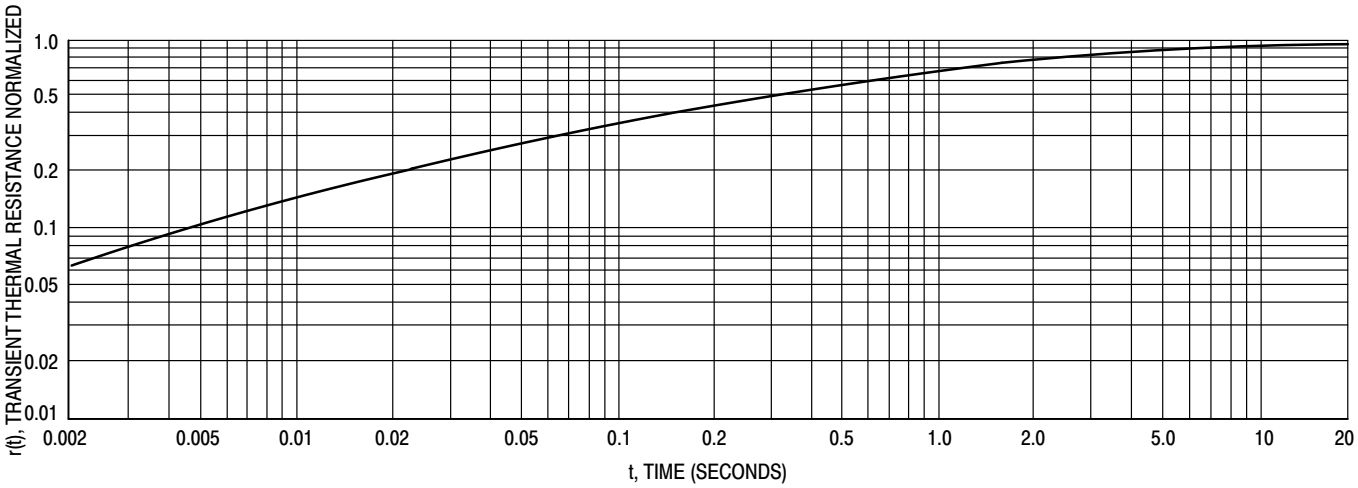


Figure 6. Thermal Response

TYPICAL CHARACTERISTICS

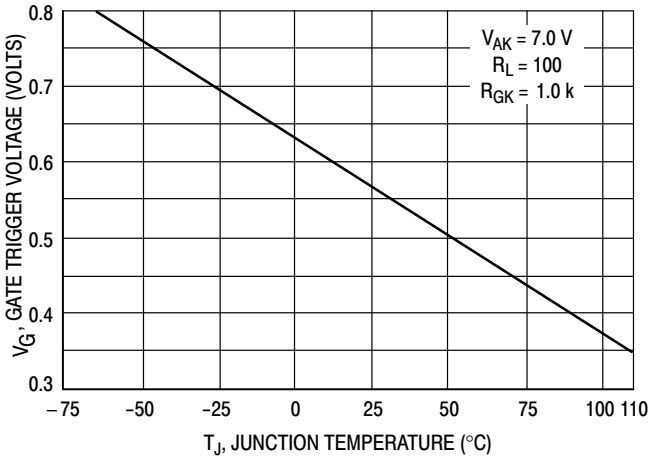


Figure 7. Typical Gate Trigger Voltage

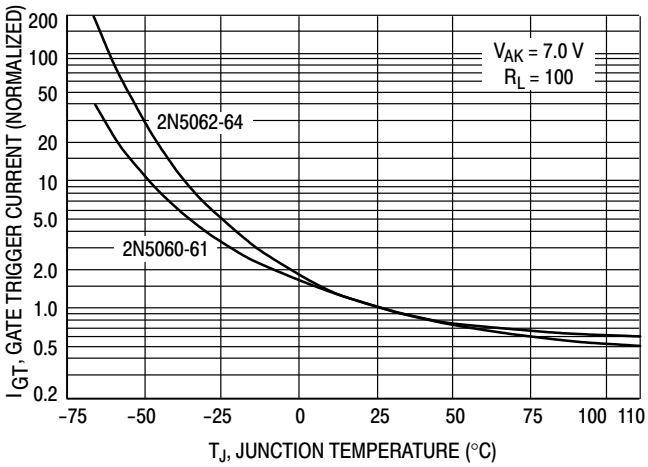


Figure 8. Typical Gate Trigger Current

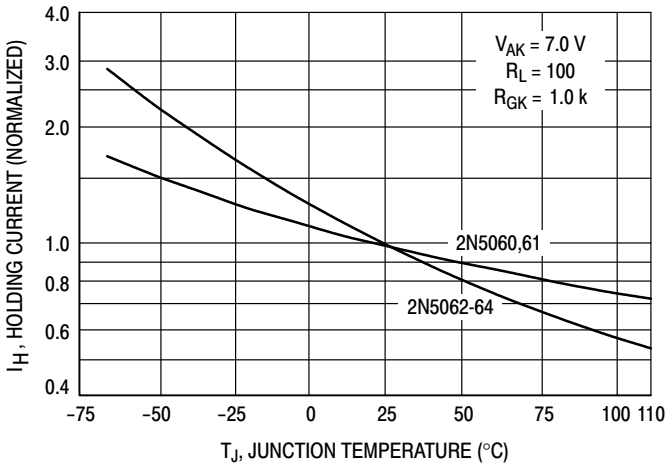


Figure 9. Typical Holding Current

Downloaded from Arrow.com.

ORDERING INFORMATION

Device	Package	Shipping†
2N5060G	TO−92 (Pb−Free)	5000 Units / Box
2N5060RLRA	TO−92	2000 / Tape & Reel
2N5060RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5060RLRMG	TO−92 (Pb−Free)	2000 / Ammo Pack
2N5061G	TO−92 (Pb−Free)	5000 Units / Box
2N5061RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5062G	TO−92 (Pb−Free)	5000 Units / Box
2N5062RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5064RLRMG	TO−92 (Pb−Free)	2000 / Ammo Pack
2N5064RLRAG	TO−92 (Pb−Free)	2000 / Tape & Reel
2N5064G	TO−92 (Pb−Free)	5000 Units / Box

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Downloaded from Arrow.com.

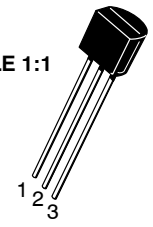
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

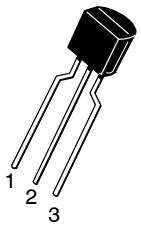
TO−92 (TO−226)
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

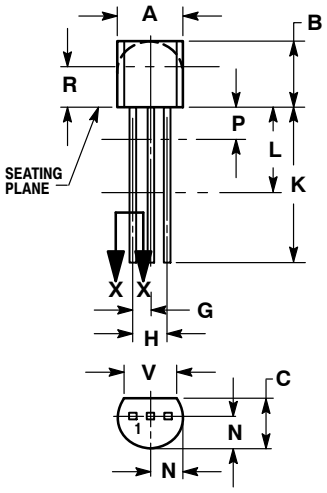
SCALE 1:1



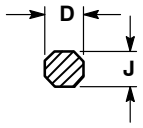
STRAIGHT LEAD
BULK PACK



BENT LEAD
TAPE & REEL
AMMO PACK



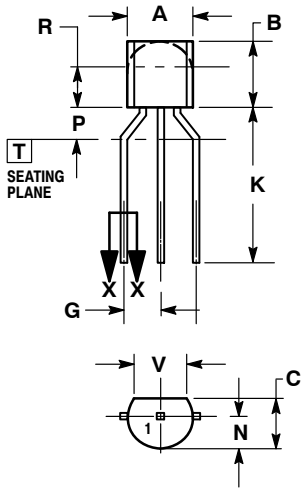
STRAIGHT LEAD
BULK PACK



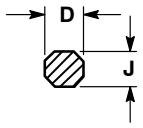
SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.175	0.205	4.45	5.20
B	0.170	0.210	4.32	5.33
C	0.125	0.165	3.18	4.19
D	0.016	0.021	0.407	0.533
G	0.045	0.055	1.15	1.39
H	0.095	0.105	2.42	2.66
J	0.015	0.020	0.39	0.50
K	0.500	---	12.70	---
L	0.250	---	6.35	---
N	0.080	0.105	2.04	2.66
P	---	0.100	---	2.54
R	0.115	---	2.93	---
V	0.135	---	3.43	---



BENT LEAD
TAPE & REEL
AMMO PACK



SECTION X−X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

	MILLIMETERS	
DIM	MIN	MAX
A	4.45	5.20
B	4.32	5.33
C	3.18	4.19
D	0.40	0.54
G	2.40	2.80
J	0.39	0.50
K	12.70	---
N	2.04	2.66
P	1.50	4.00
R	2.93	---
V	3.43	---

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42022B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
STATUS:	**ON SEMICONDUCTOR STANDARD**	
NEW STANDARD:		
DESCRIPTION:	**TO−92 (TO−226)**	**PAGE 1 OF 3**

Downloaded from Arrow.com.

TO−92 (TO−226)
CASE 29−11
ISSUE AM

DATE 09 MAR 2007

STYLE 1:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 6:
PIN 1. GATE
2. SOURCE & SUBSTRATE
3. DRAIN

STYLE 7:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 8:
PIN 1. DRAIN
2. GATE
3. SOURCE & SUBSTRATE

STYLE 9:
PIN 1. BASE 1
2. EMITTER
3. BASE 2

STYLE 10:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 11:
PIN 1. ANODE
2. CATHODE & ANODE
3. CATHODE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. GATE
3. MAIN TERMINAL 2

STYLE 13:
PIN 1. ANODE 1
2. GATE
3. CATHODE 2

STYLE 14:
PIN 1. EMITTER
2. COLLECTOR
3. BASE

STYLE 15:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2

STYLE 16:
PIN 1. ANODE
2. GATE
3. CATHODE

STYLE 17:
PIN 1. COLLECTOR
2. BASE
3. EMITTER

STYLE 18:
PIN 1. ANODE
2. CATHODE
3. NOT CONNECTED

STYLE 19:
PIN 1. GATE
2. ANODE
3. CATHODE

STYLE 20:
PIN 1. NOT CONNECTED
2. CATHODE
3. ANODE

STYLE 21:
PIN 1. COLLECTOR
2. EMITTER
3. BASE

STYLE 22:
PIN 1. SOURCE
2. GATE
3. DRAIN

STYLE 23:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 24:
PIN 1. EMITTER
2. COLLECTOR/ANODE
3. CATHODE

STYLE 25:
PIN 1. MT 1
2. GATE
3. MT 2

STYLE 26:
PIN 1. V_{CC}
2. GROUND 2
3. OUTPUT

STYLE 27:
PIN 1. MT
2. SUBSTRATE
3. MT

STYLE 28:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 29:
PIN 1. NOT CONNECTED
2. ANODE
3. CATHODE

STYLE 30:
PIN 1. DRAIN
2. GATE
3. SOURCE

STYLE 31:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 32:
PIN 1. BASE
2. COLLECTOR
3. EMITTER

STYLE 33:
PIN 1. RETURN
2. INPUT
3. OUTPUT

STYLE 34:
PIN 1. INPUT
2. GROUND
3. LOGIC

STYLE 35:
PIN 1. GATE
2. COLLECTOR
3. EMITTER

Downloaded from Arrow.com.

ISSUE	REVISION	DATE
AM	ADDED BENT−LEAD TAPE & REEL VERSION. REQ. BY J. SUPINA.	09 MAR 2007

ON Semiconductor and ON are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

Downloaded from Arrow.com.

onsemi, ONSEMI , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

◊

Downloaded from Arrow.com.