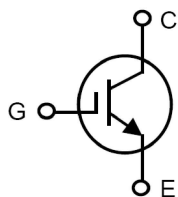


XPT™ 650V IGBTs GenX4™

IXXK160N65B4 IXXX160N65B4

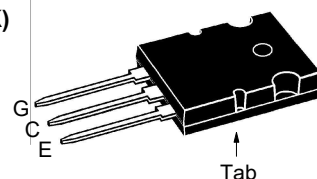
Extreme Light Punch Through
IGBT for 10-30kHz Switching



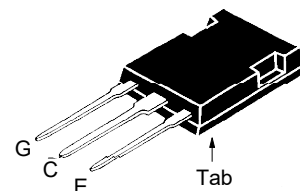
$$\begin{aligned} V_{CES} &= 650V \\ I_{C110} &= 160A \\ V_{CE(sat)} &\leq 1.80V \\ t_{fi(typ)} &= 90ns \end{aligned}$$

Symbol	Test Conditions	Maximum Ratings	
V_{CES}	$T_J = 25^\circ\text{C to } 175^\circ\text{C}$	650	V
V_{CGR}	$T_J = 25^\circ\text{C to } 175^\circ\text{C}, R_{GE} = 1M\Omega$	650	V
V_{GES}	Continuous	± 20	V
V_{GEM}	Transient	± 30	V
I_{C25}	$T_C = 25^\circ\text{C}$ (Chip Capability)	310	A
I_{LRMS}	Leads Current Limit	160	A
I_{C110}	$T_C = 110^\circ\text{C}$	160	A
I_{CM}	$T_C = 25^\circ\text{C}, 1\text{ms}$	860	A
SSOA (RBSOA)	$V_{GE} = 15V, T_{VJ} = 150^\circ\text{C}, R_G = 1\Omega$ Clamped Inductive Load	$I_{CM} = 320$ $@V_{CE} \leq V_{CES}$	A
t_{sc} (SCSOA)	$V_{GE} = 15V, V_{CE} = 360V, T_J = 150^\circ\text{C}$ $R_G = 10\Omega$, Non Repetitive	10	μs
P_C	$T_C = 25^\circ\text{C}$	940	W
T_J		-55 ... +175	$^\circ\text{C}$
T_{JM}		175	$^\circ\text{C}$
T_{stg}		-55 ... +175	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering 1.6 mm (0.062 in.) from Case for 10s	300	$^\circ\text{C}$
M_d	Mounting Torque (TO-264)	1.13/10	Nm/lb.in.
F_C	Mounting Force (PLUS247)	20..120 /4.5..27	N/lb.
Weight	TO-264	10	g
	PLUS247	6	g

TO-264
(IXXK)



PLUS247
(IXXX)



G = Gate E = Emitter
C = Collector Tab = Collector

Features

- Optimized for 10-30kHz Switching
- Square RBSOA
- Short Circuit Capability
- International Standard Packages
- High Current Handling Capability

Advantages

- High Power Density
- Low Gate Drive Requirement

Applications

- Power Inverters
- UPS
- Motor Drives
- SMPS
- PFC Circuits
- Battery Chargers
- Welding Machines
- Lamp Ballasts

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{CES}	$I_C = 250\mu\text{A}, V_{GE} = 0V$	650		V
$V_{GE(th)}$	$I_C = 250\mu\text{A}, V_{CE} = V_{GE}$	4.0		6.5 V
I_{CES}	$V_{CE} = V_{CES}, V_{GE} = 0V$ $T_J = 150^\circ\text{C}$			25 μA 1.5 mA
I_{GES}	$V_{CE} = 0V, V_{GE} = \pm 20V$			± 200 nA
$V_{CE(sat)}$	$I_C = 160A, V_{GE} = 15V$, Note 1 $T_J = 150^\circ\text{C}$		1.54 1.85	V V

Symbol Test Conditions

(T_J = 25°C Unless Otherwise Specified)

Characteristic Values

		Min.	Typ.	Max.
g_{fs}	I _C = 60A, V _{CE} = 10V, Note 1	40	70	S
C_{ies}	V _{CE} = 25V, V _{GE} = 0V, f = 1MHz		8220	pF
C_{oes}			500	pF
C_{res}			295	pF
Q_{g(on)}	I _C = 160A, V _{GE} = 15V, V _{CE} = 0.5 • V _{CES}		425	nC
Q_{ge}			82	nC
Q_{gc}			193	nC
t_{d(on)}	Inductive load, T _J = 25°C I _C = 80A, V _{GE} = 15V V _{CE} = 400V, R _G = 1Ω Note 2		52	ns
t_{ri}			64	ns
E_{on}			3.30	mJ
t_{d(off)}			220	ns
t_{fi}			90	ns
E_{off}			1.88	3.00 mJ
t_{d(on)}	Inductive load, T _J = 150°C I _C = 80A, V _{GE} = 15V V _{CE} = 400V, R _G = 1Ω Note 2		43	ns
t_{ri}			50	ns
E_{on}			4.30	mJ
t_{d(off)}			220	ns
t_{fi}			160	ns
E_{off}			2.36	mJ
R_{thJC}				0.16 °C/W
R_{thCS}		0.15		°C/W

Notes:

1. Pulse test, t ≤ 300μs, duty cycle, d ≤ 2%.
2. Switching times & energy losses may increase for higher V_{CE}(clamp), T_J or R_G.

Littelfuse reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered 4,835,592 4,931,844 5,049,961 5,237,481 6,162,665 6,404,065 B1 6,683,344 6,727,585 7,005,734 B2 7,157,338B2
by one or more of the following U.S. patents: 4,860,072 5,017,508 5,063,307 5,381,025 6,259,123 B1 6,534,343 6,710,405 B2 6,759,692 7,063,975 B2
4,881,106 5,034,796 5,187,117 5,486,715 6,306,728 B1 6,583,505 6,710,463 6,771,478 B2 7,071,537

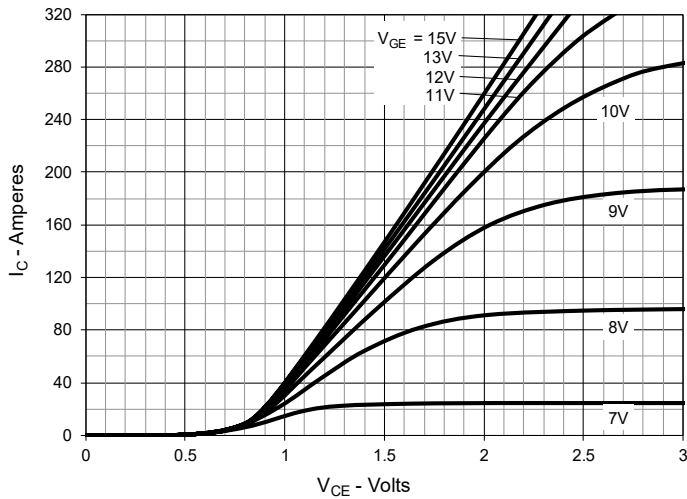
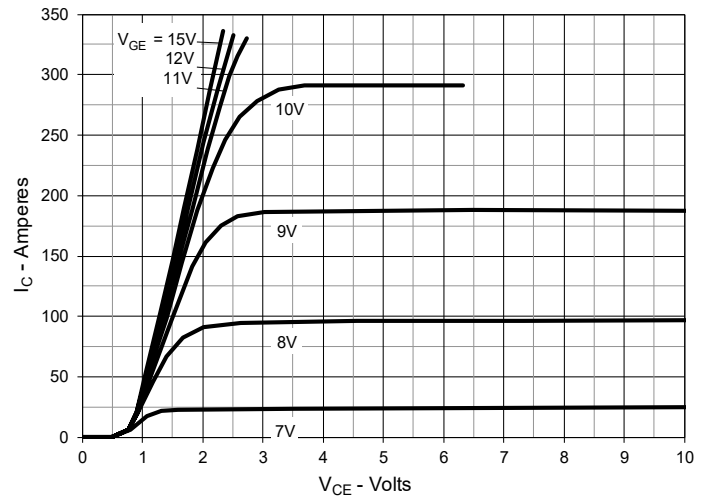
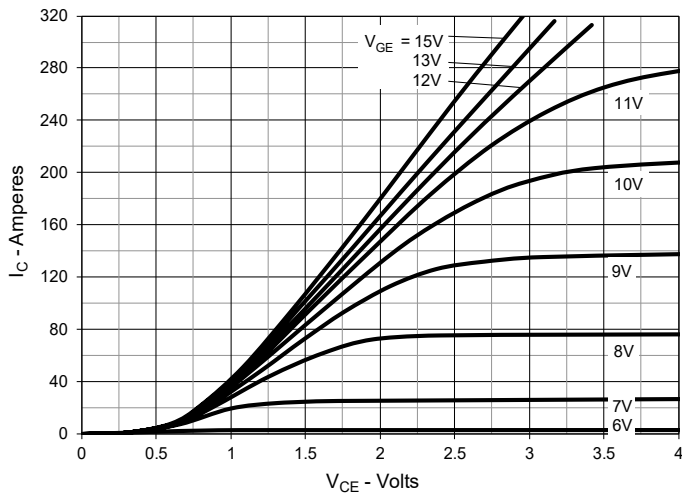
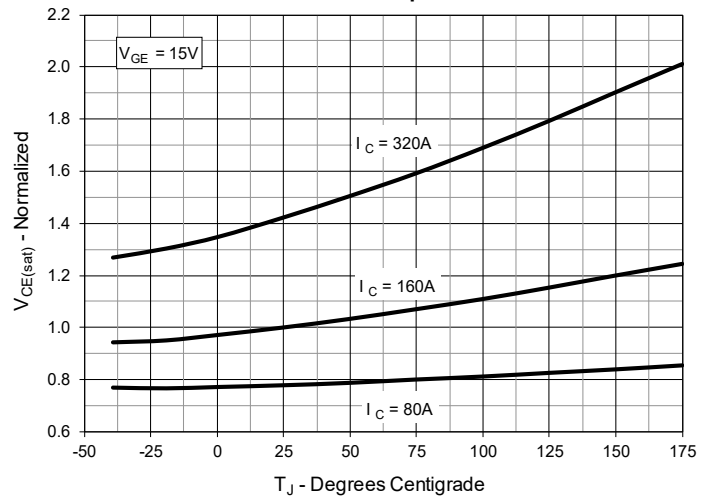
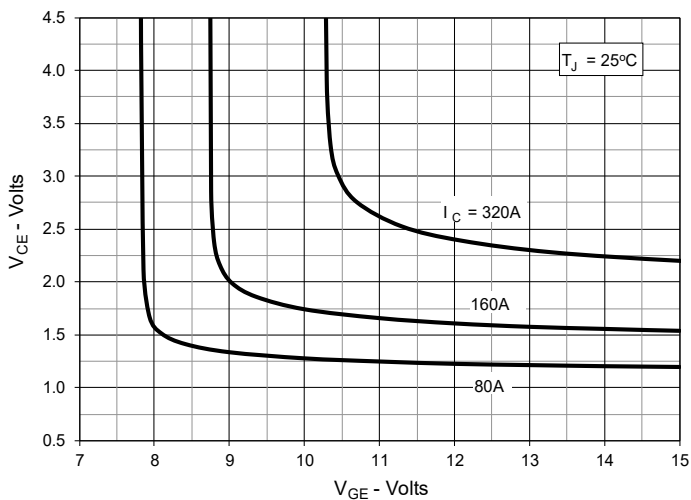
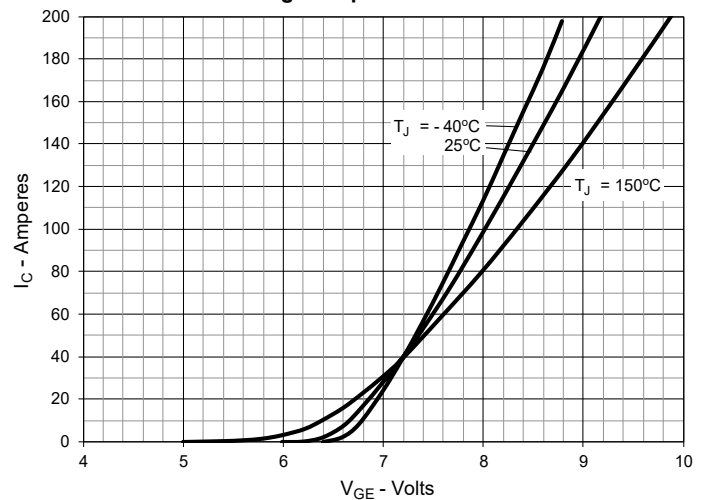
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 3. Output Characteristics @ $T_J = 150^\circ\text{C}$

Fig. 4. Dependence of $V_{CE(sat)}$ on Junction Temperature

Fig. 5. Collector-to-Emitter Voltage vs. Gate-to-Emitter Voltage

Fig. 6. Input Admittance


Fig. 7. Transconductance

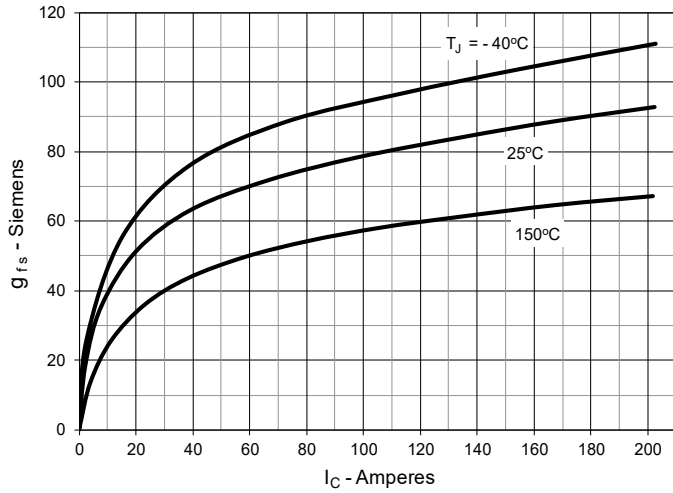


Fig. 8. Gate Charge

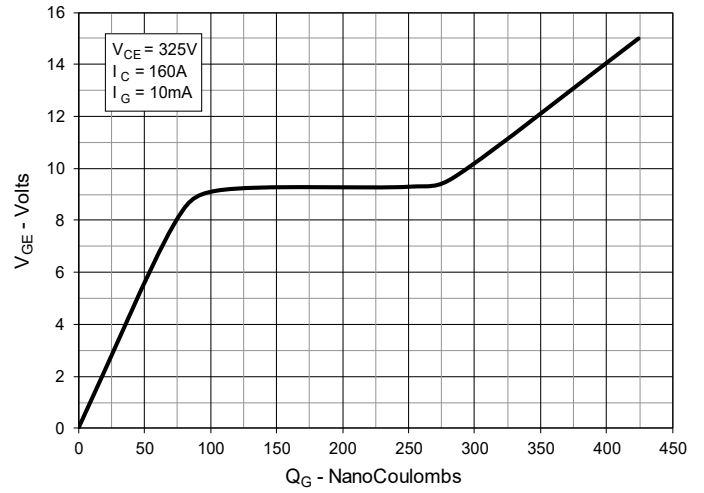


Fig. 9. Capacitance

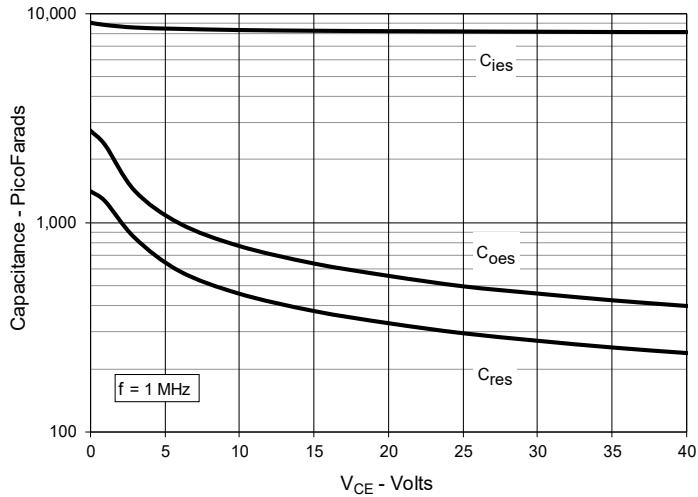


Fig. 10. Reverse-Bias Safe Operating Area

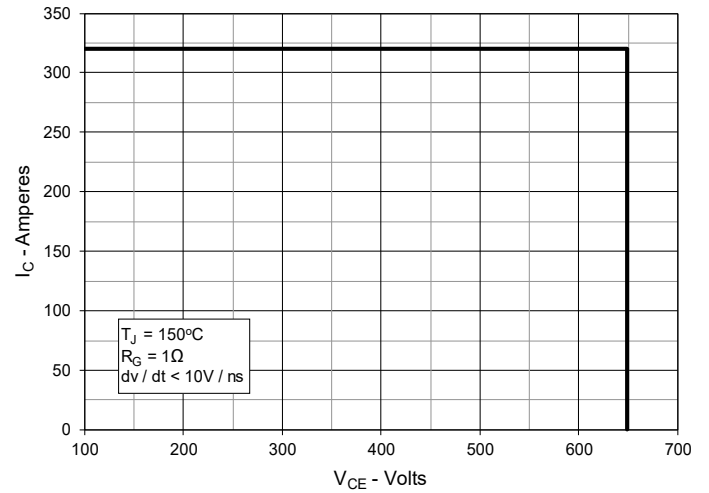


Fig. 11. Maximum Transient Thermal Impedance

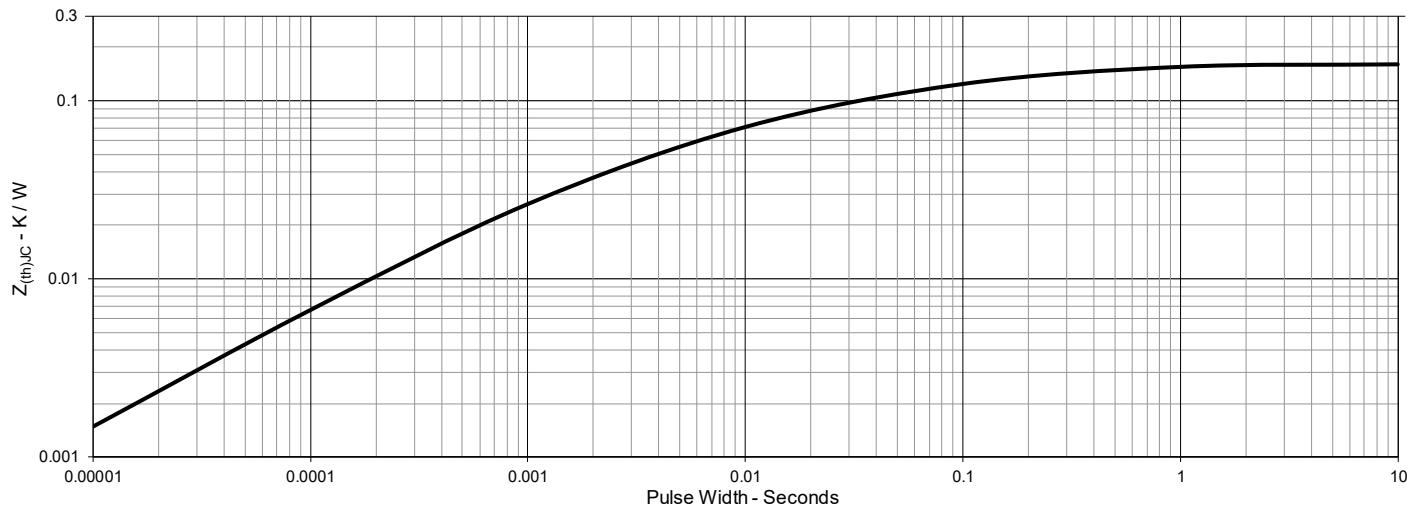


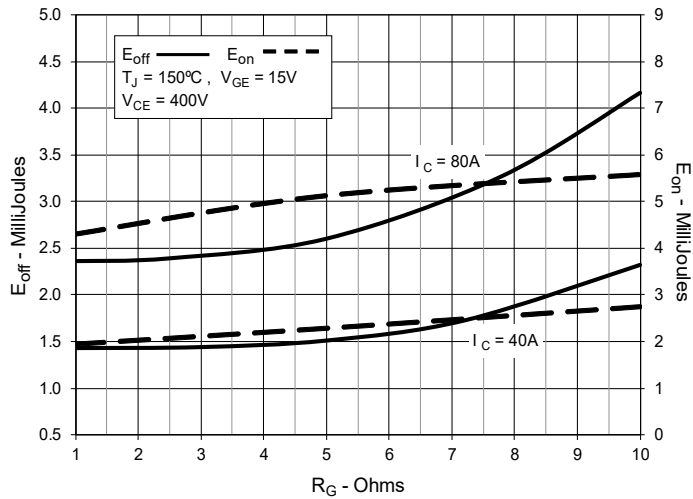
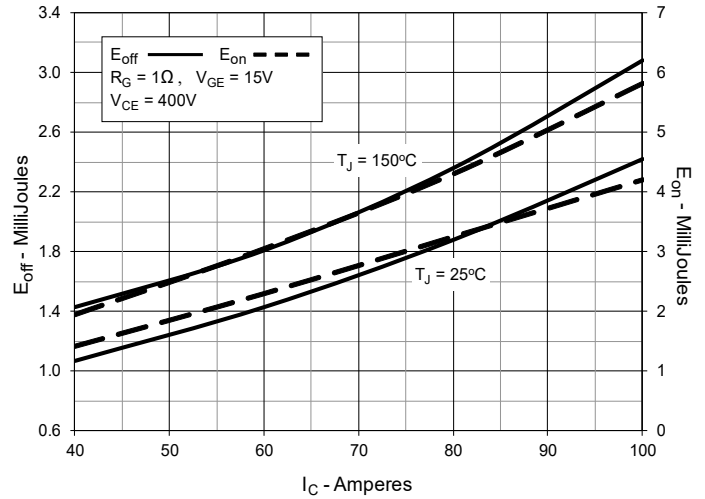
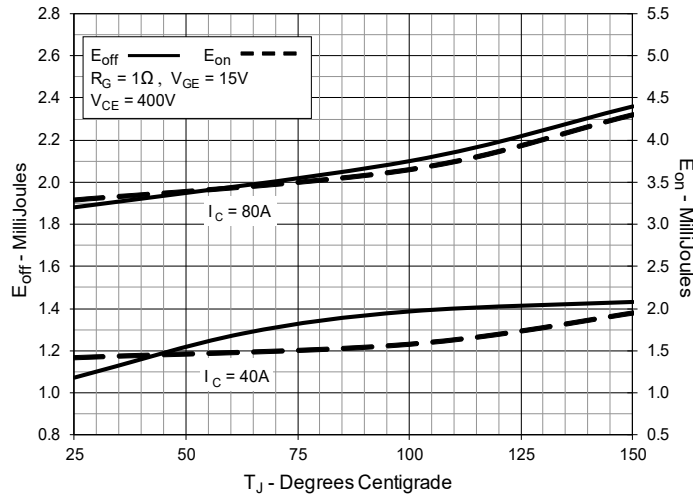
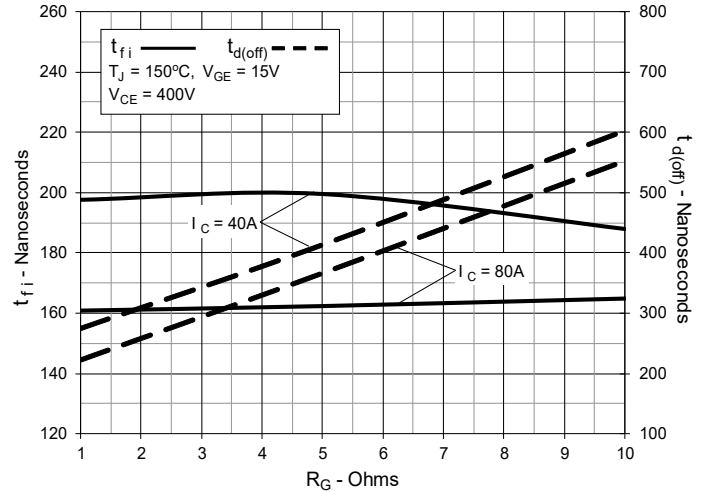
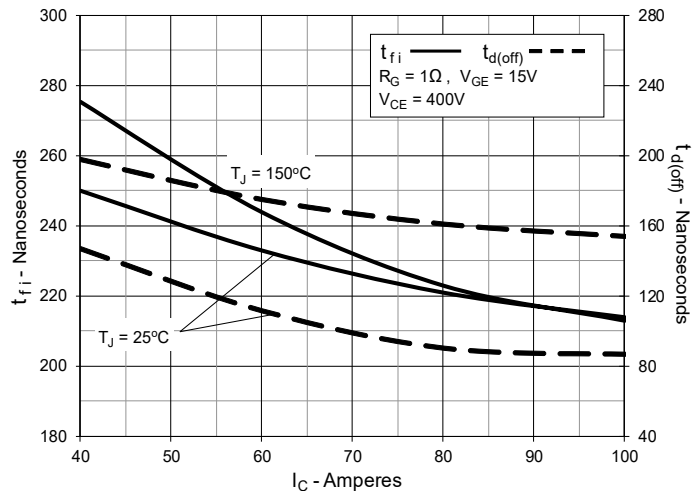
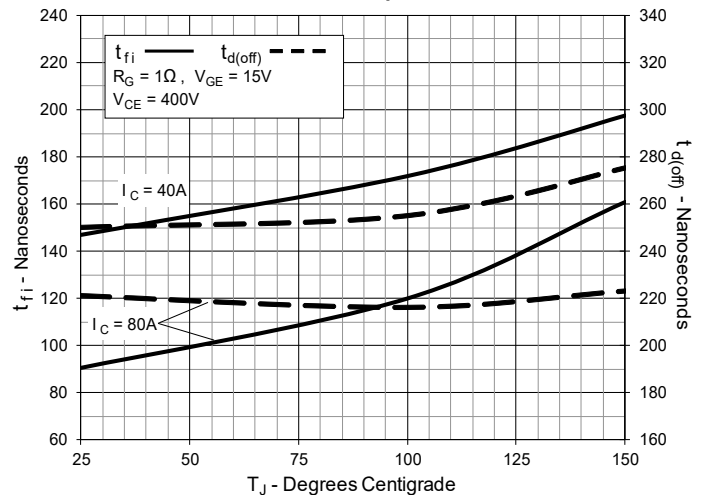
Fig. 12. Inductive Switching Energy Loss vs. Gate Resistance

Fig. 13. Inductive Switching Energy Loss vs. Collector Current

Fig. 14. Inductive Switching Energy Loss vs. Junction Temperature

Fig. 15. Inductive Turn-off Switching Times vs. Gate Resistance

Fig. 16. Inductive Turn-off Switching Times vs. Collector Current

Fig. 17. Inductive Turn-off Switching Times vs. Junction Temperature


Fig. 18. Inductive Turn-on Switching Times vs. Gate Resistance

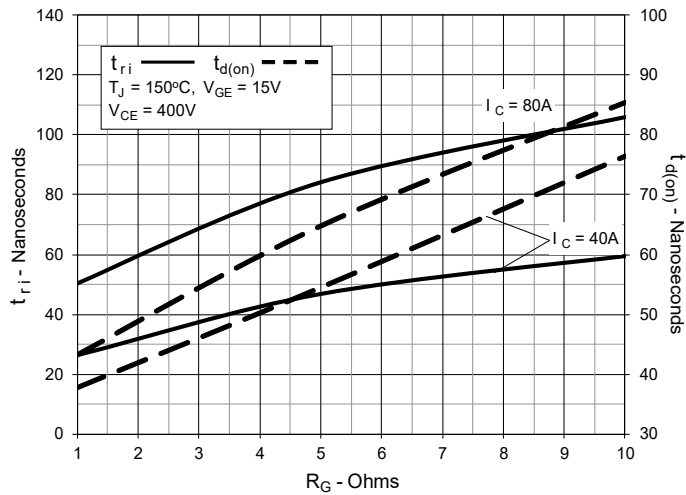


Fig. 19. Inductive Turn-on Switching Times vs. Collector Current

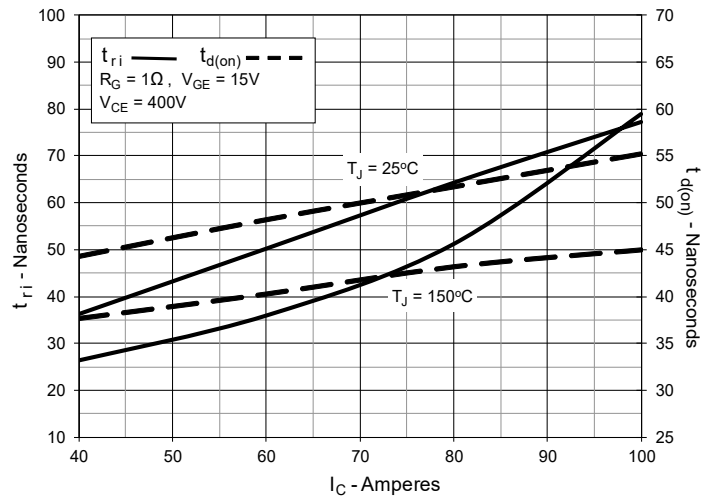
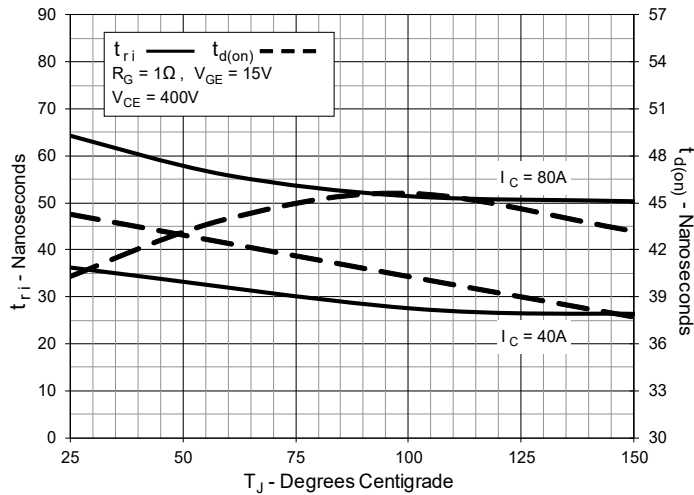
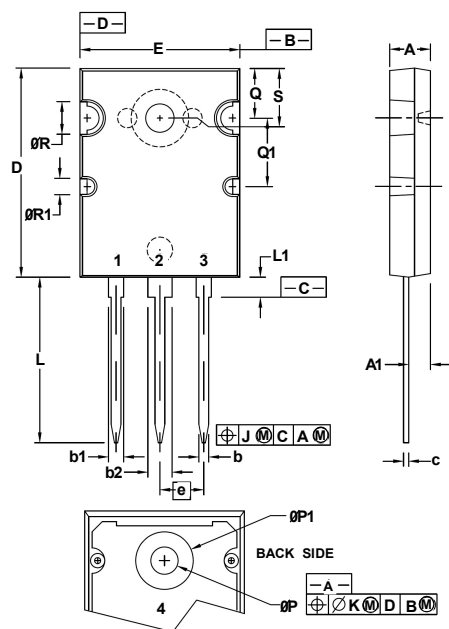
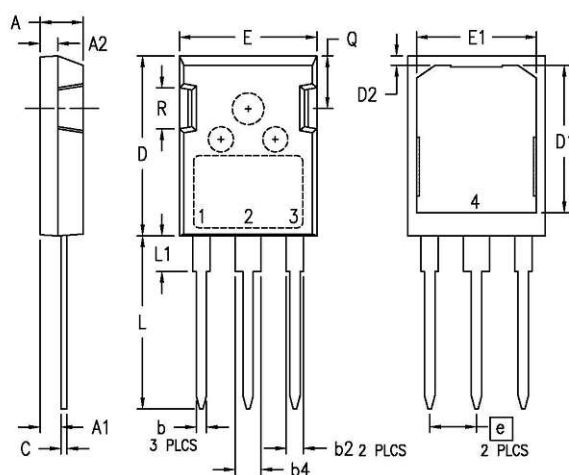


Fig. 20. Inductive Turn-on Switching Times vs. Junction Temperature



TO-264 Outline


SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215 BSC		5.46 BSC	
J	.000	.010	0.00	0.25
K	.000	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
øP	.122	.138	3.10	3.51
øP1	.270	.290	6.86	7.37
Q	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
øR	.155	.187	3.94	4.75
øR1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS247 Outline


SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.190	.205	4.83	5.21
A1	.090	.100	2.29	2.54
A2	.075	.085	1.91	2.16
b	.045	.055	1.14	1.40
b2	.075	.087	1.91	2.20
b4	.115	.126	2.92	3.20
C	.024	.031	0.61	0.80
D	.819	.840	20.80	21.34
D1	.650	.690	16.51	17.53
D2	.035	.050	0.89	1.27
E	.620	.635	15.75	16.13
E1	.520	.560	13.08	14.22
e	.215 BSC		5.45 BSC	
L	.780	.810	19.81	20.57
L1	.150	.170	3.81	4.32
Q	.220	.244	5.59	6.20
R	.170	.190	4.32	4.83

NOTE: 1. This drawing will meet all dimensions requirement of JEDEC outline TO-247 AD (R-PSIP-F3) except screw mounting hole.
 2. Pin #2 is connected to the bottom heatsink (#4).
 3. Lead finish - One of the following depending on the packaging plants.
 3.1 Matte pure tin plating on the leads and back heatsink.
 3.2 Pb free solder dip on the leads and pre Ni plated back heatsink.

