

TMPN3150B1AFG

Neuron[®] Chip for Distributed Intelligent Control Networks (LONWORKS[®])

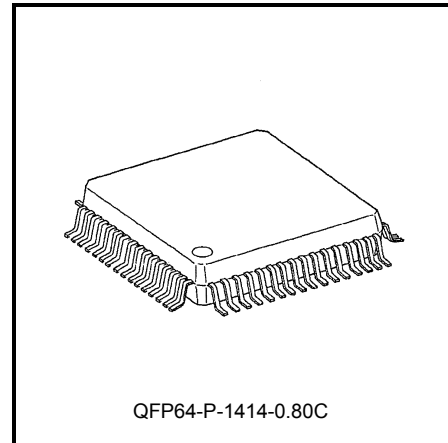
The TMPN3150B1AFG is a Neuron Chip that configures LONWORKS nodes in combination with external memory.

Neuron Chips have all the built-in communications and control functions required to implement LONWORKS nodes. These nodes may then be easily integrated into highly reliable distributed intelligent control networks.

The typical functions for this chip are described below.

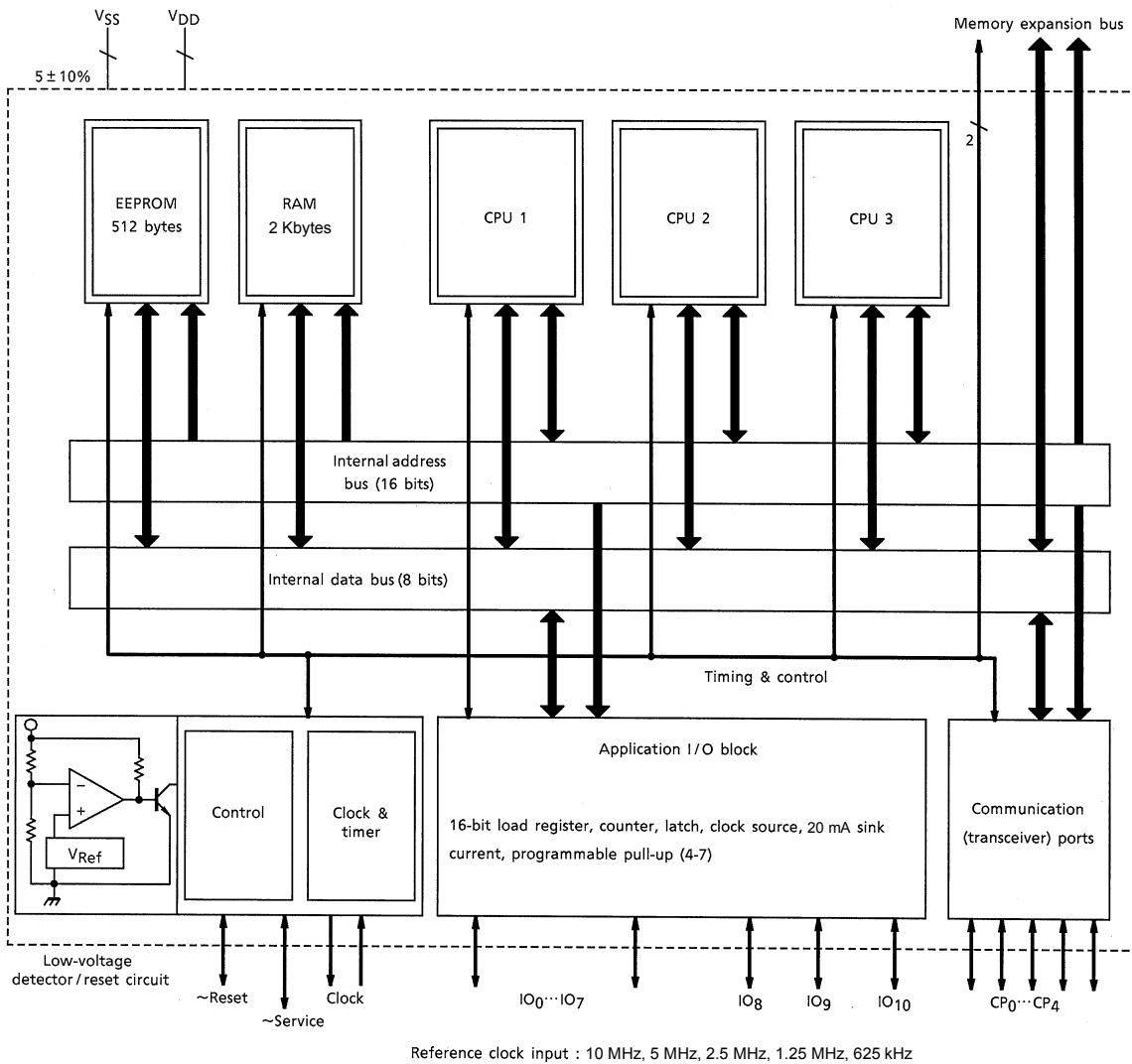
Features

- I/O functions
 - Eleven programmable I/O pins
 - Two programmable 16-bit timers and counters built in
 - Thirty-four different types of I/O functions to handle a wide range of input and output
 - ROM firmware image containing preprogrammed I/O drivers, greatly simplifying application programs.
(Stored in external ROM)
- Network functions
 - Two CPUs for communication protocol processing built in
The communications and application CPUs execute in parallel.
 - Built-in LonTalk protocol supporting all seven levels of the ISO OSI reference model
 - A highly reliable communication protocol is supplied as firmware.
 - Built-in twisted-pair wire transceiver
 - Communications modes and communication speeds supporting various types of external transceivers.
Supports twisted-pair wire, power line, radio (RF), infrared, coaxial-cable and fiber optic types.
 - Communication port transceiver modes and logical addresses stored within the EEPROM
Can be amended via the network.
- Other functions
 - Application programs are also stored within the EEPROM.
Can be updated by downloading over the network. The EEPROM can be added to externally.
 - Built-in watchdog timer
 - Each chip has a unique ID number
Effective during the logical installation of networks
 - Low electrical consumption mode supported through a sleep mode
 - Built-in low-voltage detection circuit
Prevents incorrect operations and writing errors in the EEPROM during drops in power voltage.
 - The package is QFP64-P-1414-0.80C (Lead-Free Type (Pd Preplated Frame)).



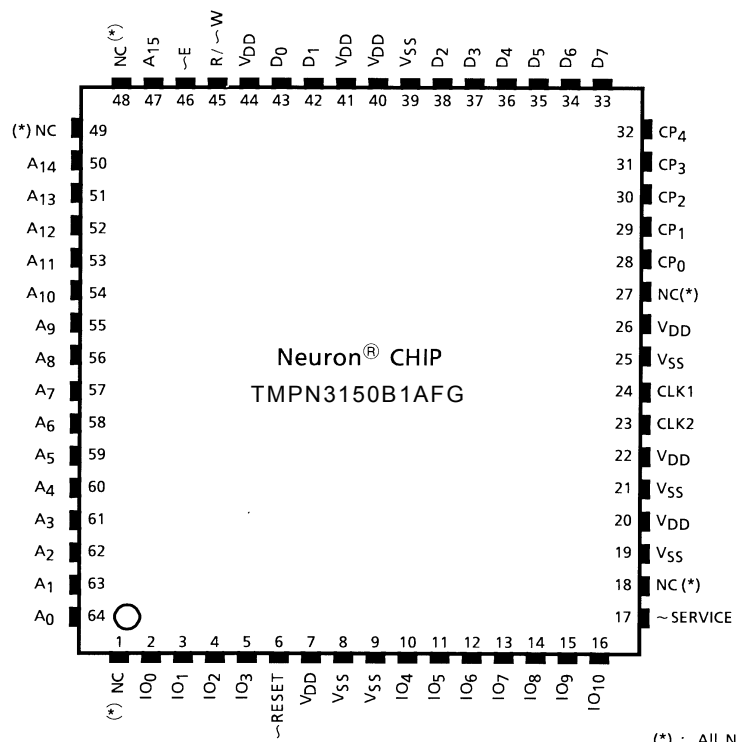
Weight: 1.0 g (typ.)

Block Diagram



Item	TMPN3150B1AFG
CPU	8-bit CPU × 3
RAM	2,048 bytes
ROM	—
EEPROM	512 bytes
16-bit Timer/Counter	2 channels
External Memory Interface	Available
Package	64-pin SOP

Pin Connections



(*) : All NC pins should be open.

Pin Functions

Pin No.	Pin Name	I/O	Pin Function
24	CLK1	Input	Oscillator connection, or external clock input
23	CLK2	Output	Oscillator connection. Leave open when external clock is input to CLK1.
6	~RESET	I/O (built-in pull-up)	Reset pin (active low)
17	~SERVICE	I/O (built-in configurable pull-up)	Service pin. Indicator output during operation.
2 to 5	IO ₀ to IO ₃	I/O	Large current sink capacity (20 mA). General I/O port.
10 to 13	IO ₄ to IO ₇	I/O (built-in configurable pull-up)	General I/O port. One of IO ₄ to IO ₇ can be specified as the No.1 timer/counter input. The output signal can be output to IO ₀ . IO ₄ can be used as the No.2 timer/counter input with IO ₁ as output.
14 to 16	IO ₈ to IO ₁₀	I/O	General I/O port. Can be used for serial communication with other devices.
43, 42, 38 to 33	D ₀ , D ₁ , D ₂ to D ₇	I/O	Data bus for memory expansion
45	R / ~W	Output	Output port for controlling read/write for memory expansion
46	~E	Output	Output port for controlling memory expansion
47, 50 to 64	A ₁₅ , A ₁₄ to A ₀	Output	Address output port for memory expansion
7, 20, 22, 26, 40, 41, 44	V _{DD}	Input	Power input (5.0 V typ.)
8, 9, 19, 21, 25, 39	V _{SS}	Input	Power input (0 V GND)
1, 18, 27, 48, 49	NC	—	Do not connect anything. Leave pins open.
28 to 32	CP ₀ to CP ₄	I/O	Bidirectional port for communications. Supports several communications protocols through specifying of mode.

- * :
- The ~SERVICE and IO₄ to IO₇ terminals are programmable pull-ups.
 - All V_{DD} terminals must be externally connected.
 - All V_{SS} terminals must be externally connected.

Maximum Ratings (V_{SS} = 0 V, V_{SS} typ.)

Item	Symbol	Rating	Unit
Power supply voltage	V _{DD}	-0.3 to 7.0	V
Input voltage	V _{IN}	-0.3 to V _{DD} +0.3	V
Power dissipation	PD	800	mW
Storage temperature	T _{stg}	-65 to 150	°C

Operating Conditions

Item	Symbol	Min	Typ.	Max	Unit
Operating voltage	V _{DD}	4.5	5.0	5.5	V
Input voltage (TTL)	V _{IH(1)}	2.0	—	V _{DD}	V
	V _{IL(1)}	V _{SS}	—	0.8	V
Input voltage (CMOS)	V _{IH(2)}	V _{DD} - 0.8	—	V _{DD}	V
	V _{IL(2)}	V _{SS}	—	0.8	V
Operating frequency	f _{osc}	0.625	—	10	MHz
Operating temperature	T _{opr}	-40	—	85	°C

Electrical Characteristics**DC characteristic (V_{DD} = 5.0 V ± 10%, V_{SS} = 0 V, Ta = -40 to 85°C)****(The above operating conditions apply unless otherwise stated.)**

Item	Symbol	Pins	Test Condition		Min	Max	Unit
LOW output voltage (1)	V _{OL} (1)	IO ₀ to IO ₃	I _{OL} = 20 mA		0	0.8	V
			I _{OL} = 10 mA		0	0.4	V
LOW output voltage (2)	V _{OL} (2)	~SERVICE	Duty cycle = 50%	I _{OL} = 20 mA	0	0.8	V
				I _{OL} = 10 mA	0	0.4	V
LOW output voltage (3)	V _{OL} (3)	CP ₂ , CP ₃	I _{OL} = 40 mA		0	1.0	V
LOW output voltage (4)	V _{OL} (4)	Others (Note 1)	I _{OL} = 1.4 mA		0	0.4	V
HIGH output voltage (1)	V _{OH} (1)	IO ₀ to IO ₃	I _{OH} = -1.4 mA		V _{DD} -0.4	V _{DD}	V
HIGH output voltage (2)	V _{OH} (2)	~SERVICE	I _{OH} = -1.4 mA		V _{DD} -0.4	V _{DD}	V
HIGH output voltage (3)	V _{OH} (3)	CP ₂ , CP ₃	I _{OH} = -40 mA		V _{DD} -1.0	V _{DD}	V
HIGH output voltage (4)	V _{OH} (4)	Others (Note 1)	I _{OH} = -1.4 mA		V _{DD} -0.4	V _{DD}	V
Input current	I _{IN}	(Note 2)	V _{IN} = V _{SS} to V _{DD}		-10	+10	μA
Pull-up current	I _{PU}	IO ₄ to IO ₇ ~SERVICE, ~RESET (Note 3)	V _{IN} = 0 V		-30	-300	μA
Low-voltage detection level	V _{LVD}	V _{DD}	—		3.8	4.5	V

Note 1: Output voltage characteristics exclude the ~RESET pin and CLK2 pin.

Note 2: Excludes pull-up input pins.

Note 3: The IO₄ to IO₇ and ~SERVICE pins have programmable pull-ups. ~RESET has a fixed pull-up.

Item		Symbol	Typ.	Max	Unit
Operating mode current consumption	10 MHz clock	$I_{DD} (OP)$	18	30	mA
	5 MHz clock		10	15	
	2.5 MHz clock		5	8	
	1.25 MHz clock		2.5	5	
	0.625 MHz clock		1.5	3	
Sleep mode current consumption		$I_{DD} (SLP)$	18	100	μA

Note: Test conditions for current dissipation

$V_{DD} = 5\text{ V}$; all output = under no load; all input $\leq 0.2\text{ V}$ or $\geq (V_{DD} - 0.2\text{ V})$; programmable pull-up = off; crystal oscillator clock input; differential receiver disabled.

The current value (typ.) is the typical value when $T_a = 25^\circ\text{C}$.

The current value (max) applies to the rated temperature range at $V_{DD} = 5.5\text{ V}$.

200 μA (typ.) to 600 μA (max) is added to the current of the differential receiver when the receiver is enabled.

The differential receiver is enabled by either of the following conditions:

- when the Neuron chip is in Run mode and the communication ports are in Differential mode;
- when the Neuron chip is in Sleep mode, the communication ports are in Differential mode, and the Comm Port Wakeup is not masked.

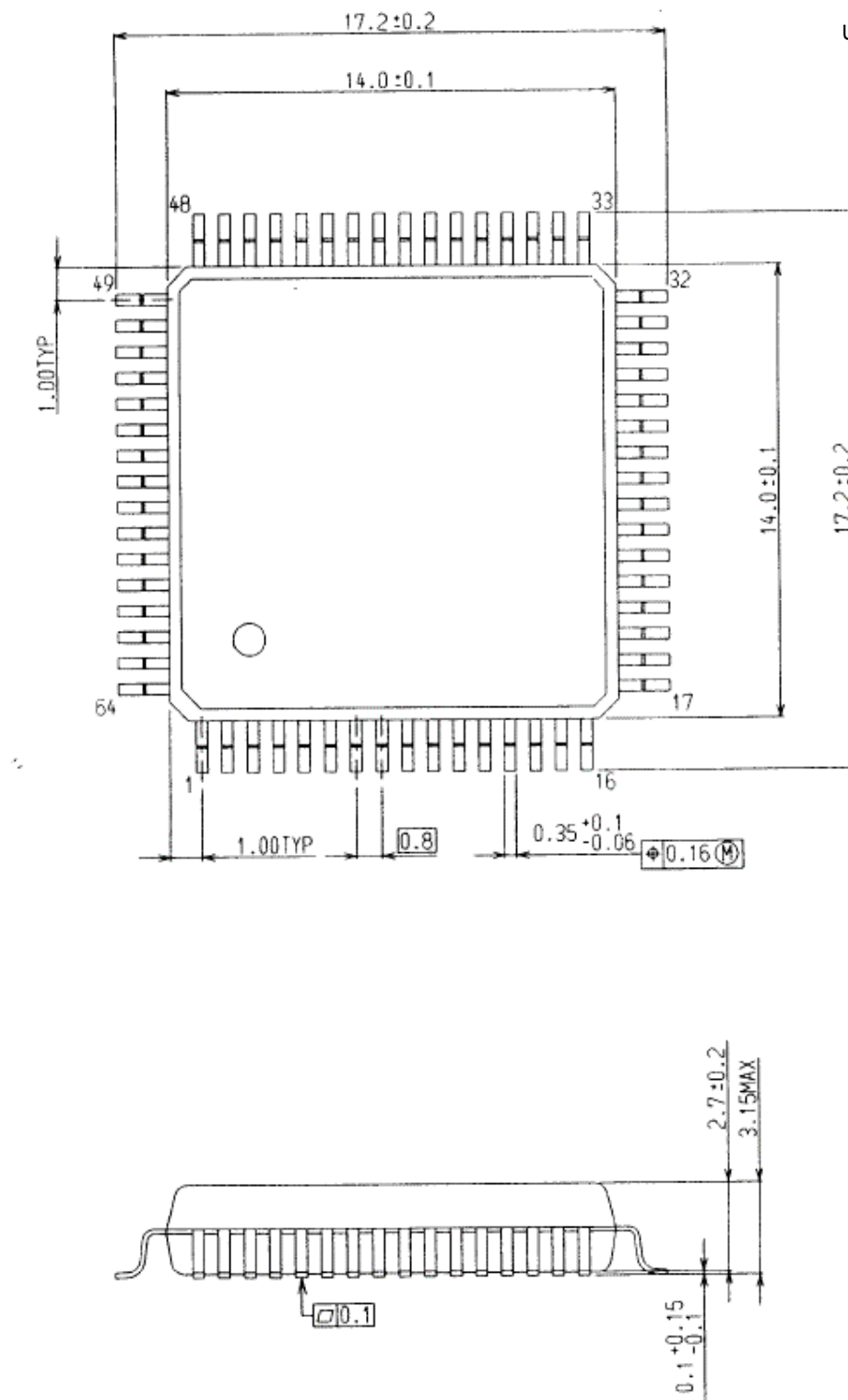
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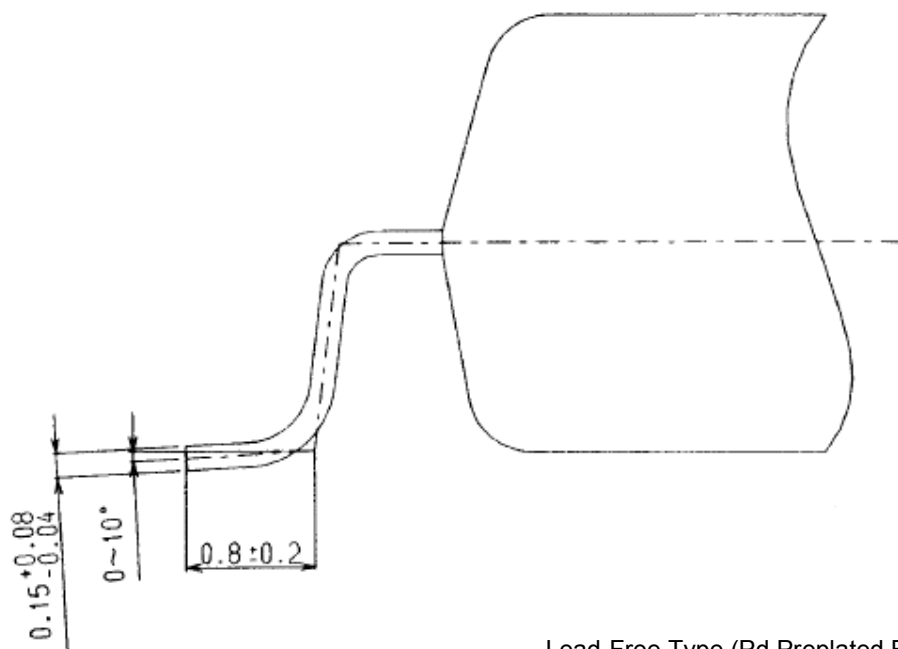
Package Dimensions

QFP64-P-1414-0.80C

UNIT: mm



UNIT: mm



About solderability, following conditions were confirmed

- Solderability
 - (1) Use of Sn-37Pb solder Bath
 - solder bath temperature = 230°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux
 - (2) Use of Sn-3.0Ag-0.5Cu solder Bath
 - solder bath temperature = 245°C
 - dipping time = 5 seconds
 - the number of times = once
 - use of R-type flux

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