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August 2014

FDMA291P

Single P-Channel 1.8V Specified PowerTrench® MOSFET

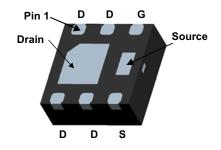
General Description

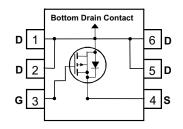
This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance.

The MicroFET 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- -6.6 A, -20V. $r_{DS(ON)} = 42 \text{ m}\Omega$ @ $V_{GS} = -4.5V$ $r_{DS(ON)} = 58 \text{ m}\Omega$ @ $V_{GS} = -2.5V$ $r_{DS(ON)} = 98 \text{ m}\Omega$ @ $V_{GS} = -1.8V$
- Low profile 0.8 mm maximum in the new package MicroFET 2x2 mm
- Free from halogenated compounds and antimony oxides
- RoHS Compliant





MicroFET 2x2

Absolute Maximum Ratings T_A=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V _{DS}	Drain-Source Voltage		-20	V
V _{GS}	Gate-Source Voltage		±8	V
1	Drain Current - Continuous	(Note 1a)	-6.6	A
I _D	– Pulsed		-24	
D	Power Dissipation for Single Operation	(Note 1a)	2.4	W
P_D		(Note 1b)	0.9	
T _J , T _{STG}	Operating and Storage Junction Temperature Range		-55 to +150	°C

Thermal Characteristics

R _{⊕JC}	Thermal Resistance, Junction-to-Case		13	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (N	Note 1a)	52	°C/W
R _{0JA}	Thermal Resistance, Junction-to-Ambient (N	Note 1b)	145	

Package Marking and Ordering Information

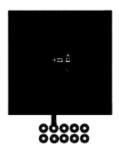
Device Marking	Device	Reel Size	Tape width	Quantity
291 FDMA291P		7"	8mm	3000 units

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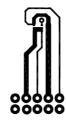
Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics		1		ı	
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, \qquad I_{D} = -250 \mu\text{A}$	-20			V
ΔBV _{DSS} ΔΤ _J	Breakdown Voltage Temperature Coefficient	I_D = -250 μ A, Referenced to 25°C		-12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μΑ
I _{GSS}	Gate-Body Leakage	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA
On Char	acteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \ \mu A$	-0.4	-0.7	-1.0	V
$\Delta V_{GS(th)} \over \Delta T_{J}$	Gate Threshold Voltage Temperature Coefficient	I_D = -250 μ A, Referenced to 25°C		3		mV/°C
r _{DS(on)}	Static Drain–Source On–Resistance	$\begin{split} V_{GS} = -4.5 \ V, & I_D = -6.6 \ A \\ V_{GS} = -2.5 \ V, & I_D = -5.1 \ A \\ V_{GS} = -1.8 \ V, & I_D = -3.9 \ A \\ V_{GS} = -4.5 \ V, I_D = -6.6 \ A, \ T_J = 125 ^{\circ} C \end{split}$		36 51 79 49	42 58 98 64	mΩ
g _{FS}	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -6.6 \text{ A}$		16		S
Dynamic	Characteristics				•	•
C _{iss}	Input Capacitance	$V_{DS} = -10 \text{ V}, V_{GS} = 0 \text{ V},$		1000		pF
C _{oss}	Output Capacitance	f = 1.0 MHz		190		pF
C _{rss}	Reverse Transfer Capacitance]		100		pF
Switchin	g Characteristics (Note 2)					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = -10 \text{ V}, I_{D} = -1 \text{ A},$		13	23	ns
t _r	Turn-On Rise Time	$V_{GS} = -4.5 \text{ V}, R_{GEN} = 6 \Omega$		9	18	ns
$t_{d(off)}$	Turn-Off Delay Time]		42	68	ns
t _f	Turn-Off Fall Time]		25	40	ns
Q_g	Total Gate Charge	$V_{DS} = -10 \text{ V}, I_{D} = -6.6 \text{ A},$		10	14	nC
$\overline{Q_gs}$	Gate-Source Charge	$V_{GS} = -4.5 \text{ V}$		2		nC
Q_{gd}	Gate-Drain Charge	1		3		nC
Drain–So	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source	•			-2	Α
V _{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = -2 \text{ A}$ (Note 2)		-0.8	-1.2	V
t _{rr}	Diode Reverse Recovery Time	I _F = -6.6 A,		20		ns
Q _{rr}	Diode Reverse Recovery Charge	dI _F /dt = 100 A/μs		8		nC

Notes

^{1.} R_{0JA} is determined with the device mounted on a 1 in² oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0JC} is guaranteed by design while R_{0JA} is determined by the user's board design.



a. 52 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 145 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μ s, Duty Cycle < 2.0%

Typical Characteristics

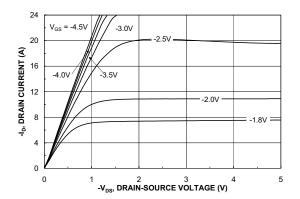


Figure 1. On-Region Characteristics.

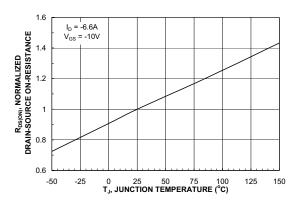


Figure 3. On-Resistance Variation with Temperature.

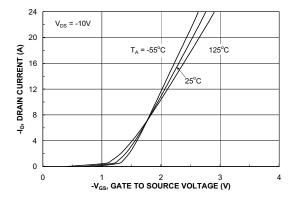


Figure 5. Transfer Characteristics.

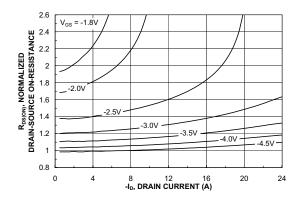


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

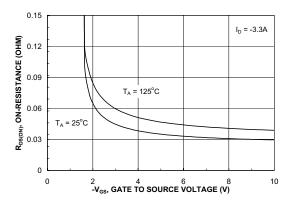


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

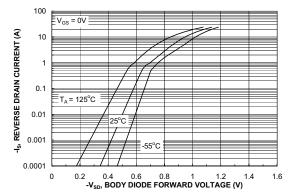
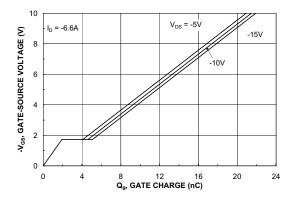


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



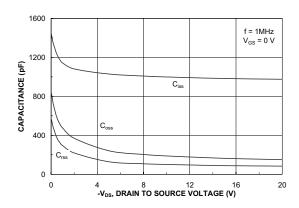
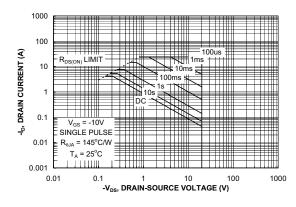


Figure 7. Gate Charge Characteristics.

Figure 8. Capacitance Characteristics.



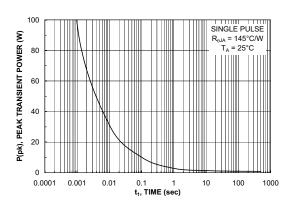


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

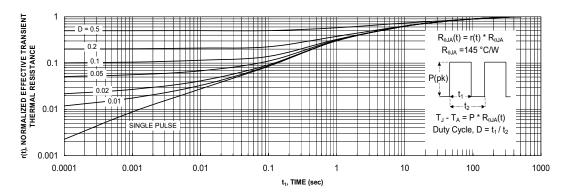
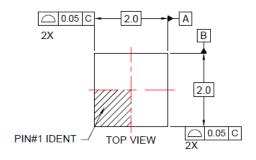
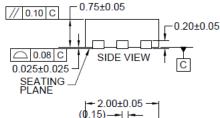


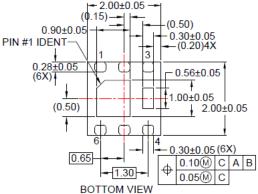
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

Dimensional Outline and Pad Layout

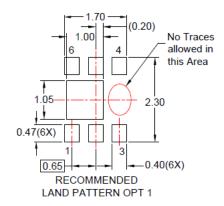


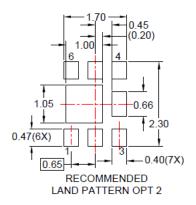




NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP06Lrev4.







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