S-19683B Series

AUTOMOTIVE, 125°C OPERATION, 36 V INPUT, 600 mA, HIGH SIDE SWITCH WITH CURRENT MONITOR

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Rev.1.2_00

This IC, developed by using CMOS technology, is a high side switch with the current monitor function.
When the Pch output transistor is turned on, voltage is supplied to the load connected to the VOUT pin. The current monitor measures the current flowing to the high side switch, outputs the voltage according to the load current, and limits the current value from exceeding the set value.
In addition, this IC has the ON / OFF circuit to control the Pch output transistor's status, ON and OFF, and the thermal shutdown circuit to limit overheating.

ABLIC Inc. offers FIT rate calculated based on actual customer usage conditions in order to support customer functional safety design.
For more information regarding our FIT rate calculation, contact our sales representatives.

Caution **This product can be used in vehicle equipment and in-vehicle equipment. Before using the product in the purpose, contact to ABLIC Inc. is indispensable.**

■ Features

- Input voltage: 4.5 V to 36.0 V
- Current consumption: During operation: 55 µA typ., 95 µA max. (T_j = –40°C to +150°C)
  During power-off: 0.6 µA typ., 2.0 µA max. (T_j = –40°C to +125°C)
- ON resistance: R_{ON} = 0.6 Ω typ., 1.0 Ω max. (T_j = –40°C to +125°C)
- Limit current: 300 mA to 600 mA, selectable in 10 mA step
- Limit current accuracy: ±10%
- Current monitor function: Possible to monitor load current by monitoring the CSO pin voltage.
- Built-in thermal shutdown circuit: Latch type*1, detection temperature 170°C typ.
- Build-in overvoltage detection circuit: Detects an output short-circuit of the higher voltage.
- Built-in ON / OFF circuit: Ensures long battery life.
- Under voltage lockout function (UVLO): 2.6 V typ. (Detection voltage)
- Operation temperature range: Ta = –40°C to +125°C
- Lead-free (Sn 100%), halogen-free
- Withstand 45 V load dump
- AEC-Q100 qualified *2

***1.** Please contact our sales representatives for products with hysteresis type.
***2.** Contact our sales office for details.

■ Applications

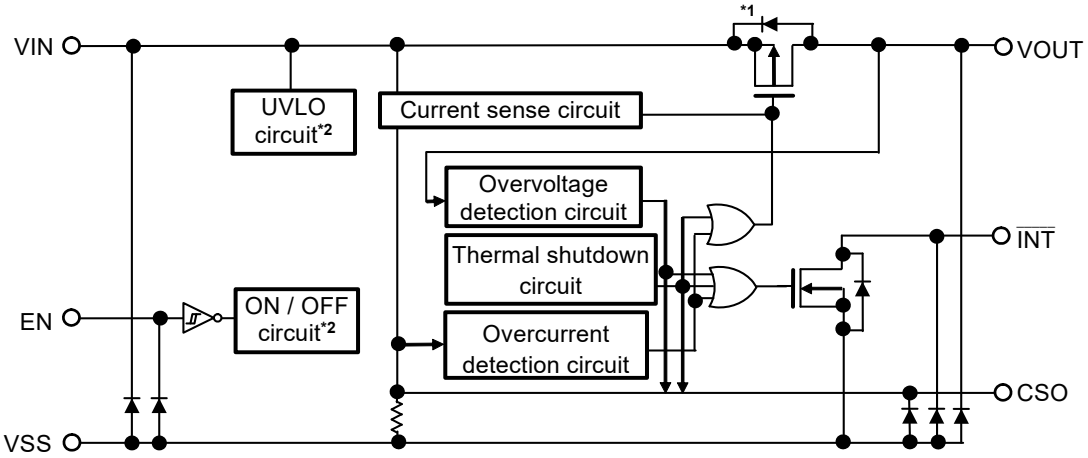
- Automotive surround camera ECU
- Connection diagnosis for camera module

■ Package

- HSNT-8(2030)

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■ Block Diagram



***1.** Parasitic diode
***2.** The ON / OFF circuit and the UVLO circuit control the internal circuit, the Pch output transistor and the Nch output transistor.

Figure 1

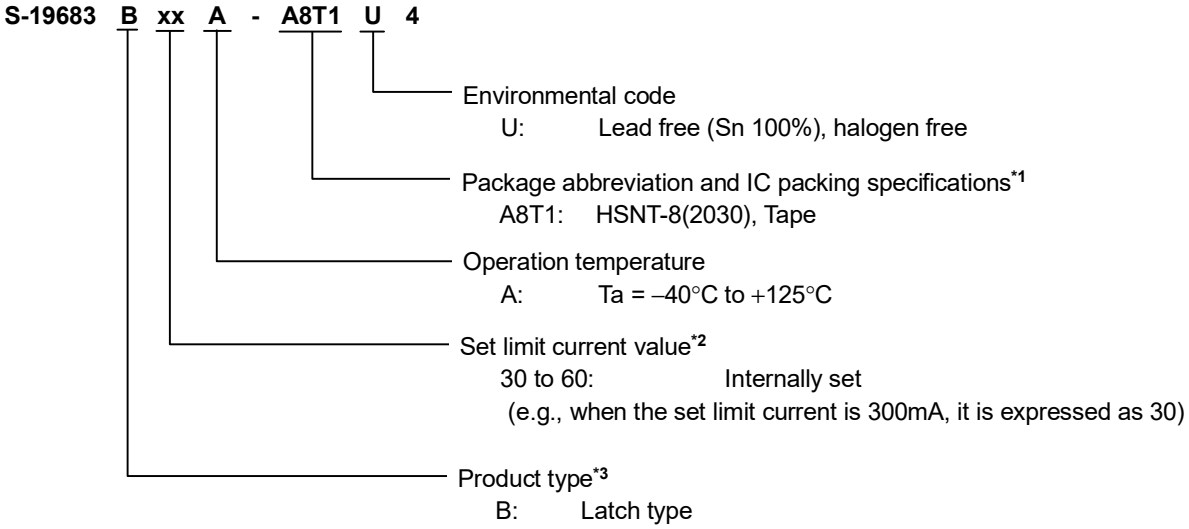
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■ AEC-Q100 Qualified

This IC supports AEC-Q100 for operation temperature grade1.
Contact our sales representatives for details of AEC-Q100 reliability specification.

■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.
***2.** Refer to "**4. Product name list**".
***3.** Refer to "**2. Function list of product types**".

2. Function list of product types

Table 1

Product Type	ON / OFF Logic	Thermal Shutdown Circuit
B	Active "H"	Latch type

Remark Please contact our sales representatives for products with hysteresis type.

3. Package

Table 2 Package Drawing Codes

Package Name	Dimension	Tape	Reel	Land
HSNT-8(2030)	PP008-A-P-SD	PP008-A-C-SD	PP008-A-R-SD	PP008-A-L-SD

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4. Product name list

ON / OFF logic: Active "H"
Thermal shutdown circuit: Latch type

Table 3

Limit Current	HSNT-8(2030)
400 mA ± 10%	S-19683B40A-A8T1U4
500 mA ± 10%	S-19683B50A-A8T1U4
600 mA ± 10%	S-19683B60A-A8T1U4

Remark Please contact our sales representatives for products other than the above.

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■ Pin Configuration

1. HSNT-8(2030)

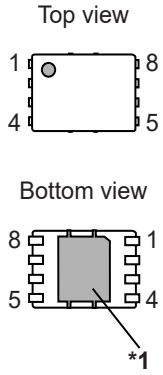


Figure 2

Table 4

Pin No.	Symbol	Description
1	VIN	Voltage input pin
2	NC*2	No connection
3	EN	Enable pin
4	VSS	GND pin
5	CSO	Current sense output pin and status output pin
6	$\overline{\text{INT}}$	Interrupt signal output pin
7	NC*2	No connection
8	VOUT	Voltage output pin

***1.** Connect the heat sink of backside at shadowed area to the board, and set electric potential GND. However, do not use it as the function of electrode.

***2.** The NC pin is electrically open.
The NC pin can be connected to the VIN or the VSS pin.

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■ Absolute Maximum Ratings

Table 5

(T_j = –40°C to +150°C unless otherwise specified)

Item	Symbol	Absolute Maximum Rating	Unit
Input voltage	V_{IN}	V_{SS} – 0.3 to V_{SS} + 45	V
	V_{EN}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 45	V
Output voltage	V_{OUT}	V_{SS} – 0.3 to V_{IN} + 1 ≤ V_{SS} + 45	V
	V_{CSO}	V_{SS} – 0.3 to V_{IN} + 0.3 ≤ V_{SS} + 7	V
	$V_{\overline{INT}}$	V_{SS} – 0.3 to V_{SS} + 7	V
Output current	I_{OUT}	800	mA
	$I_{\overline{INT}}$	13.2	mA
Junction temperature	T_j	–40 to +150	°C
Operation ambient temperature	T_{opr}	–40 to +125	°C
Storage temperature	T_{stg}	–40 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

■ Thermal Resistance Value

Table 6

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Junction-to-ambient thermal resistance*1	θ_{JA}	HSNT-8(2030)	Board A	–	181	–	°C/W
			Board B	–	135	–	°C/W
			Board C	–	40	–	°C/W
			Board D	–	42	–	°C/W
			Board E	–	32	–	°C/W

***1.** Test environment: compliance with JEDEC STANDARD JESD51-2A

Remark Refer to "■ **Thermal Characteristics**" for details of power dissipation and test board.

■ Recommended Operation Conditions

Table 7

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input voltage	V_{IN}	–	4.5	–	36.0	V
EN pin voltage	V_{EN}	–	0	–	V_{IN}	V
Input capacitance	C_{IN}	–	0.1	–	–	µF
Output capacitance	C_L	–	–	0.1	–	µF
Current sense output capacitance	C_{CSO}	–	0.01	0.1	1.0	µF
External pull-up resistor for $\overline{INT}$ pin	$R_{\overline{INT}}$	–	3	–	–	kΩ

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■ Electrical Characteristics

Table 8

(V_{IN} = 13.5 V, T_j = −40°C to +150°C unless otherwise specified)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Test Circuit
Current consumption during operation	I_{SS1}	V_{EN} = V_{IN}, I_{OUT} = 0 mA	−	55	95	µA	1
Current consumption during power-off	I_{SS2}	V_{EN} = 0 V, I_{OUT} = 0 mA T_j = −40°C to +125°C	−	0.6	2.0	µA	1
ON resistance*1	R_{ON}	V_{EN} = V_{IN}, V_{IN} ≥ 5.0 V T_j = −40°C to +125°C	−	0.6	1.0	Ω	2
Output OFF leakage current	$I_{LEAK,VOUT}$	V_{EN} = 0 V, V_{OUT} = 0 V T_j = −40°C to +125°C	−	0	2.0	µA	3
Limit current*2	I_{LIM}	−	$I_{LIM(S)}$ × 0.9	$I_{LIM(S)}$	$I_{LIM(S)}$ × 1.1	mA	3
Current limit voltage for CSO pin	V_{CSO_Ilim}	−	2.38	2.55	2.65	V	3
Output voltage during thermal shutdown detection of CSO pin	V_{CSO_TSD}	−	2.65	2.80	2.95	V	−
Output voltage during overvoltage detection of CSO pin	V_{CSO_OVD}	V_{OUT} > V_{IN} + 0.3 V	3.00	3.10	3.20	V	3
Interrupt output voltage "L"	$V_{OL,\overline{INT}}$	V_{DD} = 5.0 V, $R_{\overline{INT}}$ = 3 kΩ	−	−	0.4	V	4
Interrupt output leakage current	$I_{LEAK,\overline{INT}}$	V_{DS} = 5.0 V	−	−	1.0	µA	5
EN pin input voltage "H"	V_{SH}	−	2.0	−	−	V	6
EN pin input voltage "L"	V_{SL}	−	−	−	0.8	V	6
EN pin input current "H"	I_{SH}	V_{EN} = V_{IN}	−	0.1	1.0	µA	6
EN pin input current "L"	I_{SL}	V_{EN} = 0 V	−0.2	0	0.2	µA	6
Thermal shutdown detection temperature	T_{SD}	Junction temperature	−	170	−	°C	−
Overvoltage detection voltage	V_{OVD+}	−	−	V_{IN} + 0.12	−	V	−
Overvoltage release voltage	V_{OVD-}	−	−	V_{IN} + 0.06	−	V	−
UVLO detection voltage	V_{UVLO-}	−	2.1	2.6	−	V	−
UVLO release voltage	V_{UVLO+}	−	−	2.8	3.3	V	−
Turn-ON delay time*3	$t_{d,ON}$	I_{OUT} = 50 mA, C_L = 0.1 µF	20	75	160	µs	7
Turn-OFF delay time*3	$t_{d,OFF}$	I_{OUT} = 50 mA, C_L = 0.1 µF	5	15	60	µs	7
Turn-ON time*3	t_{ON}	I_{OUT} = 50 mA, C_L = 0.1 µF	25	85	180	µs	7
Turn-OFF time*3	t_{OFF}	I_{OUT} = 50 mA, C_L = 0.1 µF	10	35	100	µs	7
Current sense output voltage settling time 1*4	$t_{set,CS1}$	C_{CSO} = 0.1 µF	−	−	$\frac{450}{I_{LIM(S)}\,[A]}$	µs	−
Current sense output voltage settling time 2*4	$t_{set,CS2}$	C_{CSO} = 0.1 µF	−	−	$\frac{450}{I_{LIM(S)}\,[A]}$	µs	−
Interrupt "L" output delay time*5	$t_{dL,\overline{INT}}$	−	−	500	−	µs	8

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***1.** $R_{ON} = \frac{(V_{IN} - V_{OUT})}{I_{OUT}}$

***2.** I_{LIM}: Actual limit current
$I_{LIM(S)}$: Set limit current
Attention should be paid to the power dissipation when the output current is large.

***3.** Refer to **Figure 3**.

***4.** Refer to **Figure 4**. This specification is guaranteed by design.

***5.** The time from when CSO pin voltage (V_{CSO}) exceeds V_{CSO_Ilim} to when the $\overline{INT}$ pin starts to output "L" level voltage.

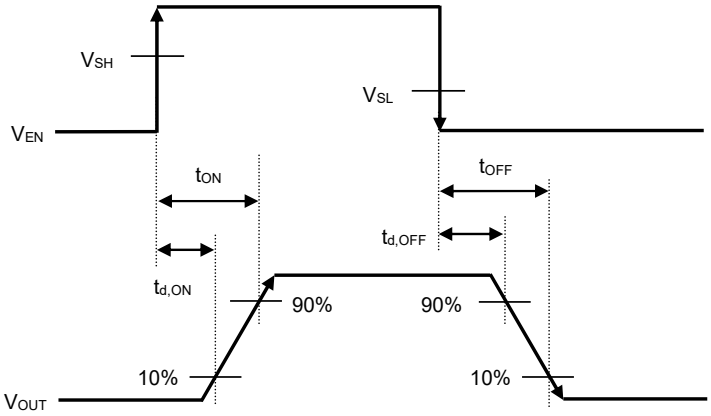


Figure 3

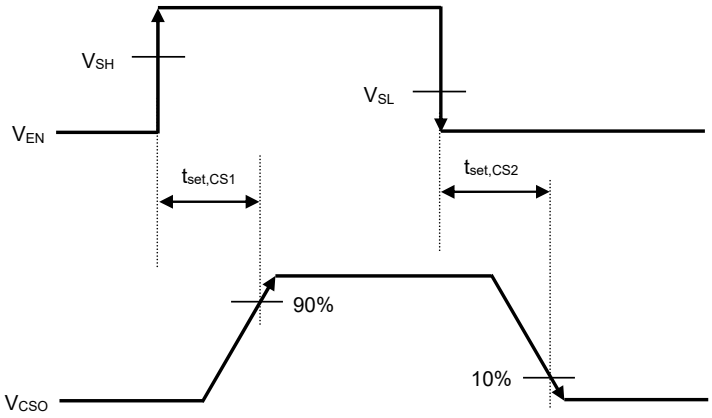


Figure 4

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■ Test Circuits

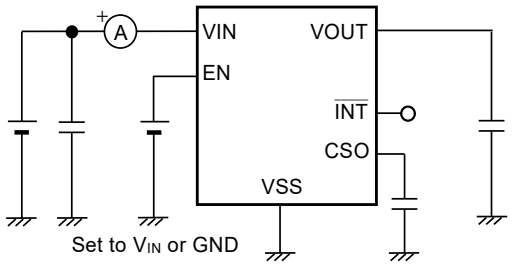


Figure 5 Test circuit 1

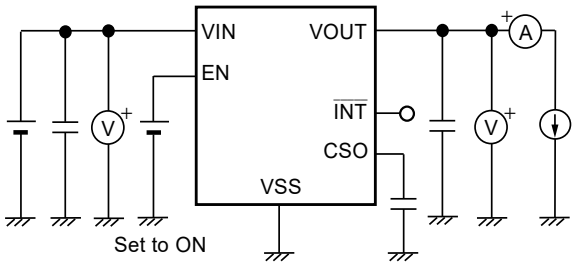


Figure 6 Test circuit 2

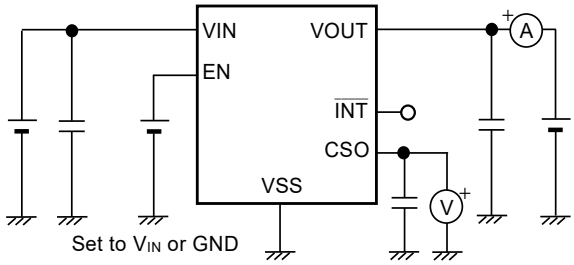


Figure 7 Test circuit 3

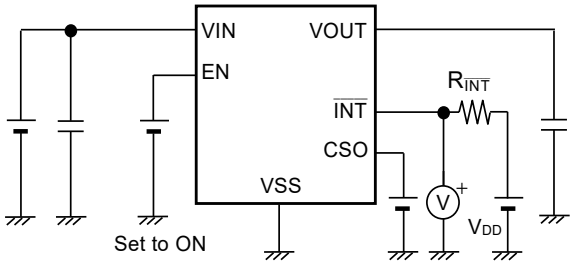


Figure 8 Test circuit 4

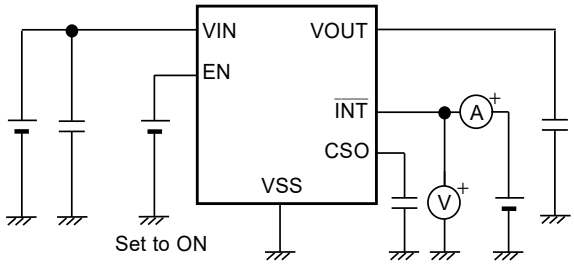


Figure 9 Test circuit 5

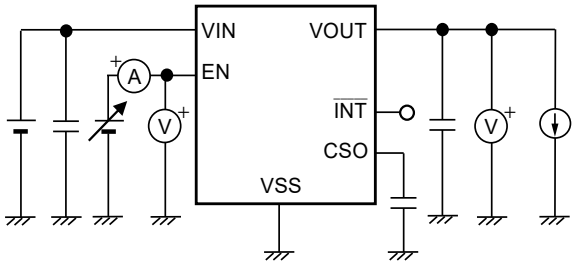


Figure 10 Test circuit 6

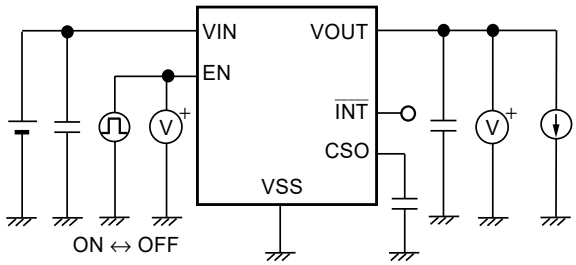


Figure 11 Test circuit 7

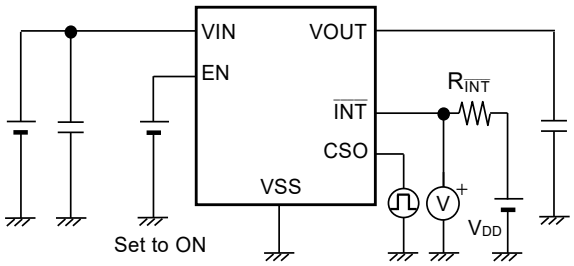
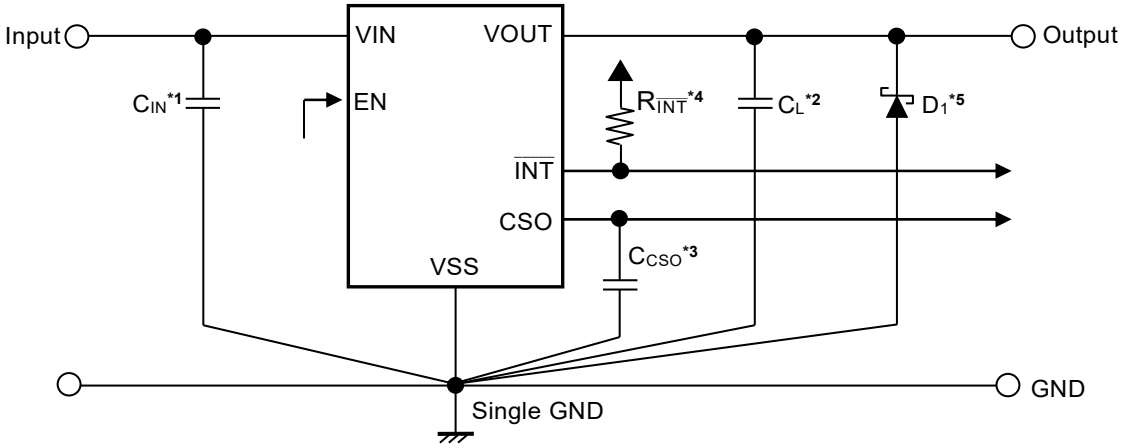


Figure 12 Test circuit 8

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■ Standard Circuit



***1.** C_{IN} is a capacitor for stabilizing the input.
***2.** C_L is a capacitor for stabilizing the output.
***3.** C_{CSO} is a capacitor for stabilizing the CSO pin output.
***4.** $R_{\overline{INT}}$ is the external pull-up resistor for the $\overline{INT}$ pin.
***5.** D_1 is a protection Schottky-barrier diode (SBD) for limiting the negative voltage caused by load circuit. Necessity of D_1 depends on the load circuit connected to output in the application.

Figure 13

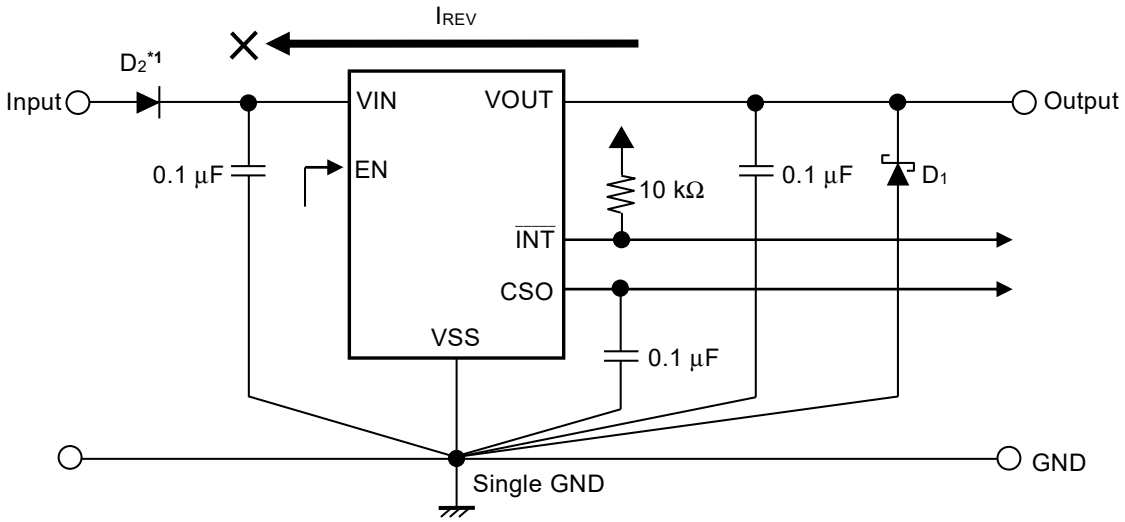
Caution The above connection diagram will not guarantee successful operation.
Perform thorough evaluation using the actual application to set the constants.

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■ Application Circuit

1. With rectifier diode for reverse current protection in input line

In **Figure 14**, D_2 is inserted between the input line and VIN pin so that the overvoltage detection circuit operates by detecting the overvoltage of the VOUT pin. If the rectifier diode is inserted between the VOUT pin and output line unlike **Figure 14**, the reverse current protection functions, but this IC cannot detect the overvoltage of the output line because the overvoltage of the VOUT pin does not occur.



***1.** D_2 is a rectifier diode for preventing reverse current (I_{REV}) from output to input.

Figure 14

Caution The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

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2. Parallel operation

Figure 15 shows a connection diagram of two ICs operated in parallel. A parallel connection can double the output current.
By connecting n*1 number of ICs in parallel, as shown in **Figure 15**, the output current can be multiplied by n times. When n number of ICs with the same set limit current is connected in parallel, the overall on-resistance ($R_{ON,n}$) becomes $R_{ON,n} = R_{ON} / n$ and the overall limit current ($I_{LIM,n}$) becomes $I_{LIM,n} = I_{LIM} \times n$.
For information on applications regarding parallel operation of this IC, refer to the "**Parallel Operation of S-19682B/19683B Series**" application note.

***1.** n: An integer greater than or equal to 2

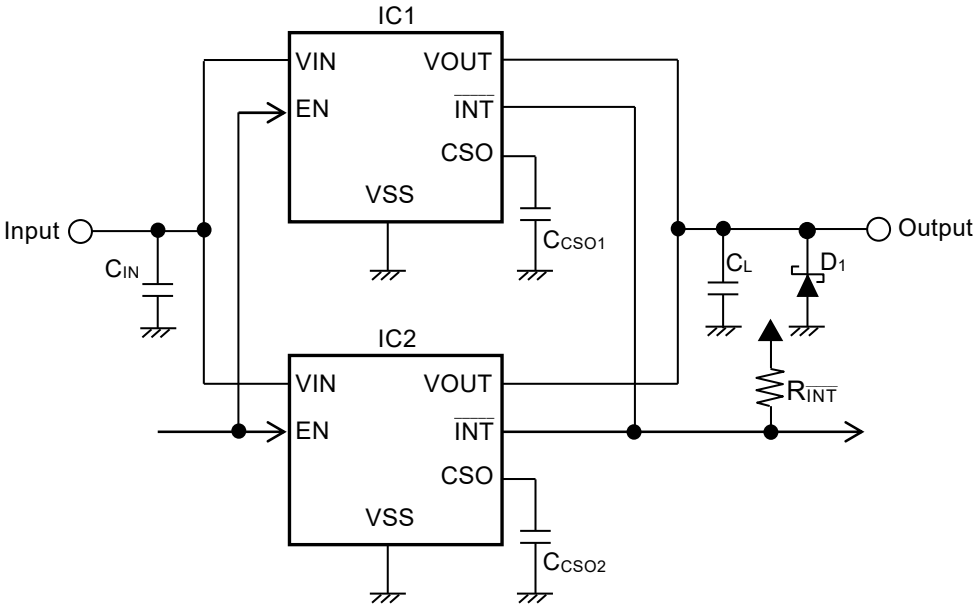


Figure 15

Caution 1. To stabilize the current balance between the ICs, the CSO pin of each IC must not be interconnected. Also, connect a capacitor to the CSO pin of each IC to stabilize CSO pin output.
2. As shown in Figure 15, the capacitor for stabilizing the input (C_{IN}), the capacitor for stabilizing the output (C_L) and the protection Schottky-barrier diode (D_1) can be shared, but the ICs should be placed close together and C_{IN}, C_L and D_1 should be located as close to the IC connection pins as possible.
3. The above connection diagram and constants will not guarantee successful operation. Perform thorough evaluation using the actual application to set the constants.

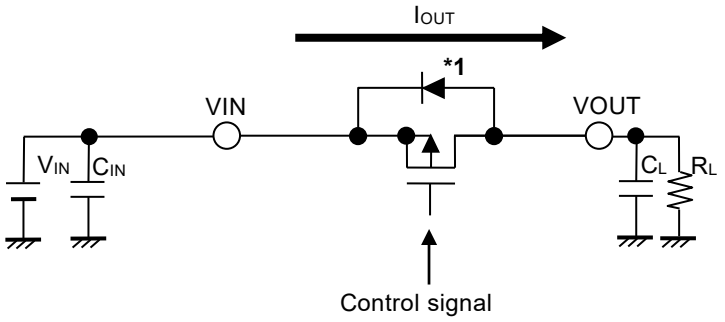
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■ Operation

1. Basic operation

Figure 16 shows the block diagram of this IC to describe the basic operation.
Connect an external power supply to the VIN pin and a load to the VOUT pin. Due to the IC internal control signal, the Pch output transistor is turned on or off, and the switch operation is performed between the VIN pin and the VOUT pin.
When the Pch output transistor is turned on, the VIN pin and the VOUT pin are connected. Since the output current which flows from the VOUT pin to the load (I_{OUT}) is supplied from VIN pin via the Pch output transistor, the current which flows in Pch output transistor will be I_{OUT}.
Since a voltage drop (V_{drop}) occurs by flowing I_{OUT} in the Pch output transistor with ON resistance (R_{ON}), the voltage supplied to the load (V_{OUT}) is calculated by using formula (1).

(1) $V_{OUT} = V_{IN} - I_{OUT} \times R_{ON}$



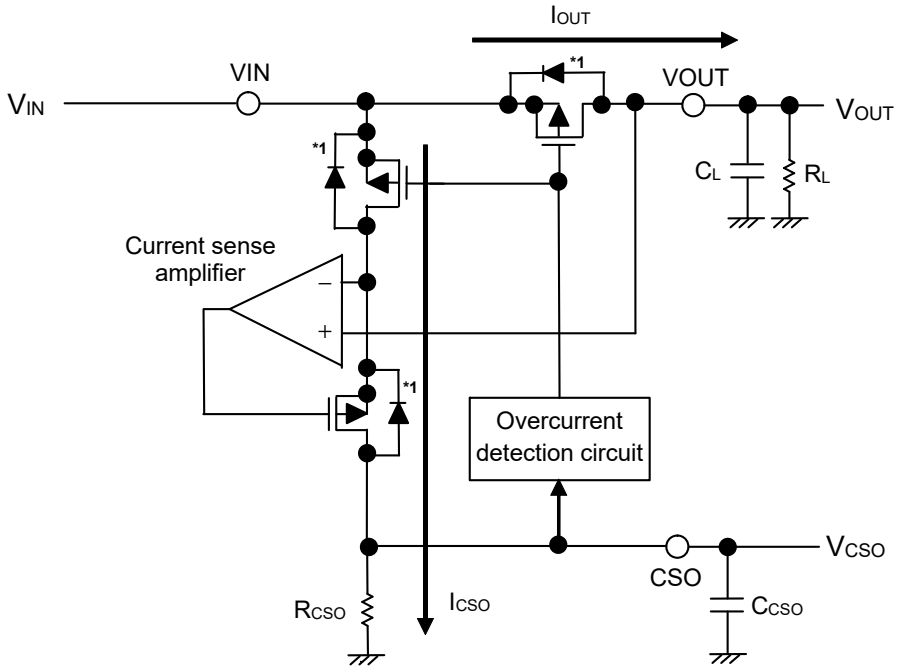
***1.** Parasitic diode

Figure 16

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2. Current monitor operation

Figure 17 shows the current monitor block diagram of this IC.
The current monitor measures the current flowing to the Pch output transistor and outputs voltage to the CSO pin by the magnification corresponding to the constant defined by internal circuits.
The current sense amplifier operates so that the sense current (I_{CSO}) flowing to the current sense resistor (R_{CSO}) is proportional to the output current (I_{OUT}). In result, the CSO pin voltage (V_{CSO}) is set as $V_{CSO} = I_{CSO} \times R_{CSO}$ and proportional to the output current (I_{OUT}). **Figure 18** shows the relation between V_{CSO} and I_{OUT} for 2 types of set limit current value.
If the V_{CSO} reaches the current limit voltage for CSO pin (V_{CSO_Ilim}), this IC becomes overcurrent limit operation status and controls the current flowing in the Pch output transistor as limit current (I_{LIM}) by lowering the output voltage (V_{OUT}).
The $\overline{INT}$ pin outputs V_{SS} level during the overcurrent limit operation.

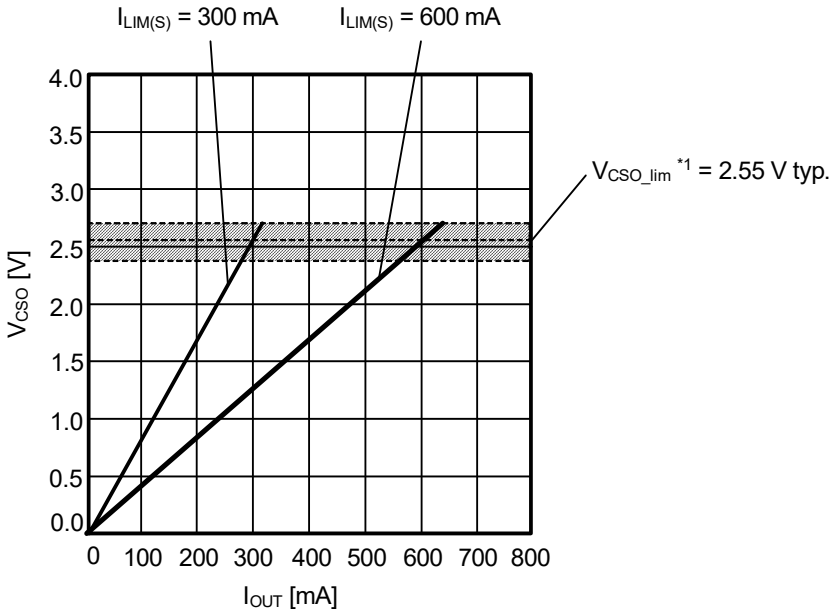


***1**. Parasitic diode

Figure 17

Caution 1. Mounted board layout should be made in such a way that no or enough less DC current flows into or from CSO pin since the effective I_{CSO} changes, otherwise correct I_{LIM} may not be provided.
2. The above connection diagram will not guarantee successful operation. Perform thorough evaluation using an actual application circuit.

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***1.** Current limit voltage for CSO pin

Figure 18

Table 9

Current Limit Circuit	VOUT Pin Voltage	CSO Pin Voltage	$\overline{INT}$ Pin Voltage
Detect	$I_{LIM} \times R_L$	2.55 V typ.	V_{SS} level
Release	Set value	Set value	Pull-up level

Remark The set limit current value ($I_{LIM(S)}$) is selectable from 300 mA to 600 mA in 10 mA step.

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3. EN pin

This pin starts and stops the switch operation and the current monitor operation. When the EN pin is set to OFF, the internal circuit stops operating and the Pch output transistor and the Nch output transistor (the $\overline{INT}$ pin) are turned off, reducing current consumption significantly.

The internal equivalent circuit related to the EN pin is configured as shown in **Figure 19**. The EN pin is internally pulled down to the VSS pin in the floating status, so the VOUT pin is set to the V_{SS} level. For the EN pin current, refer to the EN pin input current "H" in "■ **Electrical Characteristics**".

The current consumption increases when a voltage of 0.6 V to V_{IN} – 0.3 V is applied to the EN pin, so caution should be exercised.

Table 10

Product Type	EN Pin	Internal Circuit	VOUT Pin Voltage	CSO Pin Voltage	$\overline{INT}$ Pin Voltage	Current Consumption
B	"H": ON	Operate	$V_{IN} - V_{drop}$ *1	Set value	Set value	I_{SS1}
B	"L": OFF	Stop	V_{SS} level*2	Pull-down level	Pull-up level	I_{SS2}

***1.** A voltage drop occurs by flowing I_{OUT} in Pch output transistor with ON resistance (R_{ON}).

$V_{drop} = R_{ON} \times I_{OUT}$

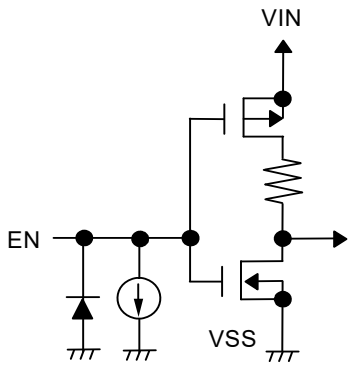


Figure 19

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4. Thermal shutdown circuit

This IC has a built-in thermal shutdown circuit to limit overheating.

When the junction temperature increases to 170°C typ., the thermal shutdown circuit becomes the detection status, and the Pch output transistor is turned off. Even if the junction temperature would decrease, the thermal shutdown circuit detection status is latched and the Pch output transistor remains in the status, OFF.
The thermal shutdown circuit detection status latch is released by using the EN pin to set the IC power-off status or lowering the input voltage (V_{IN}) to change the UVLO circuit to the detection status.
Set the V_{IN} 2.1 V or lower in order to change the UVLO circuit to the detection status.

Caution 1. When a steep fluctuation of the V_{IN} occurs, the thermal shutdown circuit may become the detection status even if the junction temperature would not reach 170°C typ., so pay enough attention to the V_{IN} to ensure stable status sufficiently. Perform thorough evaluation using the actual application.

2. If the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur in the VOUT pin due to resonance phenomenon of the inductance and the capacitance including C_L on the application. When a negative voltage exceeding the absolute maximum rating occurs, the thermal shutdown circuit may become the detection status even if the junction temperature would not reach 170°C typ. If V_{OUT} does not rise when the short-circuit is eliminated after the VOUT pin is steeply shorted with the GND, release the detection status latch.

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5. Overvoltage detection circuit

This IC detects the overvoltage when the output voltage is $V_{OUT} \geq V_{IN} + 0.12$ V typ.
When overvoltage is detected, the Pch output transistor is turned off, and the CSO pin voltage increases to 3.10 V typ. The $\overline{INT}$ pin outputs V_{SS} level.

Table 11

Overvoltage Detection Circuit	VOUT Pin Voltage	CSO Pin Voltage	$\overline{INT}$ Pin Voltage
Detect	$V_{OUT} \geq V_{IN} + 0.12$ V typ.	3.10 V typ.	V_{SS} level
Release	$V_{OUT} < V_{IN} + 0.06$ V typ.	Set value	Pull-up level

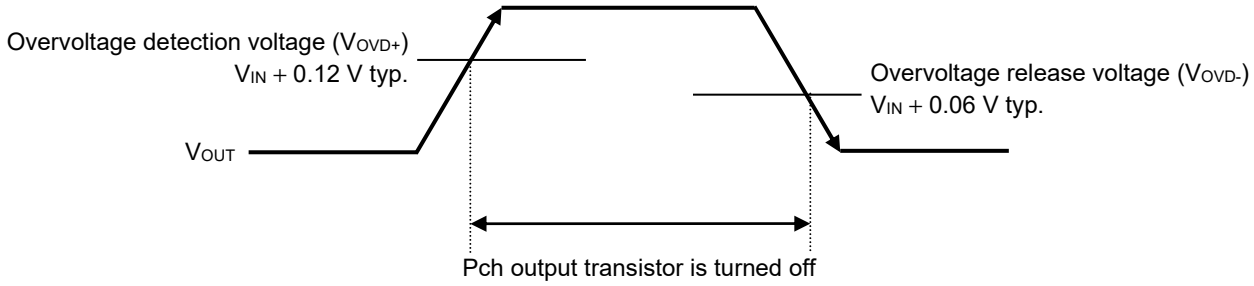


Figure 20

6. Under voltage lockout function (UVLO)

This IC has a built-in UVLO circuit. When input voltage (V_{IN}) drops lower than the UVLO detection voltage (V_{UVLO-}), the internal circuit stops operating and the Pch output transistor and the Nch output transistor ($\overline{INT}$ pin) are turned off. In the latch type thermal shutdown circuit, the detection status latch is released.
When the V_{IN} rises higher than the UVLO release voltage (V_{UVLO+}), the internal circuit starts operating. The V_{UVLO-} is 2.6 V typ. and the V_{UVLO+} is 2.8 V typ.
Even if the V_{IN} is higher than the V_{UVLO+} immediately after power supply startup, the Pch output transistor and the Nch output transistor ($\overline{INT}$ pin) are turned off until the internal IC operates stably.

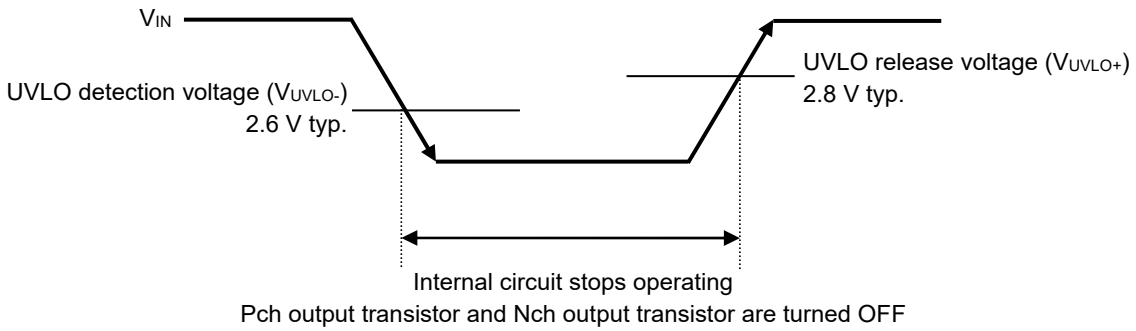


Figure 21

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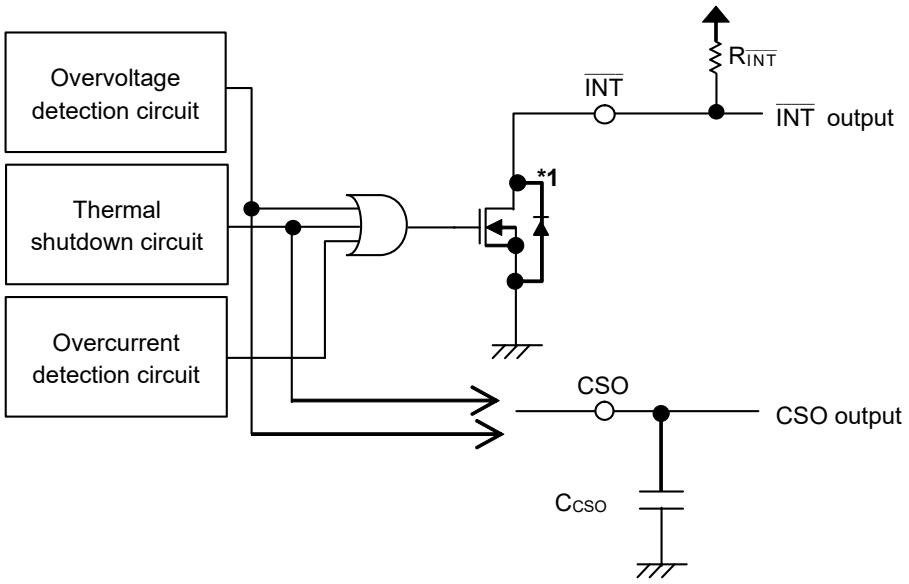
7. The CSO pin and the $\overline{\text{INT}}$ pin output function

This IC can discriminate on which one of the following 4 statuses it is operating by monitoring the CSO pin voltage.

- Normal status
- Overcurrent status
- Overheat status
- Overvoltage status

This IC can also discriminate on which one of the following 2 statuses it is operating by monitoring the $\overline{\text{INT}}$ pin voltage.

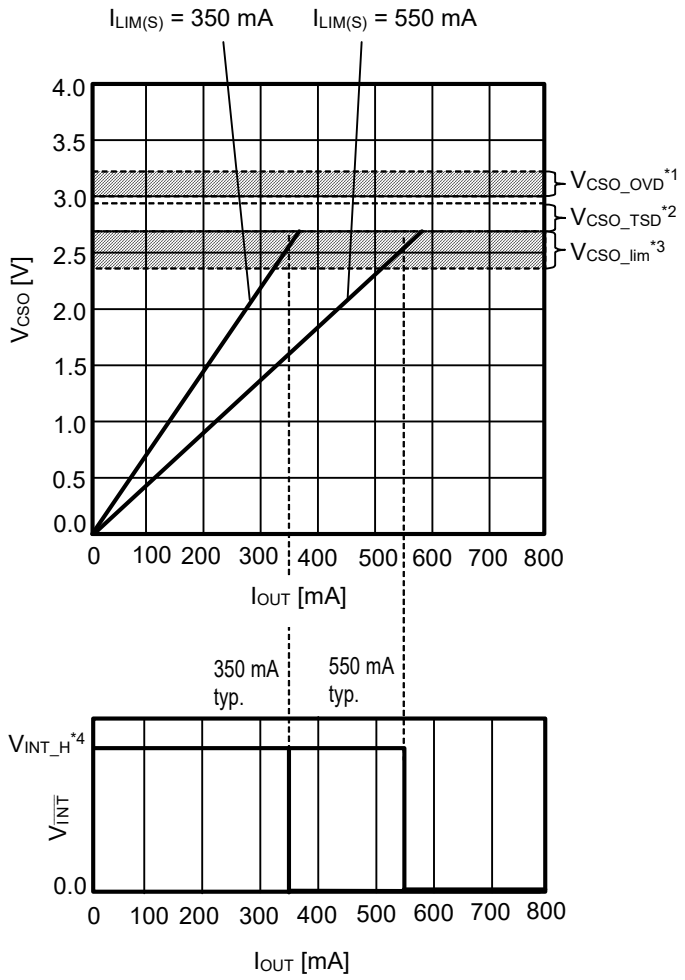
- Normal status
- Overcurrent, overheat or overvoltage status



***1.** Parasitic diode

Figure 22

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***1.** Output voltage during overvoltage detection of CSO pin
***2.** Output voltage during thermal shutdown detection of CSO pin
***3.** Current limit voltage for CSO pin
***4.** Pull-up voltage

Figure 23

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■ Precautions

- The wiring patterns for the power supply and GND should be designed so that the impedance is low.
  When mounting the input capacitor (C_{IN}) between the VIN pin and the VSS pin, and the output capacitor (C_L) between the VOUT pin and the VSS pin, connect them as close as possible to the respective destination pins of the IC.
- The following use conditions are recommended to ensure stable operation of this IC; however, perform thorough evaluation including the temperature characteristics with an actual application to select C_{IN}, C_L and C_{CSO}.

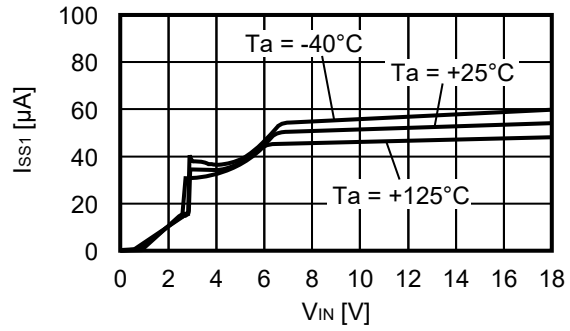
Input capacitor (C_{IN}):	A ceramic capacitor with 0.1 µF or more is recommended.
Output capacitor (C_L):	A ceramic capacitor with 0.1 µF is recommended.
Capacitor for stabilizing the CSO pin output (C_{CSO}):	A ceramic capacitor with 0.01 µF to 1 µF is recommended.

- If the VOUT pin is steeply shorted with GND, a negative voltage exceeding the absolute maximum ratings may occur in the VOUT pin due to resonance phenomenon of the inductance and the capacitance including C_L on the application. The resonance phenomenon is expected to be weakened by inserting a series resistance into the resonance path, and the negative voltage is expected to be limited by inserting a protection diode between the VOUT pin and the VSS pin.
- Make sure of the conditions for the input voltage (V_{IN}) and the load current so that the internal loss does not exceed the power dissipation.
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
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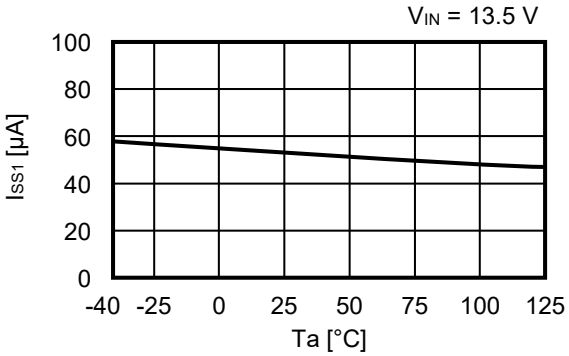
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■ Characteristics (Typical Data)

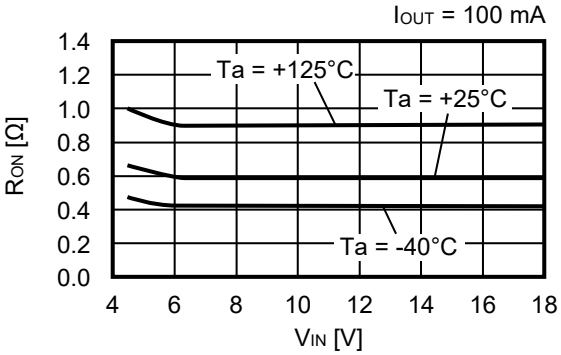
1. Current consumption during operation (I_{SS1}) vs. Input voltage (V_{IN})



2. Current consumption during operation (I_{SS1}) vs. Temperature (Ta)

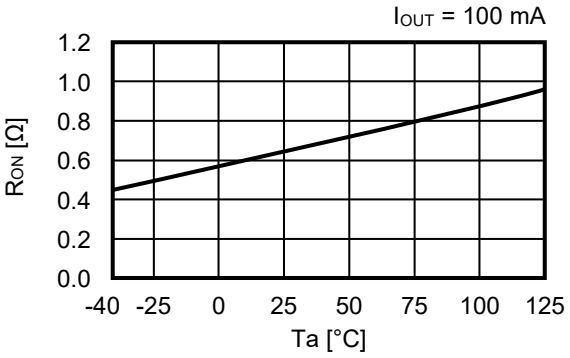


3. ON resistance (R_{ON}) vs. Input voltage (V_{IN})

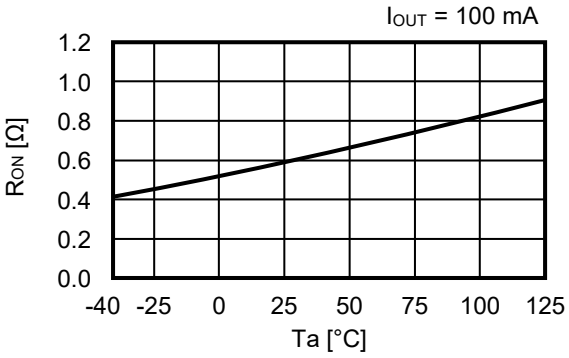


4. ON resistance (R_{ON}) vs. Temperature (Ta)

4. 1 V_{IN} = 5.0 V

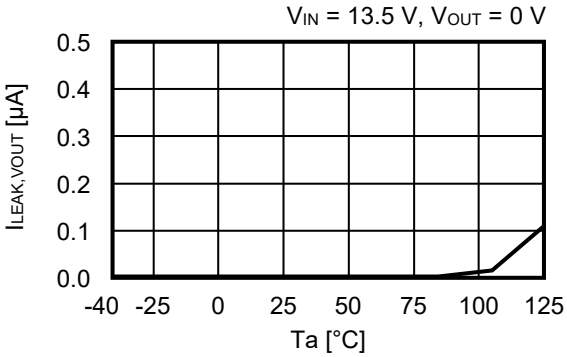


4. 2 V_{IN} = 13.5 V



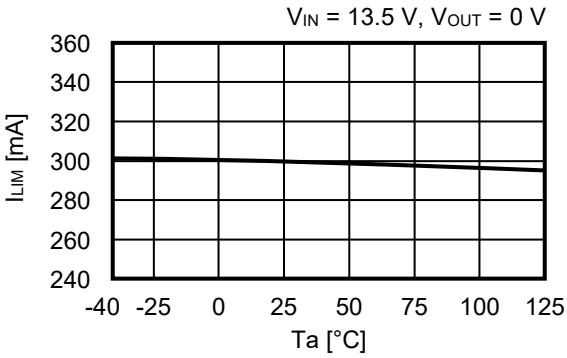
Downloaded from Arrow.com.

5. Output OFF leakage current ($I_{LEAK,VOUT}$) vs. Temperature (Ta)

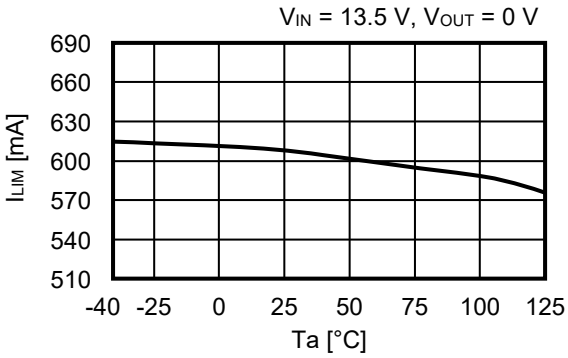


6. Limit current (I_{LIM}) vs. Temperature (Ta)

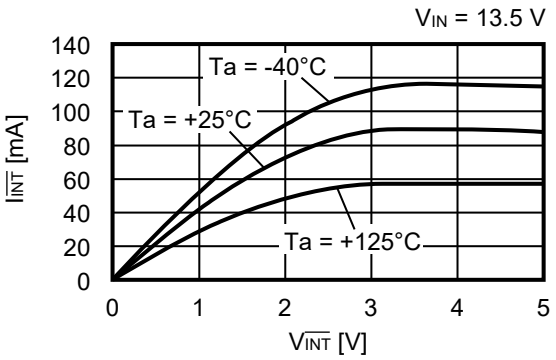
6. 1 $I_{LIM(S)}$ = 300 mA



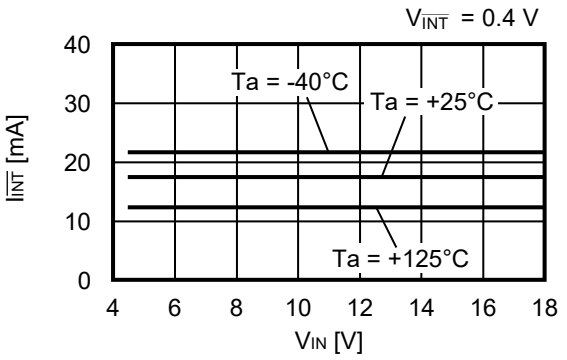
6. 2 $I_{LIM(S)}$ = 600 mA



7. $\overline{INT}$ pin output current ($I_{\overline{INT}}$) vs. $\overline{INT}$ pin voltage ($V_{\overline{INT}}$)

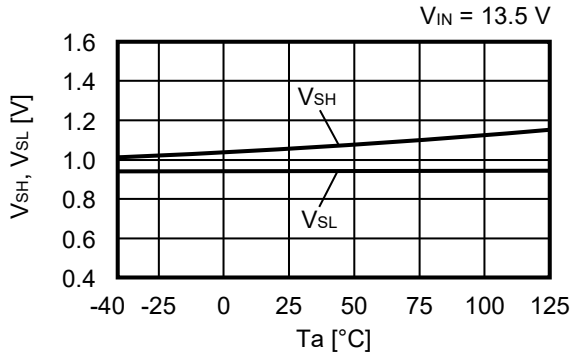


8. $\overline{INT}$ pin output current ($I_{\overline{INT}}$) vs. Input voltage (V_{IN})

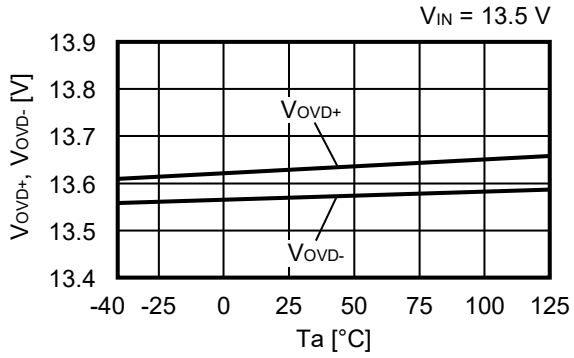


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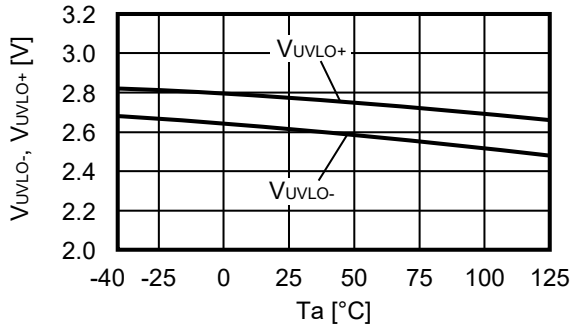
9. EN pin input voltage "H" (V_{SH}), EN pin input voltage "L" (V_{SL}) vs. Temperature (Ta)



10. Overvoltage detection voltage (V_{OVD+}), Overvoltage release voltage (V_{OVD-}) vs. Temperature (Ta)

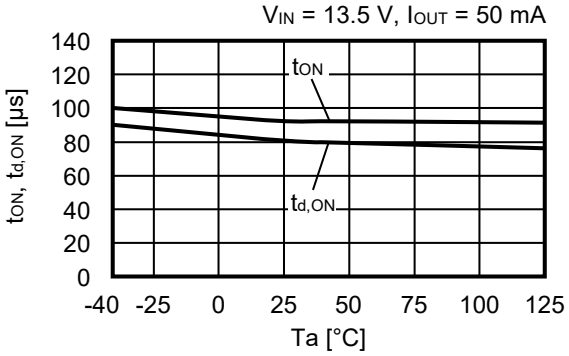


11. UVLO detection voltage (V_{UVLO-}), UVLO release voltage (V_{UVLO+}) vs. Temperature (Ta)

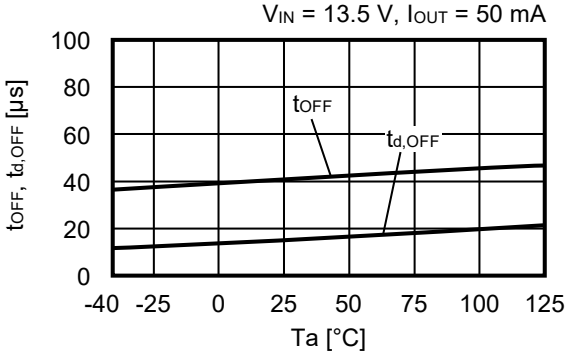


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12. Turn-ON time (t_{ON}), Turn-ON delay time ($t_{d,ON}$) vs. Temperature (Ta)

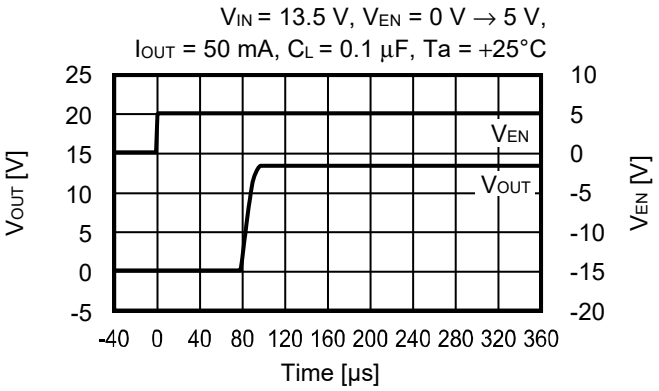


13. Turn-OFF time (t_{OFF}), Turn-OFF delay time ($t_{d,OFF}$) vs. Temperature (Ta)

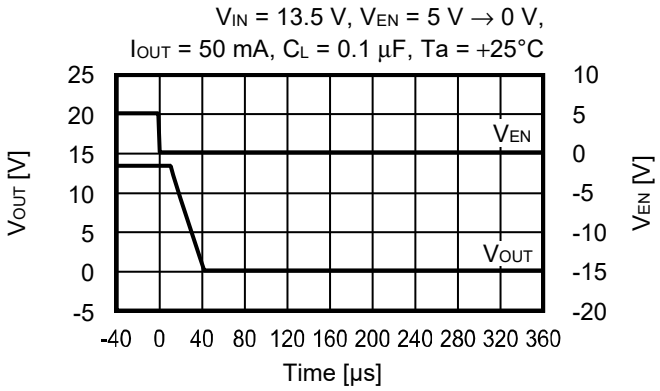


14. Transient characteristics

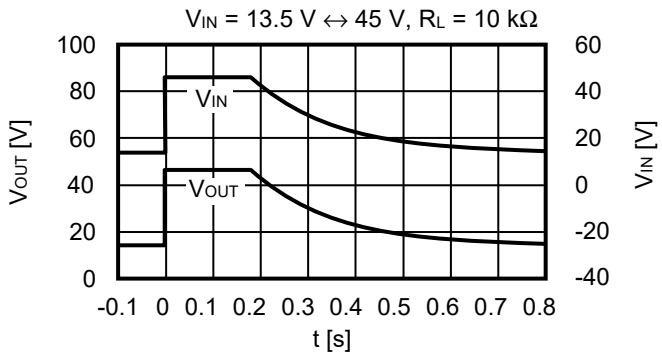
14. 1 Turn on



14. 2 Turn off



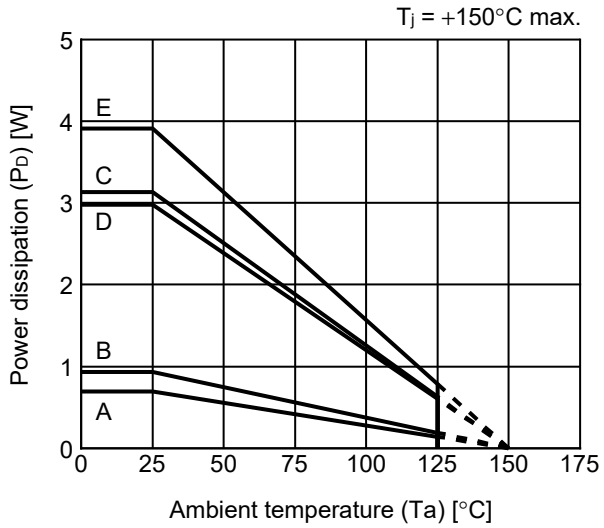
15. Load dump characteristics (Ta = +25°C)



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■ Power Dissipation

HSNT-8(2030)



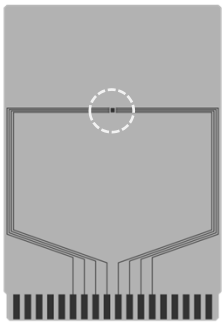
Board	Power Dissipation (P_D)
A	0.69 W
B	0.93 W
C	3.13 W
D	2.98 W
E	3.91 W

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HSNT-8(2030) Test Board

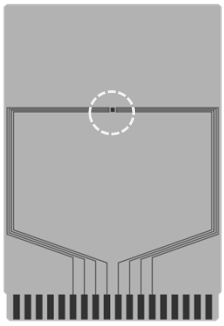
IC Mount Area

(1) Board A



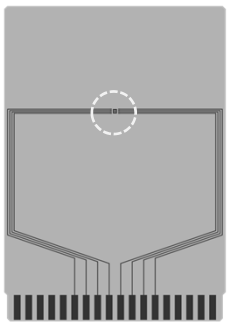
Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		2
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	-
	3	-
	4	74.2 x 74.2 x t0.070
Thermal via		-

(2) Board B



Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(3) Board C





enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Land pattern and wiring for testing: t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

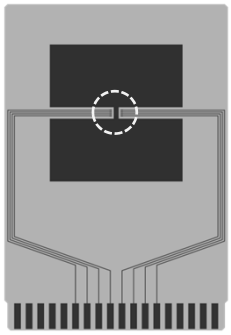
No. HSNT8-A-Board-SD-2.0

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HSNT-8(2030) Test Board

IC Mount Area

(4) Board D

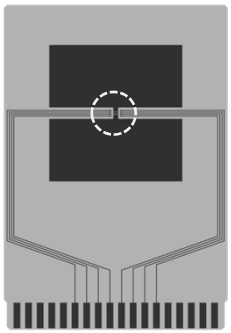




enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		-

(5) Board E



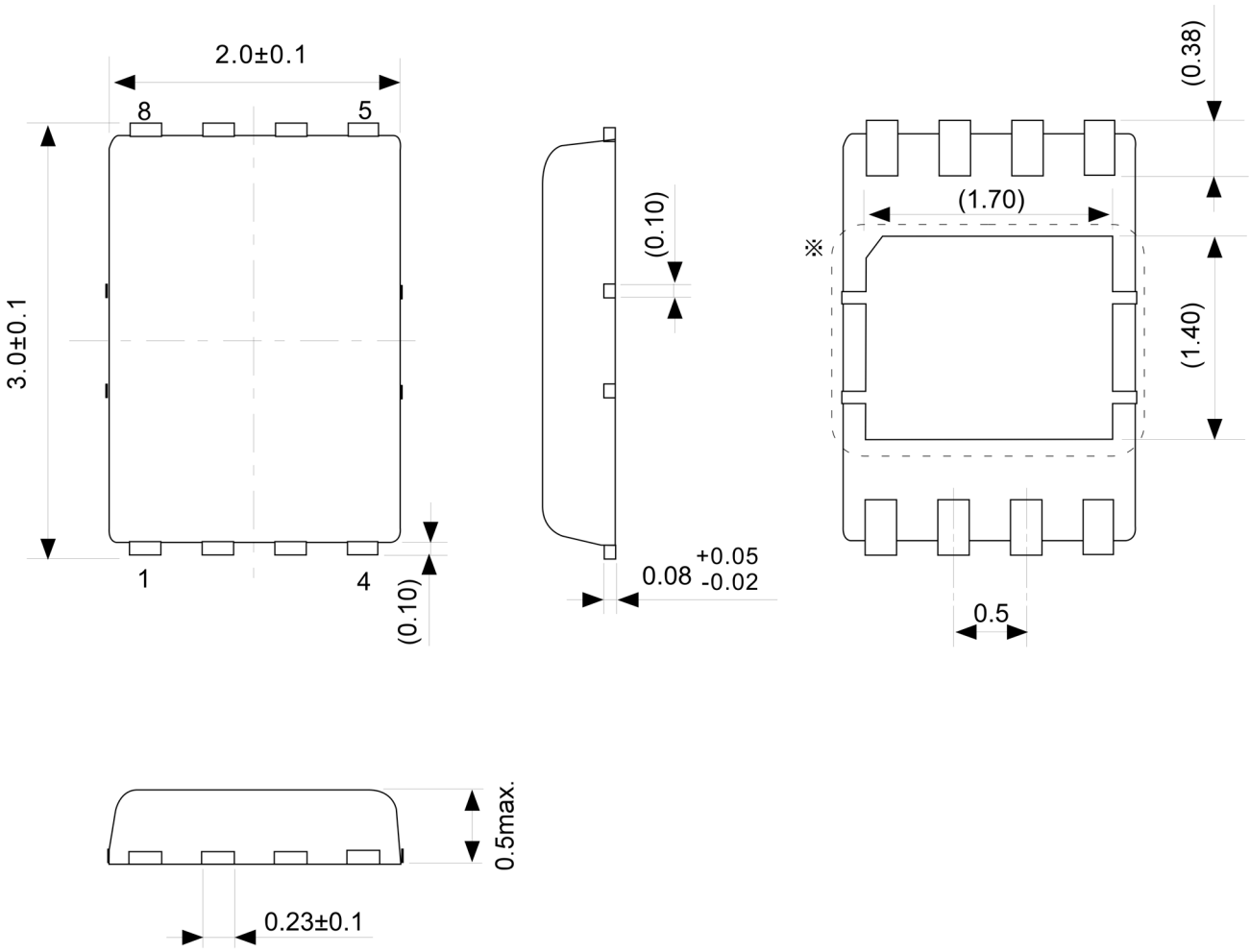


enlarged view

Item		Specification
Size [mm]		114.3 x 76.2 x t1.6
Material		FR-4
Number of copper foil layer		4
Copper foil layer [mm]	1	Pattern for heat radiation: 2000mm^2 t0.070
	2	74.2 x 74.2 x t0.035
	3	74.2 x 74.2 x t0.035
	4	74.2 x 74.2 x t0.070
Thermal via		Number: 4 Diameter: 0.3 mm

No. HSNT8-A-Board-SD-2.0

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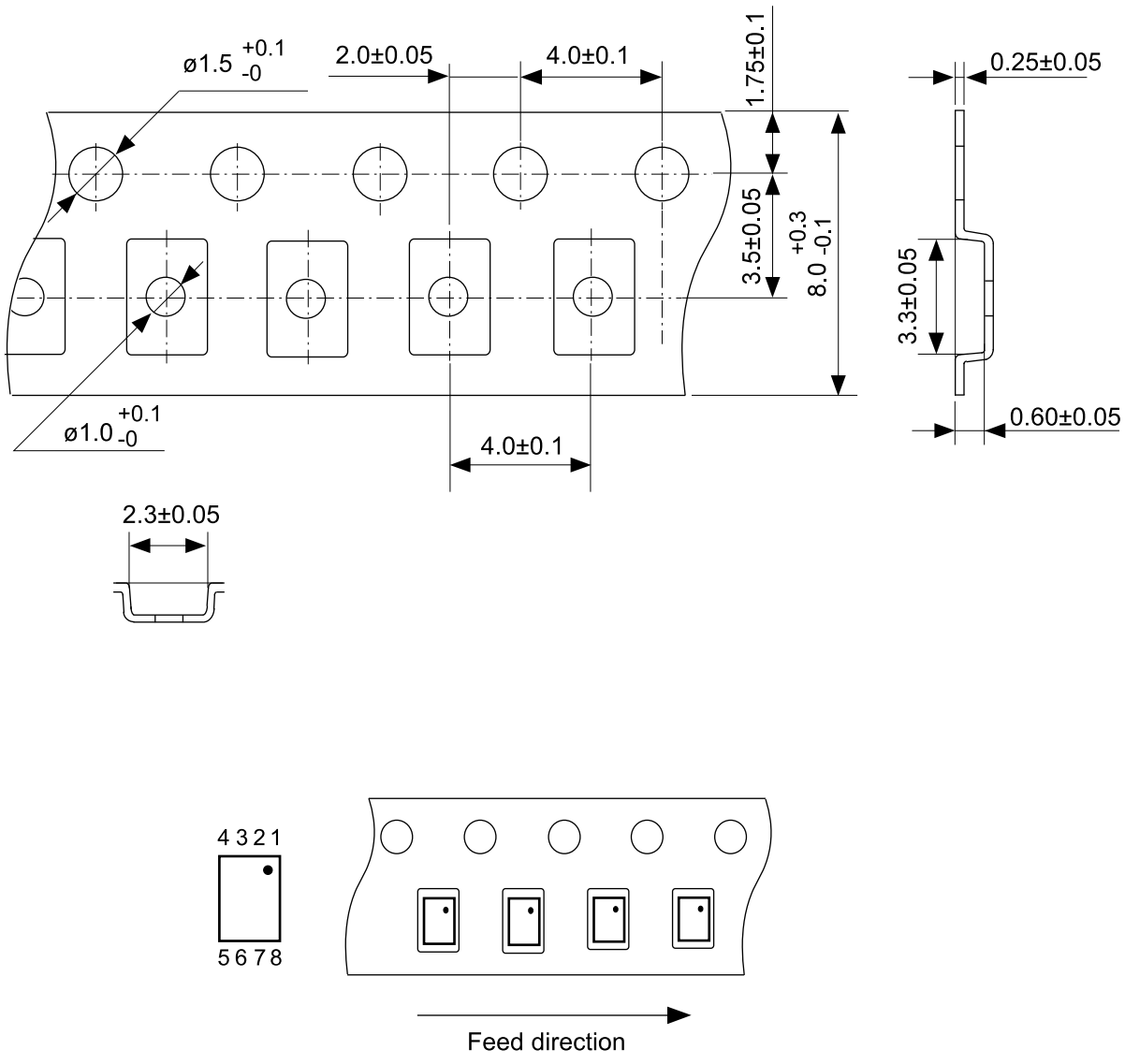


※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PP008-A-P-SD-2.0

TITLE	HSNT-8-A-PKG Dimensions
No.	PP008-A-P-SD-2.0
ANGLE	
UNIT	mm
ABLIC Inc.	

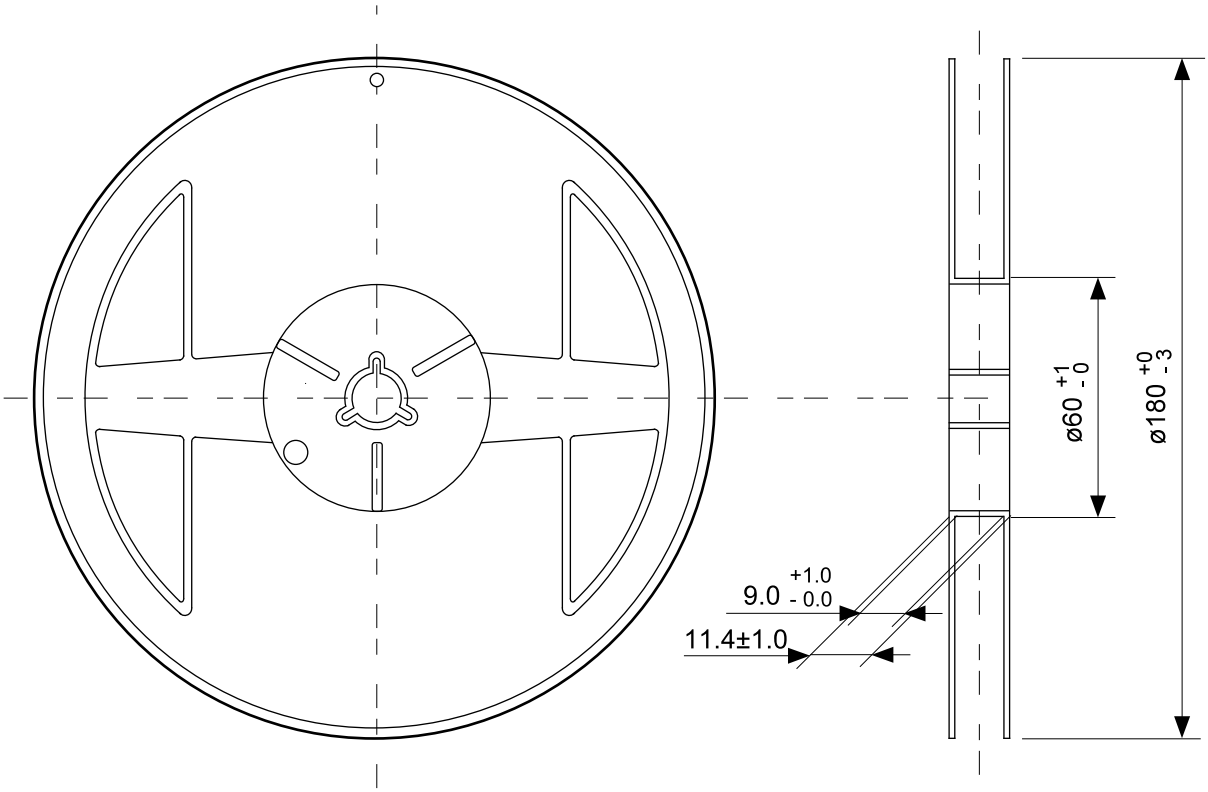
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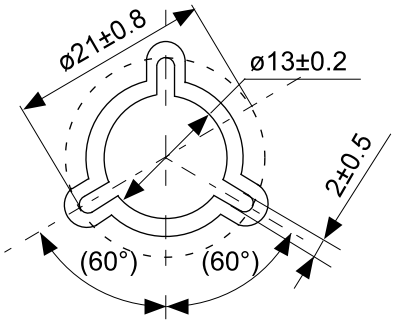
No. PP008-A-C-SD-1.0

TITLE	HSNT-8-A-Carrier Tape
No.	PP008-A-C-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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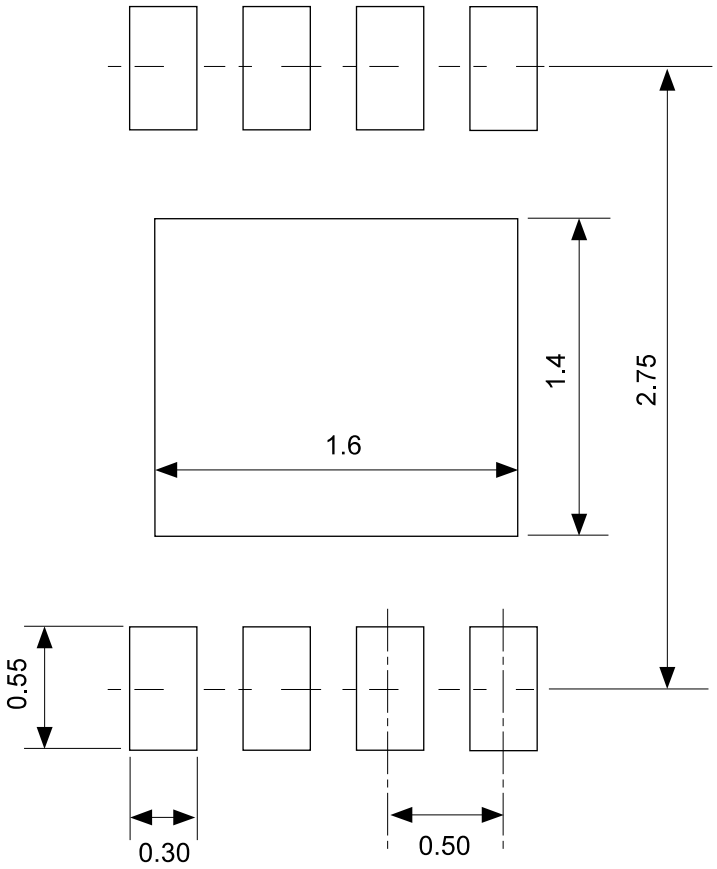
Enlarged drawing in the central part



No. PP008-A-R-SD-2.0

TITLE	HSNT-8-A-Reel		
No.	PP008-A-R-SD-2.0		
ANGLE		QTY.	5,000
UNIT	mm		
ABLIC Inc.			

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No. PP008-A-L-SD-1.0

TITLE	HSNT-8-A -Land Recommendation
No.	PP008-A-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

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