

CAS120M12BM2

1200 V, 120 A All-Silicon Carbide
High Performance, Switching Optimized, Half-Bridge Module

V_{DS}	1200 V
I_{DS}	120 A

Technical Features

- Industry Standard 62 mm Footprint
- Ultra-Low Loss, High-Frequency Operation
- Zero Reverse Recovery from Diodes
- Zero Turn-off Tail Current from MOSFET
- Normally-off, Fail-safe Device Operation
- Copper Baseplate and Aluminum Nitride Insulator



Applications

- Railway & Traction
- Solar & Renewable Energy
- EV Charging
- Industrial Automation & Testing

System Benefits

- Fast Time-to-Market with Minimal Development Required for Transition from 62 mm IGBT Packages
- Increased System Efficiency, due to Low Switching & Conduction Losses of SiC

Key Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Voltage	V _{DS}			1200	V	T _C = 25 °C	
Gate-Source Voltage, Maximum Value	V _{GS(max)}	-10		+25		Transient	Note 1 Fig. 33
Gate-Source Voltage, Recommended	V _{GS(op)}		-5/+20			Static	
DC Continuous Drain Current	I _D		200		A	V _{GS} = 20 V, T _C = 25 °C, T _{VJ} ≤ 150 °C	Notes 2, 3 Fig. 21
			144			V _{GS} = 20 V, T _C = 90 °C, T _{VJ} ≤ 150 °C	
DC Source-Drain Current (Schottky Diode)	I _{SD(SD)}		460			V _{GS} = -5 V, T _C = 25 °C, T _{VJ} ≤ 150 °C	
Pulsed Drain-Source Current	I _{DM}		480			t _{pmax} limited by T _{VJmax} V _{GS} = 20 V, T _C = 25 °C	
Power Dissipation	P _D		1000		W	T _C = 25 °C, T _{VJ} ≤ 150 °C	Note 4 Fig. 21
Virtual Junction Temperature	T _{VJ(op)}	-40		150	°C	Operation	

Note (1): Recommended turn-on gate voltage is 20 V with ±5 % regulation tolerance

Note (2): Current limit at T_C = 90 °C calculated by I_{D(max)} = $\sqrt{(P_D/R_{DS(typ)})(T_{VJ(max)}, I_{D(max)})}$

Note (3): Verified by design

Note (4): P_D = (T_{VJ} - T_C)/R_{TH(JC,typ)}


MOSFET Characteristics (Per Position) ($T_{VJ} = 25^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	1200			V	$V_{GS} = 0\text{ V}, T_{VJ} = -40^\circ\text{C}$	
Gate Threshold Voltage	$V_{GS(\text{th})}$	1.8	2.6			$V_{DS} = V_{GS}, I_D = 6\text{ mA}$	
Zero Gate Voltage Drain Current	I_{DSS}		450	3000	μA	$V_{GS} = 0\text{ V}, V_{DS} = 1200\text{ V}$	
Gate-Source Leakage Current	I_{GSS}			1.5		$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	
Drain-Source On-State Resistance (Devices Only)	$R_{DS(\text{on})}$		13.0	16.0	$\text{m}\Omega$	$V_{GS} = 20\text{ V}, I_D = 120\text{ A}$	Fig. 2 Fig. 3
			23.0			$V_{GS} = 20\text{ V}, I_D = 120\text{ A}, T_{VJ} = 150^\circ\text{C}$	
Transconductance	g_{fs}		57.4		S	$V_{DS} = 20\text{ V}, I_{DS} = 120\text{ A}$	Fig. 4
			54.4			$V_{DS} = 20\text{ V}, I_{DS} = 120\text{ A}, T_{VJ} = 150^\circ\text{C}$	
Turn-On Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$	E_{ON}		1.39 1.24 1.19		mJ	$V_{DS} = 600\text{ V},$ $I_D = 120\text{ A},$ $V_{GS} = -5\text{ V}/+20\text{ V},$ $R_{G(\text{ext})} = 2.5\text{ }\Omega,$ $L = 22.5\text{ }\mu\text{H}$	Fig. 11 Fig. 13
Turn-Off Switching Energy, $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$	E_{OFF}		0.86 0.84 0.85				
Internal Gate Resistance	$R_{G(\text{int})}$		1.8		Ω	$V_{AC} = 25\text{ mV}, f = 100\text{ kHz}$	
Input Capacitance	C_{iss}		6.47		nF	$V_{GS} = 0\text{ V}, V_{DS} = 800\text{ V},$ $V_{AC} = 25\text{ mV}, f = 200\text{ kHz}$	Fig. 9
Output Capacitance	C_{oss}		0.98				
Reverse Transfer Capacitance	C_{rss}		43.8		pF		
Gate to Source Charge	Q_{GS}		97		nC	$V_{DS} = 800\text{ V}, V_{GS} = -5\text{ V}/+20\text{ V}$ $I_D = 120\text{ A}$ Per IEC60747-8-4 pg 21	
Gate to Drain Charge	Q_{GD}		118				
Total Gate Charge	Q_G		378				
FET Thermal Resistance, Junction to Case	$R_{th\text{JC}}$		0.125	0.135	$^\circ\text{C}/\text{W}$		Fig. 17

Diode Characteristics (Per Position) ($T_{VJ} = 25^\circ\text{C}$ Unless Otherwise Specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions	Note
Diode Forward Voltage	V_F		1.53		V	$V_{GS} = -5\text{ V}, I_F = 120\text{ A}, T_{VJ} = 25^\circ\text{C}$	Fig. 7
			1.92			$V_{GS} = -5\text{ V}, I_F = 120\text{ A}, T_{VJ} = 150^\circ\text{C}$	
Reverse Recovery Time	t_{RR}		21		ns	$V_{GS} = -5\text{ V}, I_{SD} = 120\text{ A}, V_R = 600\text{ V}$ $di_F/dt = 12.5\text{ A/ns}, T_J = 150^\circ\text{C}$	Fig. 32
Reverse Recovery Charge	Q_{RR}		2.2				
Peak Reverse Recovery Current	I_{RRM}		173		A		
Diode Energy $T_{VJ} = 25^\circ\text{C}$ $T_{VJ} = 125^\circ\text{C}$ $T_{VJ} = 150^\circ\text{C}$	E_{rr}		0.75 0.86 0.89		mJ	$V_{DS} = 600\text{ V}, I_D = 120\text{ A},$ $V_{GS} = -5\text{ V}/+20\text{ V}, R_{G(\text{ext})} = 2.5\text{ }\Omega,$ $L = 22.5\text{ }\mu\text{H}$	Fig. 14 Note 5
Diode Thermal Resistance, Junction to Case	$R_{th\text{JC}}$		0.108	0.115			

Note (5): SiC Schottky diodes do not have reverse recovery energy but still contribute capacitive energy



Module Physical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Package Resistance, M1	R_{1-2}		0.60		$\mu\Omega$	$T_c = 125^\circ\text{C}$, Note: 6
Package Resistance, M2	R_{2-3}		0.51			$T_c = 125^\circ\text{C}$, Note: 6
Stray Inductance	L_{Stray}		12.9		nH	Between Terminals 1 and 3
Case Temperature	T_c	-40		125	$^\circ\text{C}$	
Weight	W		290		g	
Mounting Torque	M_s	4	5	5.5	N-m	Baseplate, M6-1.0 Bolts
		4	5	5.5		Power Terminals, M6-1.0 Bolts
Case Isolation Voltage	V_{isol}	5			kV	AC, 50 Hz, 1 min
Clearance Distance		9			mm	Terminal to Terminal
		30				Terminal to Baseplate
Creepage Distance		30				Terminal to Terminal
		40				Terminal to Baseplate

Note (6): Total Effective Resistance (Per Switch Position) = MOSFET $R_{\text{DS(on)}}$ + Switch Position Package Resistance

Typical Performance

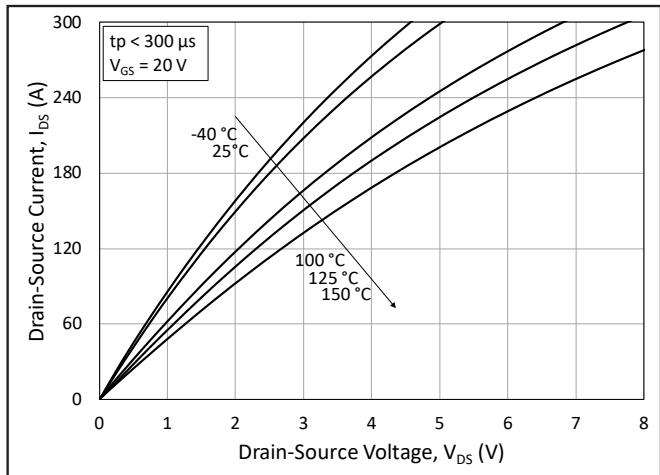


Figure 1. Output Characteristics for Various Junction Temperatures

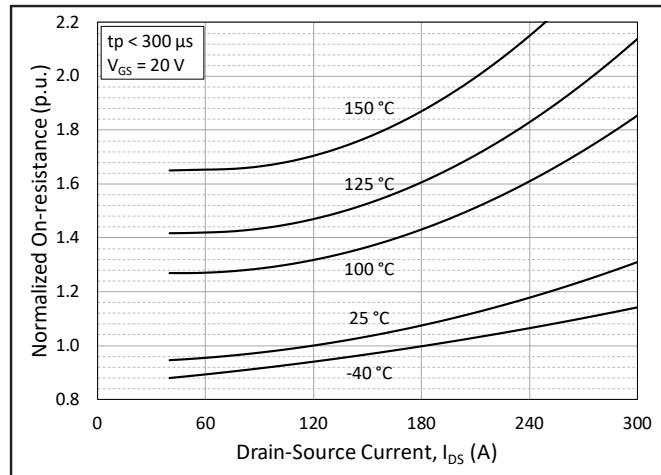


Figure 2. Normalized On-State Resistance vs. Drain Current for Various Junction Temperatures

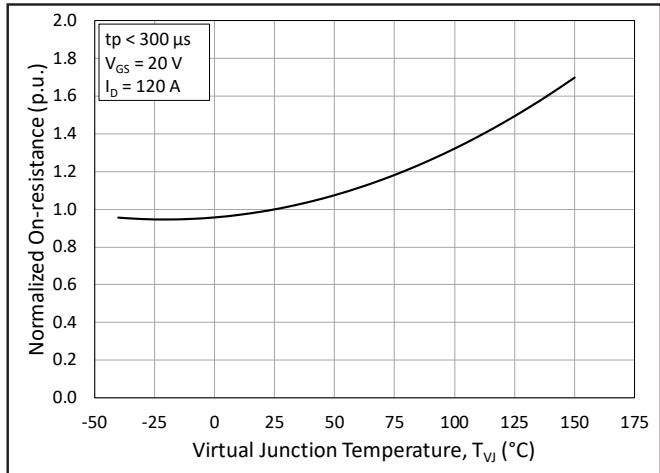


Figure 3. Normalized On-State Resistance vs. Junction Temperature

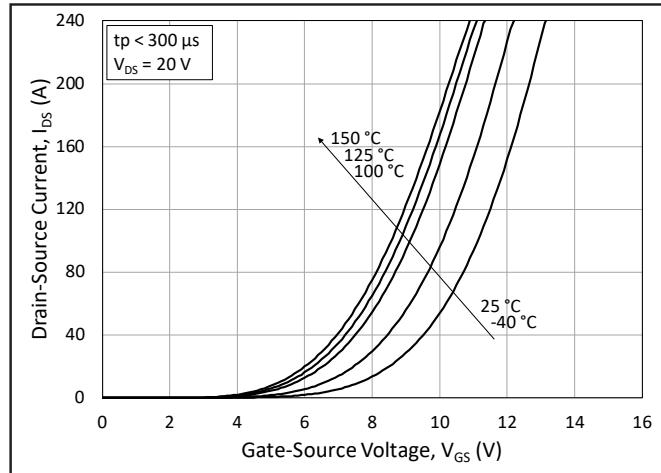


Figure 4. Transfer Characteristic for Various Junction Temperatures

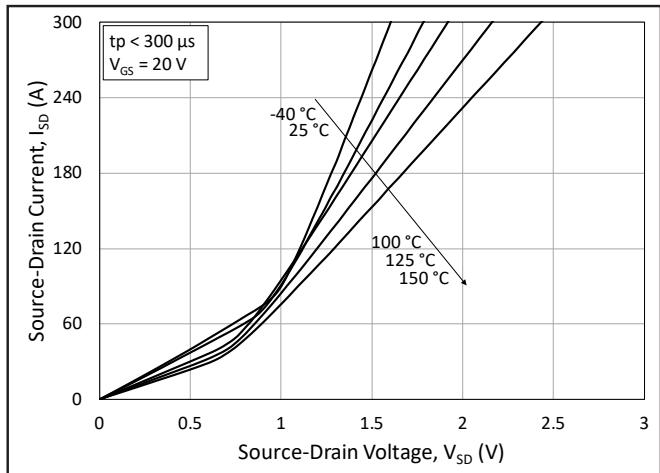


Figure 5. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 20$ V (Note: 2)

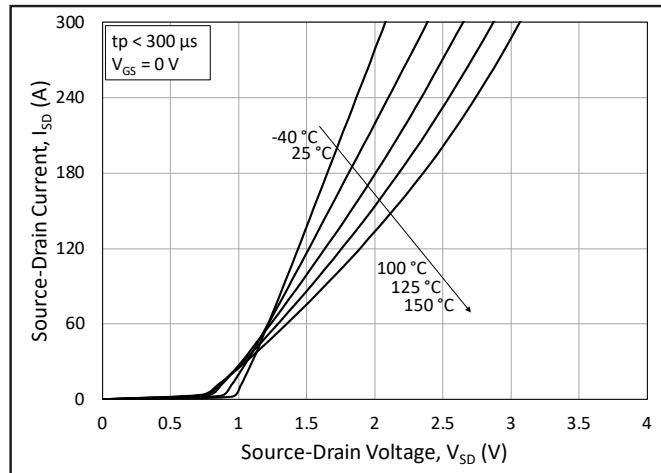


Figure 6. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = 0$ V (Diode) (Note: 2)

Typical Performance

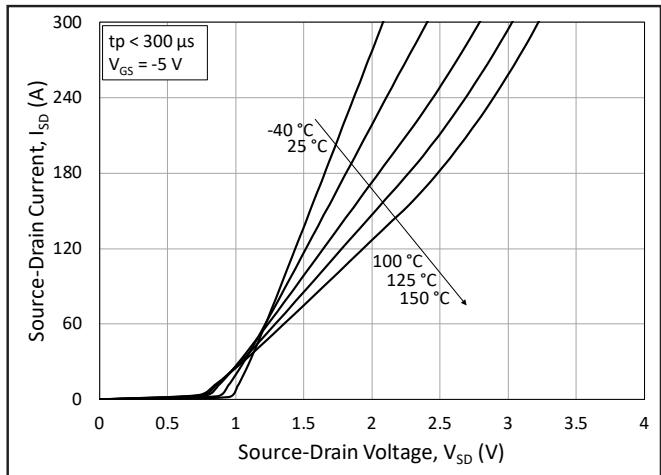


Figure 7. 3rd Quadrant Characteristic vs. Junction Temperatures at $V_{GS} = -5$ V (Diode) (Note: 2)

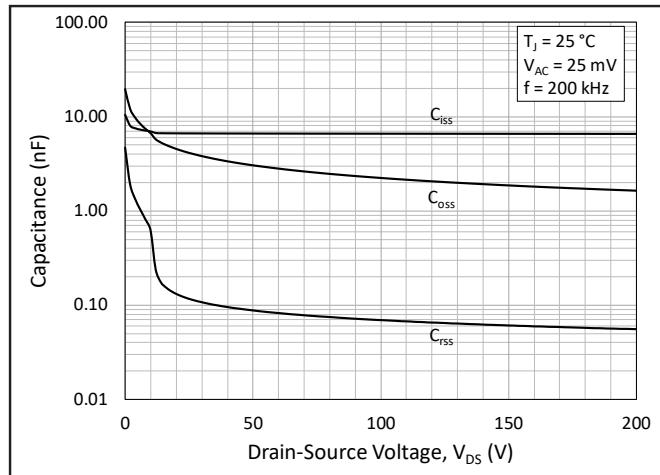


Figure 8. Typical Capacitances vs. Drain to Source Voltage (0 - 200 V)

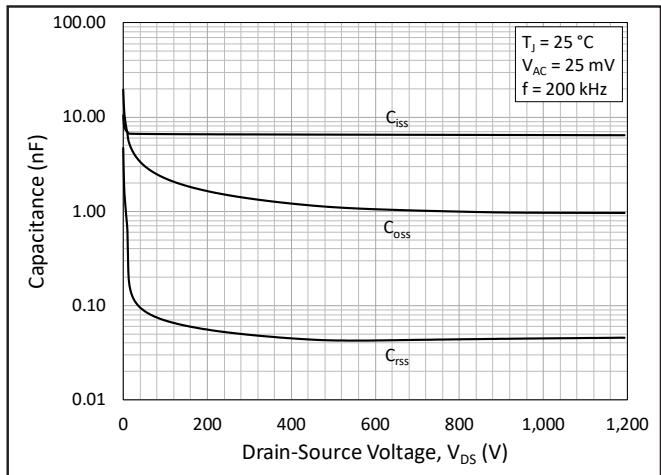


Figure 9. Typical Capacitances vs. Drain to Source Voltage (0 - 1200 V)

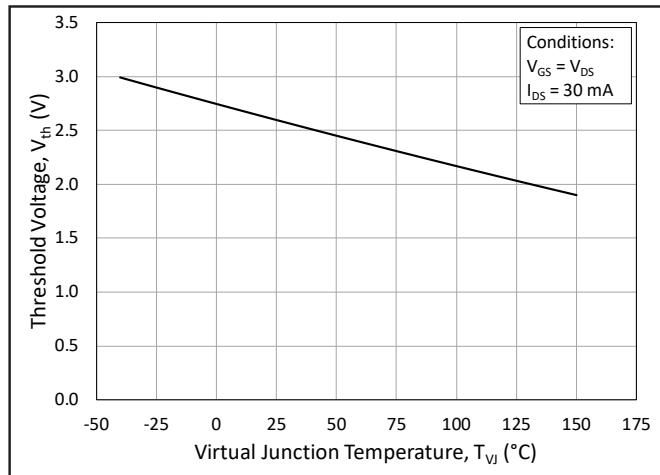


Figure 10. Threshold Voltage vs. Junction Temperature

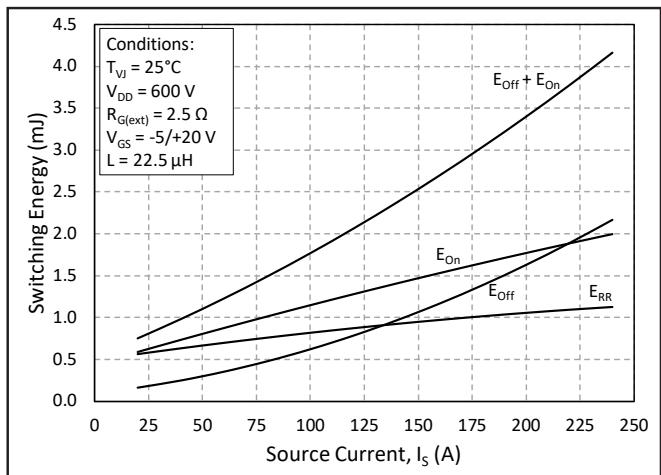


Figure 11. Switching Energy vs. Drain Current ($V_{DS} = 600$ V)

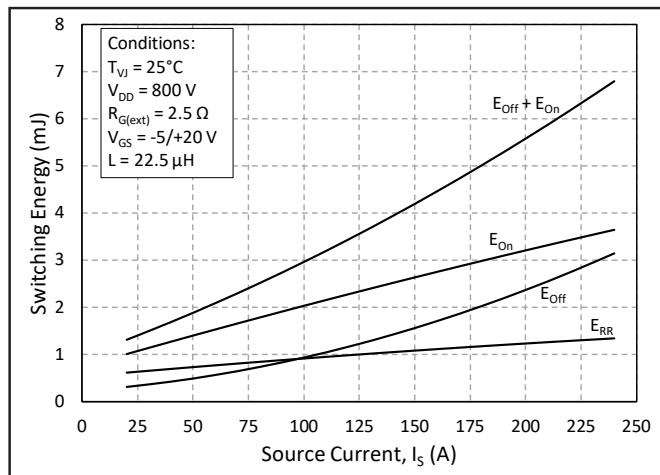


Figure 12. Switching Energy vs. Drain Current ($V_{DS} = 800$ V)

Typical Performance

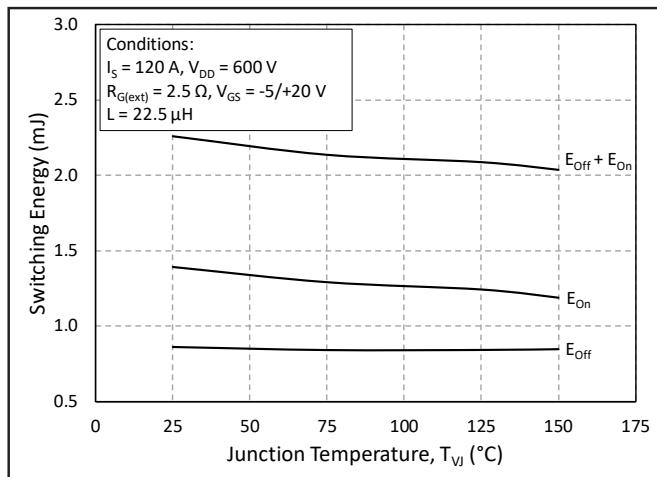


Figure 13. MOSFET Switching Energy vs. Junction Temperature

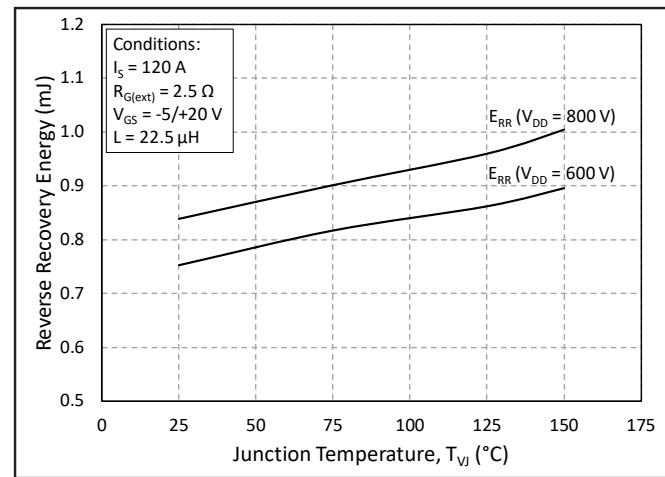


Figure 14. Reverse Recovery Energy vs. Junction Temperature (Note: 2)

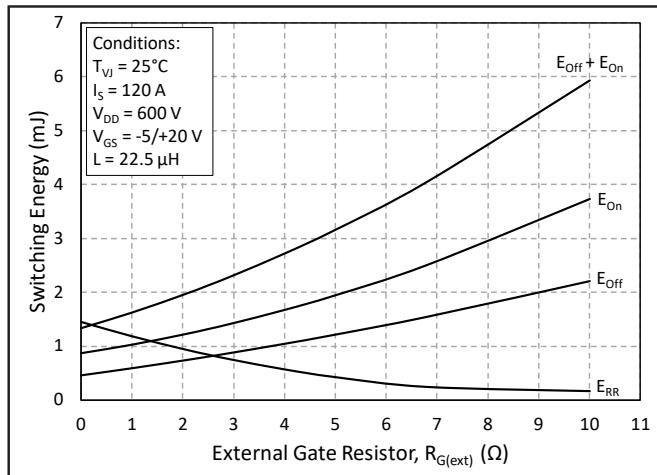


Figure 15. MOSFET Switching Energy vs. External Gate Resistance

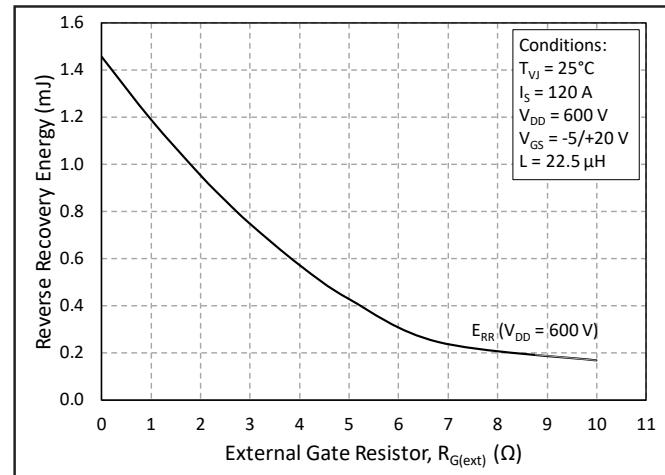


Figure 16. Reserve Recovery Energy vs. External Gate Resistance (Note: 2)

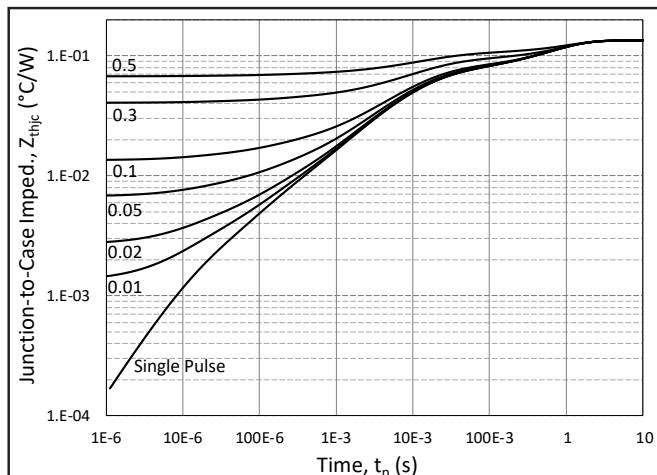


Figure 17. MOSFET Junction to Case Transient Thermal Impedance, Z_{thJC} (°C/W)

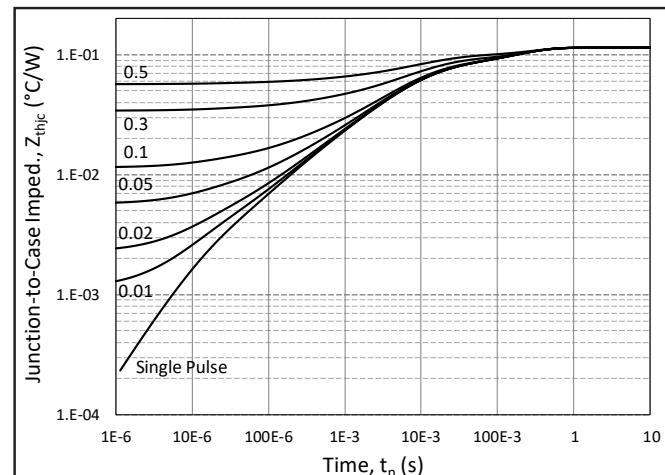


Figure 18. Diode Junction to Case Transient Thermal Impedance, Z_{thJC} (°C/W)

Typical Performance

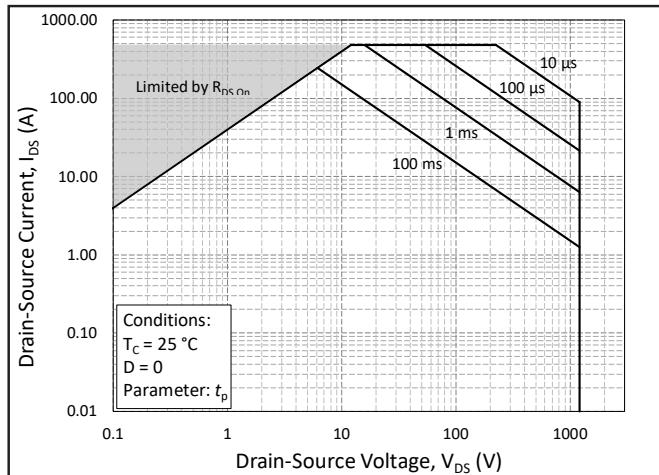


Figure 19. Forward Bias Safe Operating Area (FBSOA)

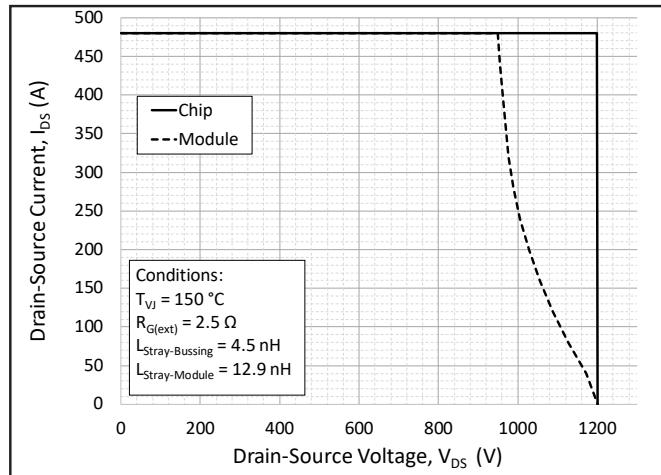


Figure 20. Reverse Bias Safe Operating Area (RBSOA)

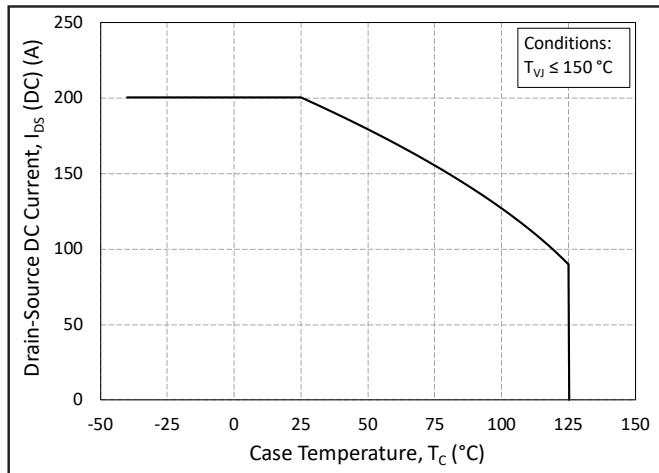


Figure 21. Continuous Drain Current Derating vs. Case Temperature

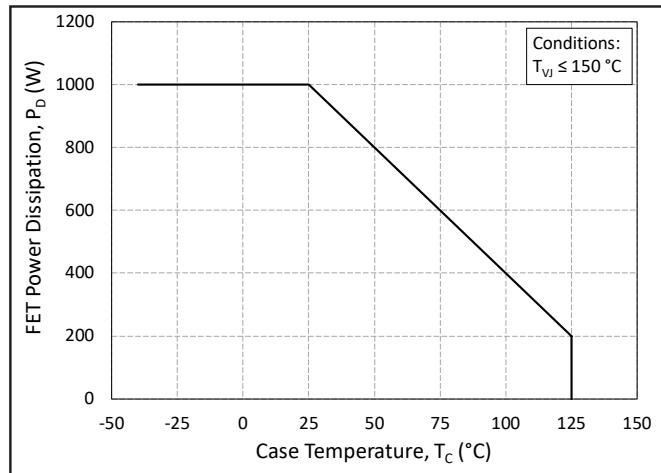


Figure 22. Maximum Power Dissipation Derating vs. Case Temperature

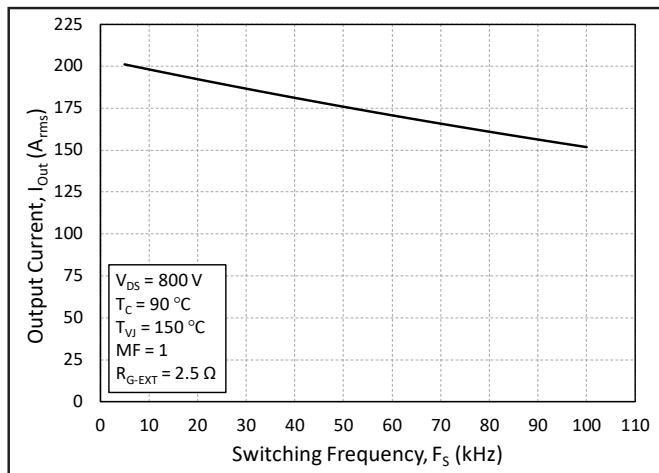
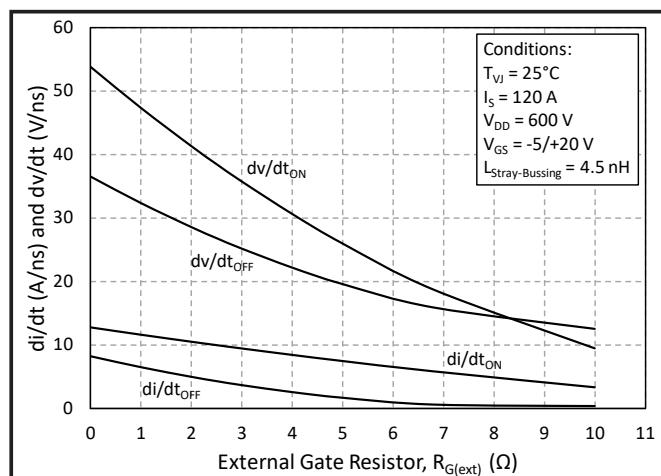
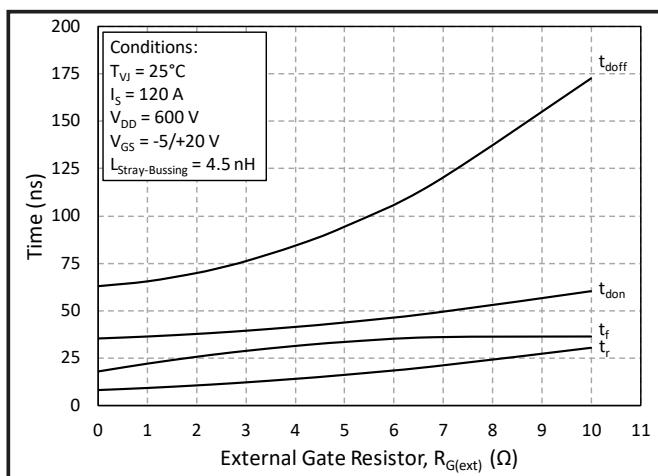
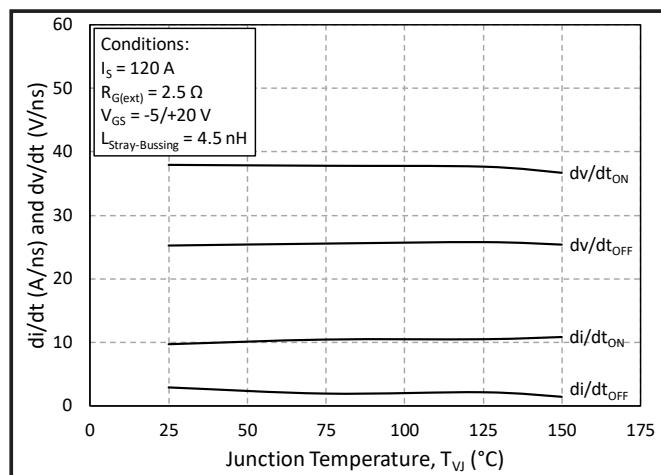
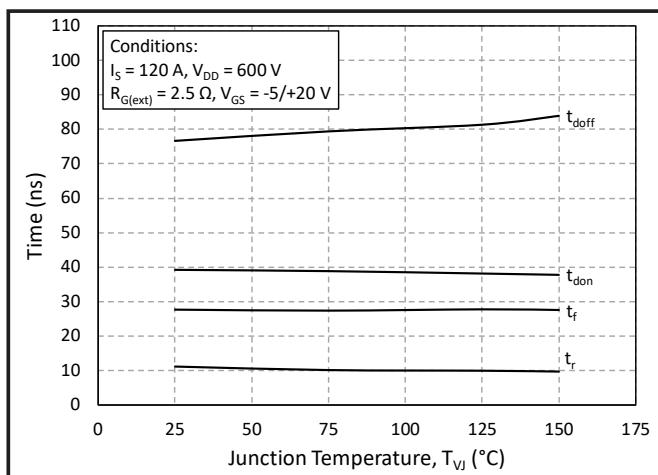
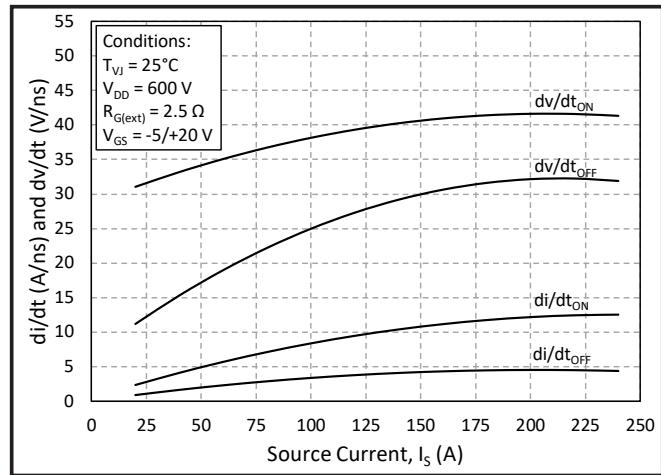
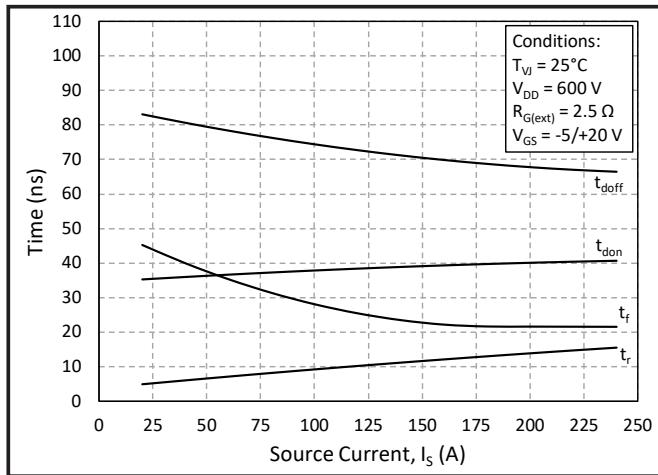


Figure 23. Typical Output Current Capability vs. Switching Frequency (Inverter Application)

Timing Characteristics



Definitions

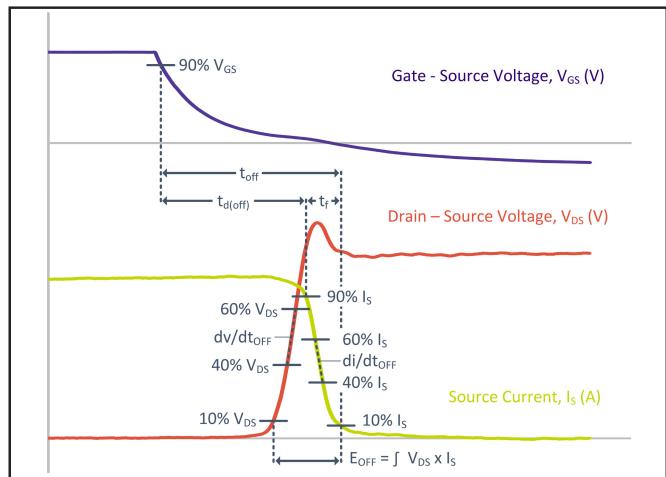


Figure 30. Turn-Off Transient Definitions

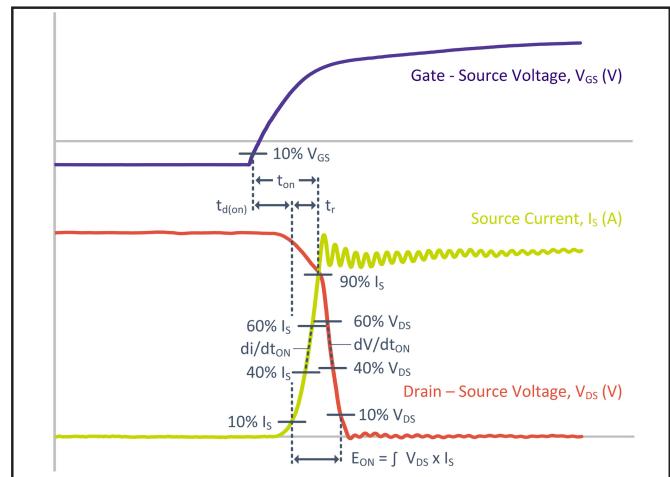


Figure 31. Turn-On Transient Definitions

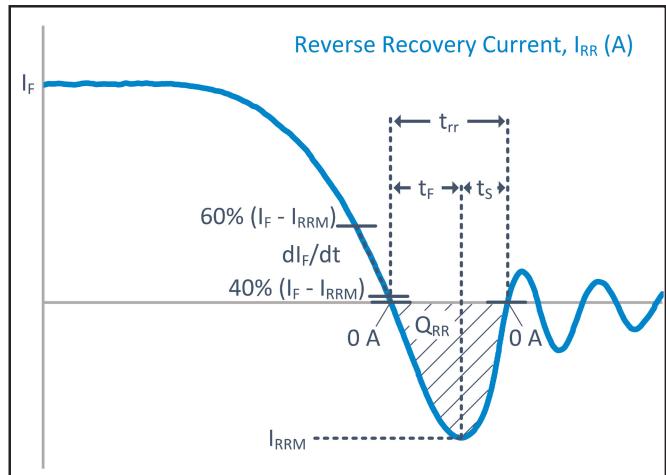


Figure 32. Reverse Recovery Definitions (Note 2)

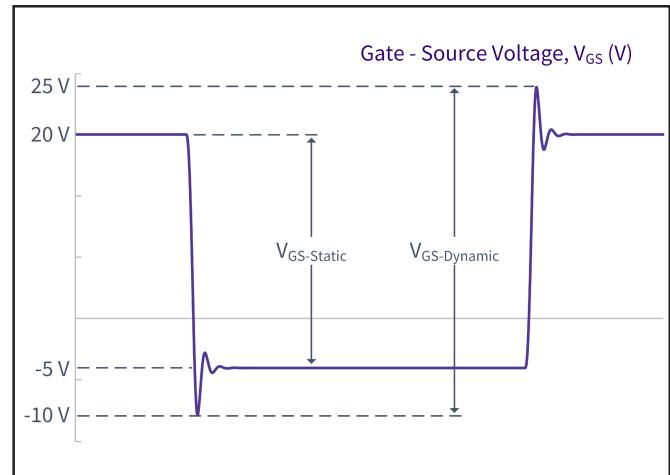
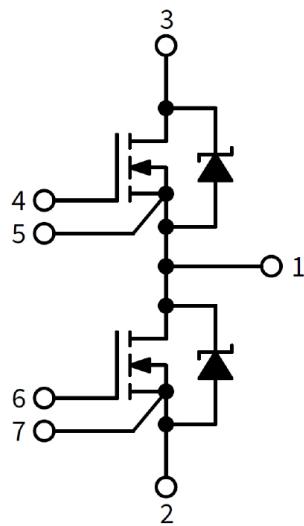


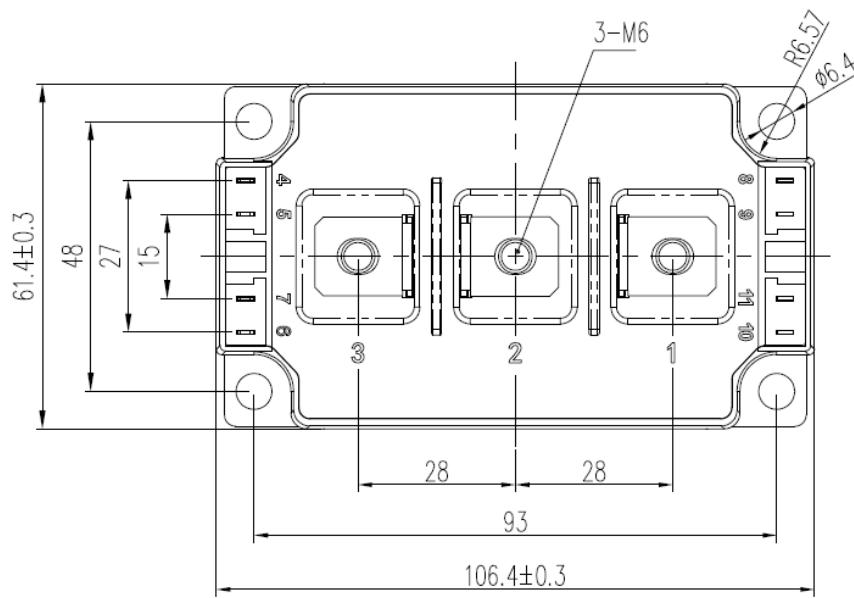
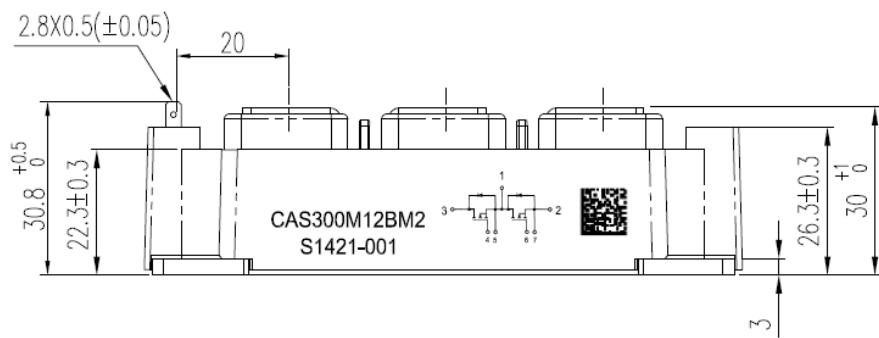
Figure 33. V_{GS} Transient Definitions



Schematic and Pin Out



Package Dimensions (mm)





Supporting Links & Tools

- [CGD1200HB2P-BM2 Evaluation Gate Driver](#)
- [CGD12HB00D: Differential Transceiver Board](#)
- [KIT-CRD-CIL12N-BM: Dynamic Performance Evaluation Board for the BM2 and BM3 Module](#)



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