# Lattice Avant Platform - Overview

# Data Sheet

FPGA-DS-02107-1.5

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| DDR | Double Data Rate |
| DDRPHY | DDR Physical Layer |
| DLLDEL | DLL Delay |
| DSP | Digital Signal Processing |
| EBR | Embedded Block RAM |
| ECC | Error Correction Coding |
| ECLK | Edge Clock |
| FIFO | First In First Out |
| GCLK | Global Clock |
| LPDDR | Low Power DDR |
| LUT | Look Up Table |
| LVCMOS | Low-Voltage Complementary Metal Oxide Semiconductor Interface Signaling |
| LVDS | Low-Voltage Differential Signaling |
| MPPCS | Multi-Protocol PCS |
| MPPHY | Multi-Protocol PHY |
| PCIe | Peripheral Component Interconnect Express |
| PCS | Physical Coding Sublayer |
| PCLK | Primary Clock |
| PDP | Pseudo Dual Port |
| PFU | Programmable Functional Unit |
| PIC | Programmable I/O Cells |
| PIO | Programmable I/O |
| PLL | Phase Locked Loops |
| RCLK | Regional Clock |
| SEU | Single Event Upset |
| SLC | System Logic Cell |
| SLVS | Scalable Low-Voltage Signaling |
| SP | Single Port |
| SPI | Serial Peripheral Interface |
| SRAM | Static Random-Access Memory |

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# 1. General Description

Lattice Avant™ is a low-power mid-range density FPGA platform optimized for a wide range of applications across multiple markets – optimized for edge computing workloads requiring large memories and DSP resources and delivering a variety of high bandwidth interfaces ideal for video processing, communications, and machine learning inferencing. A platform is built upon a programmable FPGA fabric optimized for a specific range of logic densities coupled with a collection of features that are assembled into unique device families utilizing varying amounts of features and I/O. The Lattice Avant platform enables logic capacities up to 637k System Logic Cells and capable of delivering up to 25 Gbps multi-protocol SERDES, hardened PCIe Gen4, DDR5, and DDR4/LPDDR4 memory interfaces, advanced security, and packages as small as
11 × 9 mm. This datasheet describes features which are part of the entire Lattice Avant FPGA platform. The Lattice Avant platform delivers best-in-class power efficiency while meeting performance requirements for a wide range of applications. The following families are available in the Lattice Avant Platform.

- **Lattice Avant-AT-E** family, is a family optimized for edge compute workloads. Featuring fast and flexible I/O (with support for 3.3 V I/O), it provides connectivity to external DRAM memory and fast differential interfaces.
- **Lattice Avant-AT-G** family is a general-purpose FPGA. In addition to Lattice Avant-AT-E capabilities, it features 12.5G SERDES supporting multiple popular protocols including 10G Ethernet and PCIe Gen3.
- **Lattice Avant-AT-X** family supports faster serial interfaces. In addition to Lattice Avant-AT-G device capabilities, it features 25G SERDES supporting up to PCIe Gen4 and 25G Ethernet, as well as DDR5 memories and advanced user security features.

Lattice Avant platform-based devices are supported by the Lattice Radiant™ integrated design software environment. Synthesis library support for Lattice Avant devices is available for popular logic synthesis tools. Radiant uses synthesis tool output along with constraints from its floor planning tools to place and route the user design in Lattice Avant devices. The tool extracts timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for Lattice Avant families. By using these configurable soft IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing productivity.

## 1.1. Specification Status for Avant Devices

For the status of specific Avant platform devices, refer to the Specification Status for Avant Devices table in the Lattice Avant Platform Specification Data Sheet (FPGA-DS-02112).

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## 1.2. Features

Table 1.1 shows the key features of the Lattice Avant platform.

**Table 1.1. Lattice Avant Platform Key Features**

| Programmable Architecture | System Performance |
|---|---|
| • 262k to 637k system logic cells<br>• 700 to 1800 multipliers (18 × 18) in sysDSP™ blocks<br>• 14.4 to 35.6 Mb of embedded memory (EBR)<br>• Smallest package size 9 × 11 mm | • Improved low power performance<br>• Timing closure for a typical design of up to 350 MHz<br>• EBR/DSP/Clocks up to 625 MHz<br>• Available in Commercial, Industrial, Automotive, and Defense temperature grades<br>• Defense grade[2]<br>  • Tested across the full temperature range (–55 °C to +125 °C Tj)<br>  • Normal operation and timing parameters at -40 °C to +125 °C Tj |
| **External Memory Interface Support** | **SERDES** |
| • DDR5 up to 2100 Mbps data rate[1]<br>• DDR4/LPDDR4 up to 2400 Mbps data rate<br>• Hardened DFI (DDR PHY Interface) training layer | • 25 Gbps SERDES and hardened PCIe Gen 1/2/3/4<br>• 4-28 SERDES Channels |
| **Device Security** | **High-speed and Flexible Programmable I/O** |
| • AES256-GCM encryption<br>• Up to ECC521 and RSA4096 authentication<br>• Anti-tamper and PUF/Unique ID<br>• User data encryption<br>• Side channel resistance<br>• TRNG (True Random Number Generator) | • 200 to 572 programmable sysI/O - High Performance (HP) and Wide Range (WR)<br>• 1.8 Gbps per lane MIPI DPHY<br>• 1.6 Gbps LVDS<br>• 3.3 V support |

**Notes:**

1. While the Lattice Avant HPIO can support DDR5 up to 2400 Mbps, Lattice Avant has defined DDR5 operation only up to 2100 Mbps. DDR5 operational ranges defined by JEDEC are up to 2100 Mbps and >2933 Mbps.
2. Contact Lattice Sales for more information.

**Table 1.2. Lattice Avant Families**

| Name | | Avant-AT-E | Avant-AT-G | Avant-AT-X |
|---|---|---|---|---|
| **Features** | | | | |
| **Fabric** | **LCs, DSP, EBR** | Yes | Yes | Yes |
| **Protocol** | **Max Speed** | — | 12.5 Gbps[1] | 25 Gbps[1] |
| | **PCIe Gen 1/2/3** | — | 2.5 Gbps, 5 Gbps, 8 Gbps | 2.5 Gbps, 5 Gbps, 8 Gbps |
| | **PCIe Gen 4** | — | — | 16G[1] |
| | **Ethernet to 10G** | — | Yes[1] | Yes[1] |
| | **Ethernet to 25G** | — | — | Yes[1] |
| **Memory** | **LPDDR4/DDR4[3]** | Yes | Yes | Yes |
| | **DDR5** | — | — | Yes |
| **Security** | **Bitstream Security** | Yes[2] | Yes | Yes |
| | **User Mode Security** | — | — | Yes |
| | **Anti-Tamper Module** | — | — | Yes |
| **Other** | **Soft Error Detection/Soft Error Correction** | Yes[2] | Yes | Yes |
| | **JTAG, x1/x2/x4 SPI Config** | Yes | Yes | Yes |
| | **xSPI Config** | Yes[2] | Yes | Yes |

**Notes:**

1. Protocol Performance speeds met with –3 speed grade and LFG package. Other speed grades and packages are limited to 10G.

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2. Not supported in E70B or E30B variants.
3. DDR4 is not supported in E70B or E30B variants.

**Table 1.3. Lattice Avant-AT-E Family Selection Guide**

| Device | E30 | E50 | E70 |
|---|---|---|---|
| System Logic Cells (k) | 262 | 409 | 637 |
| LUTs (k) | 163 | 255 | 397 |
| Embedded Memory (EBR) Blocks (36 kb) | 400 | 630 | 990 |
| Embedded Memory (Mb) | 14.4 | 22.7 | 35.6 |
| Distributed RAM Bits (kb) | 1700 | 2660 | 4140 |
| DSP (18 × 18 Multipliers) | 700 | 1120 | 1800 |
| High Frequency Oscillator | 1 | 1 | 1 |
| GPLL | 7 | 9 | 11 |
| **Packages (Type, Size, Ball Pitch)[1, 2]** | **Total I/O (WR – Wide Range, HP – High Performance)** | | |
| ASGA410 (FOWLP, 9 × 11 mm, 0.5 mm) | 247 (94, 153) | — | — |
| CSG841 (FCCSP, 15 × 15 mm, 0.5 mm) | — | 553 (94, 459) | 553 (94, 459) |
| CBG484 (FCCSP, 18 × 18 mm, 0.8 mm) | 349 (94, 255) | 349 (94, 255) | 349 (94, 255) |
| LFG676 (FCBGA, 27 × 27 mm, 1.0 mm) | — | — | 297 (42, 255) |
| LFG1156 (FCBGA, 35 × 35 mm, 1.0 mm) | — | — | 553 (94, 459) |

**Notes:**
1. Refer to Ordering Information for more package details.
2. *B* variants only support limited package options. Refer to Ordering Information for more details.

**Table 1.4. Lattice Avant-AT-G Family Selection Guide**

| Device | G30 | G50 | G70 |
|---|---|---|---|
| System Logic Cells (k) | 262 | 409 | 637 |
| LUTs (k) | 163 | 255 | 397 |
| Embedded Memory (EBR) Blocks (36 kb) | 400 | 630 | 990 |
| Embedded Memory (Mb) | 14.4 | 22.7 | 35.6 |
| Distributed RAM Bits (kb) | 1700 | 2660 | 4140 |
| DSP (18 × 18 Multipliers) | 700 | 1120 | 1800 |
| High Frequency Oscillator | 1 | 1 | 1 |
| GPLL | 7 | 9 | 11 |
| **Packages (Type, Size, Ball Pitch)[1]** | **Total I/O (WR – Wide Range, HP – High Performance)<br>SERDES** | | |
| ASGA410 (FOWLP, 9 × 11 mm, 0.5 mm) | 196 (43, 153)<br>4 | — | — |
| FBG644 (FCBGA, 19 x 23 mm, 0.8 mm) | 298 (43, 255)<br>12 | 298 (43, 255)<br>12 | 298 (43, 255)<br>12 |
| LFG676 (FCBGA, 27 × 27 mm, 1.0 mm) | 298 (43, 255)<br>12 | 298 (43, 255)<br>16 | 298 (43, 255)<br>16 |
| LFG1156 (FCBGA, 35 × 35 mm, 1.0 mm) | — | — | 554 (95, 459)<br>28 |

**Note:**
1. Refer to Ordering Information for more package details.

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**Table 1.5. Lattice Avant-AT-X Family Selection Guide**

| Device | X30 | X50 | X70 |
|---|---|---|---|
| System Logic Cells (k) | 262 | 409 | 637 |
| LUTs (k) | 163 | 255 | 397 |
| Embedded Memory (EBR) Blocks (36 kb) | 400 | 630 | 990 |
| Embedded Memory (Mb) | 14.4 | 22.7 | 35.6 |
| Distributed RAM Bits (kb) | 1700 | 2660 | 4140 |
| DSP (18 × 18 Multipliers) | 700 | 1120 | 1800 |
| High Frequency Oscillator | 1 | 1 | 1 |
| GPLL | 7 | 9 | 11 |
| **Packages (Type, Size, Ball Pitch)[1]** | **Total I/O (WR – Wide Range, HP – High Performance)<br>SERDES** | | |
| ASGA410 (FOWLP, 9 × 11 mm, 0.5 mm) | 196 (43, 153)<br>4 | — | — |
| FBG644 (FCBGA, 19 x 23 mm, 0.8 mm) | 298 (43, 255)<br>12 | 298 (43, 255)<br>12 | 298 (43, 255)<br>12 |
| LFG676 (FCBGA, 27 × 27 mm, 1.0 mm) | 298 (43, 255)<br>12 | 298 (43, 255)<br>16 | 298 (43, 255)<br>16 |
| LFG1156 (FCBGA, 35 × 35 mm, 1.0 mm) | — | — | 554 (95, 459)<br>28 |

**Note:**

1. Refer to Ordering Information for more package details.

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# 2. Architecture

## 2.1. Overview

Each Lattice Avant device contains arrays of logic blocks, arranged into Clock Regions (CKR). Each CKR comprises blocks such as PFUs, EBRs, DSPs, and a Clock Network that clocks synchronous elements in the CKR. Each CKR is associated with an I/O resource. An I/O resource may be a group of high-speed SERDES I/O blocks, a High-Performance I/O (HPIO) bank or a Wide-Range I/O (WRIO) bank group. The Clock Regions are arranged in two rows and multiple columns depending on the density of the device and vary in size from 26k up to 35k system logic cells.

The top and bottom periphery of the device contain Programmable I/O Cells (PIC) and SERDES I/O blocks. Interspersed within the arrays are sysMEM™ Embedded Block RAM (EBR) blocks and sysDSP Digital Signal Processing blocks.

In addition, Lattice Avant devices provide various system level hard IP functional and interface blocks such as PCIe, Multiple Protocol PCS, and Security blocks. The PCIe hard IP supports PCIe Gen4. The Lattice Avant platform also provide security and tamper detection features to help protect user designs, and cryptographic functions to help secure user data. Lattice Avant devices deliver more robust reliability by offering enhanced frame based Soft Error Detection/ Soft Error Correction (SED/SEC) functions.

The sysMEM EBR blocks are large, dedicated 36 kb fast memory blocks with built-in ECC and FIFO support. Each sysMEM block can be configured to a single port, pseudo dual port, or true dual port memory in a variety of depths and widths as RAM or ROM. The DSP block supports a variety of multiplier and adder configurations, up to 54 × 54 MULT and 48-bit accumulator, which are the building blocks for complex signal processing capabilities.

The Lattice Avant device's sysI/O buffers contain two types of I/O blocks, Wide-Range and High-Performance I/O (WRIO and HPIO). The sysI/O buffers of the Lattice Avant devices are arranged in up to 15 banks allowing the implementation of a wide variety of I/O standards. The WRIO are in the top banks, providing flexible ranges of general purpose I/O configurations up to 3.3 V VCCIO. The banks located on the bottom side of the device are dedicated to High Performance (HP) interfaces such as LVDS, MIPI DPHY, DDR5, and DDR4/LPDDR4 supporting up to 1.8 V VCCIOs.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM, and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Lattice Avant delivers a much higher FPGA LC capacity and performance than previous Lattice product families and is optimized for increased routability and utilization performance. The Lattice Avant fabric is based on LUT4s, which minimize power consumption due to its area efficiency. The registers in the PFU and sysI/O blocks in Lattice Avant devices can be configured to be SET or RESET, allowing the device to power up in a known state for predictable system function.

Other blocks provided include PLLs, DLLs, and configuration functions. There is one PLL per HPIO bank and one PLL per WRIO bank group throughout the device. Lattice Avant devices also include Lattice Memory Mapped Interface (LMMI) which is a Lattice standard to support simple read and write dynamic control register operations for select internal IP.

Every device in the family has multiple configuration ports, including Controller SPI, Target SPI, and JTAG. This family also provides a High Frequency on-chip oscillator. The Lattice Avant devices use 0.82 V as their core voltage.

Figure 2.1 , Figure 2.2, and Figure 2.3 show the high-level device floorplan of LAV-AT-E/G/X30, LAV-AT-E/G/X50, and LAV-AT-E/G/X70, respectively.

The Lattice Avant-G and Avant-X families support SERDES.

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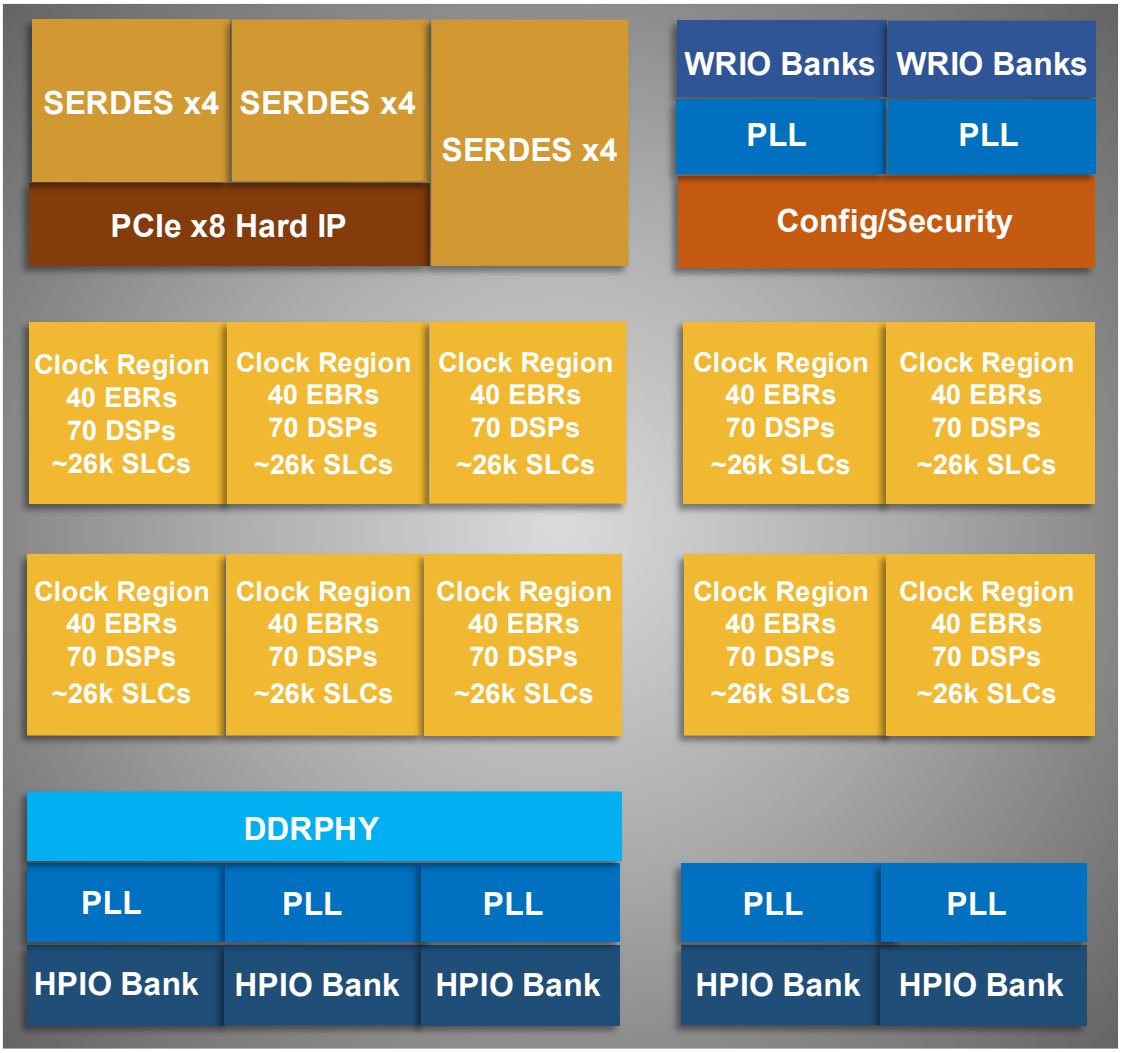


**Figure 2.1. High-level Device Floorplan (LAV-AT-E/G/X30 Device)**

**Note**: SERDES is supported in Avant-AT-G/X families.

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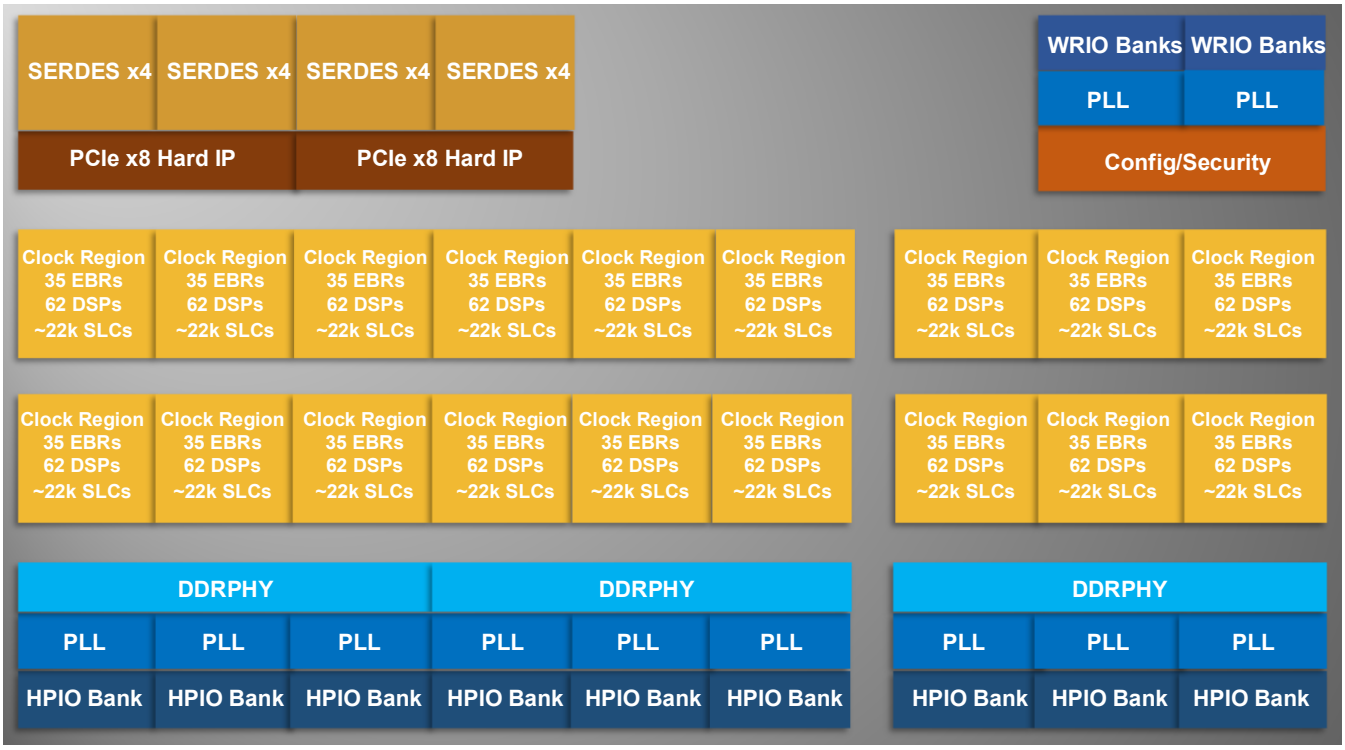


**Figure 2.2. High-level Device Floorplan (LAV-AT-E/G/X50 Device)**

**Note**: SERDES is supported in Avant-AT-G/X families.

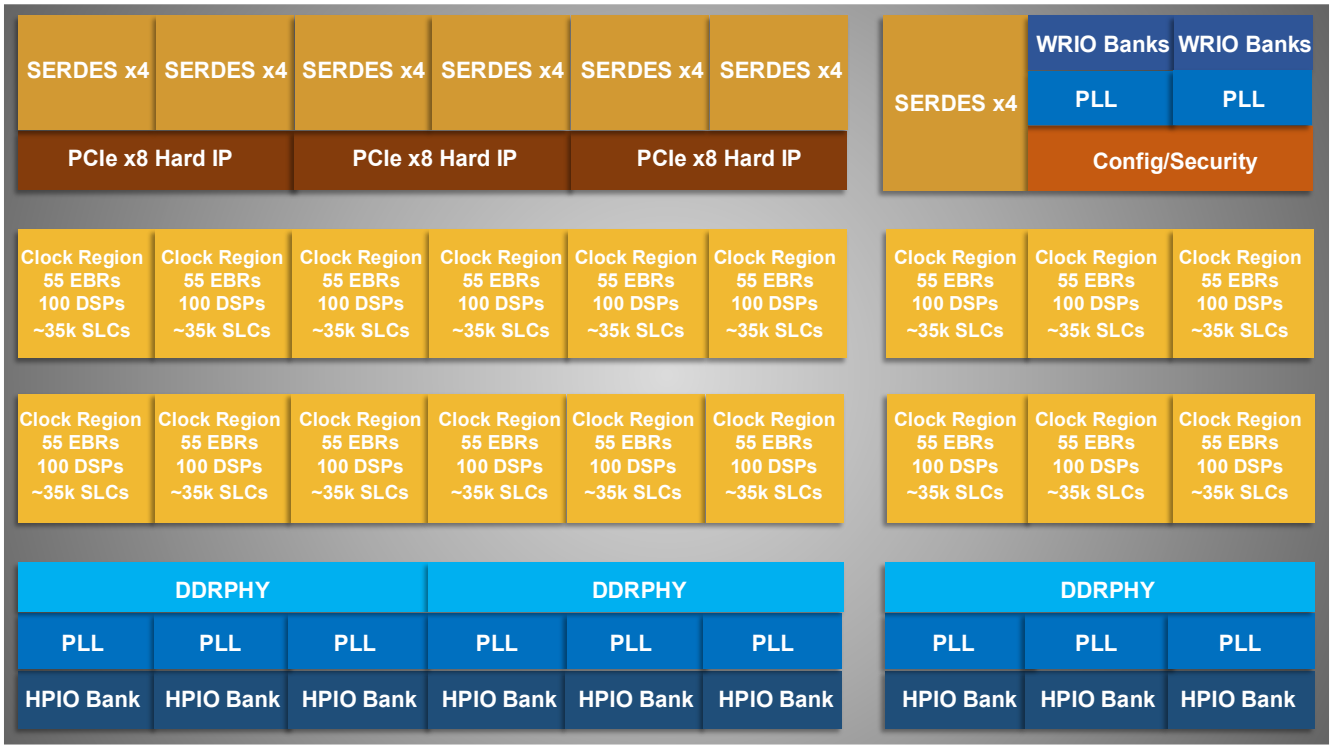


**Figure 2.3. High-level Device Floorplan (LAV-AT-E/G/X70 Device)**

**Note**: SERDES is supported in Avant-AT-G/X families.

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## 2.2. Programmable Functional Unit (PFU) Blocks

Lattice Avant delivers a higher FPGA Logic Count capability and performance compared to previous Lattice product families. It is optimized for Best-in-Class routability and utilization performance. The core of the Lattice Avant device consist of Programmable Functional Unit (PFU) blocks and each block can be used to perform Logical, Arithmetic, RAM, or ROM functions. The PFU blocks are made up of LUTs and registers. The Lattice Avant's fabric leverages its LUT4 area efficiency to generate its low power differentiation.

Each Lattice Avant PFU block includes the following resources:

- 12 LUT4+FF pairs (arranged as six slices, two LUT+FF per slice)
- Fast LUT4 input to output delay path
- Dedicated MUX to enable LUT5 support
- S44 Fast LUT-to-LUT connection
- Single port and pseudo dual port distributed RAM support
- Single Port Distributed RAM: 16 × 4, 16 × 8, 32 × 2, 32 × 4
- Pseudo Dual Port Distribute RAM: 16 × 4, 16 × 8, 32 × 2, 32 × 4
- Two 16 x 4 Distributed RAMs can fit into one PFU to get 16 x 8
- Two 32 x 2 Distributed RAMs can fit into one PFU to get 32 x 4

### 2.2.1. Slices

Each PFU contains six slices, and each slice contains two LUT4s and two FFs. All slices have 16 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six from routing and one to carry-chain (to the adjacent PFU).

### 2.2.2. Modes of Operation

Slices 0-5 of the PFU have up to four potential modes of operation: Logic, Ripple, RAM, and ROM.

**Logic Mode**

The LUTs in each slice are configured as 4-input combinatorial lookup tables in logic mode. A LUT4 can have 16 possible input combinations. Any 4-input logic functions can be generated by programming this lookup table. A LUT5 can be constructed within one slice.

**Ripple Mode**

Ripple mode supports the efficient implementation of small arithmetic functions. Ripple mode also includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2C mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

**RAM Mode**

In RAM mode the LUTs are configured as memory elements. Two sets of 16 × 4-bits or 32 x 2-bits of distributed single port RAM or pseudo dual port RAM can be constructed within one PFU. Lattice Avant device also supports distributed memory initialization.

The Lattice design tools support the creation of a variety of different sized memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.1 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in Lattice Avant devices, refer to Lattice Avant Embedded Memory User Guide (FPGA-TN-02289).

**Table 2.1. Number of Slices Required to Implement Distributed RAM**

| | SP 16 × 4 | SP 32 × 2 | PDP 16 × 4 | PDP 32 × 4 |
|---|---|---|---|---|
| Number of slices | 3 | 3 | 3 | 3 |

**Note**: SP = Single Port, PDP = Pseudo Dual Port

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**ROM Mode**

ROM mode uses the LUT logic; hence, Slice 0 through 5 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to Lattice Avant Embedded Memory User Guide (FPGA-TN-02289).

## 2.3. Routing

There are many resources provided in the Lattice Avant devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers, and metal interconnect (routing) segments.

The Lattice Avant platform has an enhanced routing architecture that produces a compact design. The Radiant software tool takes the output of the synthesis tool and places and routes the design.

## 2.4. Clocking Structure

The Lattice Avant device core architecture is constructed of a number of similar sized Clock Regions (CKR). Each CKR comprises blocks such as PFUs, EBRs, DSPs, and a Regional Clock Network. For the LAV-AT-E70 device, each CKR is about 35k System Logic Cells (SLCs). Each CKR is also associated with I/O resources. I/O resources may be a group of high speed SERDES I/O, a High-Performance I/O (HPIO) bank or a Wide-Range I/O (WRIO) bank group. The Clock Regions are arranged in two rows and multiple columns depending on the density of the device.

The Lattice Avant clocking structure consists of clock synthesis blocks (PLLs), clock tree networks (GCLK, ECLK, RCLK, and PHYCLK), on-chip oscillators, and clock modules: Clock Synchronizers and Dividers (ECLKSYNCA/ECLKDIVA), Dynamic Clock Selection (DCS), Dynamic Clock Control (DCC), and DLLDEL delay elements. Each of these functions is described as follows.

An overview of the Clocking Network is shown in Figure 2.4 for the Lattice Avant device.

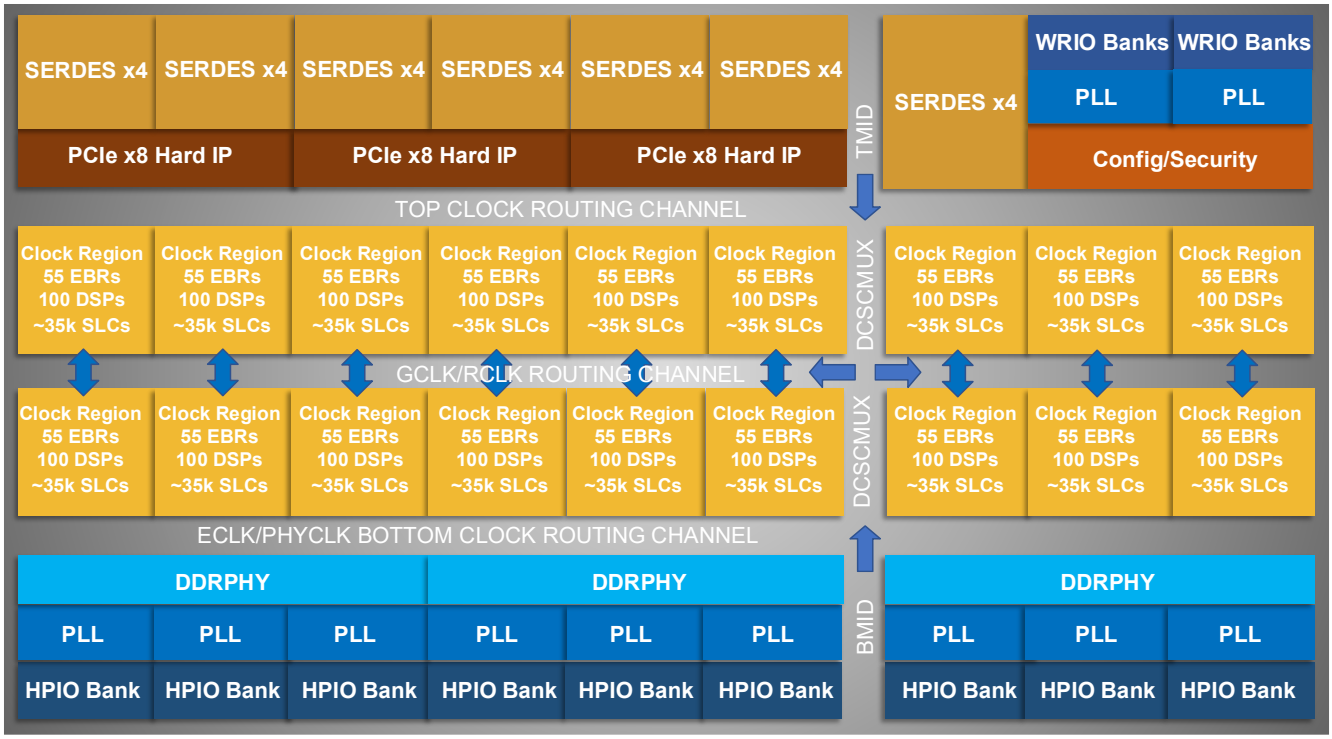


**Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-70 Device)**

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### 2.4.1. On-Chip Oscillator

The Lattice Avant device offers on board oscillator, which provides various clocks for the FPGA clock tree, Configuration block, and the system monitoring/ATM (anti-tampering) block. First, the OSC generates the user clock that drives the FPGA clock tree; this user clock is dynamically selectable between 400 MHz or 320 MHz, with 1-256 programmable divider options. Secondly, the OSC generates separate clocks for Configuration block with different frequencies of 400 MHz and 320 MHz to support SPI interface. Lastly, the OSC generates a hardened 100 MHz clock for system monitoring/ATM block.

### 2.4.2. GPLL

The Lattice Avant General Purpose PLL (GPLL) IP can be used for a variety of clock management applications such as frequency synthesis (multiplication and division of a clock), clock injection delay removal, and clock phase adjustment. The Lattice Avant GPLL supports frequency generation by integer or fractional-N synthesis. The reference clock and feedback clock can come from various sources. The GPLL (WRIO) supports six output clock selections, with each output clock having a different frequency as supported by the current VCO frequency and divider options. Each clock output can then be dynamically enabled or disabled by the user. The GPLL (HPIO) supports seven output clock selections six for driving high-speed HPIO ECLK or general purpose clocks plus an additional high-speed PHYCLK output for high-speed I/O interfaces. The Lattice Avant GPLL also supports the clock injection delay removal feature where delays associated with the GPLL, and clock tree are removed. This feature is typically used to reduce clock path delays and is performed by aligning the GPLL input clock with a feedback clock from the clock tree. The Lattice Avant GPLL further supports a clock phase adjustment feature. This feature provides the ability to set a specific phase offset between the outputs of the GPLL. Each clock output can support an independent static and dynamic phase shifts.

The GPLL IP supports the following key features:

- Frequency clock synthesis
- Clock tree delay cancellation
- Multiple reference and feedback clock selections
- Multiple and independent output clock controls
- Reference clock divider values – 1 to 64
- Integer Feedback divider values – 2 to 4095
- Output divider values – 1 to 256
- Supports Fractional-N divider with 14-bit fractional resolution
- Supports Spread Spectrum Clock Generation
  - Spreading rate adjustment range 15 kHz – 4 MHz
  - Spreading depth 0% to -10%
- VCO phase shift – 8 VCO phases
- Post Divider phase shift
- Dynamic VCO and divider phase shift
- Output clock bypass
- Programmable bandwidth
- Output synchronization to one main clock output (CLKOP)
- Dynamic programmability of GPLL registers through the LMMI interface
- Dynamic reset GPLL operation
- Glitchless Dynamic enable/disable of output clocks
- CLKOPHY with output up to 2400 MHz

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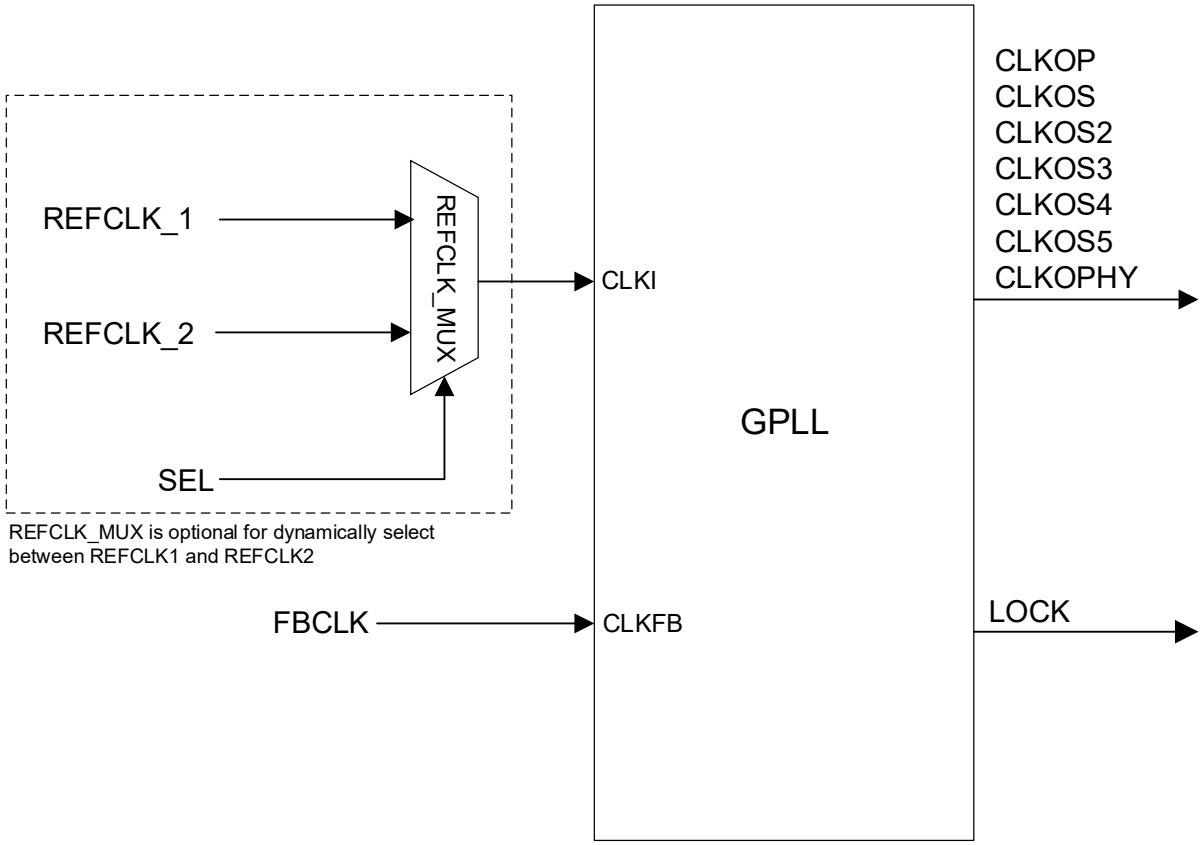


**Figure 2.5. Lattice Avant GPLL Block Diagram**

For more details on the GPLL, refer to the Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

### 2.4.3. Global Clock (GCLK)

The Global Clock Network (GCLK) provides the main clock sources in the Lattice Avant devices. The GCLK network drives the Regional Clock Networks (RCLK) of all Clock Regions (CKRs) in the device. The GCLK structure for all device densities is divided into two halves: left half and right half. Each half takes all available Global Clock sources and generates 24 independent GCLKs. These 24 GCLKs, combined with other Regional Clock sources provide 16 clocks to drive each row within a Clock Region.

Lattice Avant supports glitchless Dynamic Clock Control (DCC) feature which enables the GCLKs to be enabled or disabled to save dynamic power. There are also Dynamic Clock Selection (DCS) logic to allow glitchless selection between two clocks for the GCLK network.

### 2.4.4. Regional Clocks (RCLK)

The Regional Clock Network (RCLK) is the main clock network within a Clock Region. It is driven by the Global Clock Network and provides clock sources to all blocks (PFU, EBR, and DSP) within a Clock Region.

The RCLK network can bridge to adjacent Clock Regions to form Multi-Region Clock Networks. Specifically, it can bridge to one other Clock Region either to the left, right, top or bottom of the current Clock Region. The multi-region clock can be formed in the following topology: 1 × 1, 1 × 2, 2 × 1, 2 × 2, or 3 × 2 (column × row). See Figure 2.6 for examples of various sized clock regions outlined using colored boxes.

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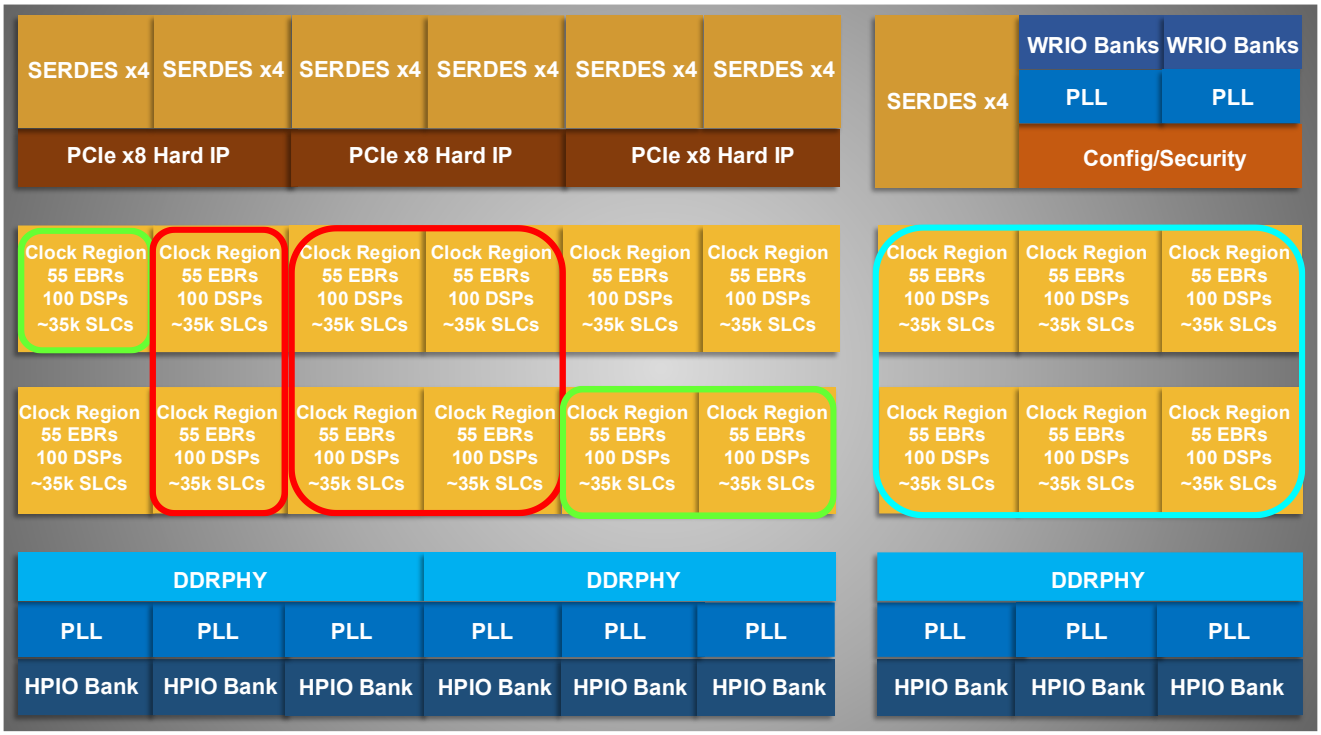


**Figure 2.6. Multi-Region Clock Formation**

The RCLKs are sourced from multiple inputs, referred to as Regional Clock sources. The Regional Clock sources that can drive the RCLKs are:

- Dedicated Clock Pins (PCLKT pins)
- GCLKs
- SERDES Clocks
- GPLL (HPIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- GPLL (WRIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- Clocks from neighboring regions, which is Regional Bridge clocks (RSBRG_* [0:3])
- Internally generated clocks (Fabric_CLK)

### 2.4.5. Edge Clock (ECLK)

Lattice Avant FPGAs have a number of high-speed Edge Clocks that are intended for use with the HPIO in the implementation of high-speed DDR I/O interfaces. These clocks, which have low injection time and skew, are suitable to drive the high-speed I/O interfaces with high fan-out capability, such as DDR Memory or Generic DDR interfaces. The Lattice Avant device has Edge Clocks (ECLK) at the bottom of the device where the HPIO banks are located. Each HPIO bank has four Edge Clocks supporting each Clock Region (CKR). The ECLK network is also able to bridge to adjacent left or right Clock Regions to form a wider ECLK network.

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Each Edge Clock can be sourced from the following:

- Dedicated Clock Pins (PCLKT pins)
- DLLDEL outputs
- GPLL (HPIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- ECLK Bridge clocks (EBRG_*[0:3])
- Internally generated clocks (Fabric_CLK)

For detailed information on Edge Clock connections, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

### 2.4.6. PHYCLK

The PHYCLK network is a special high frequency clock network that is used to support high frequency clocks for interface protocols for Fmax up to 2.4 GHz. The PHYCLK is driven only by a special output of the GPLL (HPIO) and there is one PHYCLK per I/O bank. The PHYCLK drives the High-Speed I/O interfaces and the DDRPHY hard IP at the same time. The DDRPHY hard IP spans three HPIO sectors and the full rate PHYCLK drives the DDRPHY full-rate clock port located at the center HPIO sector. The PHYCLK also drives ECLKDIV module to provide a quad-rate clock, divided by 4, frequency clock.

### 2.4.7. Clock Synchronizers and Dividers

Edge Clock Synchronizer (ECLKSYNCA) and Divider (ECLKDIVA) provide clock synchronization and clock divider functions in Lattice Avant device high speed interfaces.

For further information, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

### 2.4.8. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the global clock network. It switches between two independent input clock sources. Depending on the operational mode, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve a functioning glitchless DCS output clock, but running clocks are not required when used as a non-glitchless normal clock multiplexer.

There are four dynamic clock select blocks in the Lattice Avant devices. The DCS block allows dynamic and glitchless selection between two GCLK clock sources. The output of the DCS drives the GCLKs.

Figure 2.7 shows the timing waveforms of one of the several DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

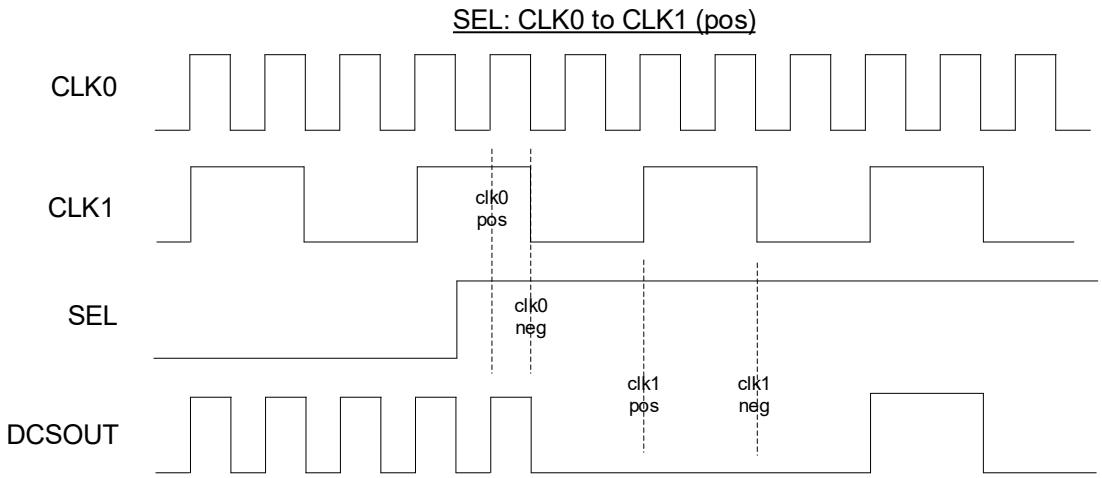


**Figure 2.7. DCS Waveforms**

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### 2.4.9. Dynamic Clock Control

The Lattice Avant device has a power-saving feature known as Dynamic Clock Control. This feature allows internal logic to dynamically enable or disable the GCLKs, thus enabling overall dynamic power consumption of the device. This gating function does not create glitches or increase the clock latency to the Global Clock network. There is a DCC element associated with each 48 GCLKs.

For more information about the DCC, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

### 2.4.10. DLL Delay (DLLDEL)

DLLDEL is a passive delay component to provide necessary clock phase shift for the dedicated clock pins before driving the GCLK and ECLK network. The adjusted phase can be dynamic or static controlled. In dynamic control mode, the delay code comes from the associated DDRDLL available on the device. In static control mode, the delay control is set by software. The delay element inside the DLLDEL can be bypassed if it is not used.

There are four DLLDEL elements for each HPIO bank and each WRIO bank group. Each DLLDEL is associated with one input clock pin/pair. There is only one DLLDEL code common to all DLLDEL modules, provided by one DDRDLL within each HPIO bank or WRIO bank group.

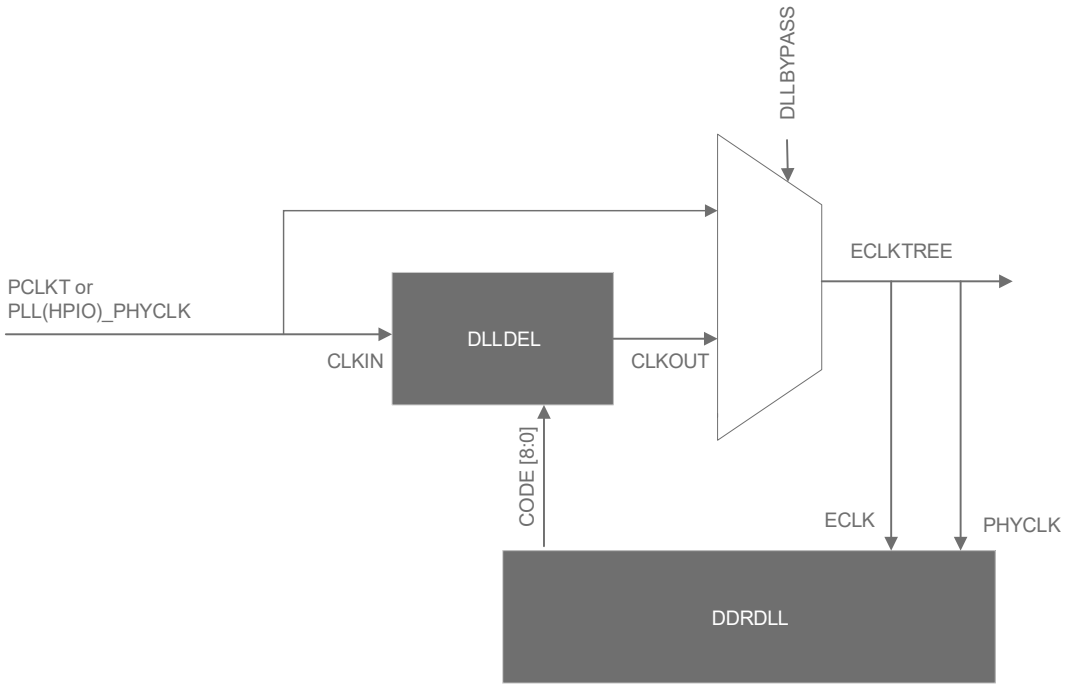


**Figure 2.8. High-Level Implementation of DLLDEL and Code Control**

## 2.5. sysMEM Memory

The Lattice Avant devices contain a number of sysMEM Embedded Block RAM (EBR). For each vertical block, it has 400 to 990 EBRs depending on the device density. The EBR consists of a 36 kb RAM with memory core, dedicated input registers and output registers as well as optional pipeline registers at the outputs. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM, and built-in FIFO. In Lattice Avant, unused EBR blocks is powered down to minimize power consumption.

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## sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.2. FIFOs can be implemented using the built-in read and write address counters and programmable full, almost full, empty and almost empty flags. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with up to 72-bit data widths. For more information, refer to Lattice Avant Embedded Memory User Guide (FPGA-TN-02289).

EBR also provides a build in ECC engine. The ECC engine supports a write data width of 64 bits, and it can be cascaded for larger data widths such as x128, ECC read may be performed in x1, x2, x4, x8, x16, x32, or x64 modes. The ECC parity generator creates and stores parity data for each 64-bit word written. When a read operation is performed, it compares the data with its associated parity data and report back if any corruption event has disturbed the data. Any single bit data disturbance is automatically corrected at the data output. In addition, two dedicated error flags indicate if a single-bit or two-bit error has occurred.

**Table 2.2 sysMEM Block Configurations**

| Single Port | Pseudo Dual Port | True Dual Port |
|---|---|---|
| 32,768 × 1 | 32,768 × 1 | 32,768 × 1 |
| 16,384 × 2 | 16,384 × 2 | 16,384 × 2 |
| 8,192 × 4 | 8,192 × 4 | 8,192 × 4 |
| 4,096x 9 | 4,096 × 9 | 4,096 × 9 |
| 2,048 × 18 | 2,048 × 18 | 2,048 × 18 |
| 1,024 × 36 | 1,024 × 36 | 1,024 × 36 |
| 512 × 72 | 512 × 72 | — |

### 2.5.1. Bus Size Matching

All the multi-port memory modes support different widths on each of the ports (except ECC mode, which only supports a write data width of 64 bits). The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

### 2.5.2. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

### 2.5.3. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

### 2.5.4. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

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### 2.5.5. FIFO Modes

The Lattice Avant platform devices support two different types of FIFOs with sysMEM: Single Clock FIFO (FIFO) and Dual Clock FIFO (FIFO_DC). FIFO Controller Implementation has options as LUT-Based, or hardware-based. It also supports the First Word Fall Through mode.

### 2.5.6. Memory Output Reset

The EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.9. The optional Pipeline Registers at the outputs of both ports are also reset in the same way.

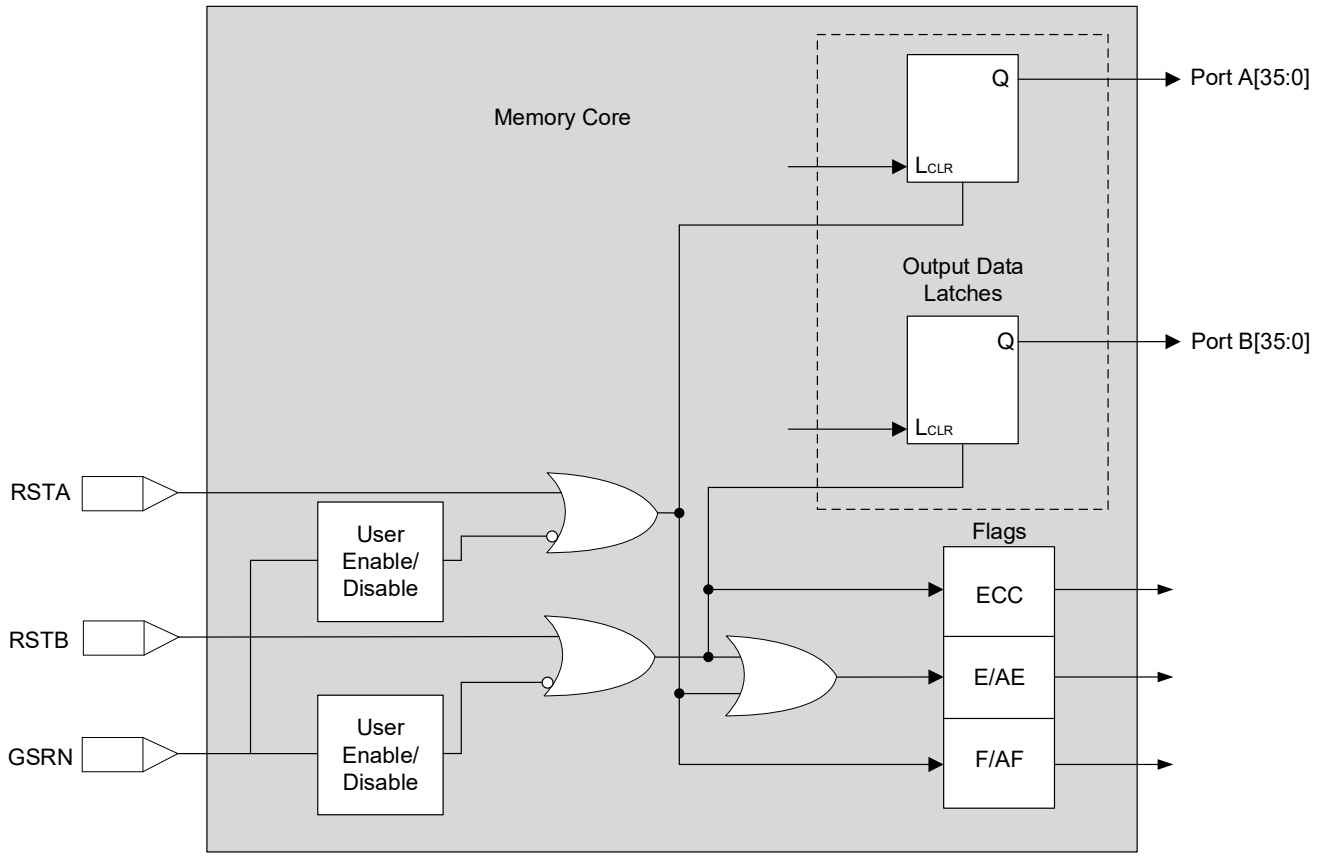


**Figure 2.9. Memory Core Reset**

For further information on the sysMEM EBR block, see the list of technical documentation in References section.

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## 2.6. sysDSP

The Lattice Avant platform provides an enhanced sysDSP architecture, making it ideally suitable for low-cost, high-performance Digital Signal Processing (DSP) applications. The internal DSP can also run up to 625 MHz maximum frequency on a fully pipelined input and output registers.

The Lattice Avant DSP block is a single-clock domain block with simpler structures to enable streamlined RTL implementation. Figure 2.10 shows the simplified DSP functional block, which can be configured to implement four 8 × 8 multipliers, three 9 × 9 multipliers, four 9 × 9 dot products, or one 18 × 18 multiplier. Each DSP block also contains an 18-bit pre-adder to support the symmetric filter and complex multiply, as well as a 48-bit adder with saturation and rounding option.

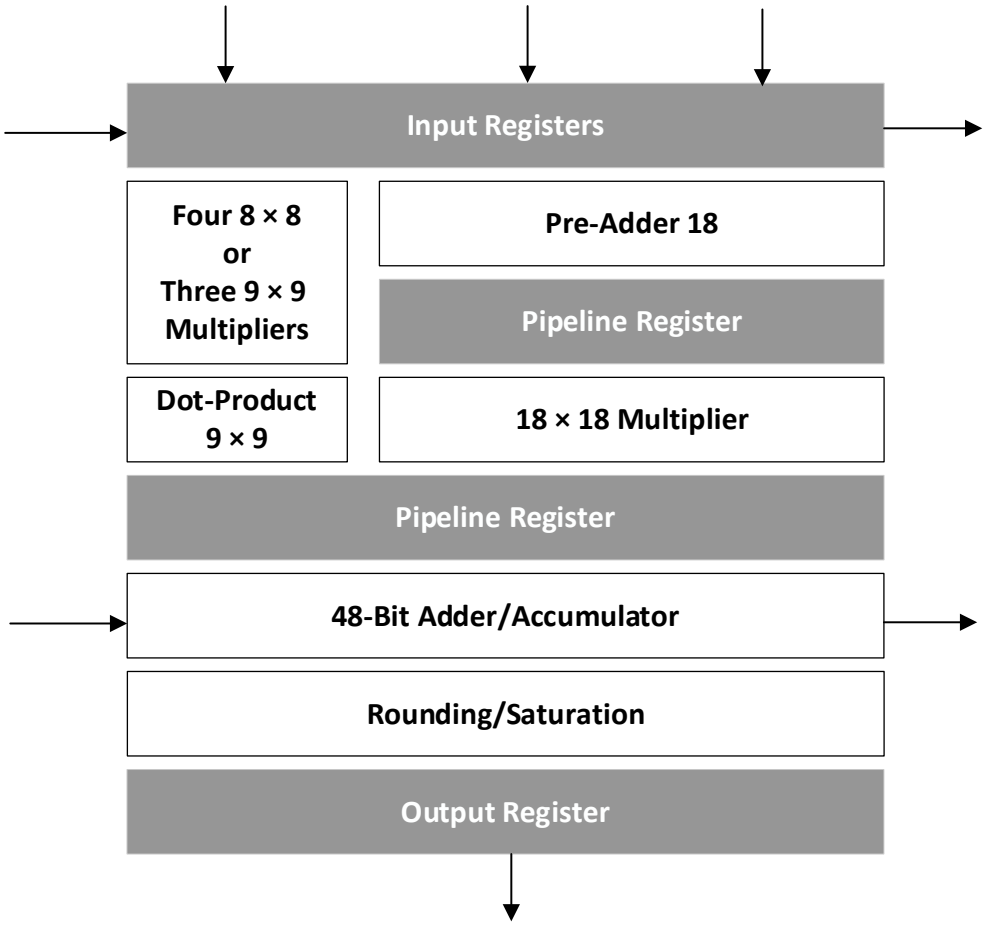


**Figure 2.10. DSP Functional Block**

The Lattice Avant sysDSP block supports the following basic elements.

- MULT8x8 (8-bit multiply)
- MULT9x9A (9-bit multiply)
- MULT18x18A (18-bit multiply)
- MULTADDSUB18x18A (18-bit multiply with pre-adder and accumulator)
- DOTPRODADDSUB9x9/DOTPRODADDSUB9x9A (9x9 multiply add with accumulator)

For further information, refer to Lattice Avant sysDSP User Guide (FPGA-TN-02293).

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## 2.7. Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVDS, HSUL, SSTL, POD, LVSTL, SLVS, SUBLVDS, LVCMOS, and MIPI DPHY.

The Lattice Avant platform contains multiple Programmable I/O Cell (PIC) blocks. Each PIC contains two Programmable I/O, PIOA and PIOB. Each PIO includes a sysI/O buffer and I/O logic. Two adjacent PIO can be joined to provide a differential I/O pair referred to as True and Comp, where True Pad is associated with the positive side of the differential I/O, and the complement with the negative.

Lattice Avant offers two types of I/O banks. The top bank I/O are WRIO (Wide Range I/O), and the bottom bank I/O are HPIO (High Performance I/O), with following feature summary:

WRIO (Wide Range I/O) operating with a VCCIO of 3.3 V down to 1.2 V:

- LVCMOS33/25/18/12
- Programmable Drive Strengths (4 to 12 mA)
- Programmable Slew rate: Fast and Slow
- Bus Keeper, Weak Pull-up and Weak Pulldown
- Open-drain support
- Complementary Outputs through the PIC
- Bypassable glitch filter on every input
- Always on Hysteresis in the single-ended Input buffer
- Early I/O feature, selectable per I/O
- 50 Ω Driver Impedance to mitigate reflections on board
- Supports complementary outputs through the external resistors for emulated LVDS and subLVDS standards

HPIO (High-Performance I/O) operating with a VCCIO of 1.8 V down to 0.9 V:

- DDR5 @ 2100 Mbps[1]
- DDR4[2]/LPDDR4 @ 2400 Mbps
- LVDS Differential on every pair of I/O @ 1600 Mbps
- SUBLVDSE on every pair of I/O @ 800 Mbps
- SUBLVDS RX on every pair of I/O @ 1600 Mbps
- MIPI DPHY - SLVS-200 @1800 Mbps[2]
- SGMII TX/RX compatible with LVDS Electrical signaling[2]
- LVCMOS18/12/10/09
- Programmable Drive Strengths (2 to 12 mA)
- On-Chip Termination
- Support programmable on-chip 100 Ω differential termination resistor
- External and Internal (trainable) VREF in each bank
- Polarity Control for Differential RX and TX Paths
- Open drain
- Programmable Slew rates: Fast and Slow
- Complementary Outputs

**Notes:**

1. While the Lattice Avant HPIO can support DDR5 up to 2400 Mbps, Lattice Avant has defined DDR5 operation only up to 2100 Mbps. DDR5 operational ranges defined by JEDEC are up to 2100 Mbps and >2933 Mbps.
2. The E70B and E30B variants have the following I/O limitations: DDR4 is not supported. LPDDR4 is limited to 1600 Mb/s. SGMII is not supported. MIPI DPHY is limited to 1200 Mbps.

For more information about DDR implementation in I/O Logic and DDR memory interface support, refer to Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

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### 2.7.1. Supported sysI/O Standards

Lattice Avant sysI/O buffers support both single-ended differential and differential standards. Single-ended standards can be further subdivided into internally ratioed standards such as LVCMOS and externally referenced standards such as HSUL and SSTL. The buffers support the LVCMOS 0.9 V, 1.0 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V standards. Differential standards supported include LVDS, SLVS, differential LVCMOS, differential SSTL, differential HSUL, differential LVSTL, and differential POD. For better support of video standards, subLVDS and MIPI DPHY are also supported. Table 2.3 and Table 2.4 provide a list of sysI/O standards supported in the Lattice Avant devices.

### 2.7.2. sysI/O Banking Scheme

Lattice Avant devices have up to 15 banks in total. For LAV-AT-70 device, there are six banks on top and nine banks on the bottom side of device. The lower density Lattice Avant device has fewer banks. The top (WRIO) banks support up to VCCIO 3.3 V while bottom (HPIO) banks support up to VCCIO 1.8 V. In addition, HPIO banks support one external VREF input for flexibility to receive the referenced input level on the same bank. And it also has the internal generated VREF input, which can be trained. DDR5 and DDR4/LPDDR4 must use internal VREF. For the WRIO bank 0, bank 1, and bank 2, these provide 52 total I/O, which is also the same for the bank 12, bank 13, and bank 14. For HPIO banks, each bank is built with 52 data I/O and other power/ground pads, and is mapped to support DDRPHY interfaces. Figure 2.11 shows the location of each bank.

**Note**: SERDES is supported in Avant-AT-G/X families.

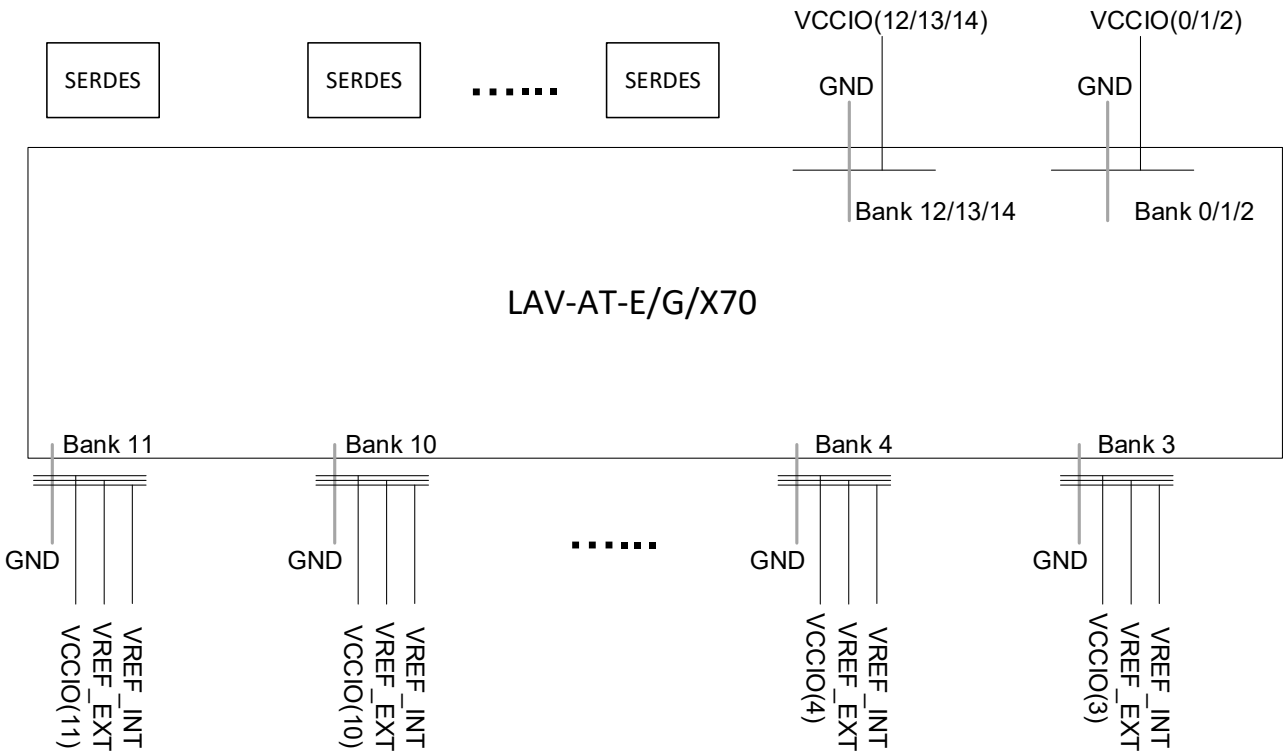


**Figure 2.11. sysI/O Banking**

#### Typical sysI/O Behavior During Power-up

The internal Power-On-Reset (POR) signal is deactivated when $V_{CC}$ and $V_{CCAUX}$ have reached satisfactory levels. After the POR signal is deactivated the FPGA core logic becomes active. It is the responsibility of the user to ensure that all other $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in Lattice Avant devices, see the list of technical documentation in References section.

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$V_{CC}$ and $V_{CCAUX}$ supply the power to the FPGA core fabric, whereas $V_{CCIO}$ supplies power to the I/O buffers. For the different power supply voltage levels supported by the I/O banks, refer to Lattice Avant sysI/O User Guide (FPGA-TN-02297) for detailed information.

### sysI/O Standards Supported by I/O Bank

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 2.3 and Table 2.4 summarize the I/O standards supported on various sides of the Lattice Avant device.

**Table 2.3. Single-Ended I/O Standards Supported on Various Sides**

| Standard | Top (WRIO) | Bottom (HPIO) | Input | Output | Bi-directional |
|---|---|---|---|---|---|
| LVCMOS33 | Yes | — | Yes | Yes | Yes |
| LVCMOS25 | Yes | — | Yes | Yes | Yes |
| LVCMOS18 | Yes | Yes | Yes | Yes | Yes |
| LVCMOS12 | Yes | Yes | Yes | Yes | Yes |
| LVCMOS10 | — | Yes | Yes | Yes | Yes |
| LVCMOS09 | — | Yes | Yes | Yes | Yes |
| SSTL 135 | — | Yes | Yes | Yes | Yes |
| HSUL12 | — | Yes | Yes | Yes | Yes |
| LVSTL11_I | — | Yes | Yes | Yes | Yes |
| LVSTL11_II | — | Yes | Yes | Yes | Yes |
| POD12 | — | Yes | Yes | Yes | Yes |
| POD11 | — | Yes | Yes | Yes | Yes |

**Table 2.4. Differential I/O Standards Supported on Various Sides**

| Standard | Top (WRIO) | Bottom (HPIO) | Input | Output | Bi-directional |
|---|---|---|---|---|---|
| LVDS | — | Yes | Yes | Yes | Yes |
| SUBLVDS | — | Yes | Yes | — | — |
| SLVS | — | Yes | Yes | Yes | — |
| SUBLVDSE | Yes | Yes | — | Yes | — |
| LVDSE | Yes | — | — | Yes | — |
| MIPI_DPHY | — | Yes | Yes | Yes | Yes |
| SSTL135D | — | Yes | Yes | Yes | Yes |
| HSUL12D | — | Yes | Yes | Yes | Yes |
| LVSTL11D_I | — | Yes | Yes | Yes | Yes |
| LVSTL11D_II | — | Yes | Yes | Yes | Yes |
| POD12D | — | Yes | Yes | Yes | Yes |
| POD11D | — | Yes | Yes | Yes | Yes |

For more information on the various sysI/O features available on the Lattice Avant device, refer to Lattice Avant sysI/O User Guide (FPGA-TN-02297).

## 2.8. Programmable I/O Cell (PIC)

The programmable I/O cells (PIC) provide I/O function and necessary gearing logic associated with PIO. Lattice Avant consists of WRIO PIC and HPIO PIC.

WRIO PICs contain three blocks: an input register block, output register block, and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic. WRIO PICs cover the top (WRIO) banks. HPIO PICs contain gearing logic and edge monitor used for locating the center of data window. HPIO PICs cover the bottom (HPIO) banks to support DDR operation.

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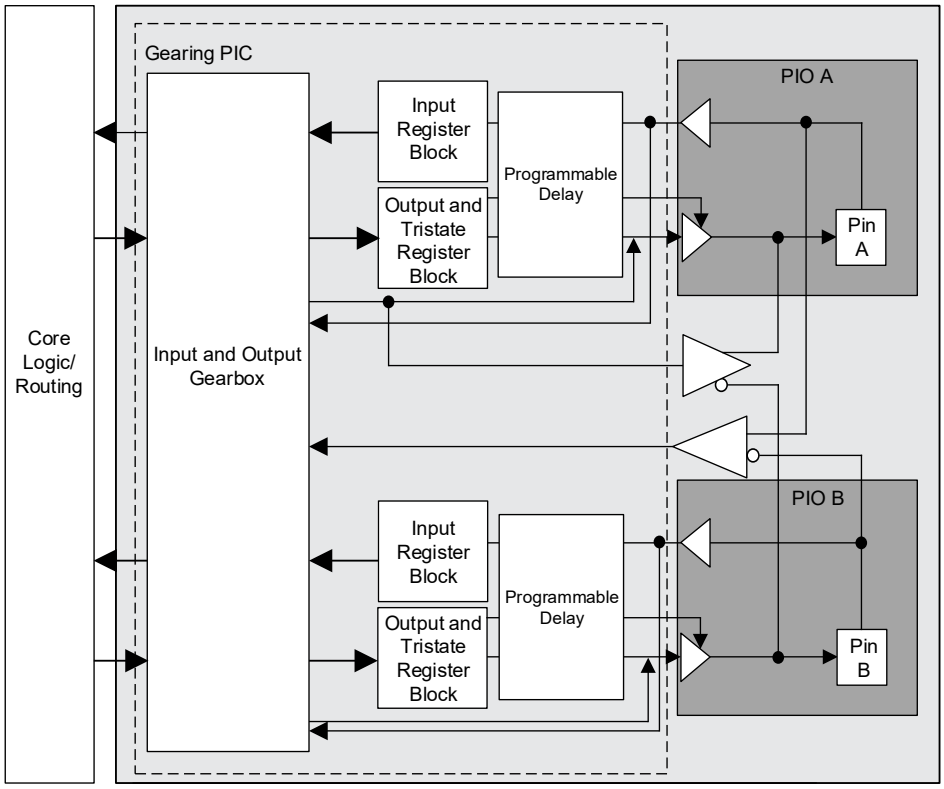


**Figure 2.12. Group of Two High Performance Programmable I/O Cells**

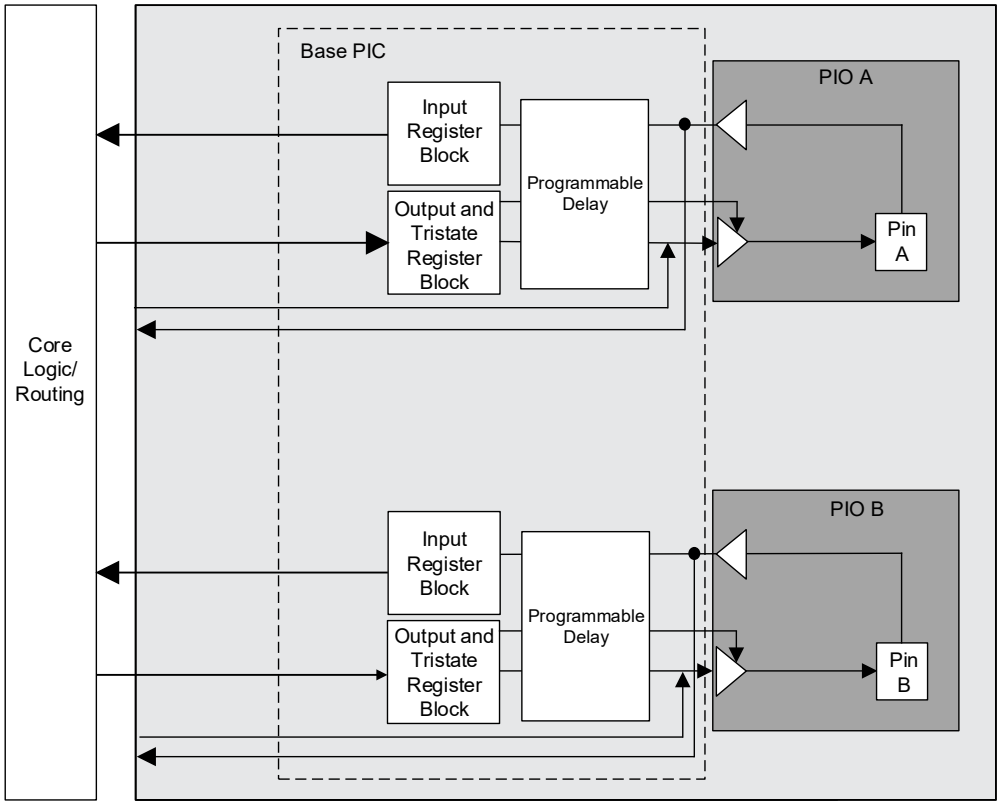


**Figure 2.13. Wide Range Programmable I/O Cells**

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### 2.8.1. Input Register Block

The input register blocks for the PIO contain delay elements and registers (IREG) that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIO on the bottom (HPIO) edges include built-in FIFO logic to interface to GDDR and xSPI.

The Input register block on the bottom (HPIO) side includes gearing logic and registers to implement 2:1, 4:1, 8:1, and 10:1 gearing functions. It can also implement the 7:1 gearing function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. For more information on gearing function, refer to Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

### 2.8.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

The Lattice Avant output data path has programmable registers (OREG/TSREG) and output gearing logic. On the bottom (HPIO) side, the output register block can support 2:1, 4:1, 8:1, 10:1, and 7:1 gearing GDDR interfaces. On the top side, the banks support 2:1 gearing. The programmable delay cells are also available in the output data path.

For more information on gearing function, refer to Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

### 2.8.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, the TD input feeds one of the flip-flops that then feeds the output.

## 2.9. DDR Memory Support

Lattice Avant DDRPHY is compliant with the DFI 4.0+ specification and supports multiple DDR memory standards: DDR5 and DDR4/LPDDR4. Table 2.5 lists a summary of Lattice Avant supported memory standards and the max speed rates.

**Table 2.5. Summary of DDR Standards and Max Rates**

| Standard | Max Speed[1] |
|---|---|
| DDR5 | 2100 Mbps[2] |
| DDR4/LPDDR4 | 2400 Mbps |

**Notes:**

1. Max speeds reflect single-rank configurations only.
2. While the Lattice Avant HPIO can support DDR5 up to 2400 Mbps, Lattice Avant has defined DDR5 operation only up to 2100 Mbps. DDR5 operational ranges defined by JEDEC are up to 2100 Mbps and >2933 Mbps.

### 2.9.1. DDRPHY Overview

The Lattice Avant DDRPHY interface provides a physical interface between the FPGA soft memory controller and DRAM device.

Lattice Avant DDRPHY shares routing resources between the PIC and DDRPHY. In cases where the DDRPHY is partially used, the I/O can be configured for non-DDR memory use.

For DQ and CA lanes, the PHYCLK can operate up to 2.4 GHz to achieve 2.4 Gbps performance while leveraging a 300 MHz fabric interface clock.

For additional details on the Lattice Avant DDRPHY, refer to the Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

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### 2.9.2. DQS Grouping for DDR Memory

Lattice Avant DDRPHY occupies three HPIO banks, where each HPIO bank has 52 I/O.

Lattice Avant memory interfaces can support up to:

- x72/x64 (three HPIO banks)
- x40/x32 (two HPIO banks)
- x16 interfaces (one HPIO banks)

In DDRPHY DDRx memory mode, the digital logic is partitioned into two types of lanes: DQ/DQS data lanes and CA lanes. For all Lattice Avant supported memory standards, a data lane occupies 11 bits in total: 8-bit DQ, DQS/DQSN, and DM/DMI/DBI. DDRPHY CA lane pin assignments are different based on the DDR standard used. The number of pins bonded out in each DQS group is package dependent.

For additional details on the portioning of the DDRPHY, refer to the Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

## 2.10. Device Configuration

All Lattice Avant devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support serial, quad, and byte configuration. The TAP, which has dedicated I/O, supports the IEEE Standard 1149.1 Boundary Scan specification. CFGMODE, PROGRAMN, INITN, and DONE are dedicated configuration pins. The remaining sysCONFIG pins are used as dual function pins. Refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299) for more information about using the dual-use pins as general purpose I/O.

The following configuration interfaces are supported:

- Controller SPI/MSPI[1] – x1, x2, x4, xSPI (x8, dual transfer rate)
- Target SPI/SSPI[1] – x1, x2, x4, xSPI (x8, dual transfer rate)
- JTAG (proprietary protocol)

**Note:**

1. Controller SPI was historically known as MSPI and Target SPI was historically known as SSPI.

On power-up, based on the voltage level (high or low) of the CFGMODE pin, the FPGA SRAM is configured by the appropriate sysCONFIG port. If CFGMODE pin is *low*, the FPGA is in Target configuration mode (Target SPI or TAP). If CFGMODE pin is driven high, the FPGA is in Controller SPI booting mode. In Controller SPI booting mode, the FPGA boots from an external SPI flash.

### 2.10.1. Enhanced Configuration Options

The Lattice Avant devices have enhanced configuration features such as:

- Early I/O release
- Bitstream Decryption
- Bitstream Authentication
- Decompression Support
- Watchdog Timer support
- Dual and Multi-boot image support

Early I/O Release is the configuration feature in which certain I/O banks are released earlier so that customer systems have minimal disruption. For more details, refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299).

Watchdog Timer is the configuration feature that helps the user to add a programmable timer option for timeout applications.

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**Dual-Boot and Multi-Boot Image Support**

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the Lattice Avant devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the Lattice Avant device can revert to the original backup golden configuration and try again. This can all be done without the power cycling the system. For more information, refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299).

### 2.10.2. JTAG

All Lattice Avant devices contain various ports that can be used for configuration, including a Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK, and TMS. The test access port uses VCCIO2 for power supply.

For more information, refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299).

### 2.10.3. Single Event Upset (SEU) Handling

Lattice Avant devices have an improved, hardware implemented, Soft Error Detection (SED) circuit which can be used to detect SRAM errors so they can be corrected, either automatically or after notification and consent. There are two layers of SED implemented in Lattice Avant making it more robust and reliable.

The SED hardware in Lattice Avant devices is part of the Configuration block. The SED module in Lattice Avant is an enhanced version as compared to the SED modules implemented in other Lattice devices. The configuration data is divided into frames so that the entire FPGA can be programmed precisely with ease. The SED hardware reads data from the FPGAs configuration memory and performs an Error Correcting Code (ECC) calculation on every frame of configuration data. With Automatic operation, once a single error is detected it is corrected automatically, a notification is generated and SED resumes operation. With Consent operation, once a single error is detected the SED hardware halts and a fabric notification is generated. You can determine whether to correct or not depending upon system considerations. If correction is desired and consent is granted, the single error is corrected and the SED resumes operation. For single bit errors, the corrected value is rewritten to the frame using ECC information. In all modes, if more than one-bit error is detected within one frame of configuration data they are uncorrectable. Nevertheless, a fabric error notification is generated and if the user takes no other action, the SED continues operation.

After the ECC is calculated on all frames of configuration data, CRC is calculated and checked for the entire bitstream. ECC and CRC checks do not include EBR and Distributed RAM contents.

For further information on SED support, refer to Lattice Avant Soft Error Detection (SED)/Correction (SEC) User Guide (FPGA-TN-02290).

## 2.11. Trace ID

Each Lattice Avant device contains a unique (per device) TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the SSPI and JTAG interfaces. For further information on TraceID, refer to Using TraceID (FPGA-TN-02084).

## 2.12. SERDES and PCS

The Lattice Avant platform SERDES/PCS is a multi-protocol PHY design with quad (x4) base. Each quad consists of the following:

- Quad x4 PMA: 4 Tx, 4 Rx, 1 common block (REFCLK,2 × Tx PLL)
- Multiple Protocol PCS (MPPCS)

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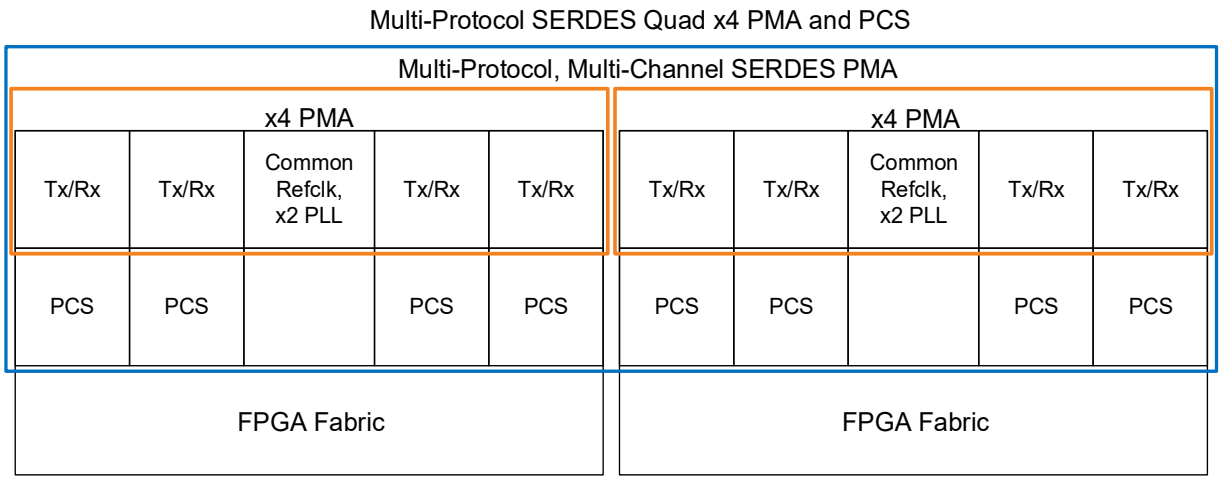


**Figure 2.14. SERDES Overview Diagram**

The Lattice Avant SERDES is in Quad x4 units. Each device may support multiple instances of Quad x4 units.

The PMA covers multiple sub-ranges of 1.25 Gbps to 26.5625 Gbps. Table 2.6 shows the list of supported protocols.

**Table 2.6. SERDES/PCS Supported Protocols**

| Protocol | PMA Support | PCS Support | Link and Upper Layer Support |
|---|---|---|---|
| PCIe Gen1/2/3/4 | Yes | Yes | Hard DLL, TL, and DMA |
| 10G Ethernet | Yes | Yes | Soft MAC in Fabric |
| 25G Ethernet | Yes | Yes | Soft MAC in Fabric |
| DisplayPort | Yes | Yes | Soft logic in Fabric |
| SLVS-EC | Yes | Yes | Soft logic in Fabric |
| CoaXPress | Yes | Yes | Soft logic in Fabric |
| CPRI | Yes | Yes | Soft logic in Fabric |
| eCPRI | Yes | Yes | Soft logic in Fabric |
| ROE | Yes | Yes | Soft logic in Fabric |
| SyncE | Yes | Yes | Soft logic in Fabric |
| JESD204B, C | Yes | Yes | Soft logic in Fabric |

**Notes:**

- Protocol performance speeds met with LFG and LBG packages. Other packages are limited to 10.3125G.
- Platform support outlined. See tables in the Features section for capabilities supported in specific family.

**Table 2.7. Lattice Avant SERDES Protocol Width Support**

| Protocol | Typical Width per link | Rate (Gbps) × Width Examples |
|---|---|---|
| PCIe | x1, x2, x4, x8 | (2.5, 5, 8, 16) × (1, 2, 4, 8) |
| Ethernet | x1, x2, x4 | 1.25 × 1, 3.125 × 1, 3.125 × 4, 5 × 1, 6.25 × 2, 10.3125 × 1, 25.78125 × 1 |
| DP/eDP | x1, x2, x4 | (1.62, 2.7, 5.4, 8.1) × (1, 2, 4) |
| SLVS-EC | x4, x8 | (1.25, 2.5, 5) × (4, 8) |
| CoaXPress | x1, x2, x4, x8 | (3, 6.25, 10, 12.5) × (1, 2, 4, 8) |
| CPRI | x1 | (1.2288, 2.4576, 3.072, 4.915, 6.144, 8.11008, 9.8304, 10.1376, 12.16512, 24.3) x (1) |
| eCPRI | x1 | 10.3125 × 1, 25.78125 × 1 |
| ROE | x1 | 10.3125 × 1, 25.78125 × 1 |
| SyncE | x1 | 1.25 × 1, 3.125 × 1, 3.125 × 4, 5 × 1, 10.3125 × 1, 25.78125 × 1 |

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| Protocol | Typical Width per link | Rate (Gbps) × Width Examples |
|---|---|---|
| JESD204B/C | x1, x2, x4, x8 | (3.125, 6.25, 12.5, 25) × (2, 4, 8) |

**Notes:**

- Protocol performance speeds met with LFG and LBG packages. Other packages are limited to 10G.
- Platform support outlined. See tables in the Features section for capabilities supported in a specific family.

In Lattice Avant, the wide bus width is supported with running reference clock distribution to each quad. Synchronization logic provided to ensure multiple x4 is in sync in the PMA IP.

The SERDES feature is not supported in the Lattice Avant-AT-E family.

### 2.12.1. SERDES/PMA Block

The PMA hard macro comprises of four lanes with a full duplex transceiver for each lane, each lane includes Transmitter (TX), Receiver (RX), Support, and test features. The TX lane receives 8, 10, 16, 20, 32, or 40 bits of transition-encoded data synchronous with a Tx clock, serializes it into a single stream of differential transmitted data and transmits to the lane. The transmitter supports multi-level output driver, multi-level transition emphasis, and multi-level Common Mode levels. The RX Lane performs a series function such as adaptive continuous-time linear equalization (CTLE), decision feedback equalization (DFE), and clock data recovery (CDR) to ensure recovered clock is used to retime received data with channel loss compensated and optimized and send it to deserializer which produces parallel data and a parallel data clock for the relevant PCS lane. The Support block provides all the common functions for the RX/TX link, TX clock generation, TX/RX termination calibration, biasing voltage, and reference clock buffering.

### 2.12.2. Multi-Protocol PCS (MPPCS)

The Lattice Avant Platform SERDES supports multi-protocol PCS with key features below:

- Encoder/Decoder: 8B10B, 64B/66B, 128B/130B.
- Comma detection and word and block alignment
- Clock tolerance Elastic FIFO
- Gearing to FPGA by 8/10/16/20/32/40/64/80/128 and 66/132/160 available in PMA direct mode.
- Built in Pipe Control Interface for PCIe fabric
- GMII/XGMII for Ethernet
- Forward Error Correction (FEC) supporting both:
  - BASE-R/Fire Code FEC
  - KR RS-FEC 528,514 FEC (Reed-Solomon)
- Programmable Interface Width/Speed to connect to either hard IP (PCIe LL controller) or FPGA fabric
- Channel bonding, for channels within quads, and between quads: Rx FIFO alignment and Tx FIFO delay adjustment to minimize channel to channel skew.
- Serial Parallel loopback mode for testability

Protocol support varies by family. See Features section for details of protocols supported in a specific family.

### 2.12.3. Multi-Protocol PHY (MPPHY) Integration

Figure 2.15 shows the MPPHY top-level integration block diagram.

Each PMA Lane has a corresponding PCS lane. The 40-bit SERDES interface between PMA, PCS, and the 32-bit PIPE interface between PCS and link layer follow the Intel Standard PHY Interface [PHY].

MPPHY can be controlled by a number of registers that can be dynamically reconfigured by user logic or configuration module through the Lattice Memory Mapped Interface (LMMI) ports

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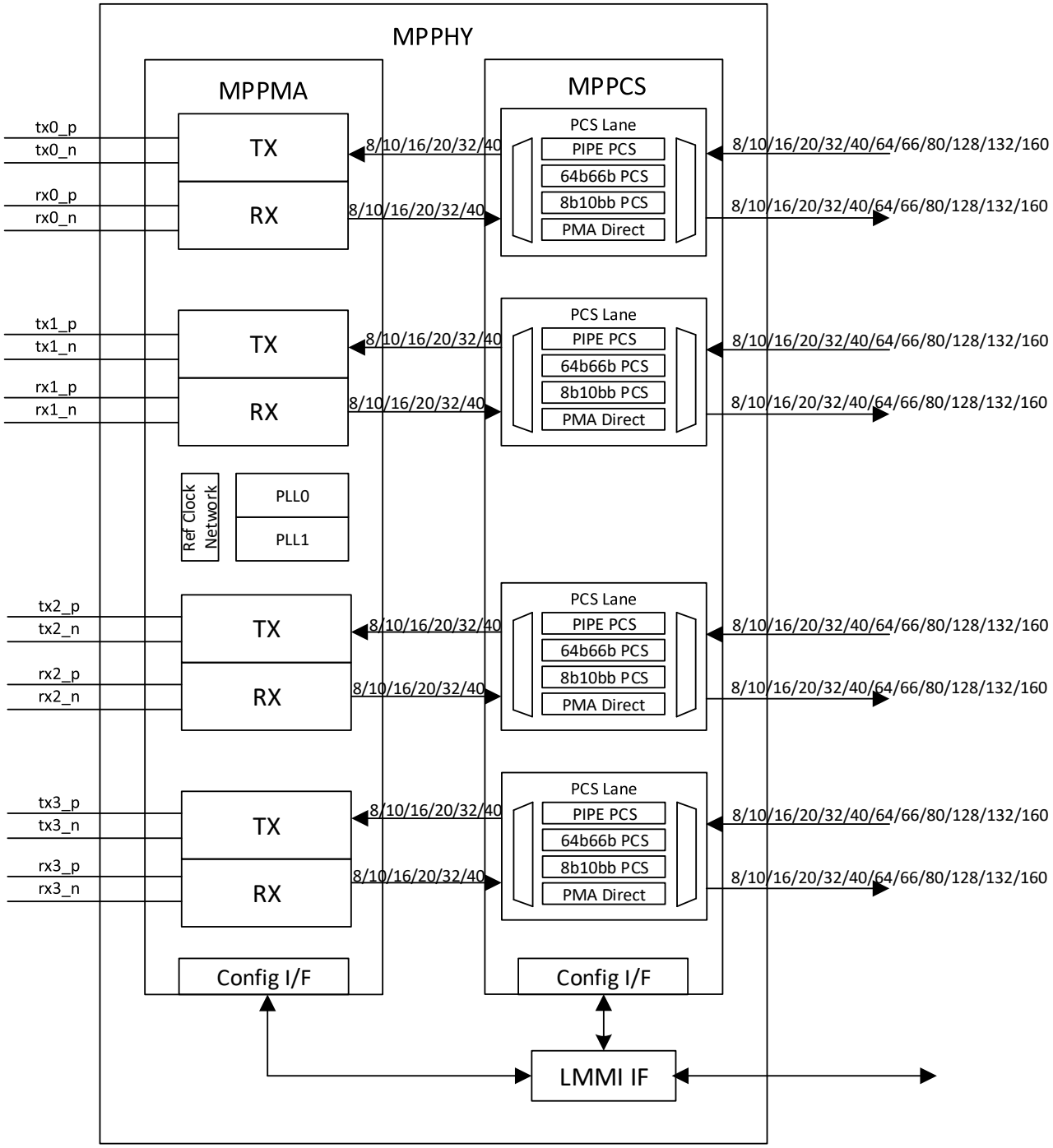


**Figure 2.15. MPPHY Top-Level Block Diagram**

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### 2.12.4. Peripheral Component Interconnect Express (PCIe)

The Lattice Avant device features up to 24 lanes of hardened PCIe, with a maximum PCIe link width of x8. The PCIe block implements all three layers defined by the PCI Express Specification: Physical, Data Link, and Transaction as shown in Figure 2.16. Below is a summary of the features supported by the PCIe block:

- PCIe Express Base Specification 4.0 compliant including compliance with earlier PCI Express Specifications
- Support for link width of x8, x4, x2, x1 PCI Express lanes. Bifurcation is supported through soft IP PCI Express Lanes
- 16.0 GT/s, 8.0 GT/s, 5.0 GT/s, and 2.5 GT/s line rate support
- Multi-function support with up to eight physical functions
- Support for Autonomous Equalization
- Support for Figure of Merit PIPE PHY Equalization
- Flexible Equalization methods (PCIe supports *Preset* only)
- ECC RAM and Parity Data Path Protection
- 64-bit User Interface, 24 Virtual Functions Data Width (per link)
- Robust Error-Handling support, including AER, ECRC generation/checking, recovery from parity and ECC errors, and error injection diagnostics.
- Optional Hardened high-performance multi-channel scatter-gather DMA controller
- Support for power management features including ASPM L0s and L1, L1 PM states with CLKREQ, Power Budgeting, and Dynamic Power Allocation

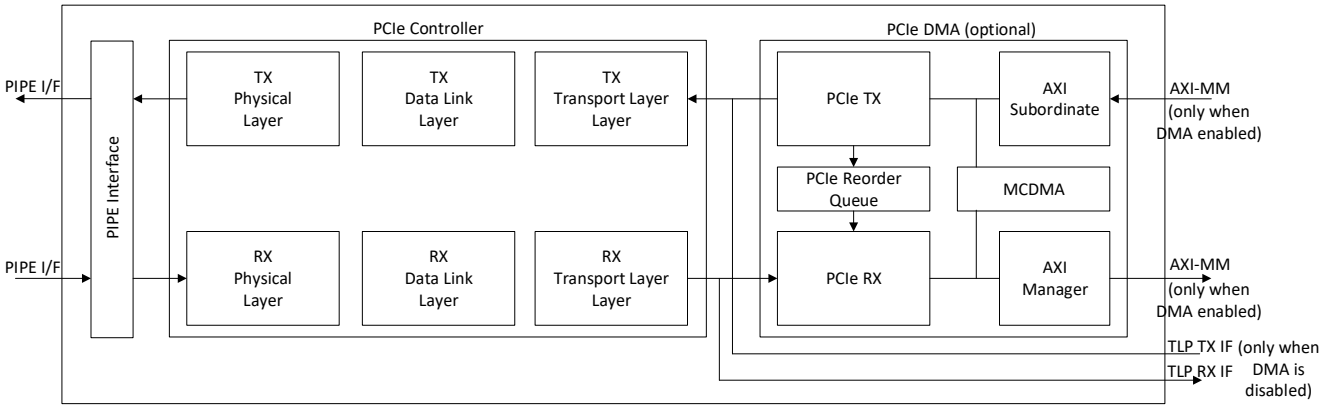


**Figure 2.16. PCIe Core**

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The hardened PCIe block can be instantiated using the PCIe IP Core through the Radiant IP Catalog and IP Block Wizard. In Figure 2.17, the PCIe core is configured as an Endpoint using a soft IP wrapper that provides useful functions such as bridging support for bus interfaces and DMA applications. In addition to the standard Transaction Layer Packet (TLP) interface, the data interface can also be configured to be AXI4 as well. The PCIe hardened block also features a register interface for the Lattice Memory Mapped Interface (LMMI). The PCIe block has many registers which contain information about the current status of the PCIe block as well as the capability to dynamically switch PCIe settings. These registers can also be accessed through the Reveal Controller Tool.

For more information about the PCIe soft IP, refer to the PCIe x8 IP Core User Guide (FPGA-IPUG-02243) document.

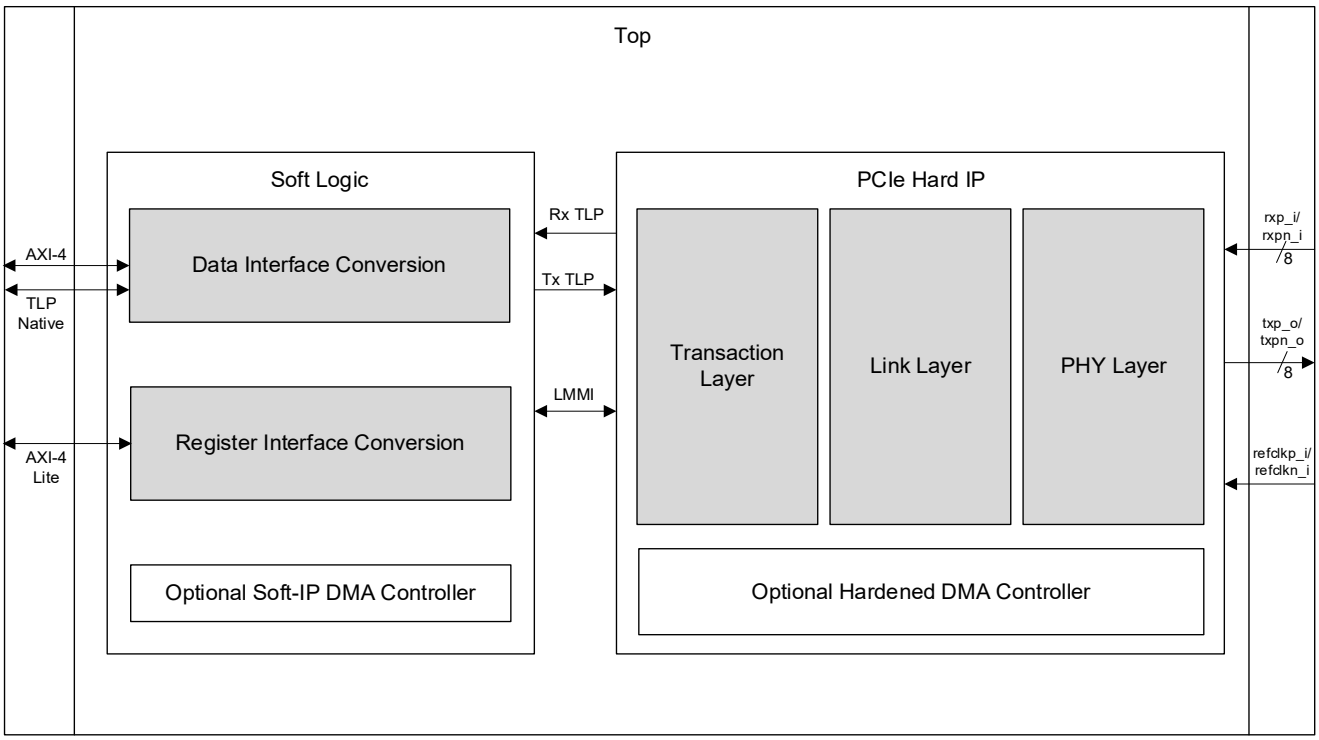


**Figure 2.17. PCIe Soft IP Wrapper**

## 2.13. Pin Migration

The Lattice Avant platform is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a low utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likelihood of success in each case. An example is that some user I/O may become No Connects in smaller devices in the same package. Refer to the Lattice Avant Pin Migration tables in the Avant-E, Avant-G, and Avant-X web pages, and Lattice Radiant software for specific restrictions and limitations.

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## 2.14. Security Engine

The Lattice Avant platform is equipped with several security features to protect and help customers secure their design. The high-level security features are:

- Bitstream Encryption
- Bitstream Authentication
- User-accessible security APIs (supported in Avant-AT-X family only)
- Physically Unclonable Function (PUF)
- Resistance to side channel analysis (SCA) and fault injection attack (FIA)
- Anti-tamper remedies, such as zeroing of storage (key storage, BBRAM, OTP) used for sensitive information storing such as keys (supported in Avant-AT-X family only).

Security support varies by family. See the Features section for details of security support in a specific family.

These security features are a significant step up in capabilities and performance compared to existing products.

Lattice Avant security engine provides several cryptographic features that customers could utilize in their design. Some of the key cryptographic features include Advanced Encryption Standard (AES), Hashing Algorithms, and true random number generator (TRNG). The Lattice Avant device also features bitstream encryption (using AES-256-GCM), used for protecting confidential FPGA bitstream data, and bitstream authentication (using ECDSA and RSA), which maintains bitstream integrity and protects the FPGA design bitstream from copying and tampering.

The security engine is responsible for the bitstream encryption as well as authentication of the Lattice Avant device. Once the bitstream is authenticated and the device is ready for user functions, the security engine is available for the user to implement various cryptographic functions in the FPGA design. The security engine utilizes a message-passing protocol through a hardware mailbox to provide an interface for calling security API. The security engine receives request messages, translates them into API calls in the Security CPU, and then sends a response message when the requested operation is complete.

The Lattice Avant-AT-X family supports the following encryption algorithms and security functions:

- True Random Number Generator (TRNG)
- AES, side channel attack resistant (256-bit keys, >3.2 Gbps throughput)
- AES, high-speed (256-bit keys, >10 Gbps throughput)
- Secure Hashing Algorithm (up to SHA3 in 512-bit mode)
- Side channel attack resistant Message Authentication Codes (up to HMAC-SHA2 in 512-bit mode)
- Side channel attack resistant RSA (up to 4k)

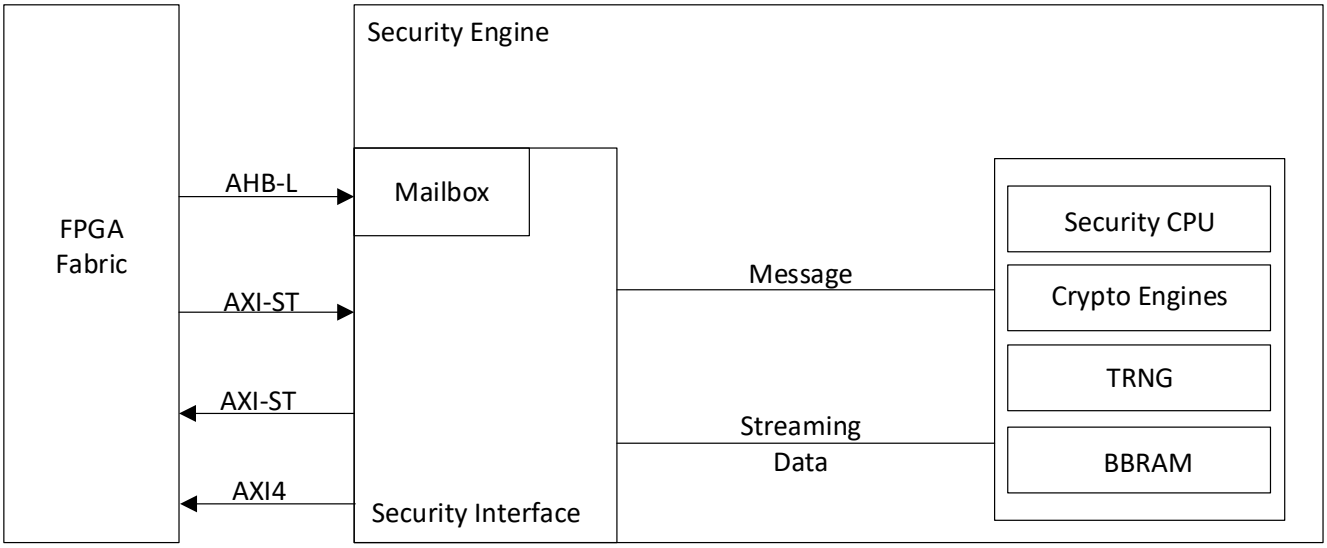


**Figure 2.18. Cryptographic Engine Block Diagram**

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Lattice Avant includes a hardened PUF with 256 bits of entropy and a stable lifetime > 20 years. The PUF provides an unclonable device-unique value which is used to derive device-specific keys for various purpose. This can be used to provide an extra layer of security unique to each device. PUF is located inside the security engine and the data it generates are never exposed outside of security engine.

Lattice Avant security engine has direct access to Battery backed RAM (BBRAM), which can be used as nonvolatile storage for sensitive information. Unlike OTP, BBRAM can be programmed more than once, and the content cannot be easily read through physical inspection. Usage of BBRAM is optional (enabled by a user writable OTP bit). By default, OTP is used for persistent storage of user-programmed secrets (such as customer public key hashes). If BBRAM is enabled, the security engine must use BBRAM instead for user-programmed secrets.

## 2.15. System Monitor/Anti-Tamper Monitor

The Anti-Tamper Monitor (ATM) measures on-die temperatures and voltages of critical power supplies using analog sensors with corresponding ADCs. Each ADC communicates with ATM using digital interface. The main usage of ATM in user application are:

- Provides continuous data samples of voltages and temperatures from multiple locations on the die so that user logic can monitor the status of the device.
- Provide interface to user logic to trigger remedy action!

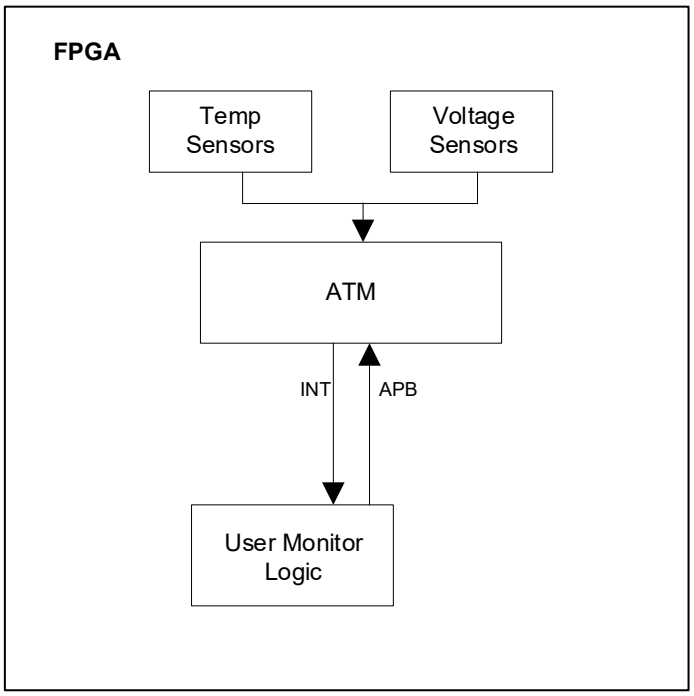


**Figure 2.19. ATM Block Diagram**

User logic can monitor certain power rail voltages and on die temperatures from sensors distributed across the die through ATM. User logic can read sample data through ATM interface and set upper/lower threshold values to trigger alarms through interrupt. User logic can trigger one of fixed set of remedy actions if required, such as zeroization of CRAMs and EBRs, zeroization of user secrets in temporary storage (SRAM) or persistent storage (OTP or BBRAM), even permanently disabling of the device through the fabric interface.

The BBRAM persistent storage is available only in the Avant-AT-X family.

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# 3. Pinout Information

## 3.1. Signal Descriptions

**Table 3.1. Signal Descriptions**

| Signal Name | Bank | Type | Description |
|---|---|---|---|
| **Power and GND** | | | |
| Vss | — | GND | Ground for internal FPGA logic and I/O |
| $V_{SSR}$ | — | GND | Reserved. Connect to Ground. |
| $V_{CC}$ | — | Power | Power supply pins for core logic. $V_{CC}$ is connected to 0.82 V (nom.) supply voltage. Power On Reset (POR) monitors this supply voltage. |
| $V_{CCAUXA}$ | — | Power | Auxiliary power supply pin for internal analog circuitry. This supply is connected to 1.8 V (nom.) supply voltage. POR monitors this supply voltage. |
| $V_{CCAUX}$ | — | Power | Auxiliary power supply. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable drive current for the I/O. |
| $V_{CCJB}$ | — | Power | Boundary Scan data path power supply. These pins should be connected to 0.82 V (nom.) to enable Boundary Scan (BSCAN) shift chain functionality, including SAMPLE, EXTEST, etc. To reduce static power consumption, these pins may be connected to board ground if BSCAN shift chain functionality is not required or no longer required. These pins should not be floated. |
| $V_{CCA_PLLx}$ | — | Power | Used by the PLL blocks. This supply is connected to 0.82 V (nom.) supply voltage. X can be various PLL numberings. |
| $V_{CC_BAT}$ | — | Power | This supply can be connected to 1.5 V (nom.) supply voltage. It allows a battery to be used to keep the volatile RAM configuration when the other DC supply source is absent. |
| $V_{CCIOx}$ | 0-14 | Power | Power supply pins for I/O bank x.<br>For x = 0, 1, 2, 12, 13, and 14, VCCIO can be connected to (nom.) 1.2 V, 1.8 V, 2.5 V, or 3.3 V.<br>For x = 3, 4, 5, 6, 7, 8, 9, 10, and 11, VCCIO can be connected to (nom.) 0.9, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V.<br>There are dedicated and shared configuration pins in banks 1 and 2. POR monitors these banks supply voltages. |
| $V_{CCA_MPQx}$ | — | Power | Power supply for the SERDES blocks.<br>X = 0, 1, 2, 3, 4, 5, 6 |
| $V_{CCH_MPQx}$ | — | Power | Power supply for the SERDES blocks.<br>X = 0, 1, 2, 3, 4, 5, 6 |
| **Dedicated SERDES I/O Pins** | | | |
| MPQx_RXyP/N | MPQ0:6 | Input | SERDES Data Differential Input Pairs. X=0, 1, 2, 3, 4, 5, 6. Y=0, 1, 2, 3 |
| MPQx_TXyDP/N | MPQ0:6 | Output | SERDES Data Differential Output Pairs. X=0, 1, 2, 3, 4, 5, 6. Y=0, 1, 2, 3 |
| MPQx_REFCLKP/N | MPQ0:6 | Input | SERDES Reference Clock Differential Input Pairs. X=0, 1, 2, 3, 4, 5, 6 |
| REXT_MPQx | MPQ0:6 | Input | SERDES External Reference Resistor Input. This is used to adjust the on-chip differential termination impedance, based on the external resistance value. X=0, 1, 2, 3, 4, 5, 6 |
| **Misc Pins** | | | |
| NC | | — | No connect. |

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| Signal Name | Bank | Type | Description |
|---|---|---|---|
| **General Purpose I/O Pins** | | | |
| WRIO[BankNumber]_[Number] [A/B] | 0, 1, 2, 12, 13, 14 | Input, Output, Bi-Dir | Programmable Wide Range User I/O:<br>[BankNumber] indicates the package pin/ball is in the bank specified.<br>[Number] identifies the PIO [A/B] pair.<br>[A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair.<br>Each A/B pair in the top bank does not support true differential input or output buffer. It supports all single-ended inputs and outputs and can be used for emulated differential output buffer.<br>Some of these user programmable I/O are used during configuration, depending on the configuration mode. The user needs to make appropriate connection on the board to isolate the two different functions before/after configuration.<br>During configuration the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and default to have weak pull-down enabled after configuration. |
| HPIO[BankNumber]_[Number] [A/B] | 3, 4, 5, 6, 7, 8, 9, 10, 11 | Input, Output, Bi-Dir | Programmable High-Performance User I/O:<br>[BankNumber] indicates the package pin/ball is in the bank specified.<br>[Number] identifies the PIO [A/B] pair.<br>[A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair.<br>Each A/B pair supports true differential input and output buffers. When configured as differential input, differential termination of 100 Ω can be selected.<br>During configuration the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and default to have weak pull-down enabled after configuration. |
| **Shared Configuration Pins**<br>**1. These pins can be used for configuration during configuration mode. When configuration is completed, these pins can be used as GPIO, or shared function in GPIO. When these pins are used in dual function, the user needs to isolate the signal paths for the dual functions on the board.**<br>**2. The pins used are defined by the configuration modes detected. Target SPI modes are detected during target activation. Pins that are not used in the configuration mode selected are tri-stated during configuration and can connect directly as GPIO in user's function.** | | | |
| WRIO2_yy/SDQ0:7 | 2 | Input, Output, Bi-Dir | Configuration:<br>Target SPI Mode: Slave Parallel Data<br>User Mode:<br>WRIO2_yy: GPIO |
| WRIO2_yy/SSDO | 2 | Input, Output, Bi-Dir | Configuration:<br>Target SPI Mode: Slave Serial Output<br>User Mode:<br>WRIO2_yy: GPIO |
| WRIO2_yy/SCSN | 2 | Input, Output, Bi-Dir | Configuration:<br>Target SPI Mode: Slave Chip Select, asserted low<br>User Mode:<br>WRIO2_yy: GPIO |
| WRIO2_yy/SCLK | 2 | Input, Output, Bi-Dir | Configuration:<br>Target SPI Mode: Slave Clock Input<br>User Mode:<br>WRIO2_yy: GPIO |

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| Signal Name | Bank | Type | Description |
|---|---|---|---|
| WRIO2_yy/SDS | 2 | Input, Output, Bi-Dir | Configuration:<br>Target SPI Mode: Slave Data Strobe<br>User Mode:<br>WRIO2_yy: GPIO |
| WRIO1_yy/MCSN | 1 | Input, Output, Bi-Dir | Configuration:<br>Controller SPI Mode: Master Chip Select, asserted low<br>User Mode:<br>WRIO1_yy: GPIO |
| WRIO1_yy/MSDO | 1 | Input, Output, Bi-Dir | Configuration:<br>Controller SPI Mode: Master Serial Data Out<br>User Mode:<br>WRIO1_yy: GPIO |
| WRIO1_yy/MDS | 1 | Input, Output, Bi-Dir | Configuration:<br>Controller SPI Mode: Master Data Strobe<br>User Mode:<br>WRIO1_yy: GPIO |
| WRIO1_yy/MDQ0:7 | 1 | Input, Output, Bi-Dir | Configuration:<br>Controller SPI Mode: Master Parallel Data<br>User Mode:<br>WRIO1_yy: GPIO |
| WRIO1_yy/MCLK | 1 | Input, Output, Bi-Dir | Configuration:<br>Controller SPI Mode: Master Clock Output<br>User Mode:<br>WRIO1_yy: GPIO |
| WRIO1_yy/MCLKN | 1 | Input, Output, Bi-Dir | Configuration:<br>Controller SPI Mode: Master Clock Output, compliment<br>User Mode:<br>WRIO1_yy: GPIO |
| WRIO1_yy/MRSTN | 1 | Input, Output, Bi-Dir | Configuration:<br>Controller SPI Mode: Master SPI Reset Output, asserted low<br>User Mode:<br>WRIO1_yy: GPIO |
| **Dedicated Pins**<br>**1. Dedicated pins are used for specific configuration functions** | | | |
| **Dedicated Pins** | | | |
| TDO | 2 | Output | Used as TDO signal for JTAG |
| TDI | 2 | Input | Used as TDI signal for JTAG |
| TMS | 2 | Input | Used as TMS signal for JTAG |
| TCK | 2 | Input | Used as TCK signal for JTAG |
| CFGMODE | 2 | Input | When low, enables JTAG and SSPI modes. When high, enables MSPI mode. |
| PROGRAMN | 2 | Input | Initiate configuration sequence when asserted LOW. |
| INITN | 2 | Input, Output, Bi-Dir | Open Drain I/O pin. This signal is driven to LOW when configuration sequence is started, to indicate the device is in initialization state. This signal is released after initialization is completed, and the configuration download can start. You can keep drive this signal LOW to delay configuration download to start. |

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| Signal Name | Bank | Type | Description |
|---|---|---|---|
| DONE | 2 | Input, Output, Bi-Dir | Open Drain I/O pin. This signal is driven to LOW during configuration time. It is released to indicate the device has completed configuration. You can keep drive this signal LOW to delay the device to wake up from configuration. |
| ERASEKEY | 1 | Input | When enabled by *Erase_Key_Pin_EN* Device Features OTP bit, triggers erase of BBRAM and OTP security key when driven high for at least 350 ms. When not used, it must be pulled low. Refer to the Lattice Avant Device Security User Guide (FPGA-TN-02337) for further information. |
| EXT_RES[3,4,5,6,7,8,9,10,11] | 3, 4, 5, 6, 7, 8, 9, 10, 11 | Input | EXT_RES: External reference resistor for HPIO bank<br>[3,4,5,6,7,8,9,10,11] = HPIO Bank number |
| **Shared CLOCK Pins**<br>**1. Some PCLK pins can also be used as GPLL reference clock input pin. Refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).** | | | |
| WRIOx_zz/PCLK[R]T[0,1,2]_[0,1]/yyyy | 0, 1, 2, 12, 13, 14 | Input, Output, Bi-Dir | User Mode:<br>WRIOx_zz: GPIO<br>PCLK: Primary Clock Refclk signal<br>[0,1,2,12,13,14] = Bank<br>[0,1] Up to 2 signals in the bank<br>yyyy: Other possible selectable specific functional |
| WRIOx_zz/PLLT[FB][0,12]_IN/yyyy | 0, 12 | Input, Output, Bi-Dir | User Mode:<br>HPIOx_zz: GPIO<br>PLL: PLL signal<br>[0,12] = Bank<br>[FB] Used if input is for PLL feedback<br>yyyy: Other possible selectable specific functional |
| HPIOx_zz/PCLK[R][T,C][3,4,5,6,7,8,9,10,11]_[0,1,2,3]/yyyy | 3, 4, 5, 6, 7, 8, 9, 10, 11 | Input, Output, Bi-Dir | User Mode:<br>HPIOx_zz: GPIO<br>PCLK: Primary Clock Refclk signal<br>[T] = For single-ended signaling, use only PCLKT pins as primary CLK pads.<br>[T,C] = True or Complement if using differential signaling<br>[3,4,5,6,7,8,9,10,11] = Bank<br>[0,1,2,3] Up to 4 signals in bank |
| HPIOx_zz/PLL[T,C][3,4,5,6,7,8,9,10,11]_IN | 3, 4, 5, 6, 7, 8, 9, 10, 11 | Input, Output, Bi-Dir | User Mode:<br>HPIOx_zz: GPIO<br>PLL: PLL input signal<br>[T] = For single-ended signaling, use only PCLKT pins as primary CLK pads.<br>[T,C] = True or Complement if using differential signaling<br>[3,4,5,6,7,8,9,10,11] = Bank |
| **Shared Reference Pins** | | | |
| HPIOx_zz/VREF[3,4,5,6,7,8,9,10,11] | 3, 4, 5, 6, 7, 8, 9, 10, 11 | Input, Output, Bi-Dir | User Mode:<br>HPIOx_zz: GPIO<br>VREF: External voltage reference for SSTL/HSUL standards<br>[3,4,5,6,7,8,9,10,11] = Bank |

**Note:**

1. Not all signals are available as external pins in all packages. Refer to the Pinout List file for various package details.

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# 3.2. Pin Information Summary

## 3.2.1. Lattice Avant-AT-E Family

**Table 3.2. Lattice Avant-AT-E Family**

| Pin Information Summary | | LAV-AT-E30 | | LAV-AT-E50 | | LAV-AT-E70 | | | | LAV-AT-E70B | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | CBG484 | CBG484 | CSG841 | CBG484 | CSG841 | LFG676 | LFG1156 | LFG676 | LFG1156 |
| **User I/O Pins** | | | | | | | | | | | |
| Wide Range Inputs/Outputs per Bank | Bank 0 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 15 | 15 |
| | Bank 1 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 |
| | Bank 2 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| | Bank 12 | 16 | 16 | 16 | 16 | 16 | 16 | 0 | 16 | 0 | 16 |
| | Bank 13 | 16 | 16 | 16 | 16 | 16 | 16 | 0 | 16 | 0 | 16 |
| | Bank 14 | 20 | 20 | 20 | 20 | 20 | 20 | 0 | 20 | 0 | 20 |
| Total Wide Range User I/O | | 95 | 95 | 95 | 95 | 95 | 95 | 43 | 95 | 42 | 94 |
| High Performance Input/Output (Pairs) | Bank 3 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 4 | — | — | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) |
| | Bank 5 | — | — | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) |
| | Bank 6 | — | — | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) |
| | Bank 7 | — | — | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) | 0 | 51 (25) |
| | Bank 8 | — | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 9 | — | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 10 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 11 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| Total High Performance I/O (Pairs) | | 153 (75) | 255 (125) | 153 (75) | 459 (225) | 255 (125) | 459 (225) | 255 (125) | 459 (225) | 255 (125) | 459 (225) |
| **Power Pins** | | | | | | | | | | | |
| $V_{CC}$ | | 40 | 40 | 24 | 48 | 24 | 48 | 26 | 24 | 26 | 24 |
| $V_{CC_PLL}$, $V_{CC_PLL_W}$ | | 5 | 4 | 4 | 7 | 4 | 7 | 4 | 4 | 4 | 4 |
| $V_{CC_BAT}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $V_{CCAUXA}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $V_{CCAUX}$ | | 11 | 3 | 3 | 7 | 3 | 7 | 4 | 3 | 4 | 3 |
| $V_{CCJB}$ | | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 23 | 44 |
| $V_{CCIO}$ | Bank 0 | 1 | 2 | 2 | 2 | 2 | 2 | 3 | 3 | 3 | 3 |
| | Bank 1 | 1 | 2 | 2 | 3 | 2 | 3 | 3 | 3 | 3 | 3 |
| | Bank 2 | 2 | 2 | 2 | 3 | 2 | 3 | 3 | 3 | 3 | 3 |
| | Bank 3 | 2 | 4 | 4 | 7 | 4 | 7 | 4 | 4 | 4 | 4 |
| | Bank 4 | — | — | 0 | 7 | 0 | 7 | 0 | 4 | 0 | 4 |
| | Bank 5 | — | — | 0 | 7 | 0 | 7 | 0 | 4 | 0 | 4 |
| | Bank 6 | — | — | 0 | 7 | 0 | 7 | 0 | 4 | 0 | 4 |
| | Bank 7 | — | — | 0 | 8 | 0 | 8 | 0 | 4 | 0 | 4 |
| | Bank 8 | — | 4 | 4 | 9 | 4 | 9 | 4 | 4 | 4 | 4 |
| | Bank 9 | — | 4 | 4 | 9 | 4 | 9 | 4 | 4 | 4 | 4 |
| | Bank 10 | 2 | 4 | 4 | 8 | 4 | 8 | 4 | 4 | 4 | 4 |
| | Bank 11 | 2 | 4 | 4 | 8 | 4 | 8 | 4 | 4 | 4 | 4 |
| | Bank 12 | 1 | 3 | 3 | 3 | 3 | 3 | 0 | 3 | 0 | 3 |
| | Bank 13 | 1 | 3 | 3 | 3 | 3 | 3 | 0 | 3 | 0 | 3 |
| | Bank 14 | 1 | 3 | 3 | 3 | 3 | 3 | 0 | 3 | 0 | 3 |
| Total Power Pins | | 70 | 68 | 68 | 151 | 68 | 151 | 65 | 87 | 88 | 131 |
| **GND and NC Pins** | | | | | | | | | | | |
| Vss | | 80 | 52 | 52 | 118 | 52 | 118 | 176 | 281 | 176 | 281 |
| $V_{SSR}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 88 | 154 | 66 | 111 |
| NC | | 0 | 0 | 0 | 0 | 0 | 0 | 36 | 63 | 36 | 63 |

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| Pin Information Summary | | LAV-AT-E30 | | LAV-AT-E50 | | LAV-AT-E70 | | | | LAV-AT-E70B | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | CBG484 | CBG484 | CSG841 | CBG484 | CSG841 | LFG676 | LFG1156 | LFG676 | LFG1156 |
| **Dedicated Misc Pins** | | | | | | | | | | | |
| JTAG (TDI, TDO, TCK, TMS) | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| PROGRAMN | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| CFGMODE | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| DONE | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INITN | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| EXT_RESn | | 3 | 5 | 5 | 9 | 5 | 9 | 5 | 9 | 5 | 9 |
| Total Dedicated Pins | | 11 | 13 | 13 | 17 | 13 | 17 | 13 | 17 | 13 | 17 |
| **Shared Pins** | | | | | | | | | | | |
| Shared Configuration Pins | Bank 1 | 13 | 13 | 13 | 13 | 13 | 13 | 13 | 13 | 13 | 13 |
| | Bank 2 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| Shared PCLK Pins | Bank 0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Bank 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 3 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 4 | 0 | 0 | 0 | 8 | 0 | 8 | 0 | 8 | 0 | 8 |
| | Bank 5 | 0 | 0 | 0 | 8 | 0 | 8 | 0 | 8 | 0 | 8 |
| | Bank 6 | 0 | 0 | 0 | 8 | 0 | 8 | 0 | 8 | 0 | 8 |
| | Bank 7 | 0 | 0 | 0 | 8 | 0 | 8 | 0 | 8 | 0 | 8 |
| | Bank 8 | 0 | 0 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 9 | 0 | 0 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 10 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 11 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 12 | 2 | 2 | 2 | 2 | 2 | 2 | 0 | 2 | 0 | 2 |
| | Bank 13 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| | Bank 14 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| Shared Reference Pins | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 4 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | Bank 5 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | Bank 6 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | Bank 7 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| | Bank 8 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 10 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 11 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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## 3.2.2. Lattice Avant-AT-G Family

**Table 3.3. Lattice Avant-AT-G Family**

| Pin Information Summary | | LAV-AT-G30 | | | LAV-AT-G50 | | LAV-AT-G70 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | FBG644 | LFG676 | LFG676 | FBG644 | LFG676 | LFG1156 | FBG644 |
| **User I/O Pins** | | | | | | | | | |
| Wide Range Inputs/Outputs per Bank | Bank 0 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| | Bank 1 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 |
| | Bank 2 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 20 | 0 |
| Total Wide Range User I/O | | 43 | 43 | 43 | 43 | 43 | 43 | 95 | 43 |
| High Performance Input/Output (Pairs) | Bank 3 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 8 | 0 | 51 (25) | 51 (25) | 51 (25) | 12 (6) | 51 (25) | 51 (25) | 12 (6) |
| | Bank 9 | 0 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 10 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 11 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| Total High Performance I/O (Pairs) | | 153 (75) | 255 (125) | 255 (125) | 255 (125) | 216 (106) | 255 (125) | 459 (225) | 216 (106) |
| **Power Pins** | | | | | | | | | |
| $V_{CC}$ | | 58 | 32 | 26 | 26 | 55 | 26 | 24 | 55 |
| $V_{CC_PLL}$, $V_{CC_PLL_W}$ | | 3 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| $V_{CC_BAT}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $V_{CCAUXA}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $V_{CCAUX}$ | | 9 | 4 | 4 | 4 | 3 | 4 | 3 | 3 |
| $V_{CCIO}$ | Bank 0 | 1 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Bank 1 | 1 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Bank 2 | 1 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Bank 3 | 2 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 8 | 0 | 4 | 4 | 4 | 2 | 4 | 4 | 2 |
| | Bank 9 | 0 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 10 | 2 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 11 | 2 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 |
| Total Non-SERDES Power Pins | | 81 | 71 | 65 | 65 | 95 | 65 | 87 | 95 |
| $V_{CCA_MPQ}$ | Bank 0 | 5 | 6 | 6 | 6 | 4 | 6 | 6 | 4 |
| | Bank 1 | 0 | 4 | 4 | 4 | 0 | 4 | 7 | 0 |
| | Bank 2 | 0 | 6 | 6 | 6 | 4 | 6 | 6 | 4 |
| | Bank 3 | 0 | 0 | 0 | 7 | 0 | 7 | 5 | 0 |
| | Bank 4 | 0 | 0 | 0 | 0 | 1 | 0 | 6 | 1 |
| | Bank 5 | 0 | 0 | 0 | 0 | 1 | 0 | 6 | 1 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |

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| Pin Information Summary | | LAV-AT-G30 | | | LAV-AT-G50 | | LAV-AT-G70 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | FBG644 | LFG676 | LFG676 | FBG644 | LFG676 | LFG1156 | FBG644 |
| $V_{CCH_MPQ}$ | Bank 0 | 3 | 6 | 6 | 6 | 2 | 6 | 5 | 2 |
| | Bank 1 | 0 | 5 | 5 | 5 | 0 | 5 | 6 | 0 |
| | Bank 2 | 0 | 7 | 6 | 6 | 2 | 6 | 5 | 2 |
| | Bank 3 | 0 | 0 | 0 | 7 | 0 | 7 | 5 | 0 |
| | Bank 4 | 0 | 0 | 0 | 0 | 1 | 0 | 5 | 1 |
| | Bank 5 | 0 | 0 | 0 | 0 | 1 | 0 | 6 | 1 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 7 | 0 |
| Total All Power Pins | | 89 | 105 | 98 | 112 | 111 | 112 | 170 | 111 |
| **GND and NC Pins** | | | | | | | | | |
| Vss | | 94 | 165 | 151 | 176 | 201 | 176 | 281 | 201 |
| NC | | — | 5 | 58 | — | — | — | — | — |
| **SERDES Pins** | | | | | | | | | |
| Dedicated SERDES Data Channels (pairs) | | 8 | 24 | 24 | 32 | 24 | 32 | 56 | 24 |
| Dedicated SERDES Clock (pairs) | | 1 | 3 | 3 | 4 | 4 | 4 | 7 | 4 |
| Dedicated SERDES Resistor Reference (single) | | 1 | 3 | 3 | 4 | 4 | 4 | 7 | 4 |
| **Dedicated Misc Pins** | | | | | | | | | |
| JTAG (TDI, TDO, TCK, TMS) | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| PROGRAMN | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| CFGMODE | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| DONE | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INITN | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ERASEKEY | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| EXT_RESn | | 3 | 5 | 5 | 5 | 4 | 5 | 9 | 4 |
| Total Dedicated Pins | | 12 | 14 | 14 | 14 | 13 | 14 | 18 | 13 |
| **Shared Pins** | | | | | | | | | |
| Shared Configuration Pins | Bank 1 | 13 | 13 | 13 | 13 | 13 | 13 | 13 | 13 |
| | Bank 2 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| Shared PCLK Pins | Bank 0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Bank 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 3 | 8 | 8 | 8 | 8 | 5 | 8 | 8 | 5 |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 8 | 0 | 8 | 8 | 8 | 0 | 8 | 8 | 0 |
| | Bank 9 | 0 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 10 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 11 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

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| Pin Information Summary | | LAV-AT-G30 | | | LAV-AT-G50 | | LAV-AT-G70 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | FBG644 | LFG676 | LFG676 | FBG644 | LFG676 | LFG1156 | FBG644 |
| Shared Reference Pins | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 8 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| | Bank 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 10 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 11 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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## 3.2.3. Lattice Avant-AT-X Family

**Table 3.4. Lattice Avant-AT-X Family**

| Pin Information Summary | | LAV-AT-X30 | | | LAV-AT-X50 | | LAV-AT-X70 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | FBG644 | LFG676 | LFG676 | FBG644 | LFG676 | LFG1156 | FBG644 |
| **User I/O Pins** | | | | | | | | | |
| Wide Range Inputs/Outputs per Bank | Bank 0 | 16 | 16 | 16 | 16 | 16 | 16 | 16 | 16 |
| | Bank 1 | 15 | 15 | 15 | 15 | 15 | 15 | 15 | 15 |
| | Bank 2 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 16 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 20 | 0 |
| Total Wide Range User I/O | | 43 | 43 | 43 | 43 | 43 | 43 | 95 | 43 |
| High Performance Input/Output (Pairs) | Bank 3 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 51 (25) | 0 |
| | Bank 8 | 0 | 51 (25) | 51 (25) | 51 (25) | 12 (6) | 51 (25) | 51 (25) | 12 (6) |
| | Bank 9 | 0 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 10 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| | Bank 11 | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) | 51 (25) |
| Total High Performance I/O (Pairs) | | 153 (75) | 255 (125) | 255 (125) | 255 (125) | 216 (106) | 255 (125) | 459 (225) | 216 (106) |
| **Power Pins** | | | | | | | | | |
| $V_{CC}$ | | 58 | 32 | 26 | 26 | 55 | 26 | 24 | 55 |
| $V_{CC_PLL}$, $V_{CC_PLL_W}$ | | 3 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| $V_{CC_BAT}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $V_{CCAUXA}$ | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| $V_{CCAUX}$ | | 9 | 4 | 4 | 4 | 3 | 4 | 3 | 3 |
| $V_{CCIO}$ | Bank 0 | 1 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Bank 1 | 1 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Bank 2 | 1 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| | Bank 3 | 2 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 4 | 0 |
| | Bank 8 | 0 | 4 | 4 | 4 | 2 | 4 | 4 | 2 |
| | Bank 9 | 0 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 10 | 2 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 11 | 2 | 4 | 4 | 4 | 5 | 4 | 4 | 5 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 3 | 0 |
| Total Non-SERDES Power Pins | | 81 | 71 | 65 | 65 | 95 | 65 | 87 | 95 |
| $V_{CCA_MPQ}$ | Bank 0 | 5 | 6 | 6 | 6 | 4 | 6 | 6 | 4 |
| | Bank 1 | 0 | 4 | 4 | 4 | 0 | 4 | 7 | 0 |
| | Bank 2 | 0 | 6 | 6 | 6 | 4 | 6 | 6 | 4 |
| | Bank 3 | 0 | 0 | 0 | 7 | 0 | 7 | 5 | 0 |
| | Bank 4 | 0 | 0 | 0 | 0 | 1 | 0 | 6 | 1 |
| | Bank 5 | 0 | 0 | 0 | 0 | 1 | 0 | 6 | 1 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |

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| Pin Information Summary | | LAV-AT-X30 | | | LAV-AT-X50 | | LAV-AT-X70 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | FBG644 | LFG676 | LFG676 | FBG644 | LFG676 | LFG1156 | FBG644 |
| $V_{CCH_MPQ}$ | Bank 0 | 3 | 6 | 6 | 6 | 2 | 6 | 5 | 2 |
| | Bank 1 | 0 | 5 | 5 | 5 | 0 | 5 | 6 | 0 |
| | Bank 2 | 0 | 7 | 6 | 6 | 2 | 6 | 5 | 2 |
| | Bank 3 | 0 | 0 | 0 | 7 | 0 | 7 | 5 | 0 |
| | Bank 4 | 0 | 0 | 0 | 0 | 1 | 0 | 5 | 1 |
| | Bank 5 | 0 | 0 | 0 | 0 | 1 | 0 | 6 | 1 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 7 | 0 |
| Total All Power Pins | | 89 | 105 | 98 | 112 | 111 | 112 | 170 | 111 |
| **GND and NC Pins** | | | | | | | | | |
| Vss | | 94 | 165 | 151 | 176 | 201 | 176 | 281 | 201 |
| NC | | — | 5 | 58 | — | — | — | — | — |
| **SERDES Pins** | | | | | | | | | |
| Dedicated SERDES Data Channels (pairs) | | 8 | 24 | 24 | 32 | 24 | 32 | 56 | 24 |
| Dedicated SERDES Clock (pairs) | | 1 | 3 | 3 | 4 | 4 | 4 | 7 | 4 |
| Dedicated SERDES Resistor Reference (single) | | 1 | 3 | 3 | 4 | 4 | 4 | 7 | 4 |
| **Dedicated Misc Pins** | | | | | | | | | |
| JTAG (TDI, TDO, TCK, TMS) | | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| PROGRAMN | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| CFGMODE | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| DONE | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| INITN | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| ERASEKEY | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| EXT_RESn | | 3 | 5 | 5 | 5 | 4 | 5 | 9 | 4 |
| Total Dedicated Pins | | 12 | 14 | 14 | 14 | 13 | 14 | 18 | 13 |
| **Shared Pins** | | | | | | | | | |
| Shared Configuration Pins | Bank 1 | 13 | 13 | 13 | 13 | 13 | 13 | 13 | 13 |
| | Bank 2 | 12 | 12 | 12 | 12 | 12 | 12 | 12 | 12 |
| Shared PCLK Pins | Bank 0 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| | Bank 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 2 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 3 | 8 | 8 | 8 | 8 | 5 | 8 | 8 | 5 |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 0 |
| | Bank 8 | 0 | 8 | 8 | 8 | 0 | 8 | 8 | 0 |
| | Bank 9 | 0 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 10 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 11 | 8 | 8 | 8 | 8 | 8 | 8 | 8 | 8 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 2 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

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| Pin Information Summary | | LAV-AT-X30 | | | LAV-AT-X50 | | LAV-AT-X70 | | |
|---|---|---|---|---|---|---|---|---|---|
| | | ASGA410 | FBG644 | LFG676 | LFG676 | FBG644 | LFG676 | LFG1156 | FBG644 |
| Shared Reference Pins | Bank 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 2 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 3 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 4 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 5 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 6 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 7 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| | Bank 8 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| | Bank 9 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 10 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 11 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| | Bank 12 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 13 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Bank 14 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

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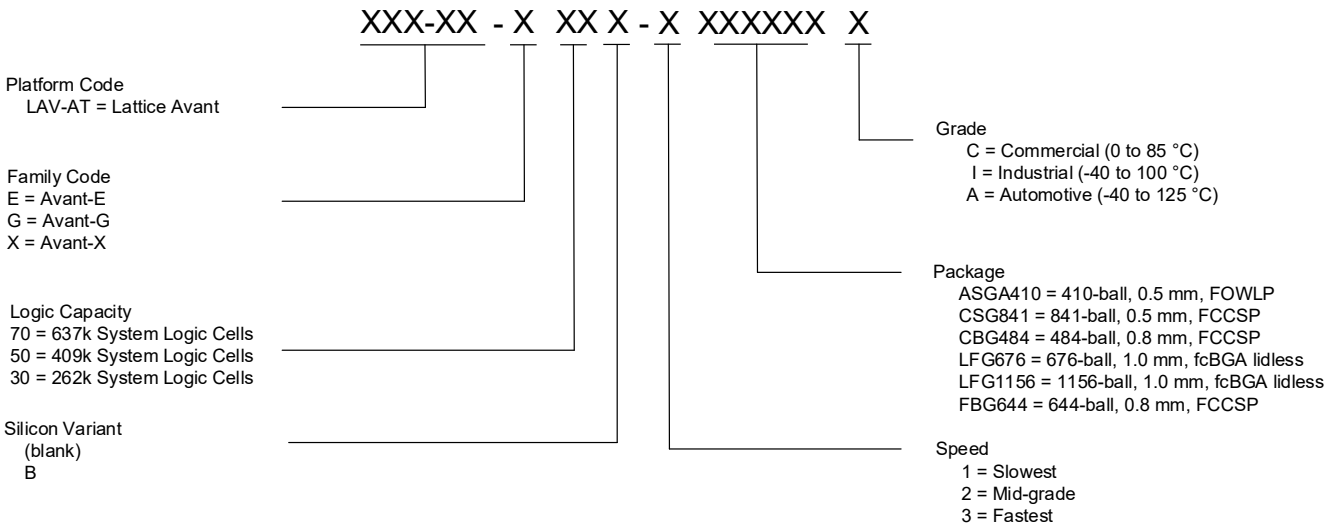
# 4. Ordering Information

Lattice provides a wide variety of services for its products including custom marking, factory programming, known good die, and application specific testing. Contact the local sales representatives for more details.

## 4.1. Lattice Avant Part Number Description

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## 4.2. Ordering Part Numbers

### 4.2.1. Commercial

**Table 4.1. Commercial Part Numbers**

| Part Number | Speed | Package | Pins | Grade | System Logic Cells (k) |
|---|---|---|---|---|---|
| LAV-AT-E70-1CBG484C | 1 | CBG484 | 484 | Commercial | 637 |
| LAV-AT-E70-2CBG484C | 2 | CBG484 | 484 | Commercial | 637 |
| LAV-AT-E70-3CBG484C | 3 | CBG484 | 484 | Commercial | 637 |
| LAV-AT-E70-1LFG676C | 1 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-E70-2LFG676C | 2 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-E70-3LFG676C | 3 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-E70-1CSG841C | 1 | CSG841 | 841 | Commercial | 637 |
| LAV-AT-E70-2CSG841C | 2 | CSG841 | 841 | Commercial | 637 |
| LAV-AT-E70-3CSG841C | 3 | CSG841 | 841 | Commercial | 637 |
| LAV-AT-E70-1LFG1156C | 1 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-E70-2LFG1156C | 2 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-E70-3LFG1156C | 3 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-E70B-1LFG1156C | 1 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-E70B-2LFG1156C | 2 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-E70B-3LFG1156C | 3 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-G70-1LFG676C | 1 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-G70-2LFG676C | 2 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-G70-3LFG676C | 3 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-G70-1LFG1156C | 1 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-G70-2LFG1156C | 2 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-G70-3LFG1156C | 3 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-G70-1FBG644C | 1 | FBG644 | 644 | Commercial | 637 |
| LAV-AT-G70-2FBG644C | 2 | FBG644 | 644 | Commercial | 637 |
| LAV-AT-G70-3FBG644C | 3 | FBG644 | 644 | Commercial | 637 |
| LAV-AT-X70-1LFG676C | 1 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-X70-2LFG676C | 2 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-X70-3LFG676C | 3 | LFG676 | 676 | Commercial | 637 |
| LAV-AT-X70-1LFG1156C | 1 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-X70-2LFG1156C | 2 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-X70-3LFG1156C | 3 | LFG1156 | 1156 | Commercial | 637 |
| LAV-AT-X70-1FBG644C | 1 | FBG644 | 644 | Commercial | 637 |
| LAV-AT-X70-2FBG644C | 2 | FBG644 | 644 | Commercial | 637 |
| LAV-AT-X70-3FBG644C | 3 | FBG644 | 644 | Commercial | 637 |
| LAV-AT-E50-1CBG484C | 1 | CBG484 | 484 | Commercial | 409 |
| LAV-AT-E50-2CBG484C | 2 | CBG484 | 484 | Commercial | 409 |
| LAV-AT-E50-3CBG484C | 3 | CBG484 | 484 | Commercial | 409 |
| LAV-AT-G50-1LFG676C | 1 | LFG676 | 676 | Commercial | 409 |
| LAV-AT-G50-2LFG676C | 2 | LFG676 | 676 | Commercial | 409 |
| LAV-AT-G50-3LFG676C | 3 | LFG676 | 676 | Commercial | 409 |
| LAV-AT-G50-1FBG644C | 1 | FBG644 | 644 | Commercial | 409 |
| LAV-AT-G50-2FBG644C | 2 | FBG644 | 644 | Commercial | 409 |
| LAV-AT-G50-3FBG644C | 3 | FBG644 | 644 | Commercial | 409 |
| LAV-AT-X50-1LFG676C | 1 | LFG676 | 676 | Commercial | 409 |

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| Part Number | Speed | Package | Pins | Grade | System Logic Cells (k) |
|---|---|---|---|---|---|
| LAV-AT-X50-2LFG676C | 2 | LFG676 | 676 | Commercial | 409 |
| LAV-AT-X50-3LFG676C | 3 | LFG676 | 676 | Commercial | 409 |
| LAV-AT-X50-1FBG644C | 1 | FBG644 | 644 | Commercial | 409 |
| LAV-AT-X50-2FBG644C | 2 | FBG644 | 644 | Commercial | 409 |
| LAV-AT-X50-3FBG644C | 3 | FBG644 | 644 | Commercial | 409 |
| LAV-AT-E30-1ASGA410C | 1 | ASGA410 | 410 | Commercial | 262 |
| LAV-AT-E30-2ASGA410C | 2 | ASGA410 | 410 | Commercial | 262 |
| LAV-AT-E30-3ASGA410C | 3 | ASGA410 | 410 | Commercial | 262 |
| LAV-AT-E30B-1ASGA410C | 1 | ASGA410 | 410 | Commercial | 262 |
| LAV-AT-E30B-2ASGA410C | 2 | ASGA410 | 410 | Commercial | 262 |
| LAV-AT-E30B-3ASGA410C | 3 | ASGA410 | 410 | Commercial | 262 |
| LAV-AT-E30-1CBG484C | 1 | CBG484 | 484 | Commercial | 262 |
| LAV-AT-E30-2CBG484C | 2 | CBG484 | 484 | Commercial | 262 |
| LAV-AT-E30-3CBG484C | 3 | CBG484 | 484 | Commercial | 262 |
| LAV-AT-G30-1ASGA410C | 1 | ASG410 | 410 | Commercial | 262 |
| LAV-AT-G30-2ASGA410C | 2 | ASG410 | 410 | Commercial | 262 |
| LAV-AT-G30-3ASGA410C | 3 | ASG410 | 410 | Commercial | 262 |
| LAV-AT-G30-1LFG676C | 1 | LFG676 | 676 | Commercial | 262 |
| LAV-AT-G30-2LFG676C | 2 | LFG676 | 676 | Commercial | 262 |
| LAV-AT-G30-3LFG676C | 3 | LFG676 | 676 | Commercial | 262 |
| LAV-AT-G30-1FBG644C | 1 | FBG644 | 644 | Commercial | 262 |
| LAV-AT-G30-2FBG644C | 2 | FBG644 | 644 | Commercial | 262 |
| LAV-AT-G30-3FBG644C | 3 | FBG644 | 644 | Commercial | 262 |
| LAV-AT-X30-1ASGA410C | 1 | ASG410 | 410 | Commercial | 262 |
| LAV-AT-X30-2ASGA410C | 2 | ASG410 | 410 | Commercial | 262 |
| LAV-AT-X30-3ASGA410C | 3 | ASG410 | 410 | Commercial | 262 |
| LAV-AT-X30-1LFG676C | 1 | LFG676 | 676 | Commercial | 262 |
| LAV-AT-X30-2LFG676C | 2 | LFG676 | 676 | Commercial | 262 |
| LAV-AT-X30-3LFG676C | 3 | LFG676 | 676 | Commercial | 262 |
| LAV-AT-X30-1FBG644C | 1 | FBG644 | 644 | Commercial | 262 |
| LAV-AT-X30-2FBG644C | 2 | FBG644 | 644 | Commercial | 262 |
| LAV-AT-X30-3FBG644C | 3 | FBG644 | 644 | Commercial | 262 |

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### 4.2.2. Industrial

**Table 4.2. Industrial Part Numbers**

| Part Number | Speed | Package | Pins | Grade | System Logic Cells (k) |
|---|---|---|---|---|---|
| LAV-AT-E70-1CBG484I | 1 | CBG484 | 484 | Industrial | 637 |
| LAV-AT-E70-2CBG484I | 2 | CBG484 | 484 | Industrial | 637 |
| LAV-AT-E70-3CBG484I | 3 | CBG484 | 484 | Industrial | 637 |
| LAV-AT-E70-1LFG676I | 1 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-E70-2LFG676I | 2 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-E70-3LFG676I | 3 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-E70-1CSG841I | 1 | CSG841 | 841 | Industrial | 637 |
| LAV-AT-E70-2CSG841I | 2 | CSG841 | 841 | Industrial | 637 |
| LAV-AT-E70-3CSG841I | 3 | CSG841 | 841 | Industrial | 637 |
| LAV-AT-E70-1LFG1156I | 1 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-E70-2LFG1156I | 2 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-E70-3LFG1156I | 3 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-E70B-1LFG1156I | 1 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-E70B-2LFG1156I | 2 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-E70B-3LFG1156I | 3 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-G70-1LFG676I | 1 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-G70-2LFG676I | 2 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-G70-3LFG676I | 3 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-G70-1LFG1156I | 1 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-G70-2LFG1156I | 2 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-G70-3LFG1156I | 3 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-G70-1FBG644I | 1 | FBG644 | 644 | Industrial | 637 |
| LAV-AT-G70-2FBG644I | 2 | FBG644 | 644 | Industrial | 637 |
| LAV-AT-G70-3FBG644I | 3 | FBG644 | 644 | Industrial | 637 |
| LAV-AT-X70-1LFG676I | 1 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-X70-2LFG676I | 2 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-X70-3LFG676I | 3 | LFG676 | 676 | Industrial | 637 |
| LAV-AT-X70-1LFG1156I | 1 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-X70-2LFG1156I | 2 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-X70-3LFG1156I | 3 | LFG1156 | 1156 | Industrial | 637 |
| LAV-AT-X70-1FBG644I | 1 | FBG644 | 644 | Industrial | 637 |
| LAV-AT-X70-2FBG644I | 2 | FBG644 | 644 | Industrial | 637 |
| LAV-AT-X70-3FBG644I | 3 | FBG644 | 644 | Industrial | 637 |
| LAV-AT-E50-1CBG484I | 1 | CBG484 | 484 | Industrial | 409 |
| LAV-AT-E50-2CBG484I | 2 | CBG484 | 484 | Industrial | 409 |
| LAV-AT-E50-3CBG484I | 3 | CBG484 | 484 | Industrial | 409 |
| LAV-AT-G50-1LFG676I | 1 | LFG676 | 676 | Industrial | 409 |
| LAV-AT-G50-2LFG676I | 2 | LFG676 | 676 | Industrial | 409 |
| LAV-AT-G50-3LFG676I | 3 | LFG676 | 676 | Industrial | 409 |
| LAV-AT-G50-1FBG644I | 1 | FBG644 | 644 | Industrial | 409 |
| LAV-AT-G50-2FBG644I | 2 | FBG644 | 644 | Industrial | 409 |
| LAV-AT-G50-3FBG644I | 3 | FBG644 | 644 | Industrial | 409 |
| LAV-AT-X50-1LFG676I | 1 | LFG676 | 676 | Industrial | 409 |
| LAV-AT-X50-2LFG676I | 2 | LFG676 | 676 | Industrial | 409 |
| LAV-AT-X50-3LFG676I | 3 | LFG676 | 676 | Industrial | 409 |

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| Part Number | Speed | Package | Pins | Grade | System Logic Cells (k) |
|---|---|---|---|---|---|
| LAV-AT-X50-1FBG644I | 1 | FBG644 | 644 | Industrial | 409 |
| LAV-AT-X50-2FBG644I | 2 | FBG644 | 644 | Industrial | 409 |
| LAV-AT-X50-3FBG644I | 3 | FBG644 | 644 | Industrial | 409 |
| LAV-AT-E30-1ASGA410I | 1 | ASGA410 | 410 | Industrial | 262 |
| LAV-AT-E30-2ASGA410I | 2 | ASGA410 | 410 | Industrial | 262 |
| LAV-AT-E30-3ASGA410I | 3 | ASGA410 | 410 | Industrial | 262 |
| LAV-AT-E30-1CBG484I | 1 | CBG484 | 484 | Industrial | 262 |
| LAV-AT-E30-2CBG484I | 2 | CBG484 | 484 | Industrial | 262 |
| LAV-AT-E30-3CBG484I | 3 | CBG484 | 484 | Industrial | 262 |
| LAV-AT-G30-1ASGA410I | 1 | ASG410 | 410 | Industrial | 262 |
| LAV-AT-G30-2ASGA410I | 2 | ASG410 | 410 | Industrial | 262 |
| LAV-AT-G30-3ASGA410I | 3 | ASG410 | 410 | Industrial | 262 |
| LAV-AT-G30-1LFG676I | 1 | LFG676 | 676 | Industrial | 262 |
| LAV-AT-G30-2LFG676I | 2 | LFG676 | 676 | Industrial | 262 |
| LAV-AT-G30-3LFG676I | 3 | LFG676 | 676 | Industrial | 262 |
| LAV-AT-G30-1FBG644I | 1 | FBG644 | 644 | Industrial | 262 |
| LAV-AT-G30-2FBG644I | 2 | FBG644 | 644 | Industrial | 262 |
| LAV-AT-G30-3FBG644I | 3 | FBG644 | 644 | Industrial | 262 |
| LAV-AT-X30-1ASGA410I | 1 | ASG410 | 410 | Industrial | 262 |
| LAV-AT-X30-2ASGA410I | 2 | ASG410 | 410 | Industrial | 262 |
| LAV-AT-X30-3ASGA410I | 3 | ASG410 | 410 | Industrial | 262 |
| LAV-AT-X30-1LFG676I | 1 | LFG676 | 676 | Industrial | 262 |
| LAV-AT-X30-2LFG676I | 2 | LFG676 | 676 | Industrial | 262 |
| LAV-AT-X30-3LFG676I | 3 | LFG676 | 676 | Industrial | 262 |
| LAV-AT-X30-1FBG644I | 1 | FBG644 | 644 | Industrial | 262 |
| LAV-AT-X30-2FBG644I | 2 | FBG644 | 644 | Industrial | 262 |
| LAV-AT-X30-3FBG644I | 3 | FBG644 | 644 | Industrial | 262 |

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### 4.2.3. Automotive

**Table 4.3. Automotive Part Numbers**

| Part Number | Speed | Package | Pins | Grade | System Logic Cells (k) |
|---|---|---|---|---|---|
| LAV-AT-E70-1CBG484A | 1 | CBG484 | 484 | Automotive | 637 |
| LAV-AT-E70-1LFG676A | 1 | LFG676 | 676 | Automotive | 637 |
| LAV-AT-E70-1CSG841A | 1 | CSG841 | 841 | Automotive | 637 |
| LAV-AT-E70-1LFG1156A | 1 | LFG1156 | 1156 | Automotive | 637 |
| LAV-AT-G70-1LFG676A | 1 | LFG676 | 676 | Automotive | 637 |
| LAV-AT-G70-1LFG1156A | 1 | LFG1156 | 1156 | Automotive | 637 |
| LAV-AT-G70-1FBG644A | 1 | FBG644 | 644 | Automotive | 637 |
| LAV-AT-X70-1LFG676A | 1 | LFG676 | 676 | Automotive | 637 |
| LAV-AT-X70-1LFG1156A | 1 | LFG1156 | 1156 | Automotive | 637 |
| LAV-AT-X70-1FBG644A | 1 | FBG644 | 644 | Automotive | 637 |
| LAV-AT-E50-1CBG484A | 1 | CBG484 | 484 | Automotive | 409 |
| LAV-AT-G50-1LFG676A | 1 | LFG676 | 676 | Automotive | 409 |
| LAV-AT-G50-1FBG644A | 1 | FBG644 | 644 | Automotive | 409 |
| LAV-AT-X50-1LFG676A | 1 | LFG676 | 676 | Automotive | 409 |
| LAV-AT-X50-1FBG644A | 1 | FBG644 | 644 | Automotive | 409 |
| LAV-AT-E30-1ASGA410A | 1 | ASGA410 | 410 | Automotive | 262 |
| LAV-AT-E30-1CBG484A | 1 | CBG484 | 484 | Automotive | 262 |
| LAV-AT-G30-1ASGA410A | 1 | ASG410 | 410 | Automotive | 262 |
| LAV-AT-G30-1LFG676A | 1 | LFG676 | 676 | Automotive | 262 |
| LAV-AT-G30-1FBG644A | 1 | FBG644 | 644 | Automotive | 262 |
| LAV-AT-X30-1ASGA410A | 1 | ASG410 | 410 | Automotive | 262 |
| LAV-AT-X30-1LFG676A | 1 | LFG676 | 676 | Automotive | 262 |
| LAV-AT-X30-1FBG644A | 1 | FBG644 | 644 | Automotive | 262 |

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# References

- Avant-E web page
- Avant-G web page
- Avant-X web page

A variety of technical notes for the Lattice Avant platform are available.

- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Lattice Avant Configuration Security User Guide (FPGA-TN-02335)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant Device Security User Guide (FPGA-TN-02337)
- Lattice Avant Hardware Checklist (FPGA-TN-02317)
- Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300)
- Lattice Avant Multi-Boot User Guide (FPGA-TN-02314)
- Lattice Avant Power User Guide (FPGA-TN-02291)
- Lattice Avant SED/SEC User Guide (FPGA-TN-02290)
- Lattice Avant SERDES/PCS User Guide (FPGA-TN-02313)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Using TraceID (FPGA-TN-02084)

For more information on Lattice Avant-related IP, reference designs, and board documents, refer to the following pages:

- SGMII and Gb Ethernet PCS IP Core – Lattice Radiant Software (FPGA-IPUG-02077)
- Avant-E Evaluation Board – User Guide (FPGA-EB-02057)
- Avant-G/X Versa Board User Guide (FPGA-EB-02063)
- IP Cores and Reference Designs for Avant Devices
- Kits, Boards, and Demonstration for Avant Devices

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org
- PCI – www.pcisig.com

Other references:

- Lattice Insights for Lattice Semiconductor training courses and learning plans
- Lattice Radiant FPGA design software

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# Revision History

**Revision 1.5, March 2026**

| Section | Change Summary |
|---|---|
| All | Made editorial fixes across the document. |
| Introduction | • Updated System Performance section to add temperature grade and defense grade bullet points, updated some bullet points of *SERDES* and *High-speed and Flexible Programmable I/O* sections, and updated table note to change DDR5 operational range to *>2933 Mbps* and add table note 2 and reference to table note in Table 1.1. Lattice Avant Platform Key Features.<br>• Updated Table 1.2. Lattice Avant Families to add *Anti-Tamper Module* row.<br>• Updated Table 1.3. Lattice Avant-AT-E Family Selection Guide to remove ASG410 package.<br>• Updated Table 1.4. Lattice Avant-AT-G Family Selection Guide and Table 1.5. Lattice Avant-AT-X Family Selection Guide to change ASG410 package to *ASGA410*, add FBG644 package, and remove SERDES table note and references. |
| Architecture | • Updated Overview and RAM Mode section content, including Figure 2.2. High-level Device Floorplan (LAV-AT-E/G/X50 Device).<br>• Updated Clocking Structure section and sub-sections content, including updating the section name and other references from PLL to GPLL.<br>• Updated Table 2.2 sysMEM Block Configurations to add 512 x 72 row.<br>• Updated Figure 2.9. Memory Core Reset to add Flags component.<br>• Updated Programmable I/O (PIO) section content including updating all MIPI references to *MIPI DPHY*.<br>• Updated Programmable I/O Cell (PIC) section content, including updating Figure 2.12. Group of Two High Performance Programmable I/O Cells and Figure 2.13. Wide Range Programmable I/O Cells and updating footnote to change DDR5 operational range to *>2933 Mbps.*<br>• Updated DDR Memory Support section content, including updating Table 2.5. Summary of DDR Standards and Max Rates table note to change DDR5 operational range to *>2933 Mbps*.<br>• Updated Device Configuration section and sub-sections content.<br>• Updated Figure 2.14. SERDES Overview Diagram to change Two Common Refclk to *Common Refclk*.<br>• Updated Table 2.6. SERDES/PCS Supported Protocols to remove PCIe Gen4 row and update row to *PCIe Gen1/2/3/4* and Table 2.7. Lattice Avant SERDES Protocol Width Support to update Ethernet row values and change column name to *Typical Width per Link*.<br>• Updated Pin Migration and System Monitor/Anti-Tamper Monitor section content. |
| Pinout Information | • Updated Table 3.1. Signal Descriptions to update *HPIO[BankNumber]_[Number] [A/B], ERASEKEY*, *EXT_RES[3,4,5,6,7,8,9,10,11]*, *HPIOx_zz/PCLK[R][T,C][3,4,5,6,7,8,9,10,11]_[0,1,2,3]/yyyy*, *HPIOx_zz/PLL[T,C][3,4,5,6,7,8,9,10,11]_IN*, *HPIOx_zz/VREF[3,4,5,6,7,8,9,10,11], WRIO2_yy/SCSN*, *WRIO1_yy/MCSN*, and *WRIO1_yy/MCLKN* Description content and added *WRIO1_yy/MRSTN* row.<br>• Updated LAV-AT-E30 (including removing ASG410), LAV-AT-E50, and LAV-AT-E70 package column values and added LAV-AT-E70B data in Table 3.2. Lattice Avant-AT-E Family.<br>• Updated LAV-AT-G30, LAV-AT-G50, and LAV-AT-G70 package column values including updating ASG410 column name to *ASGA410* and adding FBG644 columns; and added NC row in Table 3.3. Lattice Avant-AT-G Family.<br>• Updated LAV-AT-X30, LAV-AT-X50, and LAV-AT-X70 package column values including updating ASG410 column name to *ASGA410* and adding FBG644 columns; and added NC row in Table 3.4. Lattice Avant-AT-X Family. |

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| Section | Change Summary |
|---|---|
| Ordering Information | • Updated diagram in Lattice Avant Part Number Description to add Automotive grade and FBG644 package.<br>• Updated Commercial table to add LAV-AT-G70/50/30 FBG644 packages and LAV-AT-X70/50/30 FBG644 packages, update ASG410 packages to *ASGA410*, and remove LAV-AT-E30B ASG410 package.<br>• Updated Industrial table to add LAV-AT-G70/50/30 FBG644 packages and LAV-AT-X70/50/30 FBG644 packages and update ASG410 packages to *ASGA410*.<br>• Added Automotive section. |

**Revision 1.4, July 2025**

| Section | Change Summary |
|---|---|
| Introduction | • Updated Table 1.1. Lattice Avant Platform Key Features to change smallest package from 11 × 9 mm to 9 × 11 mm.<br>• Updated Table 1.2. Lattice Avant Families to remove LBG package in table note 1.<br>• Updated Table 1.3. Lattice Avant-AT-E Family Selection Guide to change package name from ASG410 to ASG410/ASGA410 and package size from 11 × 9 mm to 9 × 11 mm.<br>• Updated Table 1.4. Lattice Avant-AT-G Family Selection Guide and Table 1.5. Lattice Avant-AT-X Family Selection Guide to change ASG410 package size from 11 × 9 mm to 9 × 11 mm. |
| Pinout Information | Updated package name for LAV-AT-E30 from ASG410 to ASGA410/ASG410 in Lattice Avant-AT-E Family table. |
| Ordering Information | • Updated diagram in Lattice Avant Part Number Description to add ASGA410 package.<br>• Updated Commercial table to change LAV-AT-E30 package name from ASG410 to ASGA410 and added packages for LAV-AT-E30B.<br>• Updated Industrial table to change LAV-AT-E30 package name from ASG410 to ASGA410. |

**Revision 1.3, April 2025**

| Section | Change Summary |
|---|---|
| General Description | • Updated the following in Table 1.2. Lattice Avant Families:<br>  • Updated value of Avant-AT-E in Bitstream Security, SED/SEC, and xSPI Config.<br>  • Updated table note 2 to *Not supported in E70B or E30B variants*.<br>  • Added table note 3 that DDR4 is not supported in E70B or E30B variants.<br>  • Added reference to table note 3 and removed reference to note 2 for Avant-AT-E in LPDDR4/DDR4.<br>• Updated the following in Table 1.3. Lattice Avant-AT-E Family Selection Guide:<br>  • Updated value of E50 for CSG841.<br>  • Changed table note 2 to B variants only support limited package options. Refer to Ordering Information for more details and added reference to table note 2 in Packages section.<br>  • Removed table note 3.<br>• Removed CSG841 and LBG484 rows in Table 1.4. Lattice Avant-AT-G Family Selection Guide and Table 1.5. Lattice Avant-AT-X Family Selection Guide. |
| Architecture | • Removed xSPI and IEEE standard footnotes in Device Configuration.<br>• Updated Security Engine section content, including adding Avant-AT-X device support.<br>• Updated System Monitor/Anti-Tamper Monitor section content, including adding BBRAM information. |
| Pinout Information | • Updated Table 3.2. Lattice Avant-AT-E Family to add CSG481 package for LAV-AT-E50.<br>• Updated Table 3.3. Lattice Avant-AT-G Family to remove LBG484 package for LAV-AT-G30, CSG484 and LBG484 package for LAV-AT-G50, and CSG481 package for LAV-AT-G70.<br>• Updated Table 3.4. Lattice Avant-AT-X Family to remove LBG484 package for LAV-AT-X30, CSG484 and LBG484 package for LAV-AT-X50, and CSG481 package for LAV-AT-X70. |

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| Section | Change Summary |
|---|---|
| Ordering Information | • Updated diagram in Lattice Avant Part Number Description to remove LBG484 and CSG484 packages.<br>• Updated tables in Ordering Part Numbers to remove LFG676 for Avant-E30B, CSG841 for Avant-G/X70, and LBG484 for Avant-G/X30. |

**Revision 1.2, March 2025**

| Section | Change Summary |
|---|---|
| General Description | Updated this section to remove DDR3L instances, including in Table 1.1. Lattice Avant Platform Key Features and Table 1.2. Lattice Avant Families. |
| Architecture | • Updated the section content to remove DDR3L instances, including in Table 2.5. Summary of DDR Standards and Max Rates.<br>• Updated Peripheral Component Interconnect Express (PCIe) to correct PCIe document reference link. |

**Revision 1.1, February 2025**

| Section | Change Summary |
|---|---|
| Introduction | • Updated table note 2 in Table 1.2. Lattice Avant Families to add E30B.<br>• Updated the following in Table 1.3. Lattice Avant-AT-E Family Selection Guide:<br>  • Changed FCBGA to *FCCSP* for CBG484 and updated Total I/O and HPIO for E30 and E50.<br>  • Added table note for LFG676 support for E30B variant. |
| Architecture | • Updated Figure 2.1. High-level Device Floorplan (LAV-AT-E/G/X30 Device), Figure 2.2. High-level Device Floorplan (LAV-AT-E/G/X50 Device), Figure 2.3. High-level Device Floorplan (LAV-AT-E/G/X70 Device), Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-70 Device), and Figure 2.6. Multi-Region Clock Formation to add EBR and DSP as part of regional sources.<br>• Updated note 2 in Programmable I/O (PIO) to add E30B and LPDDR4 support.<br>• Added note 3 for IEEE support limitation in Device Configuration.<br>• Updated LMMI information in Multi-Protocol PHY (MPPHY) Integration. |
| Pinout Information | Changed Master and Slave SPI Mode to Controller and Target SPI Mode respectively in Signal Descriptions. |
| Ordering Information | • Updated diagram in Lattice Avant Part Number Description to add temperature ranges in the grades and added Mid-grade to -2 speed.<br>• Added E30B part numbers in Ordering Part Numbers. |
| References | Added section content including document references for SERDES, Multi-boot, SED/SEC, Avant-G/X versa board. |

**Revision 1.0, June 2024**

| Section | Change Summary |
|---|---|
| All | • Moved document status to *Production Release*.<br>For the status of specific devices, refer to the *Specification Status for Avant Devices* table in the Lattice Avant Platform Specification Data Sheet (FPGA-DS-02112).<br>• Changed SerDes to *SERDES* across the document, including figures.<br>• Changed 25G to *25 Gbps* across the document. |
| General Description | • Updated description in Lattice Avant-AT-E bullet point.<br>• Added Specifications Status for Avant Devices section.<br>• Updated DDR5 data rate from 2133 to 2100 Mbps in Table 1.1. Lattice Avant Platform Key Features.<br>• Updated Table 1.2. Lattice Avant Families table note to add -3 speed grade and reference to table note in Ethernet to 10G (Avant-AT-G/X); added table note 2 and reference to table |

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| Section | Change Summary |
|---|---|
| | note for DDR4 (Avant-AT-E).<br>• Updated E70 total I/O and HP values for CSG841 and changed CBG484 size from<br>• 19 × 19 mm to 18 × 18 mm in Table 1.3. Lattice Avant-AT-E Family Selection Guide.<br>• Removed 12.5 Gbps in Table 1.4. Lattice Avant-AT-G Family Selection Guide and 25 Gbps in Table 1.5. Lattice Avant-AT-X Family Selection Guide. |
| Architecture | • Updated Figure 2.1. High-level Device Floorplan (LAV-AT-E/G/X30 Device), Figure 2.3. High-level Device Floorplan (LAV-AT-E/G/X70 Device), Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-70 Device), and Figure 2.6. Multi-Region Clock Formation to change Misc/Config/Security block to Config/Security.<br>• Updated Figure 2.2. High-level Device Floorplan (LAV-AT-E/G/X50 Device) to change Misc/Config/Security block to Config/Security and remove the big SERDES block.<br>• Corrected typo to SPI interface in On-Chip Oscillator.<br>• Updated DDR5 speed from 2133 to 2100 Mbps (in the bullet point and footnote) and added footnote 2 and reference to footnote for DDR4, MIPI DPHY, and SGMII TX/RX in Programmable I/O (PIO).<br>• Updated the following in Table 2.5. Summary of DDR Standards and Max Rates:<br>  • Updated DDR5 speed from 2133 to *2100* Mbps, including in the table note, and updated reference to table note.<br>  • Added Max speeds reflect single-rank configurations only information in the table note.<br>  • Removed 2400 Mbps table note, including reference to this table note.<br>• Updated the following in Table 2.6. SERDES/PCS Supported Protocols:<br>  • Removed x1, x2, x4, and x8 in CPRI Protocol.<br>  • Changed 10G to *10.3125G* in the table notes.<br>• Updated the following in Table 2.7. Lattice Avant SERDES Protocol Width Support:<br>  • Added *x2, x4, x8, x10, x12, x16* to Typical Width for Ethernet.<br>  • Removed x2, x4, x8 in Typical Width and 2, 4, 8 in Rate x Width Examples for CPRI.<br>• Added reference to Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300) document in DQS Grouping for DDR Memory.<br>• Updated ECC and CRC information in Single Event Upset (SEU) Handling.<br>• Updated the following in Multi-Protocol PCS (MPPCS):<br>  • Changed Comma detection and word alignment bullet point to *Comma detection and word and block alignment*.<br>  • Added *66/132/160 available in PMA direct mode* to the Gearing to FPGA bullet point.<br>  • Updated bullet point to *Built in Pipe Control Interface for PCIe fabric*.<br>  • Removed XLGMII/CGMII in the Ethernet bullet point.<br>  • Removed a sub-bullet point in FEC saying that it's used in Primary use in 25G Ethernet, 24.3 Gbps CPRI, and 25G JESD204C.<br>  • Changed Parallel loopback mode for testability to *Serial Parallel loopback mode for testability*.<br>• Updated Figure 2.15. MPPHY Top-Level Block Diagram.<br>• Updated the following in Peripheral Component Interconnect Express (PCIe):<br>  • Updated Support of link width bullet point to *Support for link width of x8, x4, x2, x1 PCI Express lanes. Bifurcation is supported through softIP PCI Express Lanes*.<br>  • Added 24 virtual functions in Multi-function support bullet point.<br>  • Removed *and Software Controlled* in Support for Autonomous bullet point.<br>  • Removed *and Up/Down* in Support for Figure of Merit bullet point.<br>  • Updated close-captioned text to *PCIe supports Preset only* in Flexible Equalization methods bullet point.<br>  • Updated to *64-bit User Interface Data Width (per lane)* bullet point.<br>  • Updated Figure 2.16. PCIe Core.<br>• Updated Figure 2.18. Cryptographic Engine Block Diagram to add AXI4 connection.<br>• Changed Lattice Avant-E to Lattice Avant-AT-E in System Monitor/Anti-Tamper Monitor. |

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### Revision 0.82, May 2024

| Section | Change Summary |
|---|---|
| General Description | Corrected Table 1.4. Lattice Avant-AT-G Family Selection Guide and Table 1.5. Lattice Avant-AT-X Family Selection Guide to properly removed strikeout packages CSG484 and LBG484 (including removing reference to table note 2) for Avant-AT-G/X50. |
| Ordering Information | Corrected Ordering Part Numbers tables to properly remove strikeout OPNs CSG484 and LBG484 for Avant-AT-G/X50. |

### Revision 0.81, March 2024

| Section | Change Summary |
|---|---|
| General Description | • Updated the following in Table 1.2. Lattice Avant Families:<br>  • Changed SerDes to *Protocol*.<br>  • Changed Avant-AT-G and Avant-AT-X values to *Yes* in Ethernet to 10G.<br>  • Changed Avant-AT-X value to *Yes* in Ethernet to 25G.<br>  • Added footnote and reference footnote for Max Speed (Avant-AT-G/X), PCIe Gen4 (Avant-AT-X), and Ethernet to 25G (Avant-AT-X).<br>  • Added footnote and reference to footnote 2 for LFG1156 (E70) and changed CSG841 size to 15 × 15 mm in Table 1.3. Lattice Avant-AT-E Family Selection Guide.<br>• Updated the following in Table 1.4. Lattice Avant-AT-G Family Selection Guide and Table 1.5. Lattice Avant-AT-X Family Selection Guide:<br>  • Changed CSG841 size to *15 × 15 mm*.<br>  • Added footnote and reference to footnote 2 for ASG410 and CSG841.<br>  • Removed CSG484 and LBG484 packages. |
| Architecture | • Added table notes for Protocol Performance in Table 2.6. SERDES/PCS Supported Protocols and Table 2.7. Lattice Avant SERDES Protocol Width Support.<br>• Updated the following in Multi-Protocol PCS (MPPCS):<br>  • Changed Lattice Avant SerDes to *Lattice Avant Platform SerDes*.<br>  • Added Protocol Support information at the end of the bulleted list.<br>• Added Security Support information at the bottom of the first bulleted list in Security Engine section. |
| Ordering Information | • Updated diagram in Lattice Avant Part Number Description to add Silicon Variant description.<br>• Updated tables in Ordering Part Numbers to add E70B and remove OPNS for Avant-AT-G/X50 CSG484 and LBG484. |
| References | Corrected document IDs for Lattice Avant Configuration Security and Lattice Avant Device Security user guides. |

### Revision 0.80, December 2023

| Section | Change Summary |
|---|---|
| All | • Added Lattice Avant-AT-G and Avant-AT-X support across the document.<br>• Added LAV-AT-G30, LAV-AT-G50, LAV-AT-G70, LAV-AT-X30, LAV-AT-X50, and LAV-AT-X70 devices across the document. |
| Disclaimers | Updated this section. |
| General Description | • Updated Lattice Avant-AT-X bullet point to reword and add PCIe Gen4 and 25G Ethernet information.<br>• Updated Table 1.2. Lattice Avant Families to add Avant-AT-G and Avant-AT-X devices.<br>• Updated Table 1.3. Lattice Avant-AT-E Family Selection Guide to add LUT row, changed GPLL values and change Total I/O values.<br>• Added Table 1.4. Lattice Avant-AT-G Family Selection Guide and Table 1.5. Lattice Avant-AT-X Family Selection Guide. |
| Architecture | • Updated Figure 2.1. High-level Device Floorplan (LAV-AT-E/G/X30 Device), Figure 2.2. High- |

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| Section | Change Summary |
|---|---|
| | level Device Floorplan (LAV-AT-E/G/X50 Device), Figure 2.3. High-level Device Floorplan (LAV-AT-E/G/X70 Device), Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-70 Device), and Figure 2.6. Multi-Region Clock Formation to include Avant-AT-G and Avant-AT-X support and change the figure captions. Added note for the high-level floorplans that SerDes is supported in Avant-AT-G/X devices.<br>• Added two bullet points for Two Distributed RAMs for each PFU in Programmable Functional Unit (PFU) Blocks section.<br>• Changed 450 MHz, 360 MHz, and 112 MHz to 400 MHz, 320 MHz, and 100 MHz in On-Chip Oscillator section.<br>• Updated Figure 2.5. Lattice Avant PLL Block Diagram and removed optional delay in PLL section.<br>• Removed information on RCLK providing clock sources to other blocks and removed CLKOPHY in PLL HPIO outputs in Regional Clocks (RCLK).<br>• Updated Figure 2.11. sysI/O Banking to include SerDes support and change to LAV-AT-E/G/X70.<br>• Added note in sysI/O Banking Scheme section that SerDes is supported in Avant-AT-G/X devices.<br>• Added footnote for Avant-AT-G/X devices in Table 2.5. Summary of DDR Standards and Max Rates.<br>• Added reference to SED/SEC document in Single Event Upset (SEU) Handling. |
| Pinout Information | • Added VCCJB row in Signal Descriptions.<br>• Updated Lattice Avant-AT-E Family in Pin Information Summary to change the following:<br>  • Added $V_{CCJB}$ row.<br>  • Updated LAV-AT-E30 ASG410 and LAV-AT-E70 CBG484 columns.<br>  • Updated LAV-AT-E70 LFG676 and LFG1156 values for WRIO Bank 0, Total WRIO, Total HPIO, $V_{CC}$, Total Power Pins, GND and NC pins, and Shared PCLK Pins (Bank 0, 3, 8, 9, 10, 11).<br>• Added Lattice Avant-AT-G Family and Lattice Avant-AT-X Family. |
| Ordering Information | • Updated figure in Lattice Avant Part Number Description to include Avant-AT-G/X support and add CSG484 and LBG484 packages.<br>• Added packages for Avant-AT-G and Avant-AT-X devices in Ordering Part Numbers tables. |
| References | Changed section name from Supplemental Information to References, corrected document link for Avant Power User Guide, added Configuration Security and Device Security documents in the list, and added webpage links for Avant-G and Avant-X. |

**Revision 0.74, October 2023**

| Section | Change Summary |
|---|---|
| All | • Changed Lattice Avant-E to *Lattice Avant-AT-E* across the document.<br>• Changed device names to LAV-AT-E30, LAV-AT-E50, and LAV-AT-E70 across the document.<br>• Changed logic cells (LCs) to *system logic cells (SLCs)* across the document. |
| Disclaimers | Updated this section. |
| Inclusive Language | Added this section. |
| Acronyms in This Document | Changed Logic Cell (LC) to System Logic Cells (SLC). |
| General Description | • Updated General Description section to change 477k to 637k.<br>Updated Table 1.1. Lattice Avant Platform Key Features to remove note referring to DDR4/LPPDR4 and change system logic cell count to 262k to 637k.<br>• Updated the following in Table 1.3. Lattice Avant-AT-E Family Selection Guide:<br>  • Changed device name to E30, E50, and E70.<br>  • Updated system logic cells to 262k, 409k, and 637k.<br>  • Changed name to GPLL (WRPLL, HPPLL) and count to 1, 5 for E30, 2, 7 for E50, and 2, 9 for E70.<br>  • Changed package from ASG324 to *ASG410* and package type to FOWLP. |

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| Section | Change Summary |
|---|---|
| | • Changed package from CSG676 to *CSG841*.<br>• Changed package name from LBG484 to *CBG484*; and package type to FCCSP.<br>• Updated WRIO and HPIO count for all packages.<br>• Removed CSG484 package, LFG676 for E30 and E50, and LFG1156 for E50. |
| Functional Description | • Changed 20k up to 27k logic cells to *26k up to 35k system logic cells* in Overview section.<br>• Updated Figure 2.1. High-level Device Floorplan (LAV-AT-E30 Device), Figure 2.2. High-level Device Floorplan (LAV-AT-E50 Device), Figure 2.3. High-level Device Floorplan (LAV-AT-E70 Device), Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-E70 Device), and Figure 2.6. Multi-Region Clock Formation.<br>• Updated RAM Mode to add 32 x 2 bits.<br>• Updated the following in Clocking Structure.<br>  • Changed 27k logic cells to *35k system logic cells (SLCs)*.<br>  • Changed ECLKSYNC/ECLKDIV to ECLKSYNCA/ECLKDIVA.<br>  • Changed user clock value to 450 MHz and 360 MHz.<br>• Updated RAM Mode to add 32 x 2 bits.<br>• Updated the following in Clocking Structure.<br>  • Changed ECLKSYNC/ECLKDIV to ECLKSYNCA/ECLKDIVA.<br>  • Changed user clock value to 450 MHz and 360 MHz.<br>• Updated the following in sysDSP:<br>  • Removed DSP Features table.<br>  • Updated Figure 2.10. DSP Functional Block to simplify the diagram, including description and block elements in the section.<br>• Changed 500k to E70 device and updated Figure 2.11. sysI/O Banking to change to LAV-AT-E70 in sysI/O Banking Scheme section.<br>• Removed note referring to DDR4/LPDDR4 in Table 2.5. Summary of DDR Standards and Max Rates.<br>• Changed Octal SPI to xSPI in Input Register Block.<br>• Updated the following in Device Configuration:<br>  • Changed Octal SPI to xSPI.<br>  • Applied inclusive language and added note 2 to define Controller and Target SPI.<br>  • Added Bitstream Authentication bullet point in Enhanced Configuration Options.<br>• Updated the following in SerDes and PCS:<br>  • Updated common block value to 2 × Tx PLL.<br>  • Updated Figure 2.14 SerDes Overview Diagram to change to Two Common Refclk PLL.<br>  • Added 32 and 40 bits in SERDES/PMA Block.<br>  • Removed modes of operations bullet points. |
| Pinout Information | • Updated the following in Signal Descriptions:<br>  • Applied inclusive language in Shared Configuration Pins.<br>  • Added $V_{SSR}$ row.<br>  • Removed $V_{CCHP}$ and $V_{CCLK}$ rows.<br>  • Moved EXT_RES row to *Dedicated Pins* group and removed HPIO references.<br>• Updated the following in Pin Information Summary.<br>  • Updated LAV-AT-E70 LFG676 values of WRIO Bank 12, Bank 13, and Bank 14 to *0*; Total WRIO to *43*; HPIO Bank 3, Bank 8 up to Bank 11 to *51*; Total HPIO to *255;* $V_{CC}$ to *26*.<br>  • Updated LAV-AT-E70 LFG1156 values of HPIO Bank 3 to Bank 11 to *51*; Total HPIO to *259*; $V_{CC}$ to *24*.<br>  • Added $V_{CC_PLL_W}$ to $V_{CC_PLL}$ row and changed LAV-AT-70E LFG676 and LFG1156 values to *4*.<br>  • Updated LAV-AT-E70 LFG676 value of $V_{CCAUXA}$ to *4*.<br>  • Updated LAV-AT-E70 LFG676 and LFG1156 values of Total Power Pins to *65* and *87*.<br>  • Updated LAV-AT-E70 LFG676 and LFG1156 values of $V_{SS}$ to *176* and *281*; NC to *36* and *63*; Shared Reference Pins Bank 3, Bank 8 up to 11 to *2*.<br>  • Added CBG484 package and changed to CSG841 in LAV-AT-E70. |

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| Section | Change Summary |
|---|---|
| | • Changed to ASG410 and CBG484 package in LAV-AT-E30.<br>• Added $V_{SSR}$ and EXT_RESn rows.<br>• Removed $V_{CCCLK}$ and $V_{CCHP}$ rows.<br>• Removed LFG676 in LAV-AT-E30; CSF484, LFG676, and LFG1156 in LAVT-AT-E50. |
| Ordering Information | • Updated the following in Lattice Avant Part Number Description:<br>  • Re-arranged Family Code and Logic Capacity position and updated X values for Logic Capacity.<br>  • Updated device and system logic cell values.<br>  • Updated packages to change to ASG410, 410-ball, FOWLP; removed CSG676 package; changed to FCCSP for CBG484; changed from CSG484 to *CSG841*.<br>• Updated Commercial and Industrial tables to change column name from Temp to *Grade*. |
| Supplemental Information | • Rearranged list in alphabetical order.<br>• Added references to the Avant-E, Lattice Insights, and Lattice Radiant Web Pages.<br>• Updated this section to add references to SGMII and Gb Ethernet PCS IP Core and Lattice Avant Evaluation Board. |

### Revision 0.73, March 2023

| Section | Change Summary |
|---|---|
| All | Minor adjustments in formatting across the document. |
| Architecture | Updated Table 2.3. Single-Ended I/O Standards Supported on Various Sides to change Output and Bi-directional values for LVCMOS10 and LVCMOS09 to Yes. |
| Supplemental Information | Added reference links for the IP, Reference Design, and Boards web page. |

### Revision 0.72, February 2023

| Section | Change Summary |
|---|---|
| Acronyms in This Table | Updated DDRPHY definition and added LPDDR definition. |
| General Description | • Updated DDRS and LPDDR4 to DDR5, DDR4/LPDDR4, and DDR3L in the General Description section.<br>• Updated the following in Table 1.1. Avant Platform Key Features:<br>  • Changed DDR5 value to 2133 Mbps; added footnote and reference to footnote 1.<br>  • Changed DDR4 and LPDDR4 value to 2400 Mbps; added footnote and reference to footnote 2.<br>  • Added DDR3L value.<br>• Updated Table 1.2. Avant Families to rearrange LPDDR4/DDR4 to DDR4/LPDDR4. |
| Architecture | • Changed DDR3L/4/5, LPDDR2/3/4 to DDR5, DDR4/LPDDR4, and DDR3L in Overview section.<br>• Changed the following in Programmable I/O (PIO) section:<br>  • Reorder top bullet items to DDR5, DDR4/LPDDR4, and DDR3L.<br>  • Changed DDR5 value to 2133 Mbps, added footnote reference 1, and updated footnote 1.<br>  • Added footnote 2 and footnote reference to DDR4/LPDDR4.<br>  • Removed LPDDR2 and LPDDR3.<br>• Changed DDR5, LPDDR4, DDR4 to DDR5 and DDR4/LPDDR4 in sysI/O Banking Scheme section.<br>• Changed the following in DDR Memory Support:<br>  • Changed DDR3L/DDR4/DDR5 and LPDDR2/LPDDR3/LPDDR4 to DDR5, DDR4/LPDDR4, and DDR3L.<br>  • Updated Table 2.6. Summary of DDR Standards and Max Rates to reorder standards and remove LPDDR2 and LPDDR3. |

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**Revision 0.71, December 2022**

| Section | Change Summary |
|---|---|
| All | • Updated document to include Avant-E information only.<br>• Adjustments in formatting across the document. |
| Acronyms in This Document | Added description for DDLDEL, DDRPHY, GCLK, PIO, MPPCS, MPPHY, and RCLK. |
| Introduction | • Updated section content including the following:<br>  • Changed smallest package size to 11 x 9 mm in Table 1.1. Avant Platform Key Features.<br>  • Updated Table 1.2. Avant Families to include only Avant-E and Future Avant Families information, and updated Security row to Security/Hardened Crypto.<br>  • Updated the following in Table 1.3. Avant-E Family Selection Guide:<br>  • Added CSG484 and CSG676 packages.<br>  • Changed package LFG672 to LFG676.<br>  • Added type in the packages.<br>  • Updated Total I/O values in the table.<br>  • Added table note 2 to include reference to the Ordering Information section.<br>  • Removed LFG900 package.<br>  • Removed WRPLL and HPPLL references. |
| Architecture | • Changed WRPLL and HPPLL references to PLL (WRIO) and PLL (HPIO), and CIBCLK to Fabric_CLK across this section.<br>• Updated section names of DLL Delay (DLLDEL), Multi-Protocol PCS (MPPCS), and Multi-Protocol PHY (MPPHY) Integration.<br>• Updated sysI/O buffer information in the Overview section.<br>• Updated Figure 2.1. High-level Device Floorplan (LAV-AT-200E Device), Figure 2.2. High-level Device Floorplan (LAV-AT-300E Device), Figure 2.3. High-level Device Floorplan (LAV-AT-500E Device), Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-500E Device), Figure 2.6. Multi-Region Clock Formation, and Figure 2.11. sysI/O Banking to include Avant-E information only.<br>• Updated slice input to 16 in Slices section.<br>• Updated user clock frequency to 400 or 320 MHz in On-Chip Oscillator section.<br>• Updated Integer Feedback divider values, Spreading depth, and Glitchless Dynamic output bullet points and Figure 2.5. Avant PLL Block Diagram in PLL section.<br>• Updated Figure 2.8. High-Level Implementation of DLLDEL and Code Control to change HPPLL_PHYCLK to PLL(HPIO)_PHYCLK.<br>• Updated Table 2.2 sysMEM Block Configurations to remove 512 x 72.<br>• Updated Figure 2.9. Memory Core Reset to update Port A and B to [35:0].<br>• Updated Figure 2.10. DSP Functional Block.<br>• Changed programmable drive strength to 4 to 12 mA in Programmable I/O (PIO) section.<br>• Updated Figure 2.12. Group of Two High Performance Programmable I/O Cells and Figure 2.13. Wide Range Programmable I/O Cells to add bounding box.<br>• Updated Table 2.6. Summary of DDR Standards and Max Rates to change DDR5 max speed to 2133 Mbps, including the table note.<br>• Updated Device Configuration section content to reword INIT/DONE information and added note for Octal SPI.<br>• Updated the following in SerDes and PCS:<br>  • Added note that the SerDes feature is note supported in Avant-E.<br>  • Updated Figure 2.14. SerDes Overview Diagram to make the lines more visible and updated Quad color to blue and Multi-Channel to orange.<br>  • Updated Table 2.7. SerDes/PCS Supported Protocols to correct 10G Ethernet, 25G Ethernet, CPRI, eCPRI, ROE, and SyncE protocols, update table note reference, and change information in the table note to Avant platform.<br>  • Updated Table 2.8. Avant SerDes Protocol Width Support to change Rate (Gbps) x Width Example values for Ethernet, CPRI, eCPRI, ROE, and SyncE.<br>  • Updated Figure 2.17. PCIe Soft IP Wrapper to add TLP native and AXI-4 Lite.<br>• Added note in Security Engine section that this feature is note supported in Avant-E. |

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| Section | Change Summary |
|---|---|
| | • Added note in System Monitor/Anti-Tamper Monitor section that this feature is note supported in Avant-E. |
| Pinout Information | • Removed nominal value for VCCA_MPQx and VCCH_MPQx in Signal Descriptions.<br>• Updated Pin Information Summary section to include Avant-E information only, added packages for CSG484 and CSG676, change LFG672 to LFG676, and removed 900 package. |
| Ordering Information | Updated Ordering Information to include only Avant-E information, change LFG672 to LFG676, Family Code to Platform Code, and Variant Code to Family Code, and add CSG484 and CSG676 packages. |

**Revision 0.70, May 2022**

| Section | Change Summary |
|---|---|
| All | Advance release. |

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