



DRV8828 H-Bridge Motor Controller IC

1 Features

- Single H-Bridge Current-Control Motor Driver
- 8.2-V to 45-V Operating Supply Voltage Range
- Capable of Driving One Winding of a Bipolar Stepper Motor or One DC Motor
- Five Bit Current Control Allows up to 32 Current Levels
- Low MOSFET $R_{DS(on)}$ Typical $0.65\ \Omega$ (HS + LS)
- 3-A Maximum Drive Current at 24 V, 25°C
- Built In 3.3-V Reference Output
- Parallel Digital Control Interface
- Thermal Enhanced Surface Mount Package
- Protection Features
 - Overcurrent Protection (OCP)
 - Thermal Shutdown (TSD)
 - VM Undervoltage Lockout (UVLO)
 - Fault Condition Indication Pin (nFAULT)

2 Applications

- Automatic Teller Machines
- Money Handling Machines
- Video Security Cameras
- Printers
- Scanners
- Office Automation Machines
- Gaming Machines
- Factory Automation
- Robotics

3 Description

The DRV8828 provides an integrated motor driver solution for printers, scanners, and other automated equipment applications. The device has one H-bridge driver, and can drive one winding of a bipolar stepper motor or one DC motor. The output driver block consists of N-channel power MOSFET's configured as a full H-bridge to drive the motor winding. The DRV8828 is capable of driving up to 3-A of output current (with proper heatsinking at 24 V and 25°C).

A simple parallel digital control interface is compatible with industry-standard devices. Decay mode is programmable.

Internal shutdown functions are provided for overcurrent protection, short circuit protection, undervoltage lockout and overtemperature.

The DRV8828 is available in a 28-pin HTSSOP package with PowerPAD™ (Eco-friendly: RoHS & no Sb/Br).

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8828	HTSSOP (28)	9.70 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Device Schematic

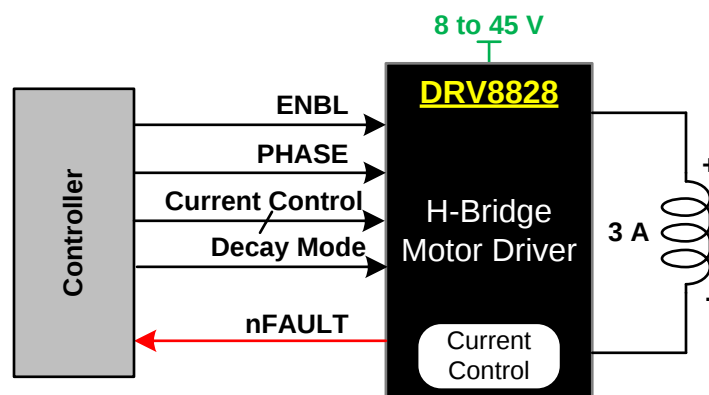


Table of Contents

1 Features	1	8 Application and Implementation	13
2 Applications	1	8.1 Application Information.....	13
3 Description	1	8.2 Typical Application	13
4 Revision History	2	9 Power Supply Recommendations	16
5 Pin Configuration and Functions	3	9.1 Bulk Capacitance Sizing	16
6 Specifications	4	10 Layout	17
6.1 Absolute Maximum Ratings	4	10.1 Layout Guidelines	17
6.2 ESD Ratings.....	4	10.2 Layout Example	17
6.3 Recommended Operating Conditions.....	4	10.3 Power Dissipation	18
6.4 Thermal Information	5	10.4 Heatsinking	18
6.5 Electrical Characteristics.....	5	11 Device and Documentation Support	19
6.6 Typical Characteristics	7	11.1 Documentation Support	19
7 Detailed Description	8	11.2 Community Resources.....	19
7.1 Overview	8	11.3 Trademarks	19
7.2 Functional Block Diagram	8	11.4 Electrostatic Discharge Caution.....	19
7.3 Feature Description.....	9	11.5 Glossary	19
7.4 Device Functional Modes.....	12	12 Mechanical, Packaging, and Orderable Information	19

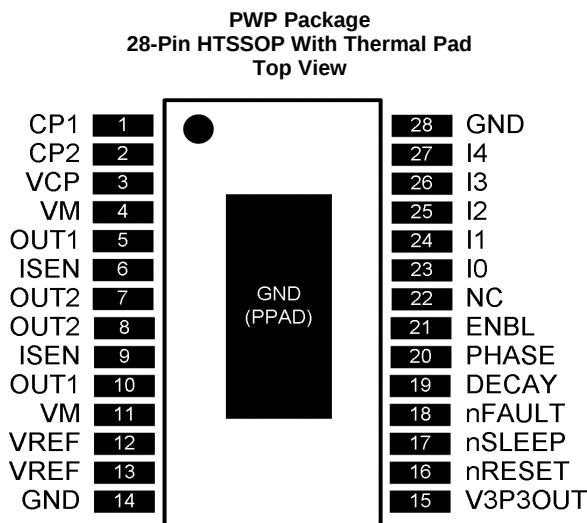
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (December 2013) to Revision G	Page
• Added <i>Pin Configuration and Functions</i> section, <i>ESD Rating</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Updated Absolute Maximum Ratings Table	1

Changes from Revision E (August 2013) to Revision F	Page
• Changed in the ELECTRICAL CHARACTERISTICS table, section DECAY INPUT, 3rd row	5

5 Pin Configuration and Functions



Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND	14, 28	-	Device ground	
VM	4, 11	-	Bridge power supply	Connect to motor supply (8 - 45 V). Both pins must be connected to same supply.
V3P3OUT	15	O	3.3-V regulator output	Bypass to GND with a 0.47-μF 6.3-V ceramic capacitor. Can be used to supply VREF.
CP1	1	I/O	Charge pump flying capacitor	Connect a 0.01-μF 50-V capacitor between CP1 and CP2.
CP2	2	I/O	Charge pump flying capacitor	
VCP	3	I/O	High-side gate drive voltage	Connect a 0.1-μF 16-V ceramic capacitor and a 1-MΩ resistor to VM.
CONTROL				
ENBL	21	I	Bridge enable	Logic high to enable H-bridge. Internal pull-down.
PHASE	20	I	Bridge phase (direction)	Logic high sets OUT1 high, OUT2 low. Internal pull-down.
I0	23	I	Current set inputs	Sets winding current as a percentage of full-scale. Internal pull-down.
I1	24	I		
I2	25	I		
I3	26	I		
I4	27	I		
DECAY	19	I	Decay mode	Low = slow decay, open = mixed decay, high = fast decay Internal pull-down and pullup.
nRESET	16	I	Reset input	Active-low reset input initializes internal logic and disables the H-bridge outputs. Internal pull-down.
VREF	12, 13	I	Current set reference input	Reference voltage for winding current set. Both pins must be connected together on the PCB. A 0.01-μF bypass capacitor to GND is recommended.
nSLEEP	17	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode. Internal pull-down.
NC	22		No connect	Leave this pin unconnected.

(1) Directions: I = input, O = output, OZ = tri-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		I/O ⁽¹⁾	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
STATUS				
nFAULT	18	O/D	Fault	Logic low when in fault condition (overtemp, overcurrent)
OUTPUT				
ISEN	6, 9	I/O	Bridge ground / Isense	Connect to current sense resistor. Both pins must be connected together on the PCB.
OUT1	5, 10	O	Bridge output 1	Connect to motor winding. Both pins must be connected together on the PCB.
OUT2	7, 8	O	Bridge output 2	

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾⁽²⁾

		MIN	MAX	UNIT
VM	Power supply voltage	−0.3	47	V
	Digital pin voltage	−0.5	7	V
VREF	Input voltage	−0.3	4	V
	ISENSE pin voltage	−0.8	0.8 ⁽³⁾	V
	Peak motor drive output current, t < 1 μs	Internally limited		A
	Continuous motor drive output current ⁽⁴⁾	0	3	A
	Continuous total power dissipation	See Thermal Information		
T _J	Operating virtual junction temperature	−40	150	°C
T _{stg}	Storage temperature	−60	150	°C

- (1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under [Recommended Operating Conditions](#) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.
- (3) Transients of +/- 1V for less than 25 ns are acceptable.
- (4) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

		VALUE	UNIT	
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±500	V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _M	Motor power supply voltage range ⁽¹⁾	8.2		45	V
V _{REF}	VREF input voltage ⁽²⁾	1		3.5	V
I _{V3P3}	V3P3OUT load current			1	mA

- (1) All V_M pins must be connected to the same supply voltage.
- (2) Operational at VREF between 0 V and 1 V, but accuracy is degraded.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		DRV8828	UNIT
		PWP (HTSSOP)	
		28 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	38.9	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	23.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	21.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	20.9	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES					
I _{VM}	VM operating supply current V _M = 24 V, f _{PWM} < 50 kHz		5	8	mA
I _{VMQ}	VM sleep mode supply current V _M = 24 V		10	20	μA
V _{UVLO}	VM undervoltage lockout voltage V _M rising		7.8	8.2	V
V3P3OUT REGULATOR					
V _{3P3}	V3P3OUT voltage I _{OUT} = 0 to 1 mA, V _M = 24 V, T _J = 25°C	3.18	3.30	3.42	V
	I _{OUT} = 0 to 1 mA	3.10	3.30	3.50	V
LOGIC-LEVEL INPUTS					
V _{IL}	Input low voltage		0.6	0.7	V
V _{IH}	Input high voltage	2		5.25	V
V _{HYS}	Input hysteresis		0.45		V
I _{IL}	Input low current VIN = 0	–20		20	μA
I _{IH}	Input high current VIN = 3.3 V			100	μA
R _{PD}	Internal pulldown resistance ENBL, PHASE, I0, I1, I2, I3, I4, nRESET		100		kΩ
	nSLEEP		1		MΩ
nFAULT OUTPUT (OPEN-DRAIN OUTPUT)					
V _{OL}	Output low voltage I _O = 5 mA			0.5	V
I _{OH}	Output high leakage current V _O = 3.3 V			1	μA
DECAY INPUT					
V _{IL}	Input low threshold voltage For slow decay mode			0.8	V
V _{IH}	Input high threshold voltage For fast decay mode	2			V
I _{IN}	Input current	–100		100	μA
R _{PU}	Internal pullup resistance		130		kΩ
R _{PD}	Internal pulldown resistance		80		kΩ
H-BRIDGE FETS					
R _{DS(ON)}	HS FET on resistance V _M = 24 V, I _O = 1 A, T _J = 25°C		0.32		Ω
	V _M = 24 V, I _O = 1 A, T _J = 85°C		0.39	0.45	Ω
R _{DS(ON)}	LS FET on resistance V _M = 24 V, I _O = 1 A, T _J = 25°C		0.33		Ω
	V _M = 24 V, I _O = 1 A, T _J = 85°C		0.39	0.45	Ω
I _{OFF}	Off-state leakage current	–40		40	μA
MOTOR DRIVER					
f _{PWM}	PWM frequency		50		kHz
t _{BLANK}	Current sense blanking time		3.75		μs
t _R	Rise time V _M = 24 V	100		360	ns

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_F	Fall time	$V_M = 24\text{ V}$	80		250	ns
t_{DEAD}	Dead time			400		ns
t_{DEG}	Input deglitch time		1.3		2.9	μs
PROTECTION CIRCUITS						
I_{OCP}	Overcurrent protection trip level		3.6		10	A
t_{TSD}	Thermal shutdown temperature	Die temperature	150	160	180	$^{\circ}\text{C}$
CURRENT CONTROL						
I_{REF}	VREF input current	$V_{REF} = 3.3\text{ V}$	–3		3	μA
V_{TRIP}	ISENSE trip voltage	$V_{REF} = 3.3\text{ V}$, 100% current setting	635	660	685	mV
ΔI_{TRIP}	Current trip accuracy (relative to programmed value)	$V_{REF} = 3.3\text{ V}$, 5% current setting	–25%		25%	
		$V_{REF} = 3.3\text{ V}$, 10% - 34% current setting	–15%		15%	
		$V_{REF} = 3.3\text{ V}$, 38% - 67% current setting	–10%		10%	
		$V_{REF} = 3.3\text{ V}$, 71% - 100% current setting	–5%		5%	
A_{ISENSE}	Current sense amplifier gain	Reference only		5		V/V

6.6 Typical Characteristics

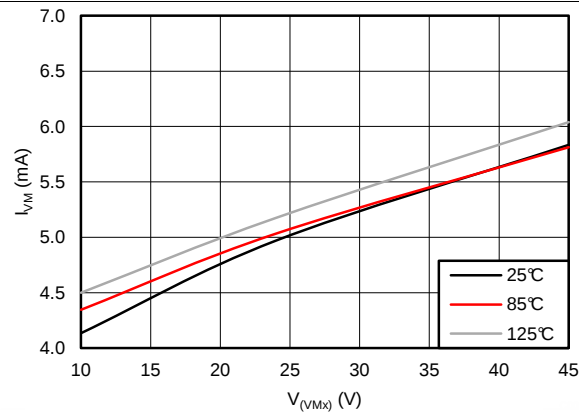


Figure 1. I_{VM} vs $V_{(VMx)}$

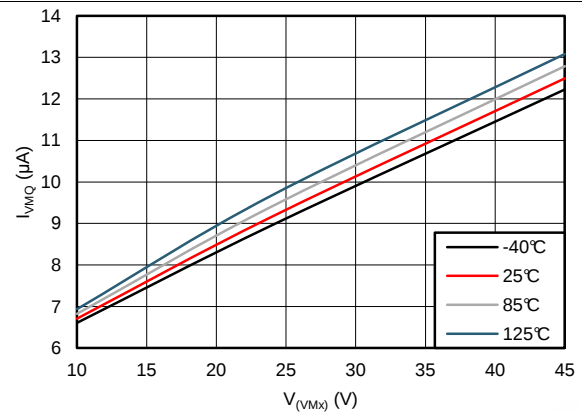


Figure 2. I_{VMQ} vs $V_{(VMx)}$

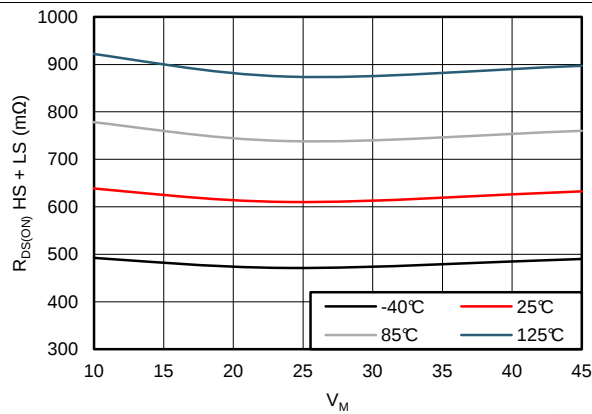


Figure 3. $R_{DS(ON)}$ vs $V_{(VMx)}$

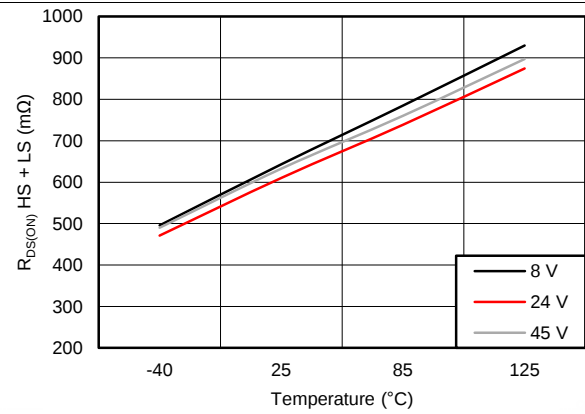


Figure 4. $R_{DS(ON)}$ vs Temperature

7.3 Feature Description

7.3.1 PWM Motor Drivers

The DRV8828 contains one H-bridge motor driver with current-control PWM circuitry. A block diagram of the motor control circuitry is shown in Figure 5. A bipolar stepper motor is shown, but the driver can also drive a DC motor.

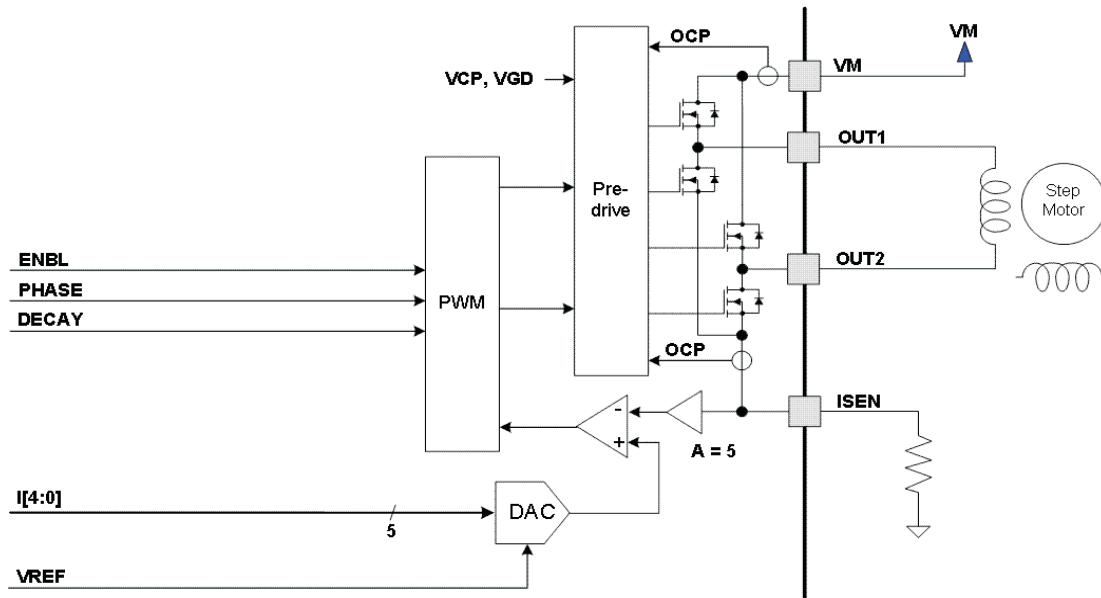


Figure 5. Motor Control Circuitry

Note that there are multiple VM, ISEN, OUT, and VREF pins. All like-named pins must be connected together on the PCB.

7.3.2 Bridge Control

The PHASE input pin controls the direction of current flow through the H-bridge. The ENBL input pin enables the H-bridge outputs when active high. The logic inputs ENBL and PHASE have internal pulldown resistors of 100 kΩ. Table 1 shows the logic.

Table 1. H-Bridge Logic

ENBL	PHASE	OUT1	OUT2
0	X	Z	Z
1	1	H	L
1	0	L	H

7.3.3 Current Regulation

The current through the motor winding is regulated by a fixed-frequency PWM current regulation, or current chopping. When the H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding. Once the current hits the current chopping threshold, the bridge disables the current until the beginning of the next PWM cycle.

For stepping motors, current regulation is normally used at all times, and changing the current can be used to microstep the motor. For DC motors, current regulation is used to limit the start-up and stall current of the motor.

The PWM chopping current in the bridge is set by a comparator which compares the voltage across a current sense resistor connected to the ISEN pin, multiplied by a factor of 5, with a reference voltage. The reference voltage is input from the xVREF pins, and is scaled by a 5-bit DAC that allows current settings of zero to 100% in an approximately sinusoidal sequence.

The full-scale (100%) chopping current is calculated in [Equation 1](#).

$$I_{CHOP} = \frac{V_{REFX}}{5 \cdot R_{ISENSE}} \quad (1)$$

Example:

If a 0.5-Ω sense resistor is used and the VREFx pin is 3.3 V, the full-scale (100%) chopping current will be 3.3 V / (5 x 0.5 Ω) = 1.32 A.

Five input pins (I0 - I4) are used to scale the current in the bridge as a percentage of the full-scale current set by the VREF input pin and sense resistance. The logic inputs I0, I1, I2, I3 and I4 have internal pulldown resistors of 100 kΩ. The function of the pins is shown in [Table 2](#).

Table 2. H-Bridge Pin Functions

I[4..0]	RELATIVE CURRENT (% FULL-SCALE CHOPPING CURRENT)
0x00h	0%
0x01h	5%
0x02h	10%
0x03h	15%
0x04h	20%
0x05h	24%
0x06h	29%
0x07h	34%
0x08h	38%
0x09h	43%
0x0Ah	47%
0x0Bh	51%
0x0Ch	56%
0x0Dh	60%
0x0Eh	63%
0x0Fh	67%
0x10h	71%
0x11h	74%
0x12h	77%
0x13h	80%
0x14h	83%
0x15h	86%
0x16h	88%
0x17h	90%
0x18h	92%
0x19h	94%
0x1Ah	96%
0x1Bh	97%
0x1Ch	98%
0x1Dh	99%
0x1Eh	100%
0x1Fh	100%

7.3.4 Decay Mode

During PWM current chopping, the H-bridge is enabled to drive current through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 6 as case 1. The current flow direction shown indicates the state when the PHASE pin is high.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. As the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 6 as case 2.

In slow decay mode, winding current is re-circulated by enabling both of the low-side FETs in the bridge. This is shown in Figure 6 as case 3.

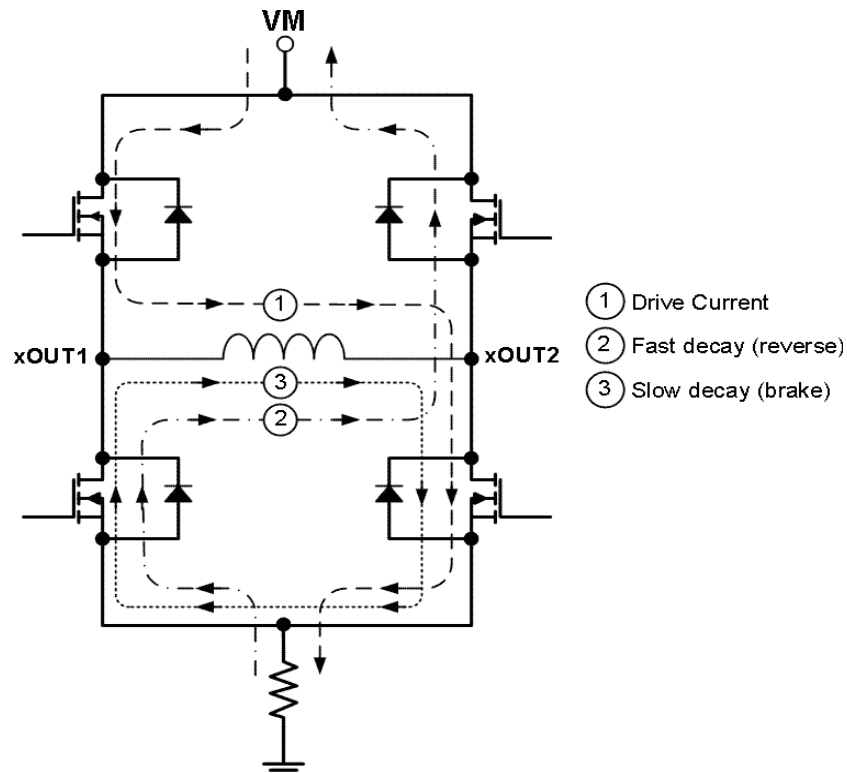


Figure 6. Decay Mode

The DRV8828 supports fast decay, slow decay and a mixed decay mode. Slow, fast, or mixed decay mode is selected by the state of the DECAY pin - logic low selects slow decay, open selects mixed decay operation, and logic high sets fast decay mode. The DECAY pin has both an internal pullup resistor of approximately 130 kΩ and an internal pulldown resistor of approximately 80 kΩ. This sets the mixed decay mode if the pin is left open or undriven.

Mixed decay mode begins as fast decay, but at a fixed period of time (75% of the PWM cycle) switches to slow decay mode for the remainder of the fixed PWM period.

7.3.5 Blanking Time

After the current is enabled in the H-bridge, the voltage on the ISEN pin is ignored for a fixed period of time before enabling the current sense circuitry. This blanking time is fixed at 3.75 μs. Note that the blanking time also sets the minimum on time of the PWM.

7.3.6 Protection Circuits

The DRV8828 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.6.1 Overcurrent Protection (OCP)

An analog current limit circuit on each FET limits the current through the FET by removing the gate drive. If this analog current limit persists for longer than the OCP time, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. The device will remain disabled until either nRESET pin is applied, or VM is removed and re-applied.

Overcurrent conditions on both high and low side devices; i.e., a short to ground, supply, or across the motor winding will all result in an overcurrent shutdown. Note that overcurrent protection does not use the current sense circuitry used for PWM current control, and is independent of the I_{SENSE} resistor value or VREF voltage.

7.3.6.2 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled and the nFAULT pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume.

7.3.6.3 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pins falls below the undervoltage lockout threshold voltage, all circuitry in the device will be disabled and internal logic will be reset. Operation will resume when V_M rises above the UVLO threshold.

7.4 Device Functional Modes

7.4.1 nRESET and nSLEEP Operation

The nRESET pin, when driven active low, resets the internal logic. It also disables the H-bridge drivers. All inputs are ignored while nRESET is active. The nRESET pin has an internal pulldown resistor of 100 k Ω . The nSLEEP pin has an internal pulldown resistor of 1 M Ω .

Driving nSLEEP low will put the device into a low power sleep state. In this state, the H-bridge is disabled, the gate drive charge pump is stopped, the V3P3OUT regulator is disabled, and all internal clocks are stopped. In this state all inputs are ignored until nSLEEP returns inactive high. When returning from sleep mode, some time (approximately 1 ms) needs to pass before the motor driver becomes fully operational.

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

The DRV8828 is used in brushed motor or stepper motor control. The onboard current regulation allows for limiting the motor current through simple pin configurations.

8.2 Typical Application

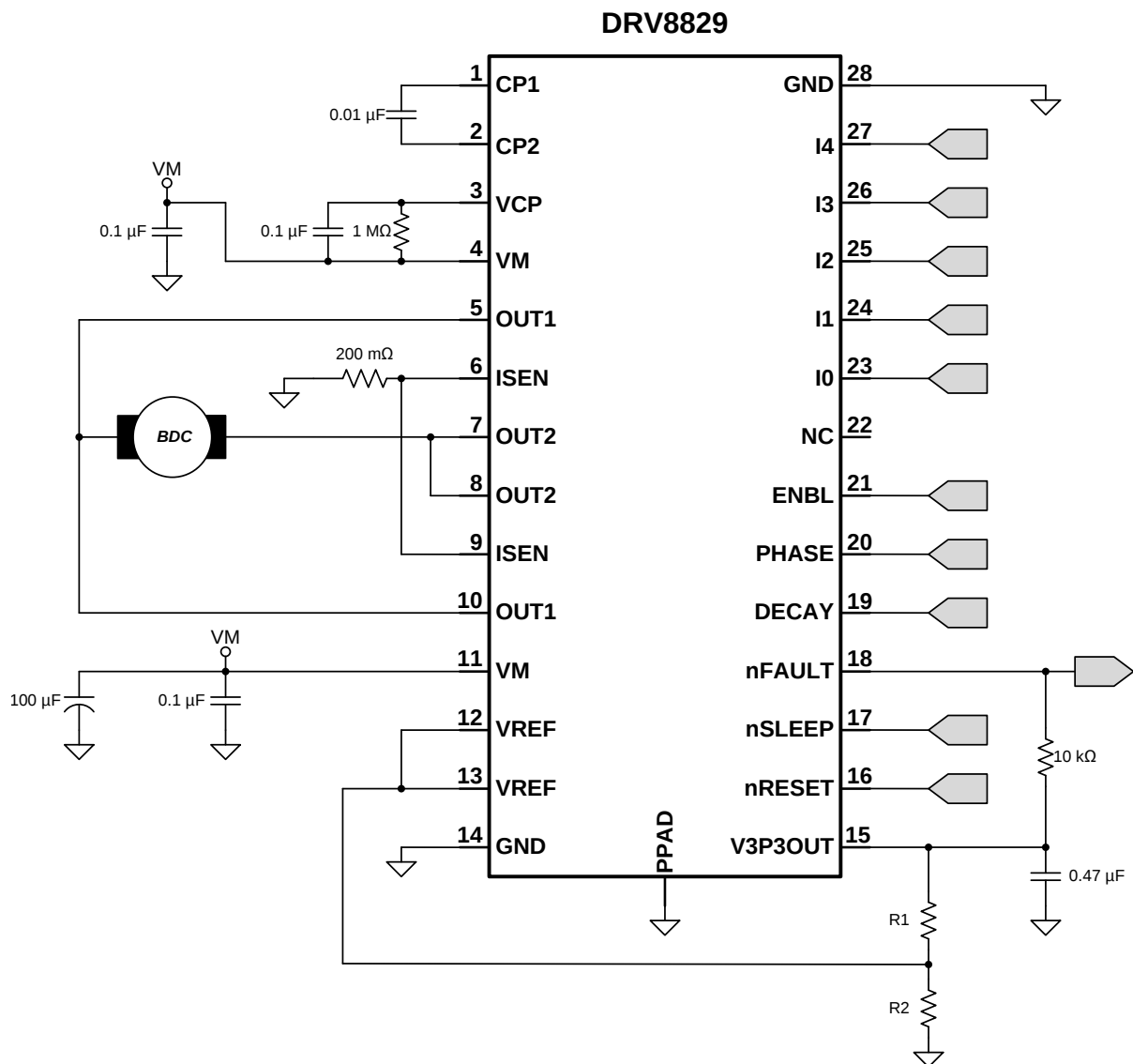


Figure 7. Motor Control Circuitry

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters listed in [Table 3](#)

Table 3. Design Parameters

PARAMETER	REFERENCE	VALUE
Supply Voltage	VM	24 V
Motor Winding Resistance	R _M	3.9 Ohm
Motor Winding Inductance	L _M	2.9 mH
Target Chopping Current	I _{TRIP}	1.5 A
Sense Resistor	R _{SENSE}	200 mΩ
VREF Voltage	VREF	1.5 V

8.2.2 Detailed Design Procedure

8.2.2.1 Current Regulation

The maximum current (ITRIP) is set by the Ix pins, the VREF analog voltage, and the sense resistor value (RSENSE). When starting a brushed DC motor, a large inrush current may occur because there is no back-EMF and high detent torque. Current regulation will act to limit this inrush current and prevent high current on start-up.

$$I_{TRIP} = \frac{VREF}{(5 \times R_{SENSE})} \quad (2)$$

Example - If the desired chopping current is 1.5 A:

- Set R_{SENSE} = 200 mΩ
- VREF would have to be 1.5 V
- Create a resistor divider network from V3P3OUT (3.3 V) to set VREF = 1.5 V
- Set R2 = 10 kΩ and set R1 = 12 kΩ

8.2.2.2 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

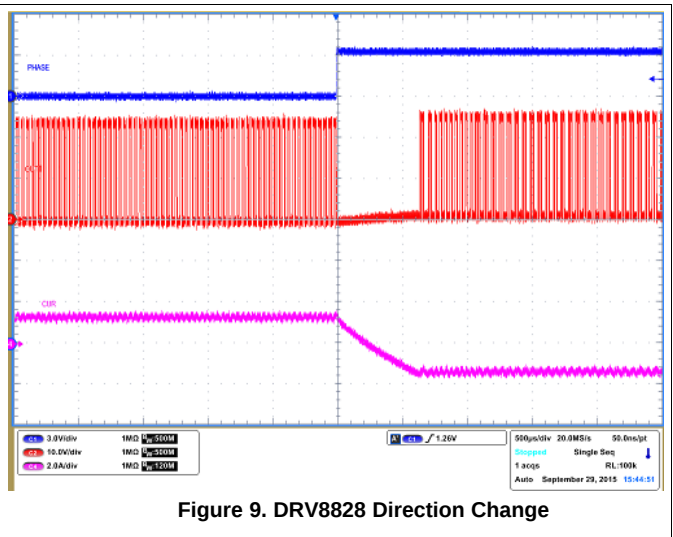
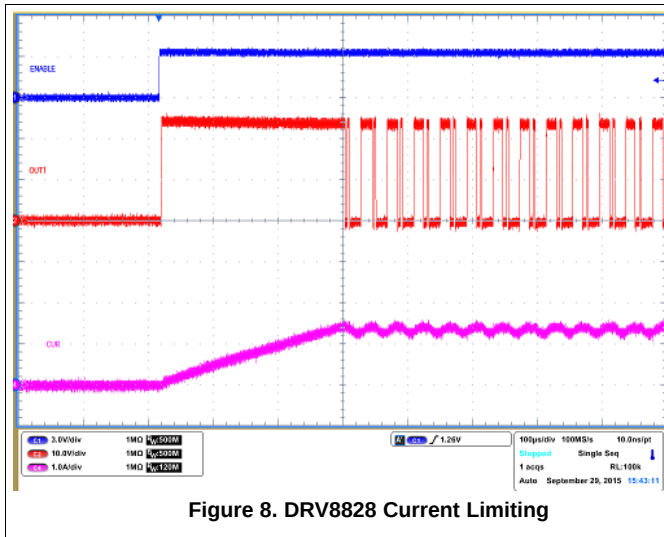
- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals Irms² x R. For example, if the RMS motor current is 1.5 A and a 200 mΩ sense resistor is used, the resistor will dissipate 1.5 A² x 0.2 Ω = 0.3 W. The power quickly increases with greater current levels.

Resistors typically have a rated power within some ambient temperature range, along with a de-rated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.2.3 Application Curves



9 Power Supply Recommendations

The DRV8828 is designed to operate from an input voltage supply (VM) range from 8.2 V to 45 V. The device has an absolute maximum rating of 47 V. A 0.1- μ F ceramic capacitor rated for VM must be placed at each VM pin as close to the DRV8828 as possible. In addition, a bulk capacitor must be included on VM.

9.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system.
- The power supply's capacitance and ability to source current.
- The amount of parasitic inductance between the power supply and motor system.
- The acceptable voltage ripple.
- The type of motor used (Brushed DC, Brushless DC, Stepper).
- The motor braking method.

The inductance between the power supply and motor drive system will limit the rate current can change from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

The voltage rating for bulk capacitors should be greater than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

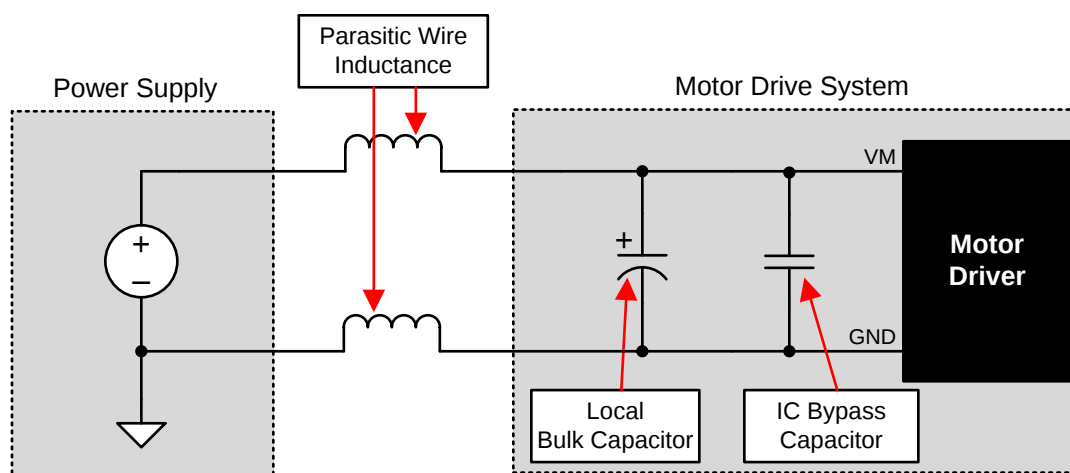


Figure 10. Setup of Motor Drive System With External Power Supply

10 Layout

10.1 Layout Guidelines

Each VM terminal must be bypassed to GND using a low-ESR ceramic bypass capacitors with recommended values of 0.1 μF rated for VM. These capacitors should be placed as close to the VM pins as possible with a thick trace or ground plane connection to the device GND pin.

The VM pin must be bypassed to ground using a bulk capacitor rated for VM. This component may be an electrolytic.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.1 μF rated for VM. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 0.47 μF rated for 16 V. Place this component as close to the pins as possible. In addition, place a 1 M Ω between VM and VCP.

Bypass V3P3OUT to ground with a ceramic capacitor rated 6.3 V. Place this bypassing capacitor as close to the pin as possible.

The current sense resistor should be placed as close as possible to the device pins to minimize trace inductance between the pin and resistor.

10.2 Layout Example

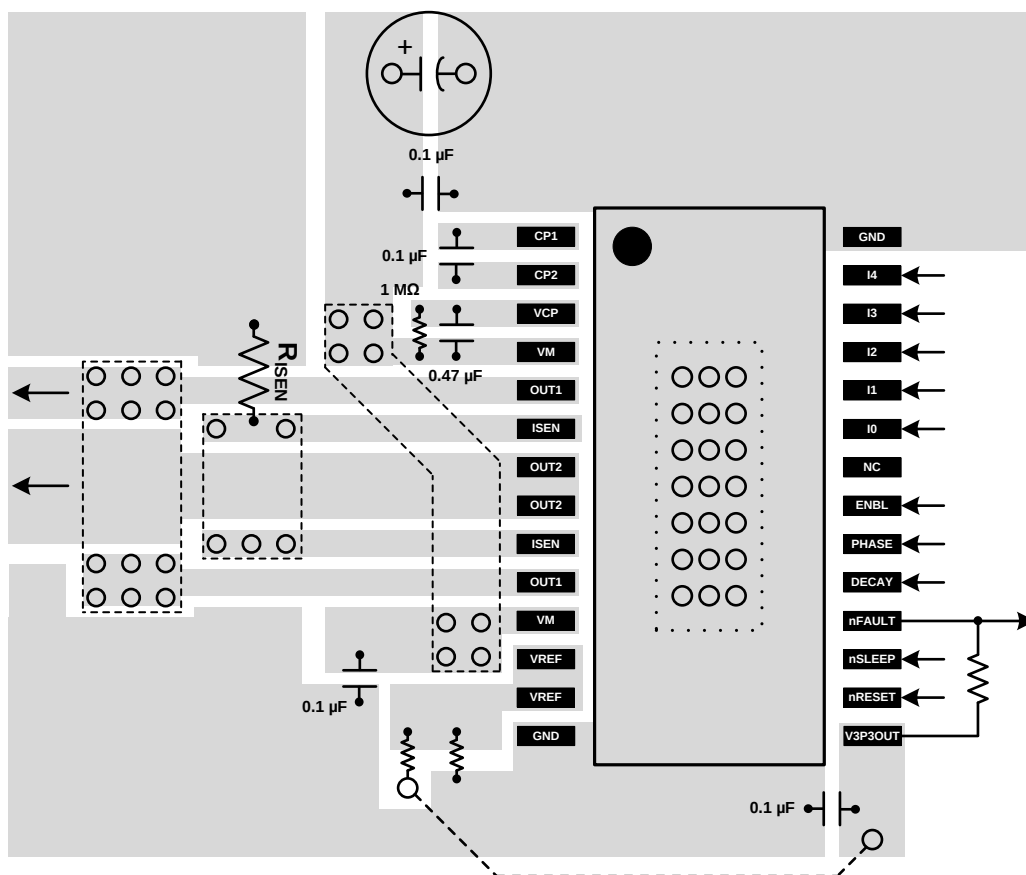


Figure 11. Example Layout

10.3 Power Dissipation

Power dissipation in the DRV8828 is dominated by the power dissipated in the output FET resistance, or $R_{DS(on)}$. Average power dissipation when running a brushed DC motor can be roughly estimated by Equation 3.

$$P_{TOT} = 2 \times R_{DS(on)} \times I_{OUT(RMS)}^2 \quad (3)$$

Where:

- P_{TOT} is the total power dissipation
- $R_{DS(on)}$ is the resistance of each FET (high-side and low-side)
- $I_{OUT(RMS)}$ is the RMS output current being applied to the motor

The maximum amount of power that can be dissipated in the devices is dependent on ambient temperature and heatsinking. $R_{DS(on)}$ increases with temperature, so as the device heats, the power dissipation increases. This must be taken into consideration when sizing the heatsink.

10.4 Heatsinking

The PowerPAD™ package uses an exposed pad to remove heat from the device. For proper operation, this pad must be thermally connected to copper on the PCB to dissipate heat. On a multi-layer PCB with a ground plane, this can be accomplished by adding a number of vias to connect the thermal pad to the ground plane. On PCBs without internal planes, copper area can be added on either side of the PCB to dissipate heat. If the copper area is on the opposite side of the PCB from the device, thermal vias are used to transfer the heat between top and bottom layers.

For details about how to design the PCB, refer to TI application report [SLMA002](#), *PowerPAD™ Thermally Enhanced Package* and TI application brief [SLMA004](#), *PowerPAD™ Made Easy*, available at www.ti.com.

In general, the more copper area that can be provided, the more power can be dissipated.

10.4.1 Thermal Information

The DRV8828 has thermal shutdown (TSD) as described above. If the die temperature exceeds approximately 150°C, the device will be disabled until the temperature drops to a safe level.

Any tendency of the device to enter TSD is an indication of either excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- PowerPAD™ Thermally Enhanced Package, [SLMA002](#)
- PowerPAD™ Made Easy, [SLMA004](#)

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DRV8828PWP	Obsolete	Production	HTSSOP (PWP) 28	-	-	Call TI	Call TI	-40 to 85	DRV8828
DRV8828PWPR	Active	Production	HTSSOP (PWP) 28	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DRV8828

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8828PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8828PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

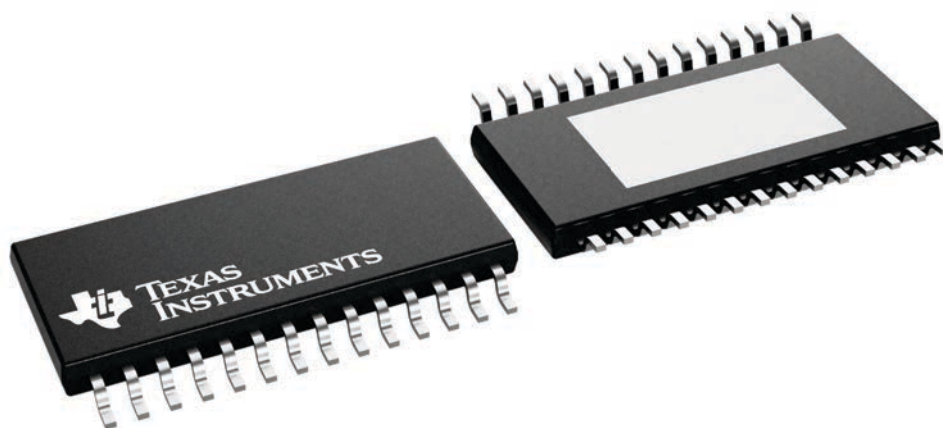
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

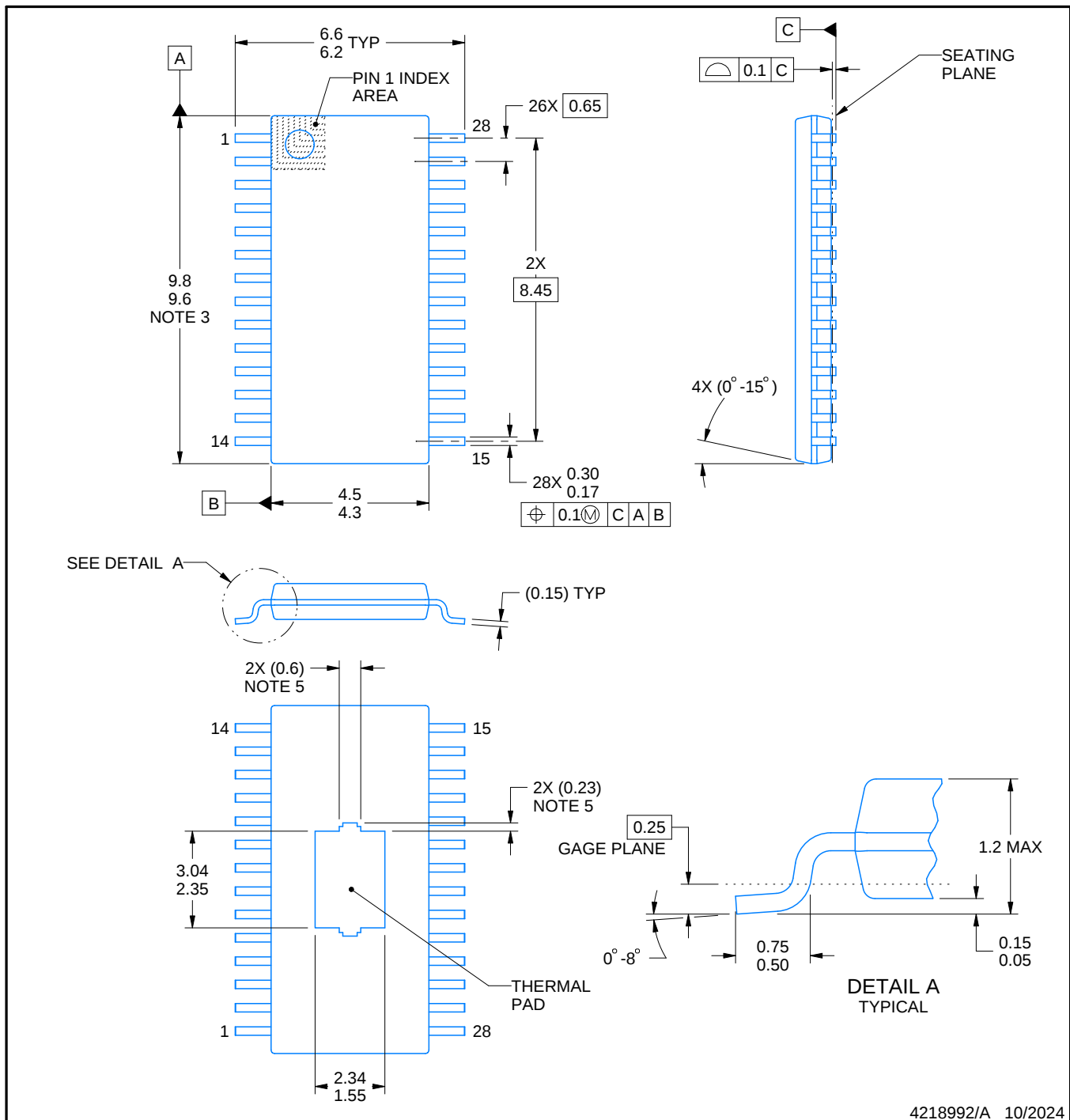
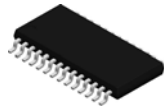
4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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4218992/A 10/2024

NOTES:

PowerPAD is a trademark of Texas Instruments.

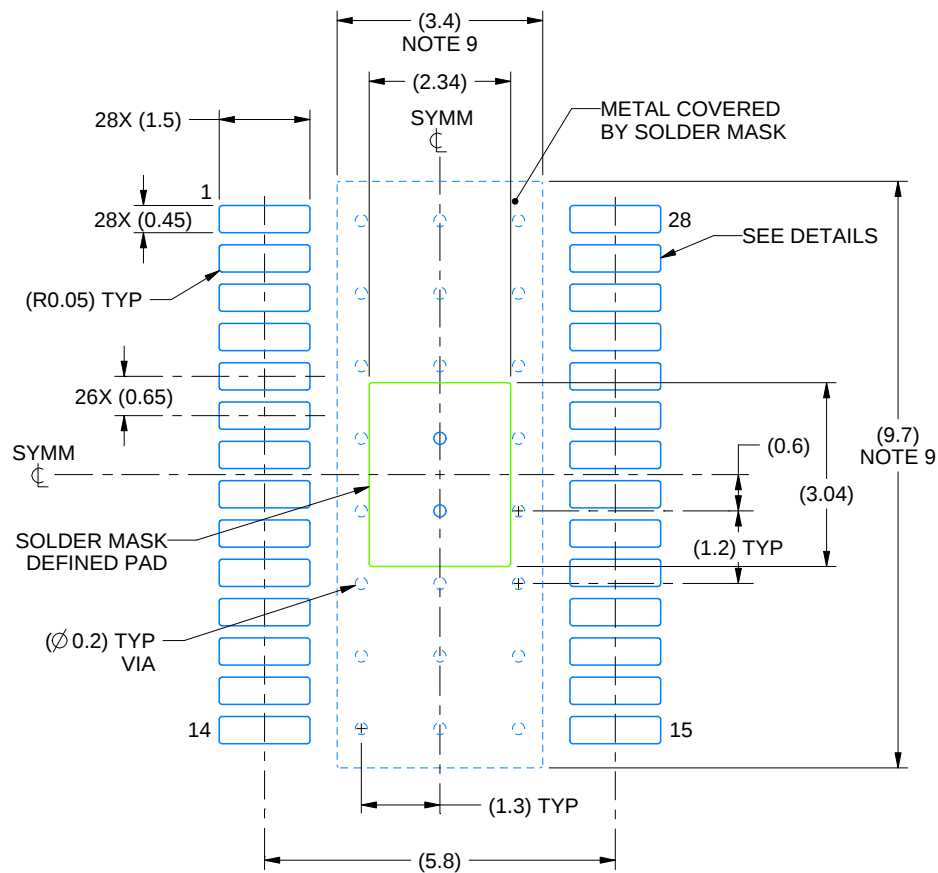
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

EXAMPLE BOARD LAYOUT

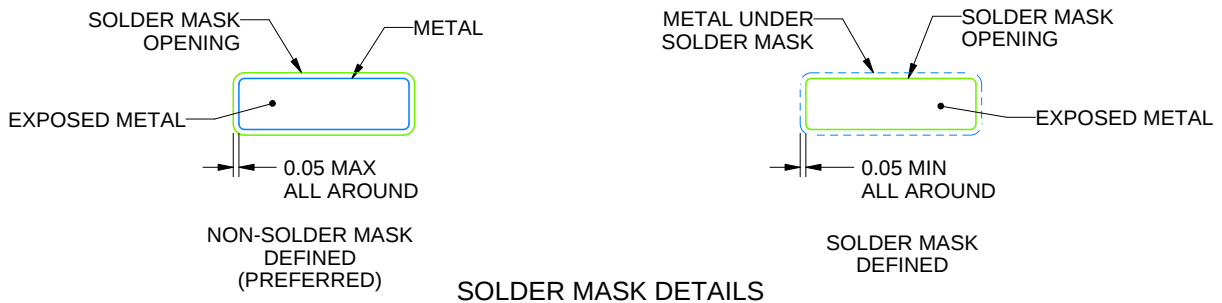
PWP0028H

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



4218992/A 10/2024

NOTES: (continued)

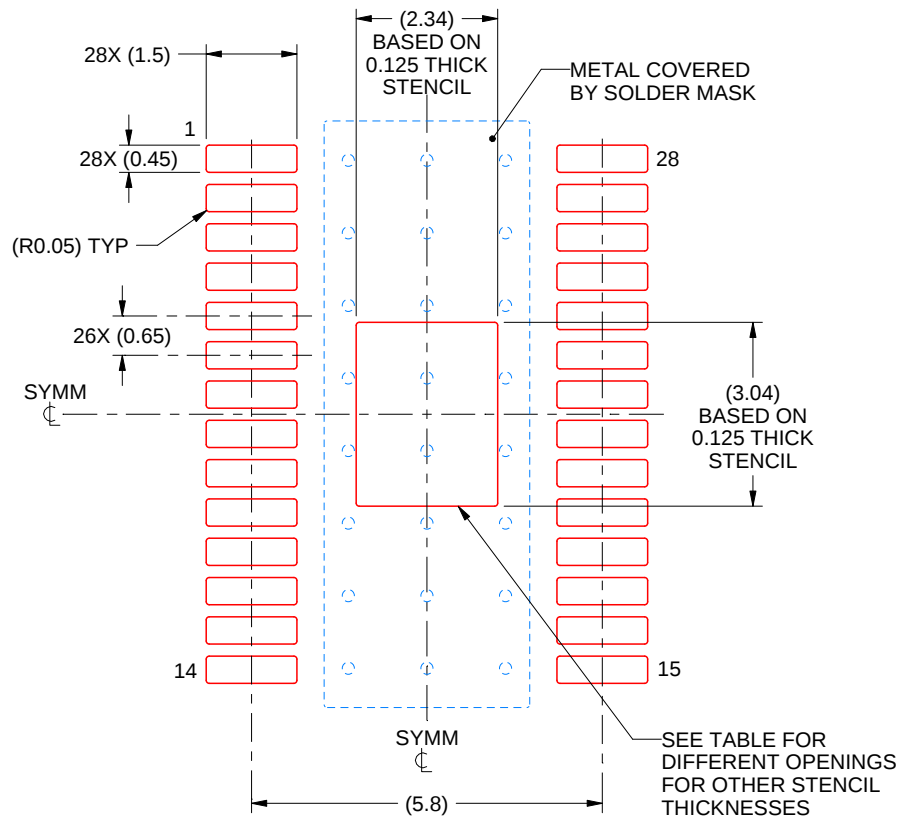
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

PWP0028H

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 3.40
0.125	2.34 X 3.04 (SHOWN)
0.15	2.14 X 2.78
0.175	1.98 X 2.57

4218992/A 10/2024

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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