

NID5001N

Self-Protected FET with Temperature and Current Limit

HDPlus devices are an advanced series of power MOSFETs which utilize ON Semiconductor's latest MOSFET technology process to achieve the lowest possible on-resistance per silicon area while incorporating smart features. Integrated thermal and current limits work together to provide short circuit protection. The devices feature an integrated Drain-to-Gate Clamp that enables them to withstand high energy in the avalanche mode. The Clamp also provides additional safety margin against unexpected voltage transients. Electrostatic Discharge (ESD) protection is provided by an integrated Gate-to-Source Clamp.

Features

- Low $R_{DS(on)}$
- Current Limitation
- Thermal Shutdown with Automatic Restart
- Short Circuit Protection
- $IdSS$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Slew Rate Control for Low Noise Switching
- Overvoltage Clamped Protection
- Pb-Free Package is Available

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage Internally Clamped	V_{DSS}	42	Vdc
Drain-to-Gate Voltage Internally Clamped ($R_{GS} = 1.0 \text{ M}\Omega$)	V_{DGR}	42	Vdc
Gate-to-Source Voltage	V_{GS}	± 14	Vdc
Drain Current – Continuous	I_D	Internally Limited	
Total Power Dissipation @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 1) @ $T_A = 25^\circ\text{C}$ (Note 2)	P_D	64 1.0 1.56	W
Thermal Resistance, Junction-to-Case Junction-to-Ambient (Note 1) Junction-to-Ambient (Note 2)	$R_{\theta JC}$ $R_{\theta JA}$ $R_{\theta JA}$	1.95 120 80	$^\circ\text{C}/\text{W}$
Single Pulse Drain-to-Source Avalanche Energy ($V_{DD} = 25 \text{ Vdc}$, $V_{GS} = 5.0 \text{ Vdc}$, $I_L = 4.5 \text{ Apk}$, $L = 120 \text{ mH}$, $R_G = 25 \Omega$)	E_{AS}	1215	mJ
Operating and Storage Temperature Range	T_J, T_{Stg}	-55 to 150	$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Minimum FR4 PCB, steady state.
2. Mounted onto a 2" square FR4 board
(1" square, 2 oz. Cu 0.06" thick single-sided, t = steady state).

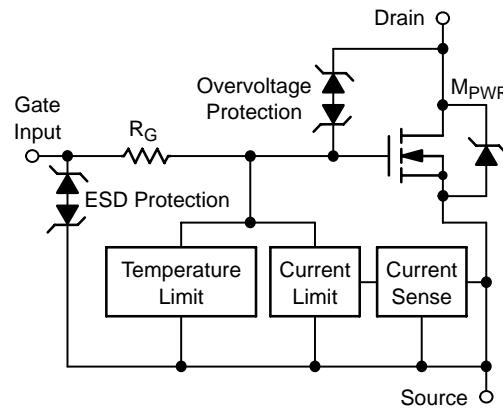


ON Semiconductor®

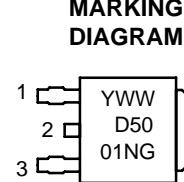
<http://onsemi.com>

V_{DSS} (Clamped)	$R_{DS(on)}$ TYP	I_D MAX (Limited)
42 V	23 m Ω @ 10 V	33 A*

*Max current may be limited below this value depending on input conditions.



DPAK
CASE 369C
STYLE 2



Y = Year
WW = Work Week
D5001N = Device Code
G = Pb-Free Package

1 = Gate
2 = Drain
3 = Source

ORDERING INFORMATION

Device	Package	Shipping [†]
NID5001NT4	DPAK	2500/Tape & Reel
NID5001NT4G	DPAK (Pb-Free)	2500/Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NID5001N

MOSFET ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Clamped Breakdown Voltage ($V_{GS} = 0 \text{ Vdc}$, $I_D = 250 \mu\text{Adc}$) ($V_{GS} = 0 \text{ Vdc}$, $I_D = 250 \mu\text{Adc}$, $T_J = 150^\circ\text{C}$)	$V_{(BR)DSS}$	42 42	46 44	50 50	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 32 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$) ($V_{DS} = 32 \text{ Vdc}$, $V_{GS} = 0 \text{ Vdc}$, $T_J = 150^\circ\text{C}$)	I_{DSS}		1.5 6.5	5.0	μAdc
Gate Input Current ($V_{GS} = 5.0 \text{ Vdc}$, $V_{DS} = 0 \text{ Vdc}$)	I_{GSSF}		50	100	μAdc

ON CHARACTERISTICS

Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1.2 \text{ mAdc}$) Threshold Temperature Coefficient	$V_{GS(\text{th})}$	1.0	1.8 5.0	2.0	Vdc -mV/°C
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 10 \text{ Vdc}$, $I_D = 5.0 \text{ Adc}$, $T_J @ 25^\circ\text{C}$) ($V_{GS} = 10 \text{ Vdc}$, $I_D = 5.0 \text{ Adc}$, $T_J @ 150^\circ\text{C}$)	$R_{DS(\text{on})}$		23 43	29 55	mΩ
Static Drain-to-Source On-Resistance (Note 3) ($V_{GS} = 5.0 \text{ Vdc}$, $I_D = 5.0 \text{ Adc}$, $T_J @ 25^\circ\text{C}$) ($V_{GS} = 5.0 \text{ Vdc}$, $I_D = 5.0 \text{ Adc}$, $T_J @ 150^\circ\text{C}$)	$R_{DS(\text{on})}$		28 50	34 60	mΩ
Source-Drain Forward On Voltage ($I_S = 5 \text{ A}$, $V_{GS} = 0 \text{ V}$)	V_{SD}		0.80	1.1	V

SWITCHING CHARACTERISTICS

Turn-on Time	$V_{GS} = 5.0 \text{ Vdc}$, $V_{DD} = 25 \text{ Vdc}$ $I_D = 1.0 \text{ Adc}$, Ext $R_G = 2.5 \Omega$	$T_{(\text{on})}$		32	40	μs
Turn-off Time		$T_{(\text{off})}$		68	75	
Turn-on Time	$V_{GS} = 10 \text{ Vdc}$, $V_{DD} = 25 \text{ Vdc}$, $I_D = 1.0 \text{ Adc}$, Ext $R_G = 2.5 \Omega$	$T_{(\text{on})}$		11	15	
Turn-off Time		$T_{(\text{off})}$		86	95	
Slew Rate On	$R_L = 4.7 \Omega$, $V_{in} = 0 \text{ to } 10 \text{ V}$, $V_{DD} = 12 \text{ V}$	$-dV_{DS}/dt_{\text{on}}$		0.5		V/ μs
Slew-Rate Off	$R_L = 4.7 \Omega$, $V_{in} = 10 \text{ to } 0 \text{ V}$, $V_{DD} = 12 \text{ V}$	dV_{DS}/dt_{off}		0.35		V/ μs

SELF PROTECTION CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Current Limit	($V_{GS} = 5.0 \text{ Vdc}$) $V_{DS} = 10 \text{ V}$ ($V_{GS} = 5.0 \text{ Vdc}$, $T_J = 150^\circ\text{C}$)	I_{LIM}	21 12	30 19	36 30	Adc
	($V_{GS} = 10 \text{ Vdc}$) $V_{DS} = 10 \text{ V}$ ($V_{GS} = 10 \text{ Vdc}$, $T_J = 150^\circ\text{C}$)		29 13	41 24	49 31	
Temperature Limit (Turn-off)	$V_{GS} = 5.0 \text{ Vdc}$	$T_{LIM(\text{off})}$	150	175	200	°C
Temperature Limit (Circuit Reset)	$V_{GS} = 5.0 \text{ Vdc}$	$T_{LIM(\text{on})}$	135	160	185	°C
Temperature Limit (Turn-off)	$V_{GS} = 10 \text{ Vdc}$	$T_{LIM(\text{off})}$	150	165	185	°C
Temperature Limit (Circuit Reset)	$V_{GS} = 10 \text{ Vdc}$	$T_{LIM(\text{on})}$	135	150	170	°C

ESD ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Electro-Static Discharge Capability Human Body Model (HBM) Machine Model (MM)	ESD	4000 400			V
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3. Pulse Test: Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL PERFORMANCE CURVES

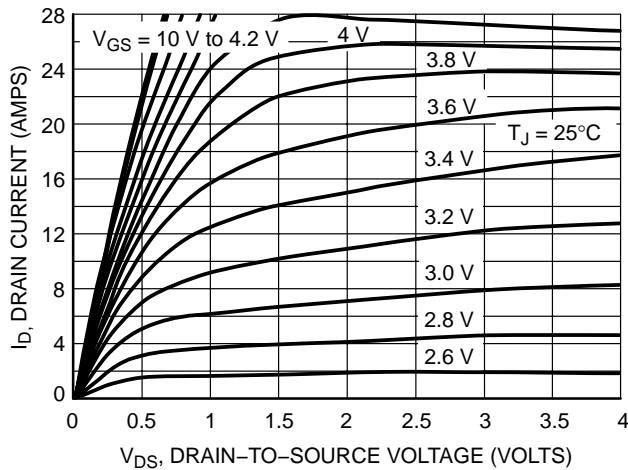


Figure 1. On-Region Characteristics

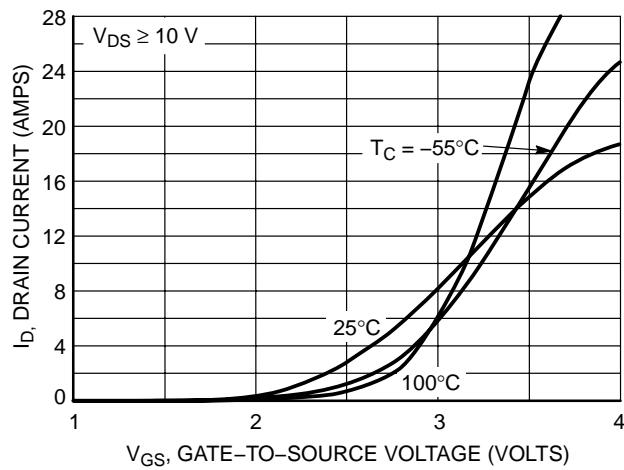


Figure 2. Transfer Characteristics

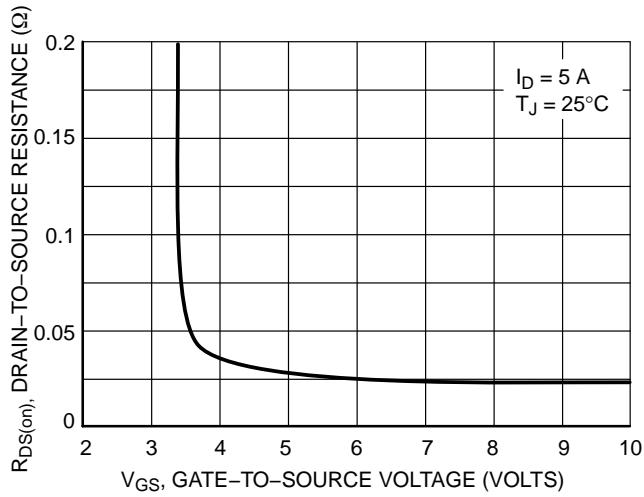


Figure 3. On-Resistance vs. Gate-to-Source Voltage

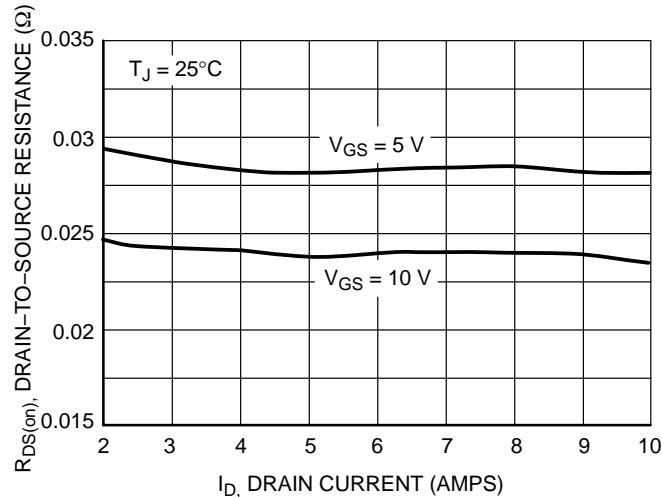


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

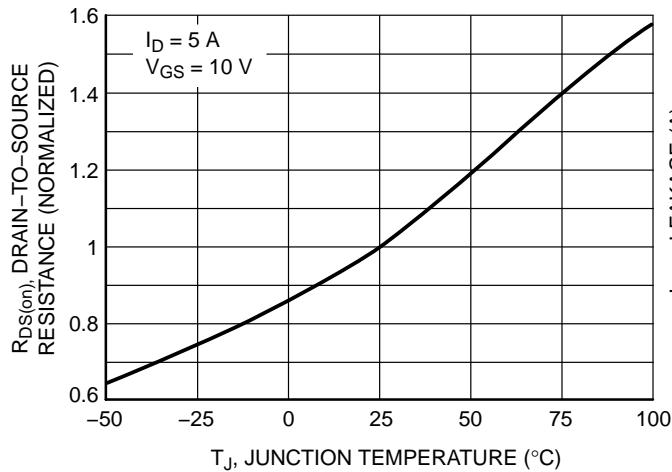


Figure 5. On-Resistance Variation with Temperature

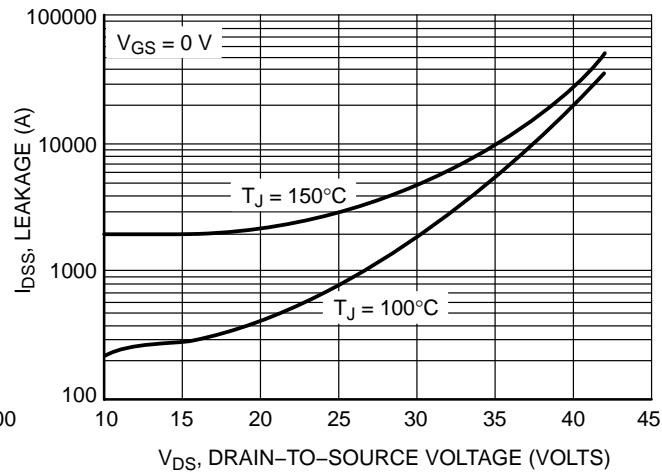


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES

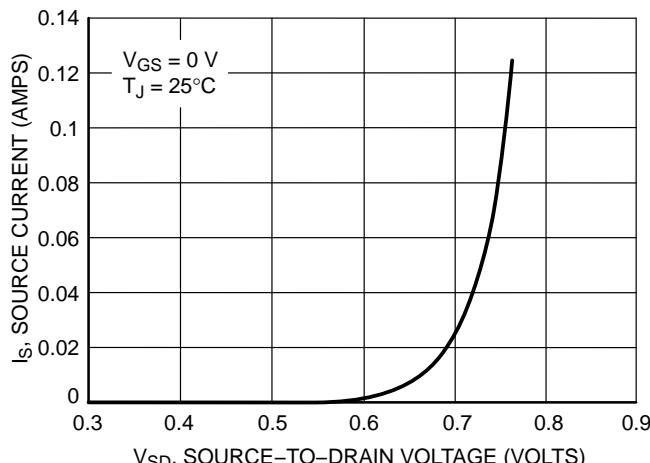


Figure 7. Diode Forward Voltage vs. Current

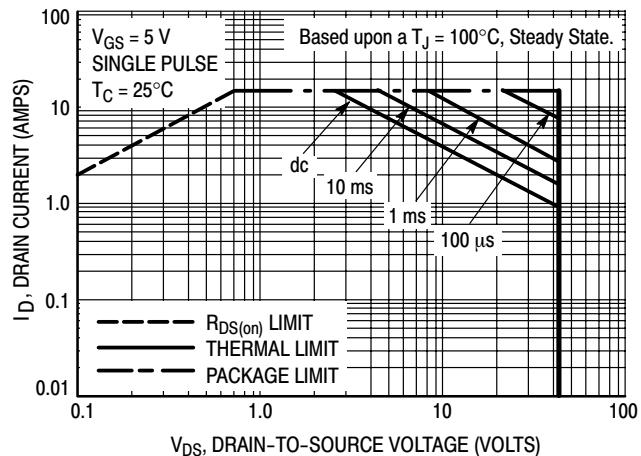
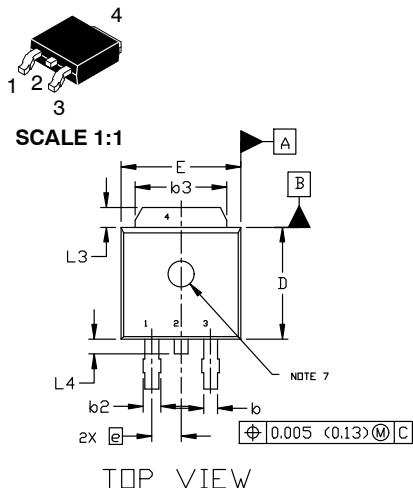


Figure 8. Maximum Rated Forward Biased Safe Operating Area

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

onsemi™



DPAK (SINGLE GAUGE)
CASE 369C
ISSUE G

DATE 31 MAY 2023

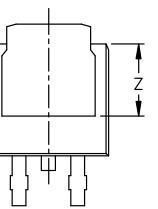
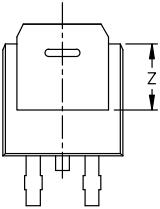
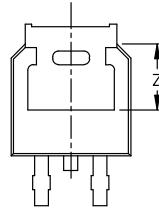
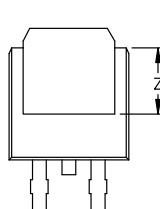
NOTES:

1. DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
7. OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC	0.229 BSC		
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114 REF	0.290 REF		
L2	0.020 BSC	0.51 BSC		
L3	0.035	0.050	0.89	1.27
L4	----	0.040	----	1.01
Z	0.155	----	3.93	----

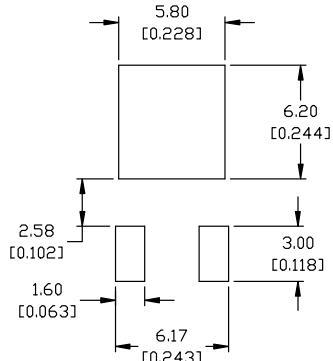
TOP VIEW

SIDE VIEW

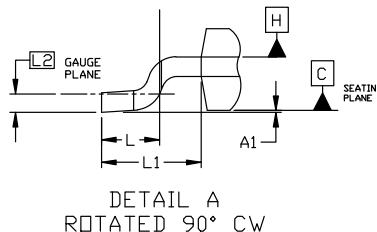


BOTTOM VIEW

BOTTOM VIEW



ALTERNATE CONSTRUCTIONS



DETAIL A
ROTATED 90° CW

RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. Emitter
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. Emitter
4. COLLECTOR

STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE

STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE

STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

XXXXXX	= Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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