

DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

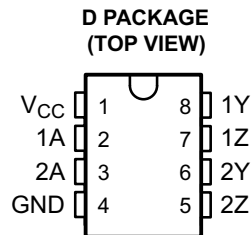
Check for Samples: [uA9638C-EP](#)

FEATURES

- Meets or Exceeds ANSI Standard EIA/TIA-422-B
- Operates From a Single 5-V Power Supply
- Drives Loads as Low as 50 Ω up to 15 Mbps
- TTL- and CMOS-Input Compatibility
- Output Short-Circuit Protection
- Interchangeable With National Semiconductor™ DS9638

SUPPORTS DEFENSE, AEROSPACE, AND MEDICAL APPLICATIONS

- Controlled Baseline
- One Assembly/Test Site
- One Fabrication Site
- Rated From -40°C to 85°C
- Extended Product Life Cycle
- Extended Product-Change Notification
- Product Traceability

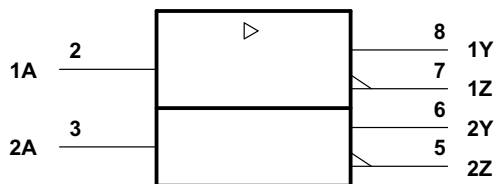


DESCRIPTION

The uA9638C is a dual high-speed differential line driver designed to meet ANSI Standard EIA/TIA-422-B. The inputs are TTL and CMOS compatible and have input clamp diodes. Schottky-diode-clamped transistors are used to minimize propagation delay time. This device operates from a single 5-V power supply and is supplied in an 8-pin package.

The uA9638 provides the current needed to drive low-impedance loads at high speeds. Typically used with twisted-pair cabling and differential receiver(s), base-band data transmission can be accomplished up to and exceeding 15 Mbps in properly designed systems. The uA9637A dual line receiver is commonly used as the receiver. For even faster switching speeds in the same pin configuration, see the SN75ALS191.

The uA9638C is characterized for operation from -40°C to 85°C .



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 1. Logic Symbol

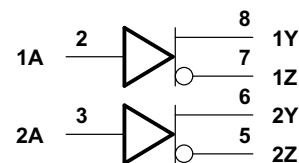


Figure 2. Logic Diagram



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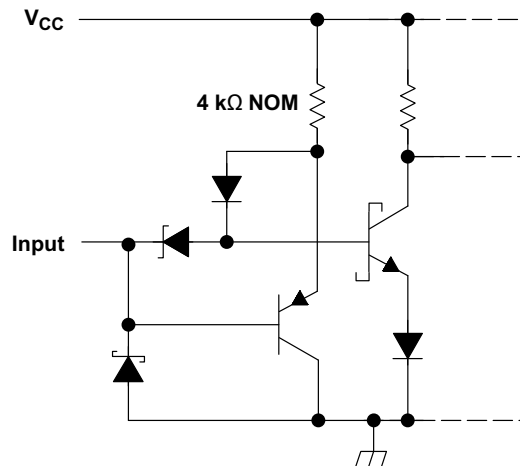
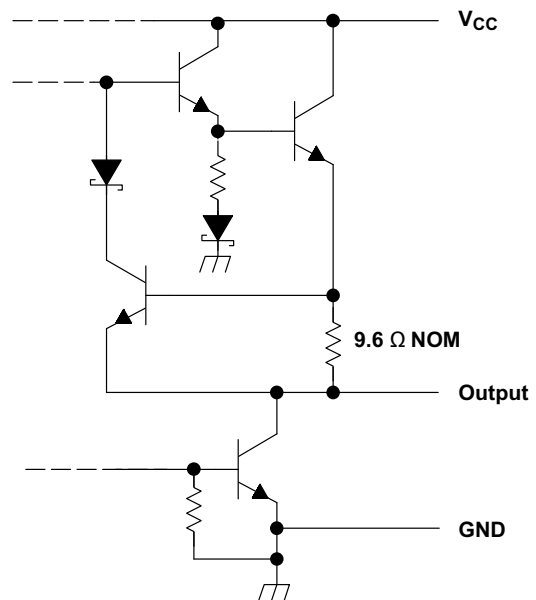
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ORDERING INFORMATION⁽¹⁾

$T_A = T_J$	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	VID NUMBER
–40°C to 85°C	SOIC - D	Reel of 2500	UA9638CIDREP	9638I	V62/12606-10XE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

SCHEMATICS OF INPUTS AND OUTPUTS**Figure 3. Equivalent of Each Input****Figure 4. Typical of All Inputs****ABSOLUTE MAXIMUM RATINGS⁽¹⁾**

over operating free-air temperature range (unless otherwise noted)

V_{CC}	Supply voltage range ⁽²⁾	–0.5 V to 7 V
V_I	Input voltage range	–0.5 V to 7 V
	Continuous total power dissipation	See Dissipation Ratings Table
	Lead temperature 1,6 mm (1/16 inch) from 10 seconds	260°C
T_A	Operating free-air temperature range	–40°C to 85°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Voltage values except differential output voltages are with respect to network GND.

(2) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		uA9638C	UNITS
		D	
		8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	114.3	°C/W
θ_{JC}	Junction-to-case thermal resistance	59.1	
θ_{JB}	Junction-to-board thermal resistance ⁽³⁾	55.3	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁴⁾	12.7	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁵⁾	54.7	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (4) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (5) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).

DISSIPATION RATINGS

PACKAGE	POWER RATING $T_A = 25^\circ\text{C}$ (mW)	DERATING FACTOR $T_A > 70^\circ\text{C}$ (mW/°C)	POWER RATING $T_A = 85^\circ\text{C}$ (mW)
D	725	8.75	199

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			-50	mA
I_{OL} Low-level output current			50	mA
T_A Operating free-air temperature	-40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
V_{IK} Input clamp voltage	$V_{CC} = 4.75\text{ V}$, $I_I = -18\text{ mA}$		-1	-1.2	V
V_{OH} High level output voltage	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$	$I_{OH} = -10\text{ mA}$ $I_{OH} = -40\text{ mA}$	2.5 2	3.5	V
V_{OL} Low level output voltage	$V_{CC} = 4.75\text{ V}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OL} = 40\text{ mA}$			0.5	V
$ V_{OD1} $ Magnitude of differential output voltage	$V_{CC} = 5.25\text{ V}$, $I_O = 0\text{ A}$		1.25 x V_{OD2}		V
$ V_{OD2} $ Magnitude of differential output voltage	$V_{CC} = 4.75\text{ V}$ to 5.25 V , $R_L = 100\ \Omega$, See Figure 5	2			V
$\Delta V_{OD} $ Change in magnitude of differential output voltage ⁽²⁾	$V_{CC} = 4.75\text{ V}$ to 5.25 V , $R_L = 100\ \Omega$, See Figure 5			±0.4	V
V_{OC} Common-mode output voltage ⁽³⁾	$V_{CC} = 4.75\text{ V}$ to 5.25 V , $R_L = 100\ \Omega$, See Figure 5			3	V

- (1) All typical values are at $V_{CC} = 5\text{ V}$ and $T_A = 25^\circ\text{C}$.
- (2) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from a high level to a low level or vice versa.
- (3) In Standard EIA-422-A, V_{OC} , which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS} .

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP ⁽¹⁾	MAX	UNIT
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage ⁽²⁾	$V_{CC} = 4.75\text{ V to } 5.25\text{ V}$, $R_L = 100\ \Omega$, See Figure 5			± 0.4	V
I_O Output current with power off	$V_{CC} = 0\text{ V}$		$V_O = 6\text{ V}$	0.1	100
			$V_O = -0.25\text{ V}$	-0.1	-100
			$V_O = -0.25\text{ V to } 6\text{ V}$	± 100	μA
I_I Input current	$V_{CC} = 5.25\text{ V}$, $V_I = 5.5\text{ V}$			50	μA
I_{IH} High-level input current	$V_{CC} = 5.25\text{ V}$, $V_I = 2.7\text{ V}$			25	μA
I_{IL} Low-level input current	$V_{CC} = 5.25\text{ V}$, $V_I = 0.5\text{ V}$			-200	μA
I_{OS} Short-circuit output current ⁽⁴⁾	$V_{CC} = 5.25\text{ V}$, $V_O = 0\text{ V}$	-50		-150	mA
I_{CC} Supply current (both drivers)	$V_{CC} = 5.25\text{ V}$, No load, All inputs at 0 V		45	65	mA

(4) Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$ Differential output delay time	$C_L = 15\text{ pF}$, $R_L = 100\ \Omega$, See Figure 6		10		ns
$t_{t(OD)}$ Differential output transition time	$C_L = 15\text{ pF}$, $R_L = 100\ \Omega$, See Figure 6		10		ns
$t_{sk(o)}$ Output skew	See Figure 6		1		ns

PARAMETER MEASUREMENT INFORMATION

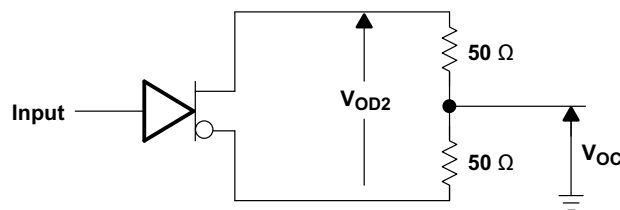
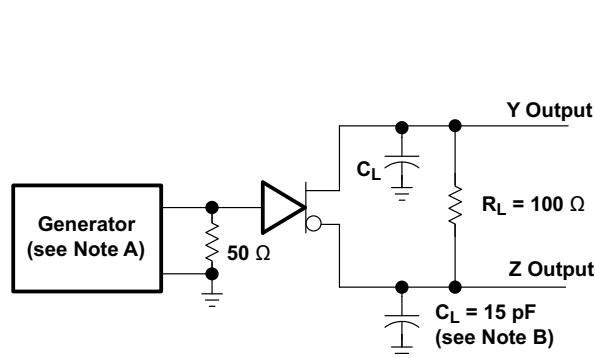
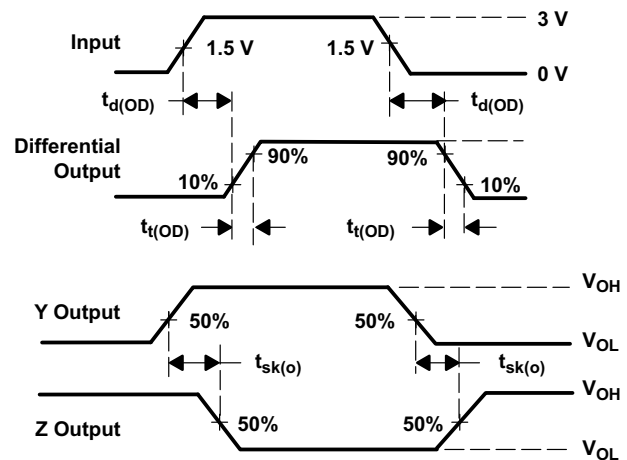


Figure 5. Differential and Common-Mode Output Voltages



TEST CIRCUIT

- The input pulse generator has the following characteristics: $Z_O = 50\ \Omega$, $PRR \leq 500\text{ kHz}$, $t_w = 100\text{ ns}$, $t_r \leq 5\text{ ns}$.
- C_L includes probe and jig capacitance.



VOLTAGE WAVEFORMS

Figure 6. Test Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
UA9638CIDREP	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I
UA9638CIDREP.A	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I
V62/12606-01XE	Active	Production	SOIC (D) 8	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	9638I

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

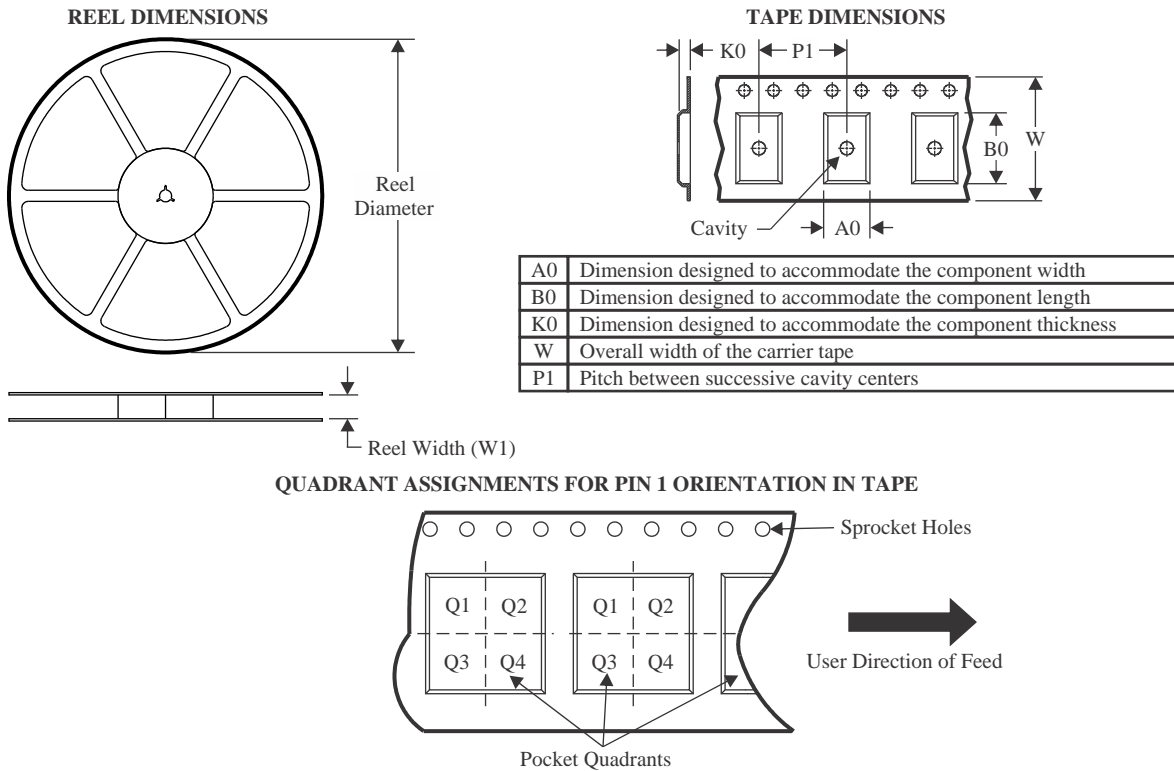
⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9638CIDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9638CIDREP	SOIC	D	8	2500	353.0	353.0	32.0

D0008A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

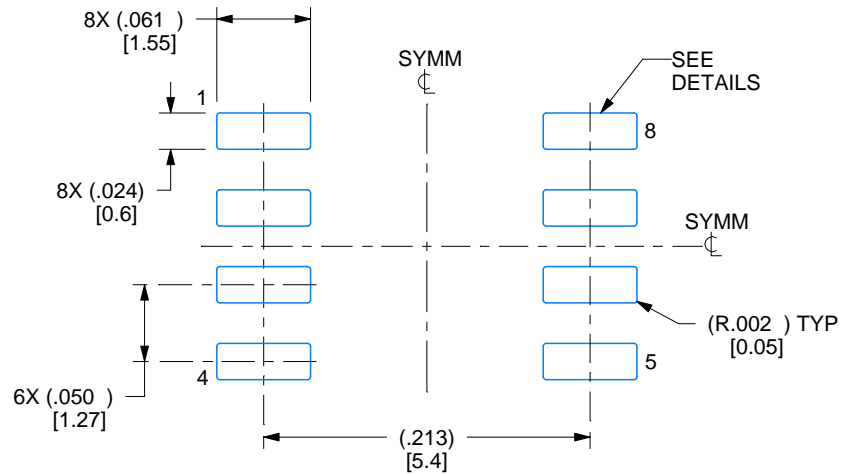
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

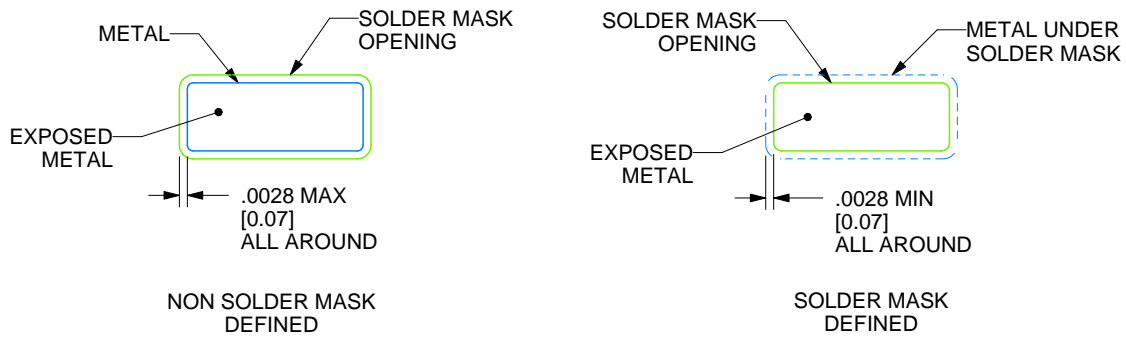
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

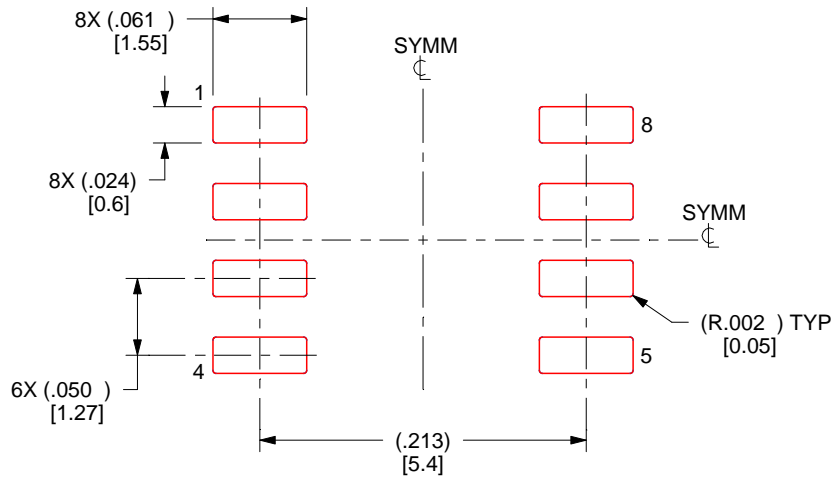
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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