

PCA9538

8-bit I²C-bus and SMBus Low-Power I/O Port with Interrupt and Reset

Rev. 8.1 — 21 May 2026

Product data sheet



1 General description

The PCA9538 is a 16-pin CMOS device that provides 8 bits of General-Purpose parallel Input/Output (GPIO) expansion with interrupt and reset for I²C-bus/SMBus applications and was developed to enhance the NXP Semiconductors family of I²C-bus I/O expanders. I/O expanders provide a simple solution when additional I/O is needed for ACPI power switches, sensors, push-buttons, LEDs, fans, and so on.

The PCA9538 consists of an 8-bit Configuration register (input or output selection), 8-bit Input Port register, 8-bit Output Port register, and an 8-bit Polarity Inversion register (active HIGH or active LOW operation). The system controller can enable the I/Os as either inputs or outputs by writing to the I/O configuration bits. The data for each input or output is kept in the corresponding Input Port or Output Port register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. The system controller can read all registers.

The PCA9538 is identical to the PCA9554 except for the removal of the internal I/O pullup resistor, which greatly reduces power consumption when the I/Os are held LOW, replacement of A2 with $\overline{\text{RESET}}$ and different address range.

The PCA9538 open-drain interrupt output ($\overline{\text{INT}}$) is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system controller that an input state has changed. The POR sets the registers to their default values and initializes the device state machine. The $\overline{\text{RESET}}$ pin causes the same reset/initialization to occur without de-powering the device.

Two hardware pins (A0 and A1) vary the fixed I²C-bus address and allow up to four devices to share the same I²C-bus/SMBus.



2 Features and benefits

- 8-bit I²C-bus GPIO with interrupt and reset
- Operating power supply voltage range of 2.3 V to 5.5 V (3.0 V to 5.5 V for PCA9538PW/Q900)
- 5 V tolerant I/Os
- Polarity Inversion register
- Active LOW interrupt output
- Active LOW reset input
- Low standby current
- Noise filter on SCL/SDA inputs
- No glitch on power up
- Internal power-on reset
- 8 I/O pins that default to 8 inputs
- 0 Hz to 400 kHz clock frequency
- ESD protection exceeds 2000 V HBM per JESD22-A114 and 1000 V CDM per JESD22-C101
- Latch-up testing is done to JEDEC Standard JESD78 that exceeds 100 mA
- Offered in three different packages: SO16, TSSOP16, and HVQFN16

3 Ordering information

[Table 1](#) describes the ordering information for PCA9538.

Table 1. Ordering information

Type number	Topside marking	Package		
		Name	Description	Version
PCA9538BS	9538	HVQFN16	Plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 4 × 4 × 0.85 mm	SOT629-1
PCA9538D	PCA9538D	SO16	Plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1
PCA9538PW	PCA9538	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
PCA9538PW/Q900 ^[1]	PCA9538	TSSOP16	Plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

[1] PCA9538PW/Q900 is AEC-Q100 compliant. Contact i2c.support@nxp.com for the PPAP.

3.1 Ordering options

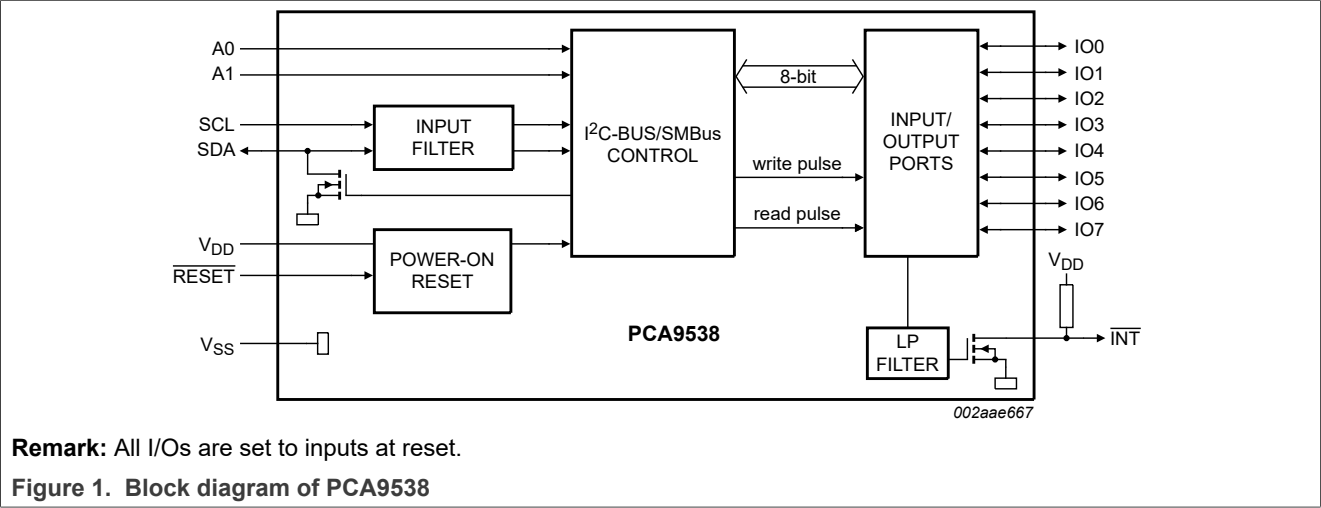
[Table 2](#) describes the ordering information for PCA9538.

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9538BS	PCA9538BS,118	HVQFN16	Reel pack, SMD, 13-inch	6000	T _{amb} = -40 ° C to +85 ° C
PCA9538D	PCA9538D,112	SO16	Tube, bulk pack	1920	T _{amb} = -40 ° C to +85 ° C
	PCA9538D,118	SO16	Reel pack, SMD, 13-inch	1000	T _{amb} = -40 ° C to +85 ° C
PCA9538PW	PCA9538PW,112	TSSOP16	Tube, bulk pack	2400	T _{amb} = -40 ° C to +85 ° C
	PCA9538PW,118	TSSOP16	Reel pack, SMD, 13-inch	2500	T _{amb} = -40 ° C to +85 ° C
PCA9538PW/Q900	PCA9538PW/Q900,118	TSSOP16	Reel pack, SMD, 13-inch	2500	T _{amb} = -40 ° C to +125 ° C

4 Block diagram

Figure 1 shows the labeled block diagram for PCA9538.

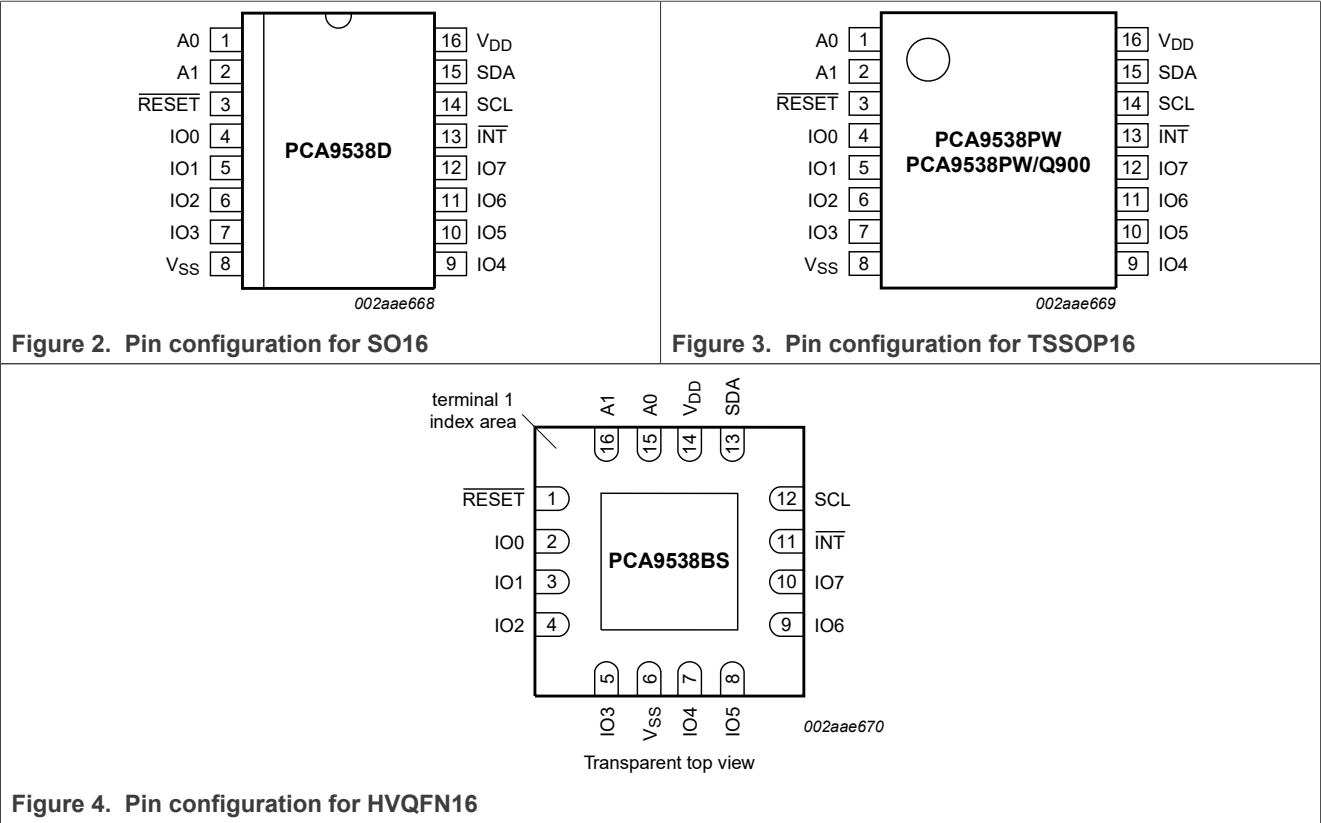


5 Pinning information

This section provides the pin configuration and description for PCA9538.

5.1 Pinning

Figure 2, Figure 3, and Figure 4 show the pinning of packages offered for PCA9538.



5.2 Pin description

Table 3 provides detailed description of various pins on packages offered for PCA9538.

Table 3. Pin description

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
A0	1	15	Address input 0
A1	2	16	Address input 1
RESET	3	1	Active LOW reset input
IO0	4	2	Input/output 0
IO1	5	3	Input/output 1
IO2	6	4	Input/output 2
IO3	7	5	Input/output 3

Table 3. Pin description...continued

Symbol	Pin		Description
	SO16, TSSOP16	HVQFN16	
V _{SS}	8	6 ^[1]	Supply ground
IO4	9	7	Input/output 4
IO5	10	8	Input/output 5
IO6	11	9	Input/output 6
IO7	12	10	Input/output 7
INT	13	11	Interrupt output (open-drain)
SCL	14	12	Serial clock line
SDA	15	13	Serial data line
V _{DD}	16	14	Supply voltage

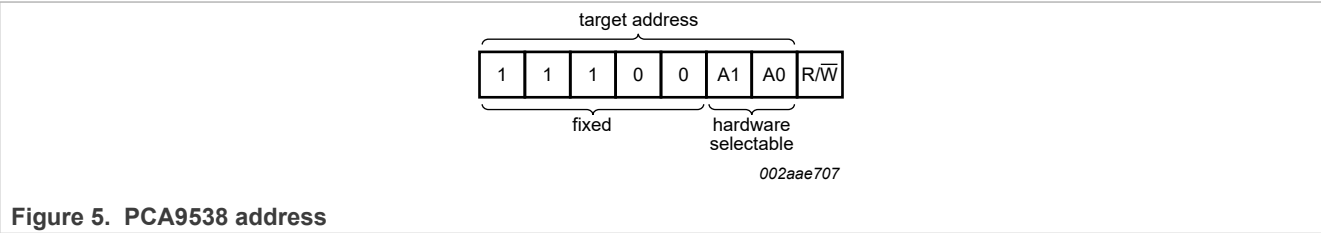
[1] HVQFN16 package die supply ground is connected to both the V_{SS} pin and the exposed center pad. The V_{SS} pin must be connected to the supply ground for proper device operation. For enhanced thermal, electrical, and board-level performance, the exposed pad must be soldered to the board using a corresponding thermal pad on the board. For proper heat conduction through the board, thermal vias must be incorporated in the printed-circuit board in the thermal pad region.

6 Functional description

Refer to [Figure 1](#).

6.1 Device address

[Figure 5](#) depicts the device address information for PCA9538.



6.2 Registers

This section describes the PCA9538 associated registers. It is further divided into the following subsections:

6.2.1 Command byte

The command byte is the first byte to follow the address byte during a write transmission. It is used as a pointer to determine which of the registers is written or read.

Table 4. Command byte

Command	Protocol	Function
0	Read byte	Input Port register
1	Read/write byte	Output Port register
2	Read/write byte	Polarity Inversion register
3	Read/write byte	Configuration register

6.2.2 Register 0 - Input Port register

This register is a read-only port. It reflects the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by Register 3. Writes to this register have no effect.

Table 5. Register 0 - Input Port register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	I7	Read only	X*	The default value 'X' is determined by externally applied logic level.
6	I6	Read only	X*	
5	I5	Read only	X*	
4	I4	Read only	X*	
3	I3	Read only	X*	
2	I2	Read only	X*	
1	I1	Read only	X*	

Table 5. Register 0 - Input Port register bit description...continued

Legend: * default value.

Bit	Symbol	Access	Value	Description
0	I0	Read only	X*	

6.2.3 Register 1 - Output Port register

This register reflects the outgoing logic levels of the pins defined as output by register 3. Bit values in this register have no effect on pins defined as inputs. Reads from this register return the value that is in the flip-flop controlling the output selection, **not** the actual pin value.

Table 6. Register 1 - Output Port register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	O7	R/W	1*	Reflects outgoing logic levels of pins defined as output by Register 3
6	O6	R/W	1*	
5	O5	R/W	1*	
4	O4	R/W	1*	
3	O3	R/W	1*	
2	O2	R/W	1*	
1	O1	R/W	1*	
0	O0	R/W	1*	

6.2.4 Register 2 - Polarity Inversion register

This register allows the user to invert the polarity of the Input Port register data. If a bit in this register is set (written with 1), the corresponding Input Port data is inverted. If a bit in this register is cleared (written with a 0), the Input Port data polarity is retained.

Table 7. Register 2 - Polarity Inversion register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	N7	R/W	0*	Inverts polarity of Input Port register data: 0 = Input Port register data retained (default value) 1 = Input Port register data inverted
6	N6	R/W	0*	
5	N5	R/W	0*	
4	N4	R/W	0*	
3	N3	R/W	0*	
2	N2	R/W	0*	
1	N1	R/W	0*	
0	N0	R/W	0*	

6.2.5 Register 3 - Configuration register

This register configures the directions of the I/O pins. If a bit in this register is set, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared, the corresponding port pin is enabled as an output. At reset, the I/Os are configured as inputs.

Table 8. Register 3 - Configuration register bit description

Legend: * default value.

Bit	Symbol	Access	Value	Description
7	C7	R/W	1*	Configures the directions of the I/O pins: 0 = Corresponding port pin enabled as an output 1 = Corresponding port pin configured as an input (default value)
6	C6	R/W	1*	
5	C5	R/W	1*	
4	C4	R/W	1*	
3	C3	R/W	1*	
2	C2	R/W	1*	
1	C1	R/W	1*	
0	C0	R/W	1*	

6.3 Power-on reset

When power is applied to V_{DD} , an internal Power-On Reset (POR) holds the PCA9538 in a reset condition until V_{DD} has reached V_{POR} . At that point, the reset condition is released and the PCA9538 registers and state machine initialize to their default states. Thereafter, V_{DD} must be lowered below 0.2 V to reset the device.

For a power reset cycle, V_{DD} must be lowered below 0.2 V and then restored to the operating voltage.

6.4 RESET input

A reset can be accomplished by holding the RESET pin LOW for a minimum of $t_{W(rst)}$. The PCA9538 registers and SMBus/I²C-bus state machine are held in their default state until the RESET input is once again HIGH. This input requires a pullup resistor to V_{DD} if no active connection is used.

6.5 Interrupt output

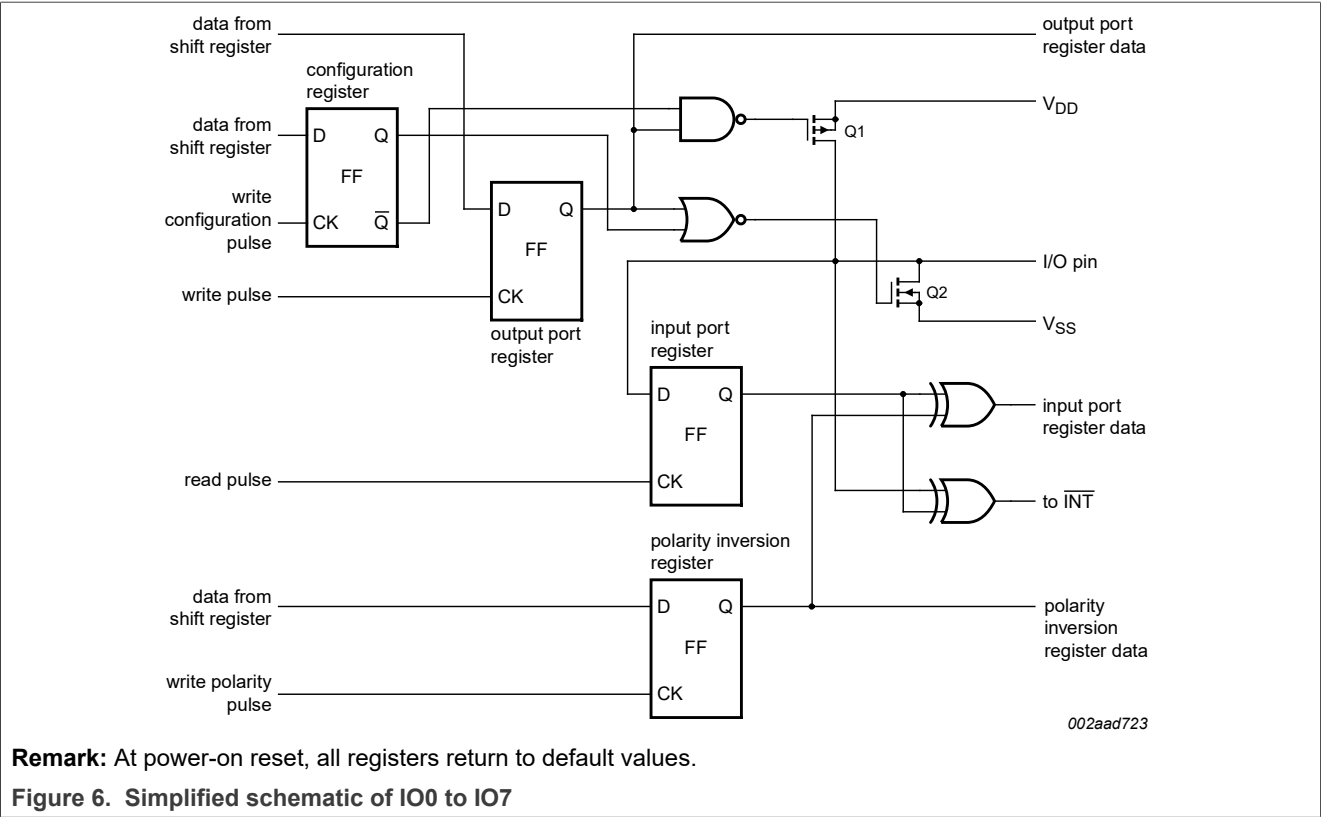
The open-drain interrupt output ($\overline{INT}$) is activated when one of the port pins changes state and the pin is configured as an input. The interrupt is deactivated when the input returns to its previous state or when the Input Port register is read.

Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register.

6.6 I/O port

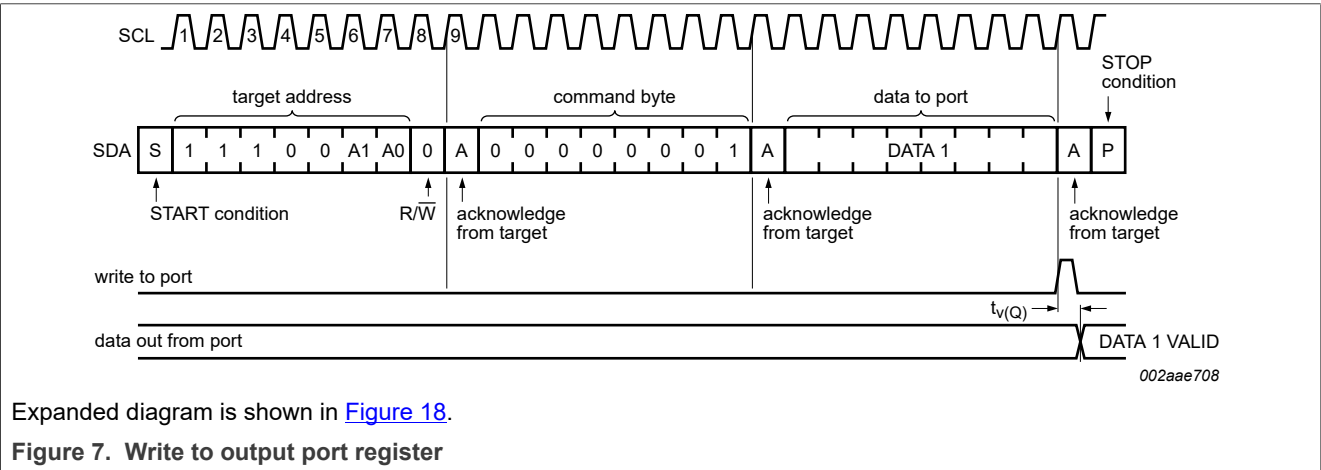
When an I/O is configured as an input, FETs Q1 and Q2 are off, creating a high-impedance input. The input voltage can be raised above V_{DD} to a maximum of 5.5 V.

If the I/O is configured as an output, then either Q1 or Q2 is enabled, depending on the state of the Output Port register. Care must be exercised if an external voltage is applied to an I/O configured as an output because of the low-impedance paths that exist between the pin and either V_{DD} or V_{SS} .



6.7 Bus transactions

Data is transmitted to the PCA9538 registers using the write mode as shown in [Figure 7](#) and [Figure 8](#). Data is read from the PCA9538 registers using the read mode as shown in [Figure 9](#) and [Figure 10](#). These devices do not implement an auto-increment function. Once a command byte is sent, the register that was addressed remains accessed by the reads until a new command byte is sent.



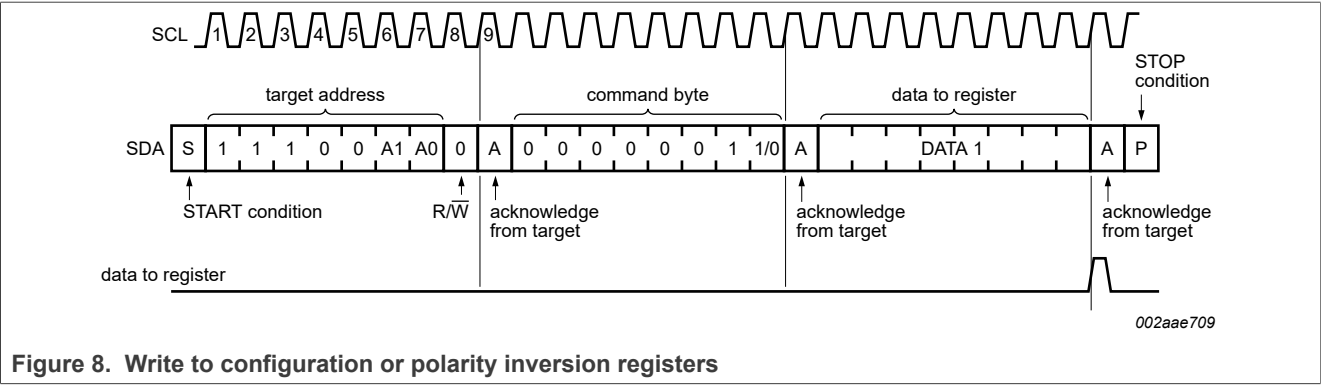


Figure 8. Write to configuration or polarity inversion registers

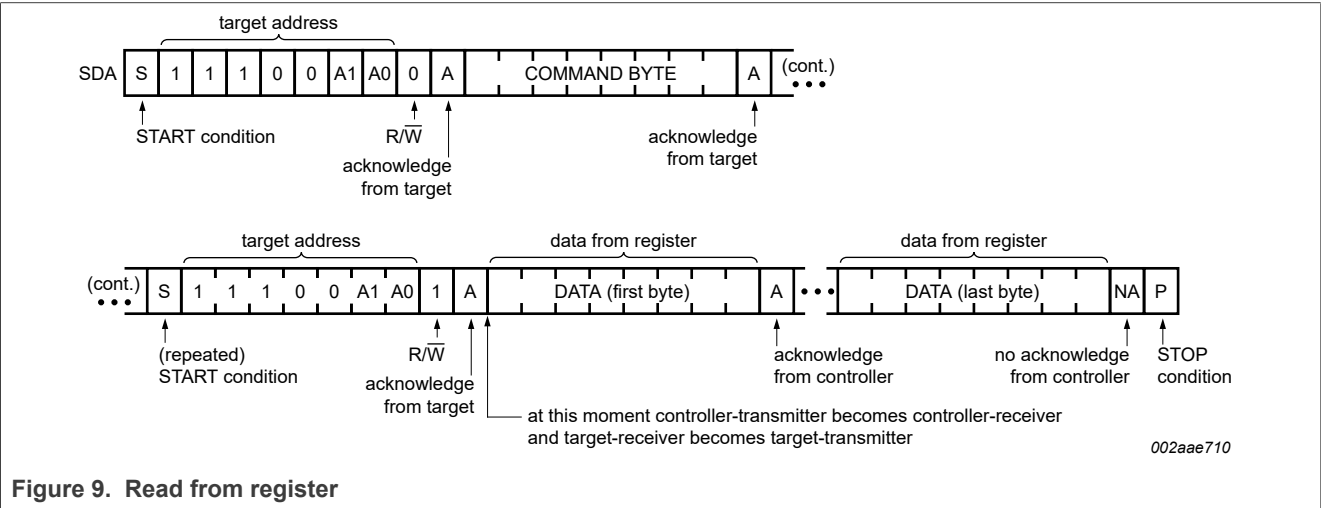
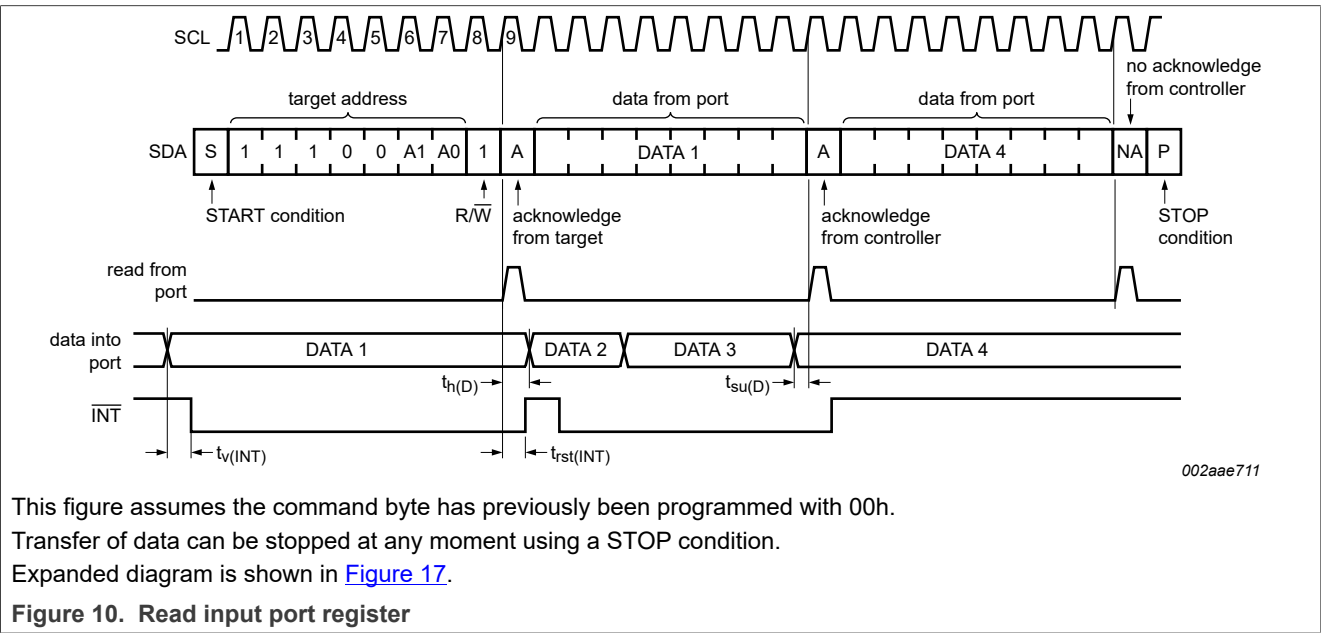


Figure 9. Read from register

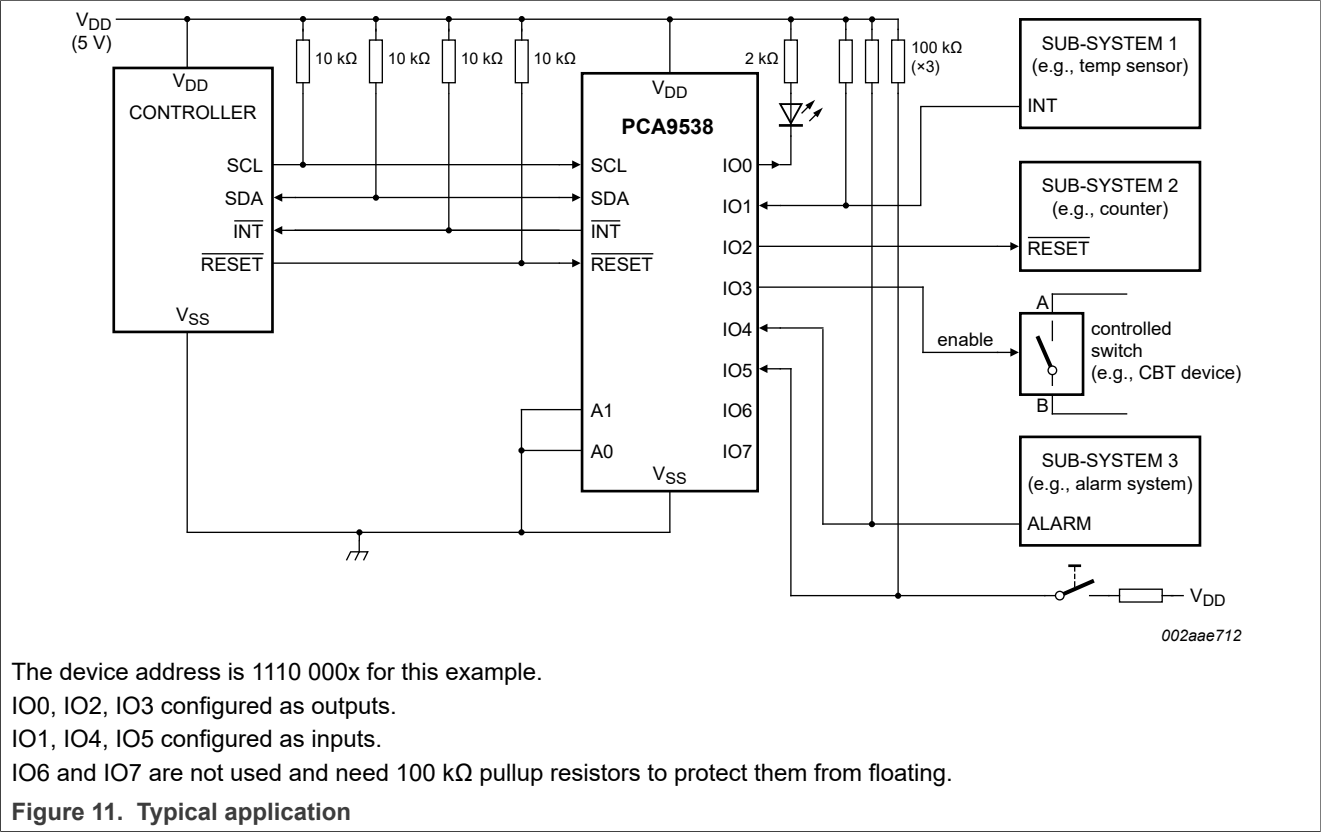


This figure assumes the command byte has previously been programmed with 00h. Transfer of data can be stopped at any moment using a STOP condition. Expanded diagram is shown in [Figure 17](#).

Figure 10. Read input port register

7 Application design-in information

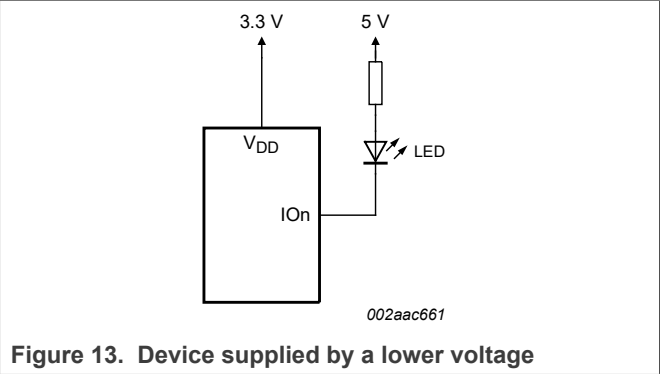
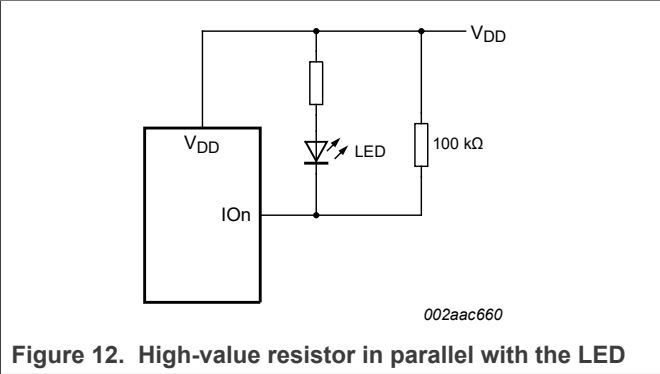
Figure 11 shows a typical application of PCA9538.



7.1 Minimizing I_{DD} when the I/Os are used to control LEDs

When the I/Os are used to control LEDs, they are normally connected to V_{DD} through a resistor as shown in Figure 11. Since the LED acts as a diode, when the LED is off the I/O V_I is about 1.2 V less than V_{DD}. The supply current, I_{DD}, increases as V_I becomes lower than V_{DD}.

Designs needing to minimize current consumption, such as battery power applications, must consider maintaining the I/O pins greater than or equal to V_{DD} when the LED is off. Figure 12 shows a high-value resistor in parallel with the LED. Figure 13 shows V_{DD} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_I at or above V_{DD} and prevents additional supply current consumption when the LED is off.



8 Limiting values

Table 9 describes the limiting values of PCA9538.

Table 9. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	Supply voltage		-0.5	+6.0	V
I _I	Input current		-	±20	mA
V _{I/O}	Voltage on an input/output pin		V _{SS} - 0.5	5.5	V
I _{O(IOn)}	Output current on pin IOn		-	±50	mA
I _{DD}	Supply current		-	85	mA
I _{SS}	Ground supply current		-	100	mA
P _{tot}	Total power dissipation		-	200	mW
T _{stg}	Storage temperature		-65	+150	°C
T _{amb}	Ambient temperature	Operating			
		All devices except PCA9538PW/Q900	-40	+85	°C
		PCA9538PW/Q900	-40	+125	°C
T _{j(max)}	Maximum junction temperature		-	+125	°C

9 Static characteristics

This section describes the static characteristics of PCA9538.

Table 10. Static characteristics for all devices except PCA9538PW/Q900

$V_{DD} = 2.3 \text{ V to } 5.5 \text{ V}$; $V_{SS} = 0 \text{ V}$; $T_{amb} = -40 \text{ }^{\circ}\text{C to } +85 \text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	Supply voltage		2.3	-	5.5	V
I_{DD}	Supply current	Operating mode; $V_{DD} = 5.5 \text{ V}$; no load; $f_{SCL} = 100 \text{ kHz}$	-	104	175	μA
I_{stbL}	LOW-level standby current	Standby mode; $V_{DD} = 5.5 \text{ V}$; no load; $V_I = V_{SS}$; $f_{SCL} = 0 \text{ kHz}$; I/O = inputs	-	0.25	1	μA
I_{stbH}	HIGH-level standby current	Standby mode; $V_{DD} = 5.5 \text{ V}$; no load; $V_I = V_{DD}$; $f_{SCL} = 0 \text{ kHz}$; I/O = inputs	-	0.25	1	μA
V_{POR}	Power-on reset voltage	No load; $V_I = V_{DD}$ or V_{SS} ^[1]	-	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	$V_{OL} = 0.4 \text{ V}$	3	7	-	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA
C_i	Input capacitance	$V_I = V_{SS}$	-	5	10	pF
I/Os						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V
I_{OL}	LOW-level output current	$V_{OL} = 0.5 \text{ V}$				
		$V_{DD} = 2.3 \text{ V}$ ^[2]	8	10	-	mA
		$V_{DD} = 3.0 \text{ V}$ ^[2]	8	14	-	mA
		$V_{DD} = 4.5 \text{ V}$ ^[2]	8	17	-	mA
		$V_{OL} = 0.7 \text{ V}$				
		$V_{DD} = 2.3 \text{ V}$ ^[2]	10	13	-	mA
		$V_{DD} = 3.0 \text{ V}$ ^[2]	10	19	-	mA
		$V_{DD} = 4.5 \text{ V}$ ^[2]	10	24	-	mA
V_{OH}	HIGH-level output voltage	$I_{OH} = -8 \text{ mA}$				
		$V_{DD} = 2.3 \text{ V}$ ^[3]	1.8	-	-	V
		$V_{DD} = 3.0 \text{ V}$ ^[3]	2.6	-	-	V
		$V_{DD} = 4.5 \text{ V}$ ^[3]	4.1	-	-	V
		$I_{OH} = -10 \text{ mA}$				
		$V_{DD} = 2.3 \text{ V}$ ^[3]	1.7	-	-	V

8-bit I²C-bus and SMBus Low-Power I/O Port with Interrupt and Reset

Table 10. Static characteristics for all devices except PCA9538PW/Q900...continued

 $V_{DD} = 2.3\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{DD} = 3.0\text{ V}$ ^[3]	2.5	-	-	V
		$V_{DD} = 4.5\text{ V}$ ^[3]	4.0	-	-	V
I_{LI}	Input leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA
C_i	Input capacitance		-	5	10	pF
Interrupt INT						
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	13	-	mA
Select inputs A0, A1, RESET						
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
I_{LI}	Input leakage current		-1	-	+1	μA

[1] V_{DD} must be lowered to 0.2 V, to reset the part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

Table 11. Static characteristics for PCA9538PW/Q900 AEC-Q100 compliant device

 $V_{DD} = 3.0\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supplies						
V_{DD}	Supply voltage		3.0	-	5.5	V
I_{DD}	Supply current	Operating mode; $V_{DD} = 5.5\text{ V}$; no load; $f_{SCL} = 100\text{ kHz}$	-	104	175	μA
I_{stbL}	LOW-level standby current	Standby mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{SS}$; $f_{SCL} = 0\text{ kHz}$; I/O = inputs	-	0.25	1	μA
I_{stbH}	HIGH-level standby current	Standby mode; $V_{DD} = 5.5\text{ V}$; no load; $V_I = V_{DD}$; $f_{SCL} = 0\text{ kHz}$; I/O = inputs	-	0.25	1	μA
V_{POR}	Power-on reset voltage	No load; $V_I = V_{DD}$ or V_{SS} ^[1]	-	1.7	2.2	V
Input SCL; input/output SDA						
V_{IL}	LOW-level input voltage		-0.5	-	+0.3 V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7 V_{DD}	-	5.5	V
I_{OL}	LOW-level output current, SDA	$V_{OL} = 0.4\text{ V}$				
		$V_{DD} = 5.5\text{ V}$	3	7	-	mA
		$V_{DD} = 3.0\text{ V}$	2.5	-	-	mA
I_L	Leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA
C_i	Input capacitance	$V_I = V_{SS}$	-	5	10	pF
I/Os						
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V

Table 11. Static characteristics for PCA9538PW/Q900 AEC-Q100 compliant device...continued

 $V_{DD} = 3.0\text{ V to }5.5\text{ V}$; $V_{SS} = 0\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
I_{OL}	LOW-level output current	$V_{OL} = 0.5\text{ V}$				
		$V_{DD} = 4.5\text{ V}$ [2]	8	17	-	mA
		$V_{DD} = 3.0\text{ V}$ [2]	7.5	-	-	mA
		$V_{OL} = 0.7\text{ V}$				
		$V_{DD} = 4.5\text{ V}$ [2]	10	24	-	mA
		$V_{DD} = 3.0\text{ V}$ [2]	9.5	-	-	mA
V_{OH}	HIGH-level output voltage	$I_{OH} = -8\text{ mA}$				
		$V_{DD} = 4.5\text{ V}$ [3]	4.1	-	-	V
		$V_{DD} = 3.0\text{ V}$ [3]	2.5	-	-	V
		$I_{OH} = -10\text{ mA}$				
		$V_{DD} = 4.5\text{ V}$ [3]	4.0	-	-	V
		$V_{DD} = 3.0\text{ V}$ [3]	2.4	-	-	V
I_{LI}	Input leakage current	$V_I = V_{DD} = V_{SS}$	-1	-	+1	μA
C_i	Input capacitance		-	5	10	pF
Interrupt $\overline{\text{INT}}$						
I_{OL}	LOW-level output current	$V_{OL} = 0.4\text{ V}$	3	13	-	mA
Select inputs A0, A1, RESET						
V_{IL}	LOW-level input voltage		-0.5	-	+0.8	V
V_{IH}	HIGH-level input voltage		2.0	-	5.5	V
I_{LI}	Input leakage current		-1	-	+1	μA

[1] V_{DD} must be lowered to 0.2 V, to reset the part.

[2] Each I/O must be externally limited to a maximum of 25 mA and the device must be limited to a maximum current of 100 mA.

[3] The total current sourced by all I/Os must be limited to 85 mA.

10 Dynamic characteristics

This section describes the dynamic characteristics of PCA9538.

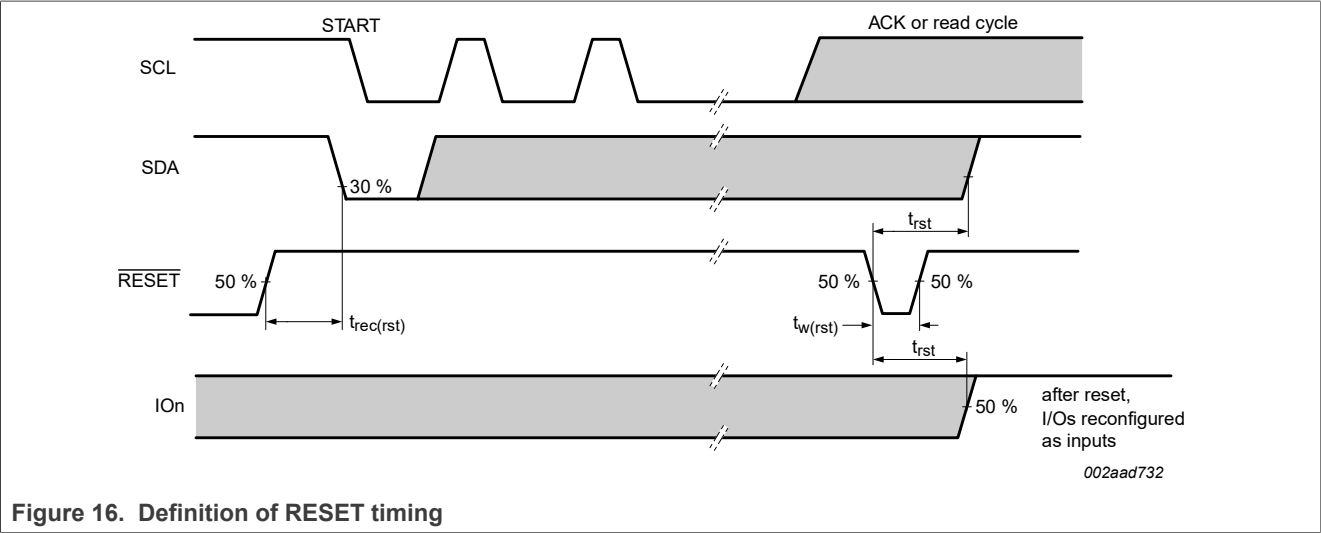
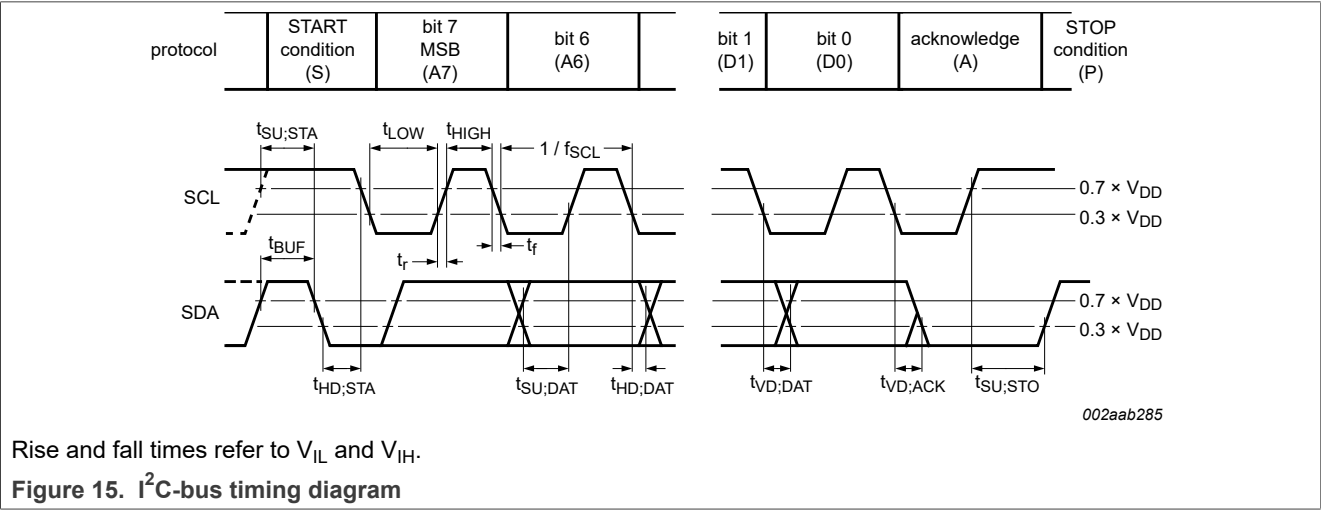
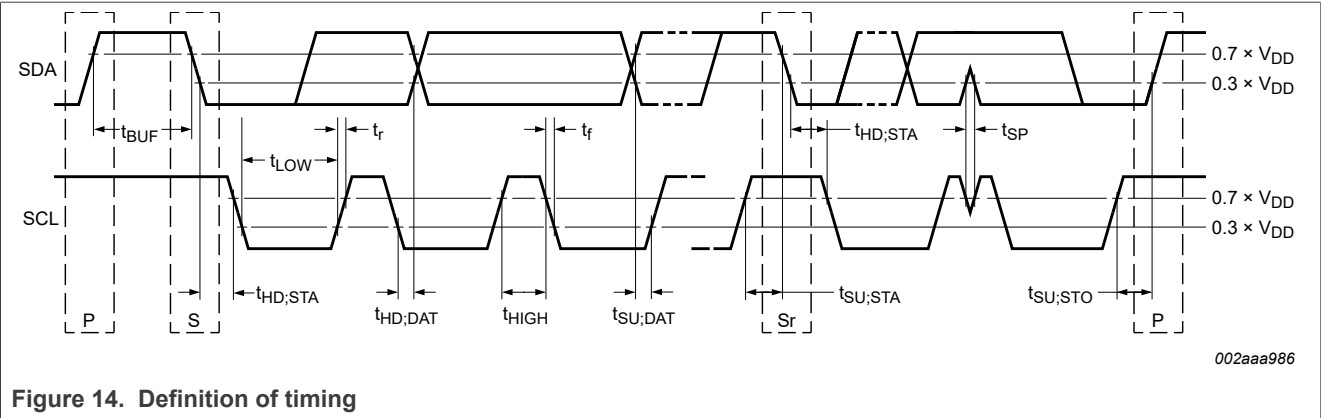
Table 12. Dynamic characteristics

Symbol	Parameter	Conditions	Standard-mode I ² C-bus		Fast-mode I ² C-bus		Unit
			Min	Max	Min	Max	
f _{SCL}	SCL clock frequency		0	100	0	400	kHz
t _{BUF}	Bus free time between a STOP and START condition		4.7	-	1.3	-	μs
t _{HD;STA}	Hold time (repeated) START condition		4.0	-	0.6	-	μs
t _{SU;STA}	Set-up time for a repeated START condition		4.7	-	0.6	-	μs
t _{SU;STO}	Set-up time for STOP condition		4.0	-	0.6	-	μs
t _{HD;DAT}	Data hold time		0	-	0	-	ns
t _{VD;ACK}	Data valid acknowledge time	[1]	0.3	3.45	0.1	0.9	μs
t _{VD;DAT}	Data valid time	[2]	300	-	50	-	ns
t _{SU;DAT}	Data set-up time		250	-	100	-	ns
t _{LOW}	LOW period of the SCL clock		4.7	-	1.3	-	μs
t _{HIGH}	HIGH period of the SCL clock		4.0	-	0.6	-	μs
t _r	Rise time of both SDA and SCL signals		-	1000	20 + 0.1C _b ^[3]	300	ns
t _f	Fall time of both SDA and SCL signals		-	300	20 + 0.1C _b ^[3]	300	ns
t _{SP}	Pulse width of spikes that must be suppressed by the input filter		-	50	-	50	ns
Port timing							
t _{V(Q)}	Data output valid time		-	200	-	200	ns
t _{SU(D)}	Data input set-up time		100	-	100	-	ns
t _{h(D)}	Data input hold time		1	-	1	-	μs
Interrupt timing							
t _{V(INT)}	Valid time on pin $\overline{\text{INT}}$		-	4	-	4	μs
t _{rst(INT)}	Reset time on pin $\overline{\text{INT}}$		-	4	-	4	μs
RESET							
t _{w(rst)}	Reset pulse width		4	-	4	-	ns
t _{rec(rst)}	Reset recovery time		0	-	0	-	ns
t _{rst}	Reset time		400	-	400	-	ns

[1] t_{VD;ACK} = time for acknowledgment signal from SCL LOW to SDA (out) LOW.

[2] t_{VD;DAT} = minimum time for the SDA data-out to be valid following SCL LOW.

[3] C_b = total capacitance of one bus line (in pF).



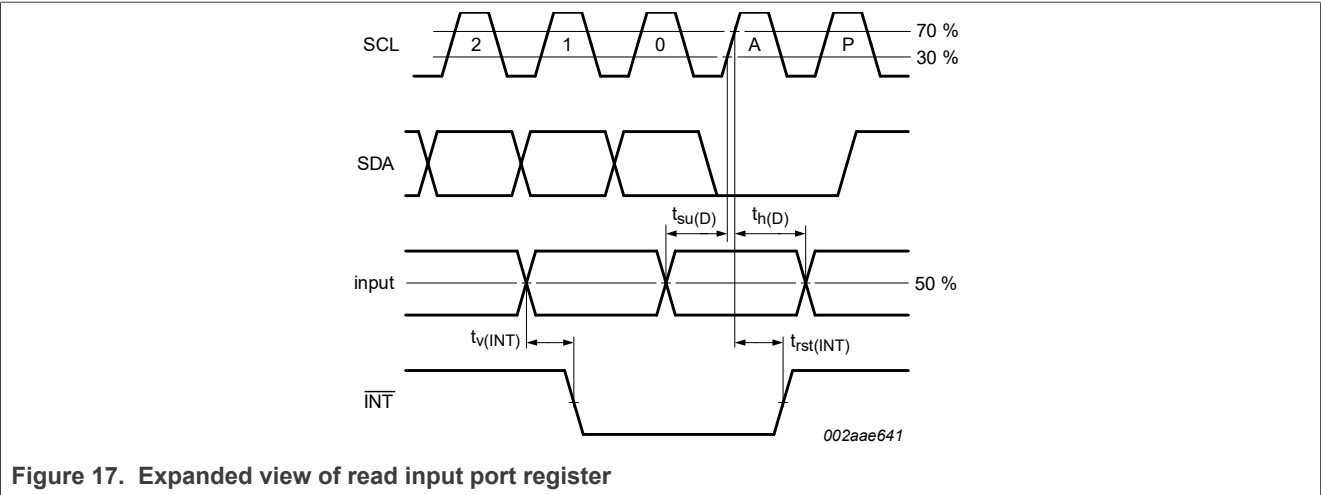


Figure 17. Expanded view of read input port register

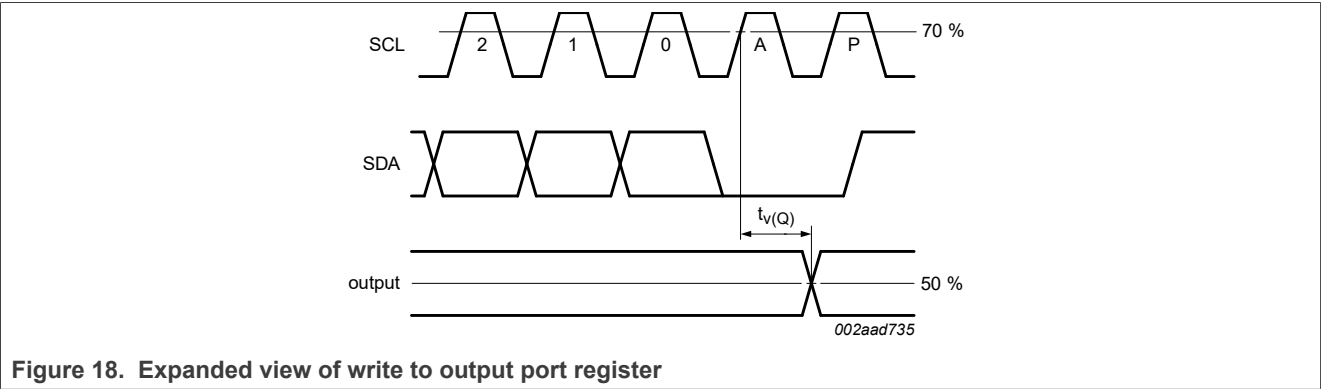


Figure 18. Expanded view of write to output port register

11 Test information

This section describes the test information regarding PCA9538.

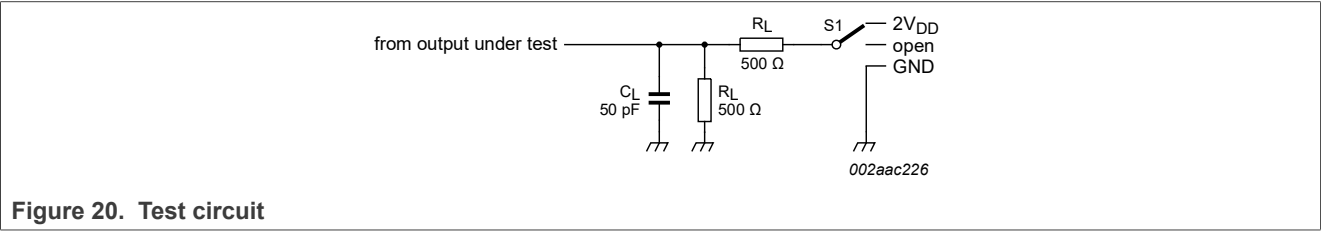
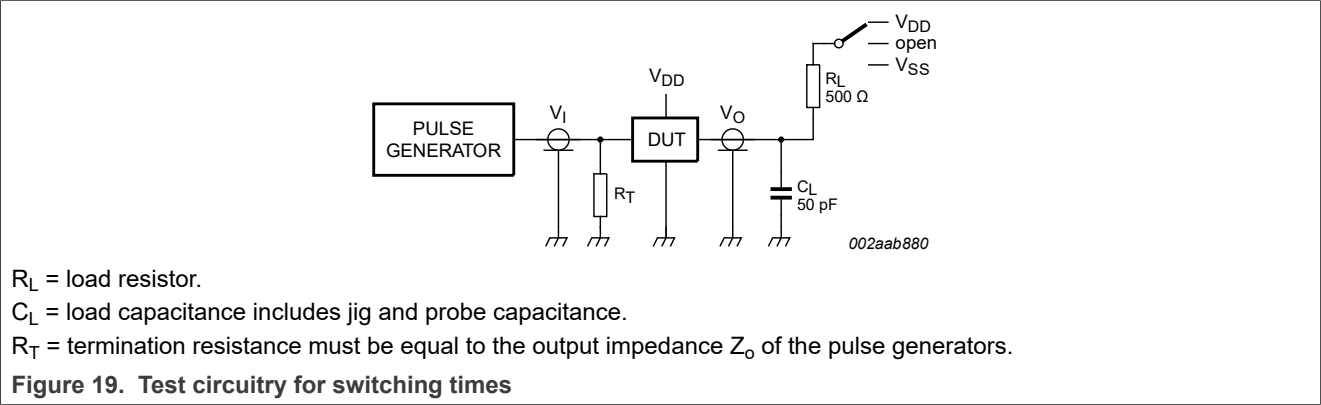
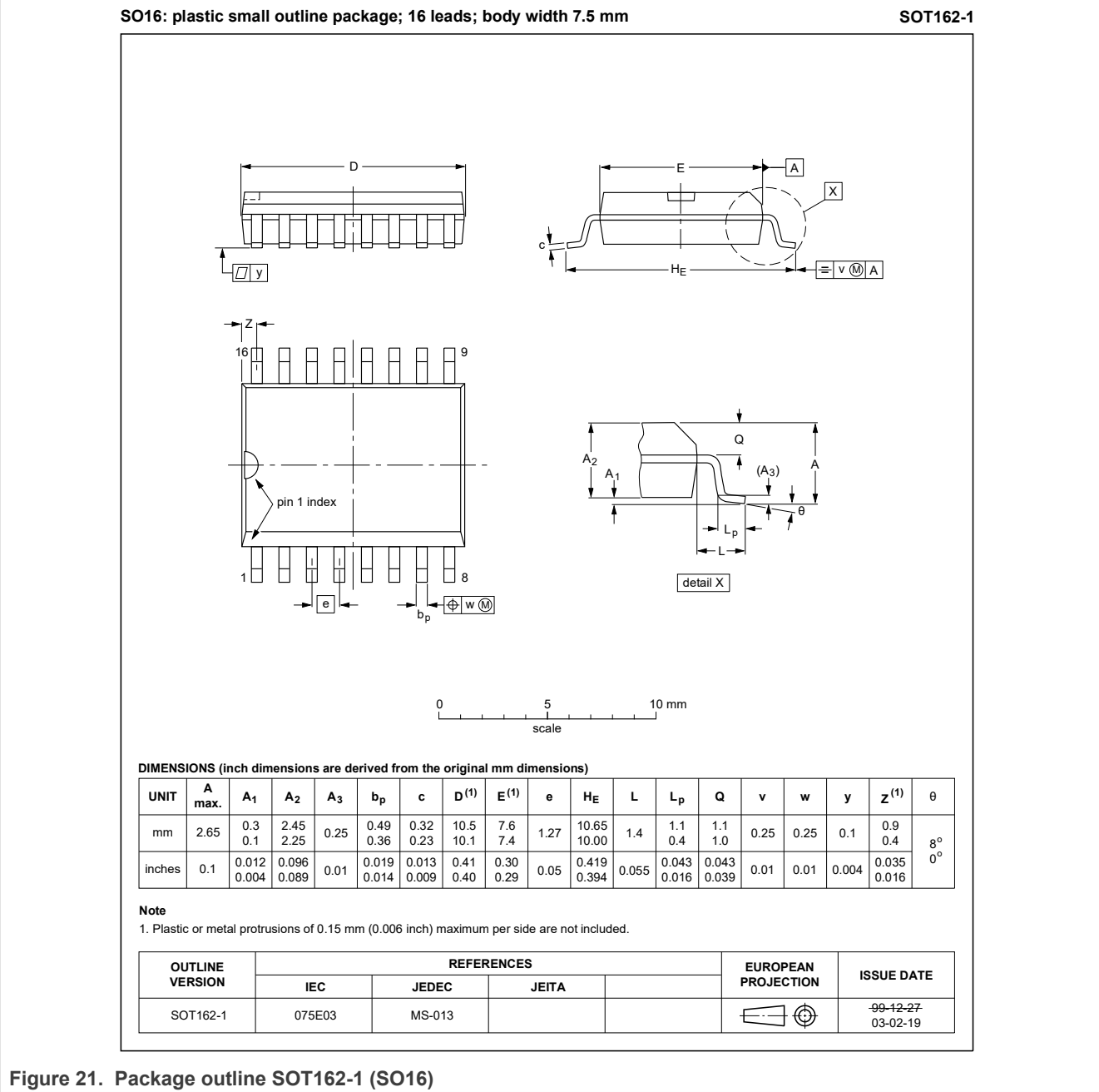


Table 13. Test data

Test	Load		Switch
	R_L	C_L	
$t_{V(Q)}$	500 Ω	50 pF	$2 \times V_{DD}$

12 Package outline

This section shows the package outline diagrams for various packages associated with PCA9538.



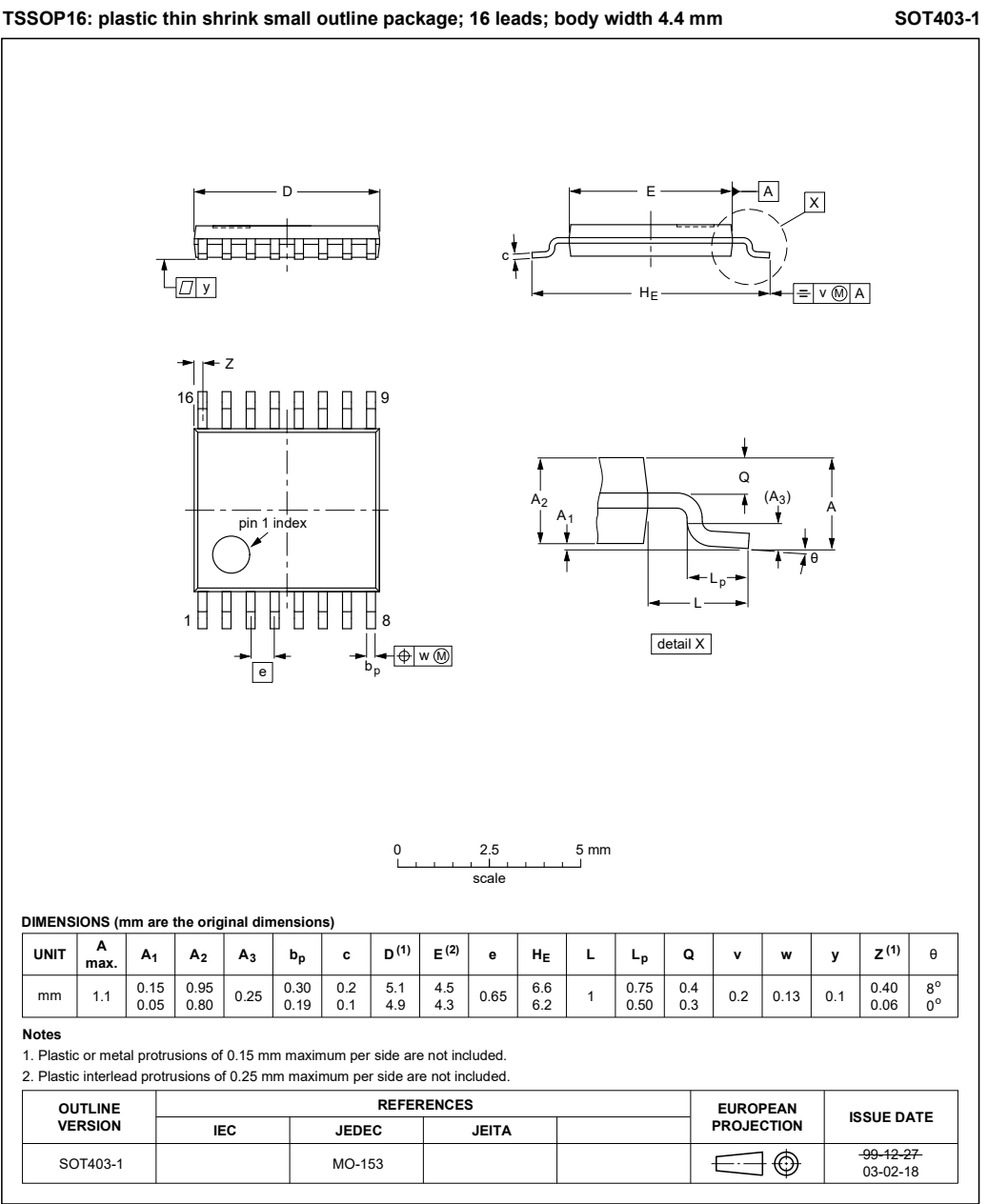


Figure 22. Package outline SOT403-1 (TSSOP16)

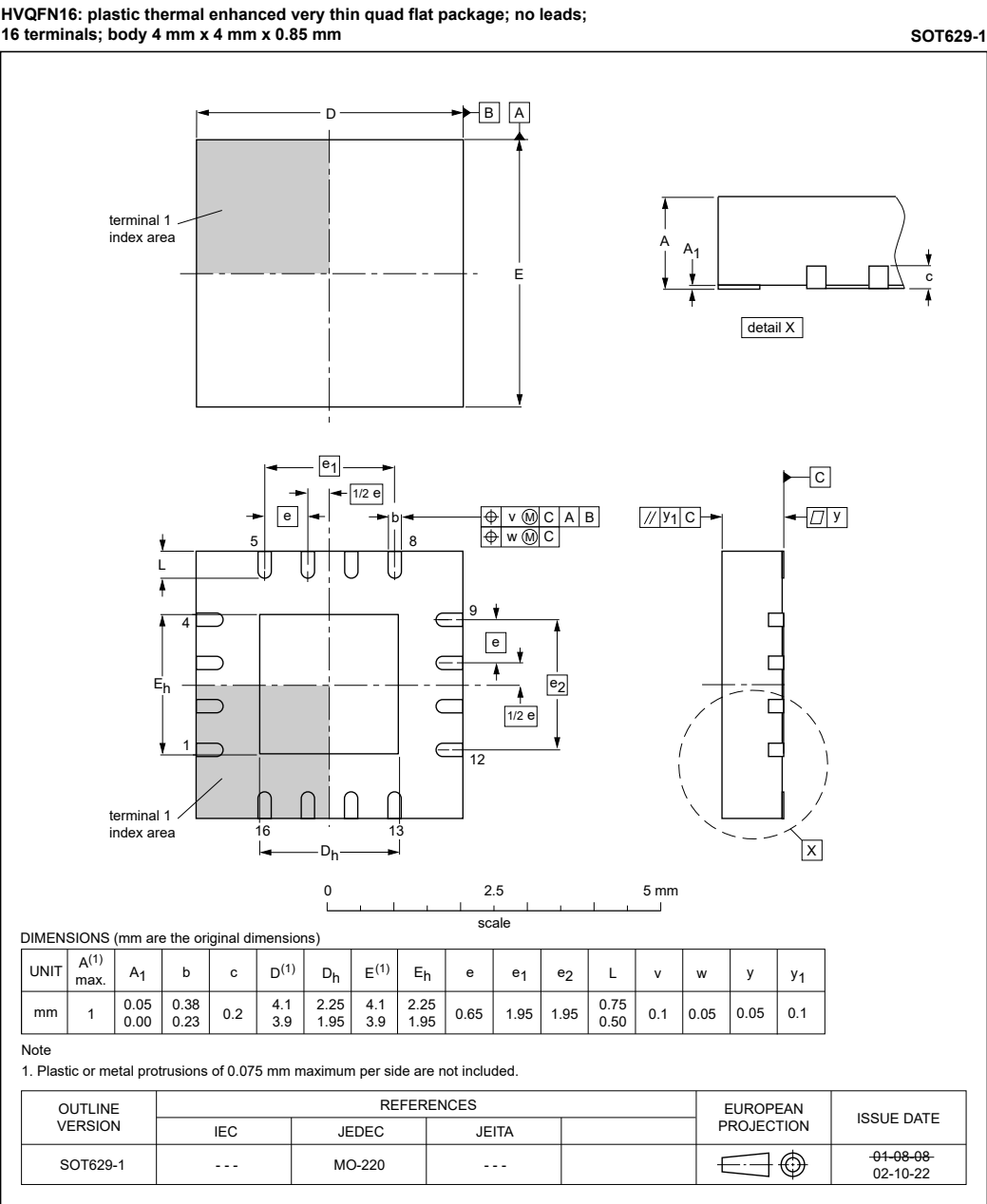


Figure 23. Package outline SOT629-1 (HVQFN16)

13 Handling information

Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

14 Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note AN10365 “*Surface mount reflow soldering description*”.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 24](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 14](#) and [Table 15](#)

Table 14. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm³)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 15. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm³)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times. Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 24](#).

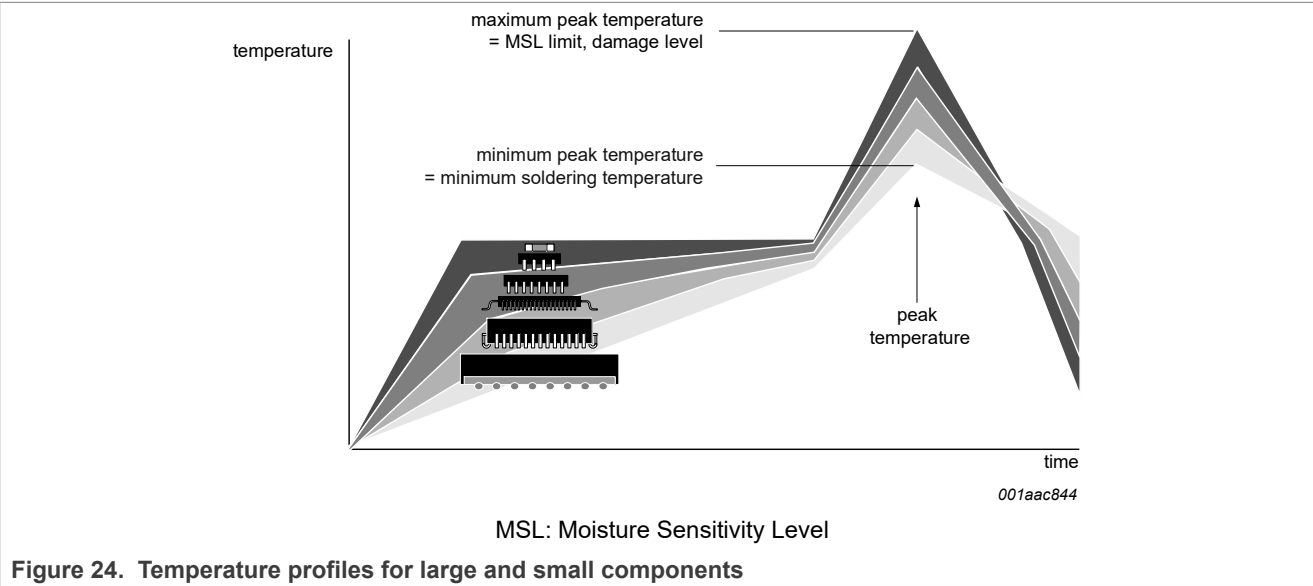


Figure 24. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

15 Soldering: PCB footprints

This section shows the PCB footprints for various packages associated with PCA9538.

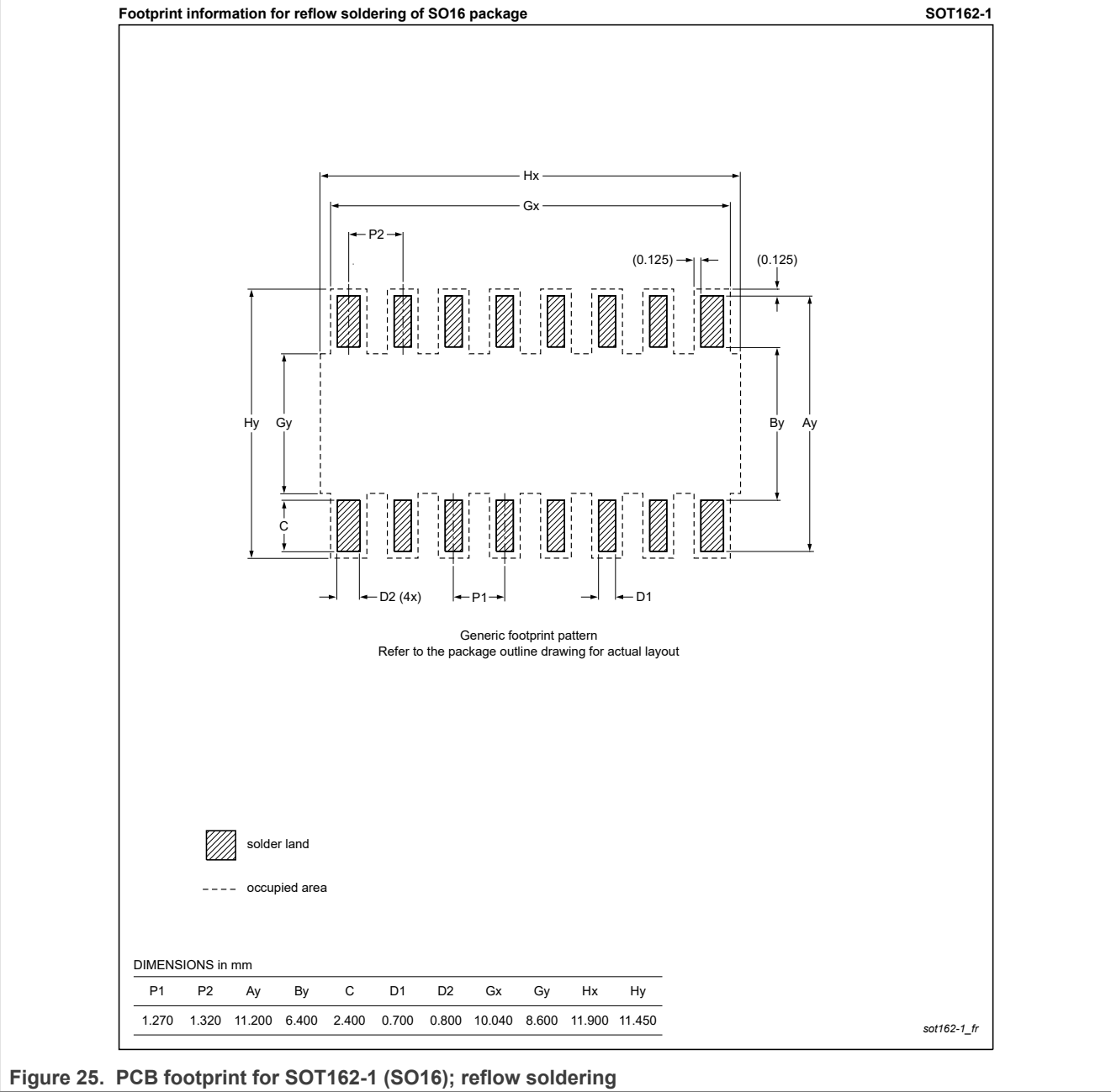


Figure 25. PCB footprint for SOT162-1 (SO16); reflow soldering

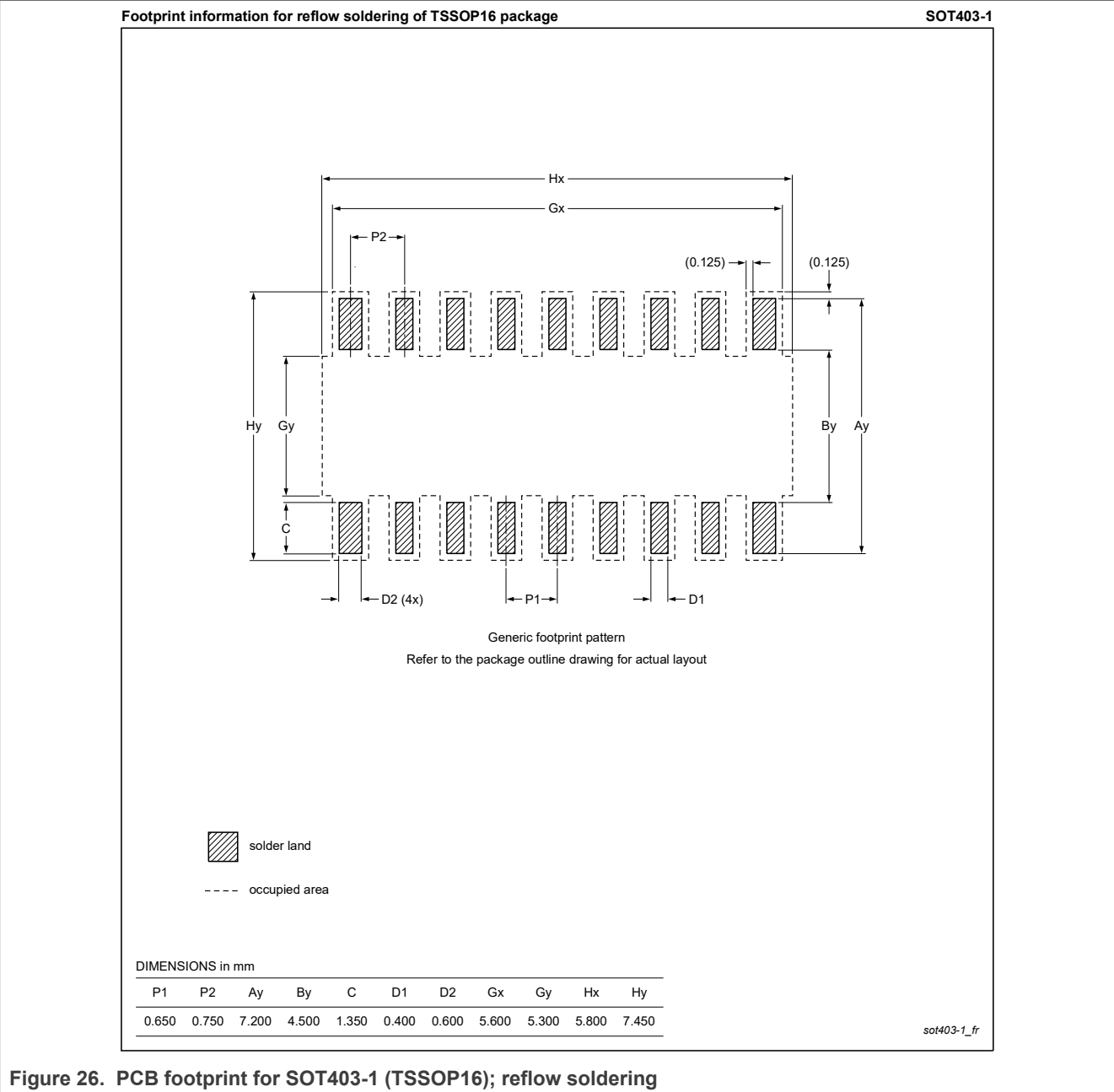


Figure 26. PCB footprint for SOT403-1 (TSSOP16); reflow soldering

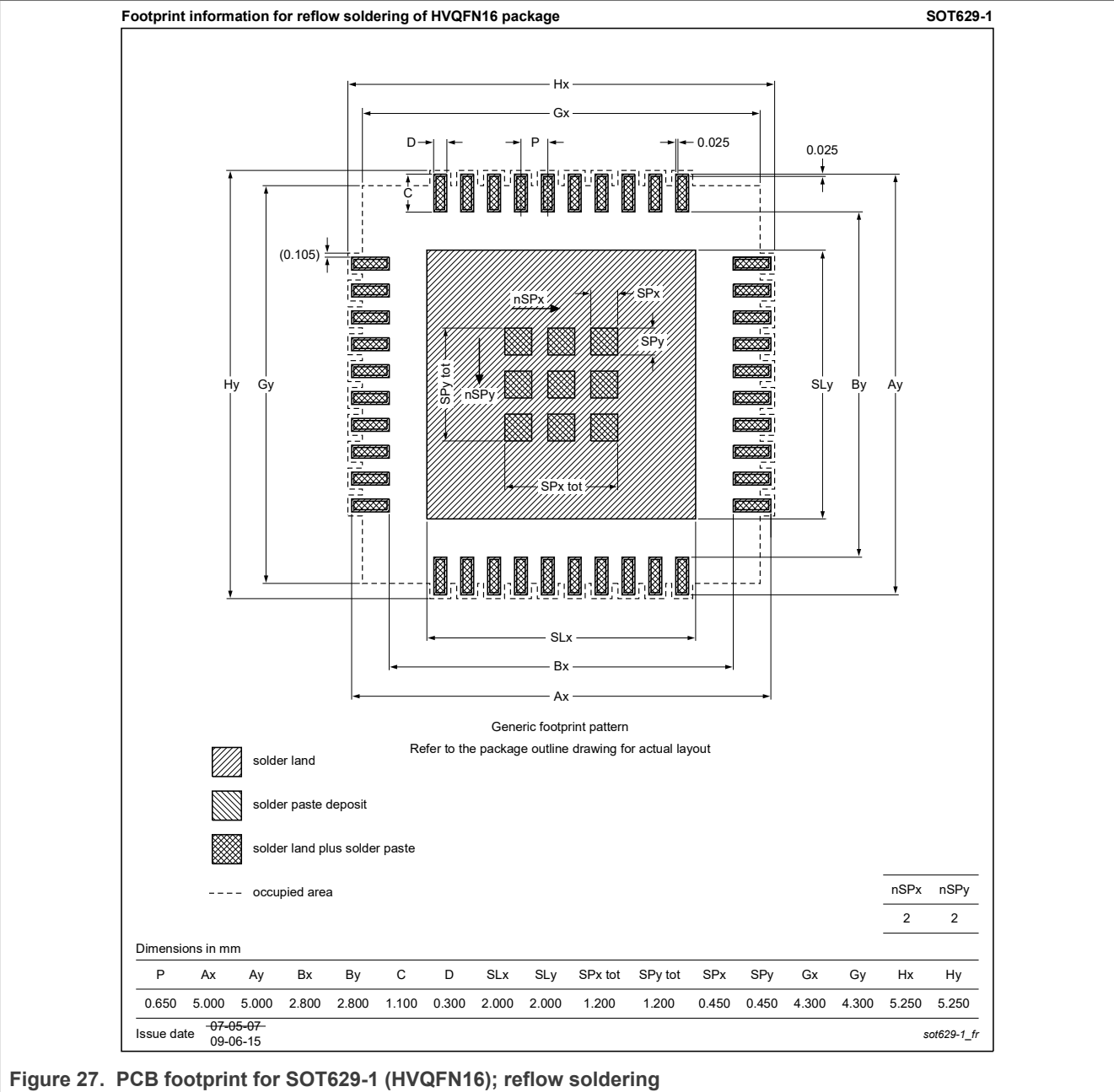


Figure 27. PCB footprint for SOT629-1 (HVQFN16); reflow soldering

16 Acronyms

Table 16 describes the acronyms used in this document.

Table 16. Acronyms

Acronym	Description
ACPI	Advanced Configuration and Power Interface
CBT	Cross-Bar Technology
CDM	Charged-Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
FET	Field-Effect Transistor
FF	Flip-Flop
GPIO	General-Purpose Input/Output
HBM	Human Body Model
I ² C-bus	Inter-Integrated Circuit bus
I/O	Input/Output
LED	Light Emitting Diode
LP	Low-Pass
POR	Power-On Reset
SMBus	System Management Bus

17 Revision history

[Table 17](#) summarizes revisions to this document.

Table 17. Revision history

Document ID	Release date	Description
PCA9538 v.8.1	21 May 2026	Updated per CIN #2026050181: - Updated Access column in Table 6 - Updated V_{IL} (max) and V_{IH} (min) values for the I/Os in Table 10 - Editorial changes
PCA9538 v.8.0	8 November 2017	Updated per CIN #2017100021: Table 10, Table 11: Corrected V_{POR} Typ and max limit
PCA9538 v.7.0	26 November 2014	Table 11: Updated I_{OL} and V_{OH}; changed operating power supply voltage range from "5.0 V ± 10 %" to "3.0 V to 5.5 V" for PCA9538PW/Q900
PCA9538 v.6.0	6 February 2013	Product data sheet
PCA9538 v.5.0	28 May 2009	Product data sheet
PCA9538 v.4.0	21 September 2006	Product data sheet
PCA9538 v.3.0 (9397 750 14176)	5 October 2004	Product data sheet
PCA9538 v.2.0 (9397 750 14049)	30 September 2004	Product data sheet
PCA9538 v.1.0 (9397 750 12881)	20 August 2004	Initial release

Legal information

Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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