



## TPS7A3501 High PSRR, Low-Noise, 1-A Power Filter

### 1 Features

- Regulates Input-to-Output Voltage:
  - User-Programmable Input-to-Output Voltage Regulation Range: 200 mV to 500 mV
- Power-Supply Rejection Ratio:
  - 42 dB at 1 MHz
  - ≥ 32 dB (360 kHz to 3.9 MHz)
- Low-Noise Output:
  - 3.8  $\mu\text{V}_{\text{RMS}}$  (10 Hz to 100 kHz)
- Output Current: Up to 1 A
- Output Voltage Range: 1.21 V to 4.5 V
- Excellent Load Transient Response
- Stable With Ceramic Capacitors as Low as 10  $\mu\text{F}$
- Current Limit and Thermal Shutdown for Fault Protection
- Available in a Low Thermal Resistance Package: 2-mm × 2-mm WSON-6
- Operating Temperature Range: –40°C to 125°C

### 2 Applications

- Post DC-DC Converter Ripple Filtering
- Base Stations and Telecom Infrastructure
- Professional Audio
- Communications
- Imaging
- Test and Measurement
- Passive Filter Replacement

### 3 Description

The TPS7A3501 is a positive voltage, low-noise (3.8- $\mu\text{V}_{\text{RMS}}$ ) power filter capable of sourcing a 1-A load suitable for quiet supply solutions. Power filters, such as the TPS7A3501, provide voltage regulation across the input and output terminals with high efficiency (low insertion loss), and power-supply rejection. The device is ideally suited as a noise filter for 3.3-V, 2.5-V, and 1.8-V supplies at up to 1 A.

The input-to-output voltage regulation is also user-programmable, from 200 mV to 500 mV, with a single external resistor. If no resistor is used, the TPS7A3501 provides 330 mV of input-to-output voltage regulation. The device is stable with 10- $\mu\text{F}$  input and output ceramic capacitors and a 10-nF noise-reduction ceramic capacitor.

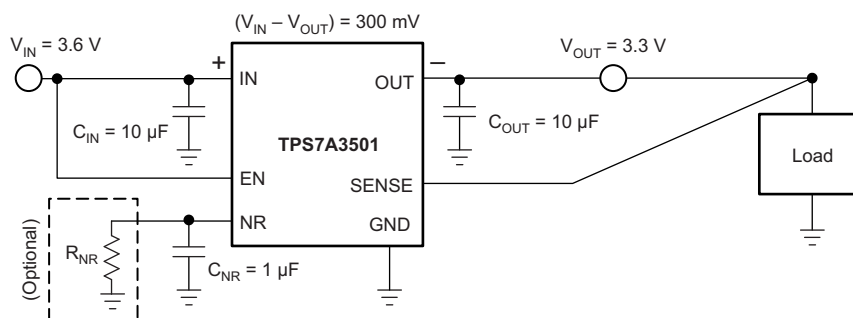
The TPS7A3501 is fully specified over a wide temperature of –40°C to 125°C. The device is offered in a low thermal resistance, 2-mm × 2-mm, WSON-6 package. Unlike passive filters, the TPS7A3501 provides thermal and current protection for itself and surrounding circuitry.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A3501	WSON (6)	2.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Typical Application Circuit



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## 4 Revision History

### Changes from Revision A (October 2013) to Revision B

Page

Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
Changed "free-air temperature" to "junction temperature" in Absolute Maximum Ratings condition statement	5
Changed Figure 14 to Figure 18: collected new data	8

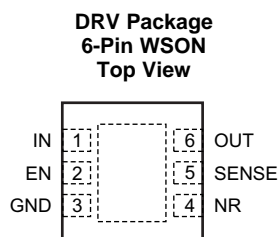
### Changes from Original (July 2013) to Revision A

Page

Changed document status to Production Data	1
Changed document title	1
Deleted second sub-bullet from first Features bullet	1
Changed sub-bullets in Power-Supply Rejection Ratio and Low-Noise Output Features bullets	1
Changed Output Current, Transient Response, Ceramic Capacitors, and Package Features bullets	1
Deleted Input Voltage Range Features bullet	1
Added Output Voltage Range Features bullet	1
Added 4th to 7th Applications bullets	1
Changed 1st and 3rd paragraphs of Description section	1
Changed voltage regulation value in second Description paragraph	1
Added changes to Typical Application Circuit	1
Changed descriptions of IN, NR, OUT, and PowerPAD pins in Pin Functions table	4
Added PowerPAD row to Pin Functions table	4
Changed associated pins of Voltage parameter in Absolute Maximum Ratings table	5
Changed T <sub>J</sub> Temperature range parameter minimum specification in Absolute Maximum Ratings table	5
Changed conditions of Electrical Characteristics table	6
Changed V <sub>IN</sub> and V <sub>OUT</sub> parameter maximum specifications in Electrical Characteristics table	6
Added V <sub>UVLO(in)</sub> parameter to Electrical Characteristics table	6
Changed V <sub>IN</sub> – V <sub>OUT</sub> voltage range, V <sub>n</sub> , and T <sub>sd</sub> parameters in Electrical Characteristics table	6

• Changed $I_{CL}$ and $I_{EN}$ parameter specifications in <i>Electrical Characteristics</i> table .....	6
• Changed $I_{GND}$ parameter typical specification in <i>Electrical Characteristics</i> table .....	6
• Changed $I_{SHDN}$ test conditions and parameter specifications in <i>Electrical Characteristics</i> table .....	6
• Changed $V_{EN(HI)}$ parameter minimum specification in <i>Electrical Characteristics</i> table .....	6
• Changed <i>Typical Characteristics</i> section .....	7
• Added <i>Functional Block Diagram</i> .....	11
• Changed <i>Application Information</i> section .....	15
• Changed <i>Board Layout Recommendations</i> section .....	19

## 5 Pin Configuration and Functions



### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	2	I	Enable pin. Driving EN high turns on the device (if driven low, EN turns off the device). EN must not be left floating and can be connected to IN if not used.
GND	3	—	Ground
IN	1	I	Input supply. A capacitor greater than or equal to 10 $\mu$ F must be tied from this pin to ground to assure stability. This configuration is especially important when long input traces or high source impedances are encountered. TI recommends using X5R- or X7R-type dielectrics to minimize the temperature variations inherent to capacitors.
NR	4	O	Noise-reduction pin. When a capacitor is connected from this pin to GND, RMS noise can be reduced to very low levels. A capacitor greater than or equal to 10 nF must be tied from this pin to ground to assure stability. TI recommends connecting a 1- $\mu$ F capacitor from NR to GND (as close to the device as possible) to maximize AC performance and minimize noise. TI recommends using X5R- or X7R-type dielectrics to minimize the temperature variations inherent to capacitors. In addition, when a resistor is connected from this pin to GND or IN, the device input-to-output voltage can be programmed; see <a href="#">Feature Description</a> for details.
OUT	6	O	Regulator output. A capacitor greater than or equal to 10 $\mu$ F must be tied from this pin to ground to assure stability. TI recommends using a X5R- or X7R-type dielectrics to minimize the temperature variations inherent to capacitors.
PowerPAD™	—	—	Connect the PowerPAD to the ground plane for improved thermal performance.
SENSE	5	I	Control-loop error amplifier input. This pin must be connected to OUT. TI recommends connecting SENSE at the point of load to maximize accuracy.

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted).<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage	IN, NR, EN	−0.3	7	V
	OUT, SENSE	−0.3	$V_{IN} + 0.3^{(2)}$	
Current	OUT	Internally limited		
Temperature	Operating junction, $T_J$	−40	125	°C
	Storage, $T_{stg}$	−55	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum rating is  $V_{IN} + 0.3$  V or + 7 V, whichever is smaller.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±250	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
$V_{IN}$	Input voltage	1.71		5	V
$I_{OUT}$	Output current	0		1	A
$T_J$	Operating junction temperature	−40		125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DRV (WSN)	UNIT
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	86.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	36.4	
$\Psi_{JT}$	Junction-to-top characterization parameter	1.8	
$\Psi_{JB}$	Junction-to-board characterization parameter	36.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	7.3	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

At  $T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ ,  $V_{IN} = 3.6\text{ V}$ ,  $R_{NR} = \infty$  (not connected),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ , and  $C_{IN} = C_{OUT} = 10\text{ }\mu\text{F}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input voltage range	1.71		5	V
$V_{UVLO(in)}$	Input supply UVLO	$V_{IN}$ increasing		1.7	V
	$V_{IN}$ hysteresis		200		mV
$V_{OUT}$	Output voltage range	1.21		4.5	V
$V_{IN} - V_{OUT}$ voltage range		200		500	mV
	$V_{OUT(nom)} = V_{IN} - 330\text{ mV}$ , $I_{OUT} \leq 1\text{ A}$ , $1.71\text{ V} \leq V_{IN} \leq 4.83\text{ V}$	297	330	363	mV
	$R_{NR\_INTERNAL}^{(1)}$	110	170	210	k $\Omega$
	$I_{NR\_INTERNAL}^{(2)}$	1.4	1.8	2.4	$\mu\text{A}$
$\Delta V_{OUT(\Delta I_{OUT})}$	Load regulation	$10\text{ mA} \leq I_{OUT} \leq 1\text{ A}$	10		$\mu\text{V/mA}$
$I_{CL}$	Output current limit	$V_{OUT} = 0.85 \times V_{OUT(nom)}$	1.1		A
$I_{GND}$	GND pin current		2.25	5	mA
$I_{EN}$	EN pin input current	$V_{EN} = V_{IN}$	1	50	nA
$I_{SHUTDOWN}$	Shutdown current ( $I_{GND}$ )	$V_{EN} \leq 0.3\text{ V}$	0.01	3	$\mu\text{A}$
PSRR	Power-supply rejection ratio	$f = 10\text{ kHz}$ , $C_{NR} = 1\text{ }\mu\text{F}$ , $I_{OUT} = 0.5\text{ A}$	55		dB
		$f = 100\text{ kHz}$ , $C_{NR} = 1\text{ }\mu\text{F}$ , $I_{OUT} = 0.5\text{ A}$	40		
		$f = 1\text{ MHz}$ , $C_{NR} = 1\text{ }\mu\text{F}$ , $I_{OUT} = 0.5\text{ A}$	42		
$V_n$	Output noise voltage	$BW = 10\text{ Hz to }100\text{ kHz}$ , $C_{NR} = 1\text{ }\mu\text{F}$ , $I_{OUT} = 1\text{ A}$	3.8		$\mu\text{V}_{RMS}$
		$BW = 100\text{ Hz to }100\text{ kHz}$ , $C_{NR} = 1\text{ }\mu\text{F}$ , $I_{OUT} = 1\text{ A}$	3.62		
		$BW = 10\text{ Hz to }1\text{ MHz}$ , $C_{NR} = 1\text{ }\mu\text{F}$ , $I_{OUT} = 1\text{ A}$	12.1		
$V_{EN(LO)}$	EN pin input low (disable)			0.4	V
$V_{EN(HI)}$	EN pin input high (enable)		1.1		V
$T_{sd}$	Thermal shutdown junction temperature	Shutdown, temperature increasing	165		$^{\circ}\text{C}$
		Shutdown, temperature hysteresis	20		

(1)  $R_{NR\_INTERNAL}$  refers to the internal resistor used to set  $(V_{IN} - V_{OUT})$  for the device when no external  $R_{NR}$  is used. See [Adjustable Voltage Drop](#) and [Typical Application Circuit](#) for details.

(2)  $I_{NR\_INTERNAL}$  refers to the internal current source used to set  $(V_{IN} - V_{OUT})$  for the device when no external  $R_{NR}$  is used. See [Adjustable Voltage Drop](#) and [Typical Application Circuit](#) for details.

## 6.6 Typical Characteristics

At  $V_{IN} = 3.6\text{ V}$ ,  $R_{NR} = \infty$  (not connected),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ , and  $C_{NR} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.

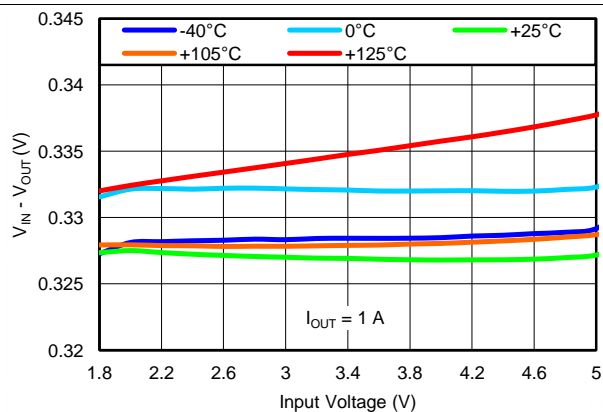


Figure 1. Line Regulation

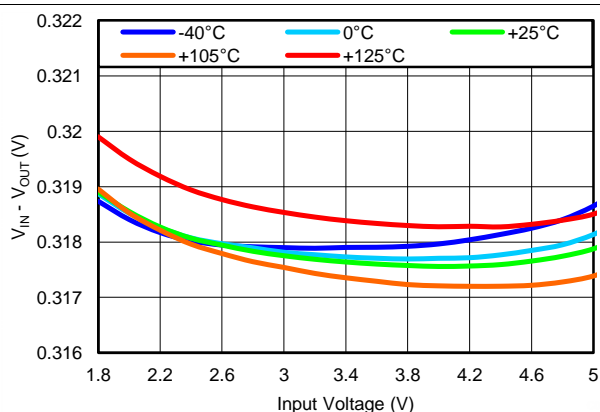


Figure 2. Line Regulation

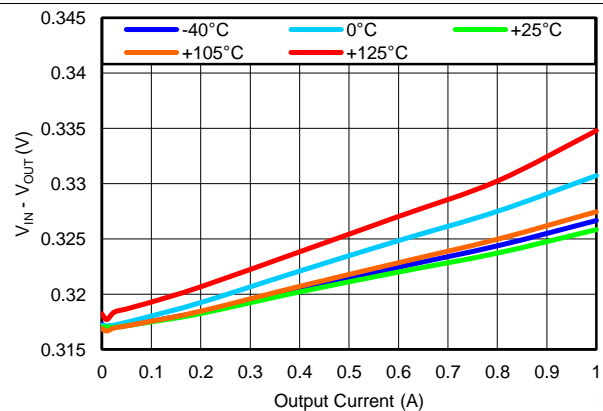


Figure 3. Load Regulation

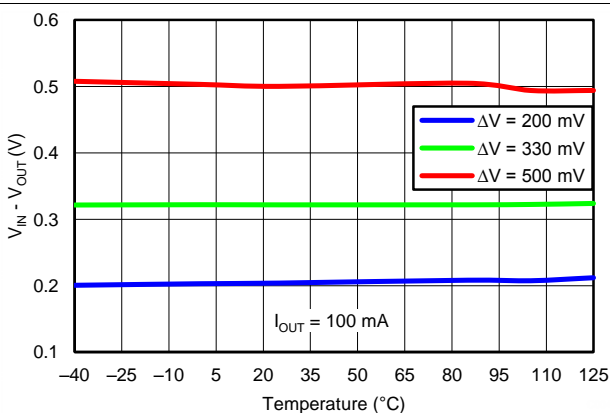


Figure 4.  $V_{\Delta}$  vs Temperature

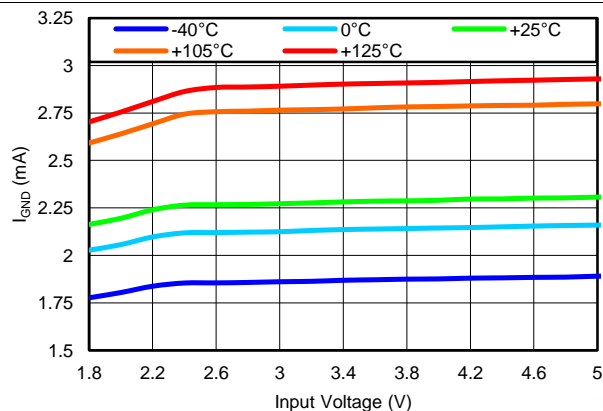


Figure 5. Ground Current vs Input Voltage

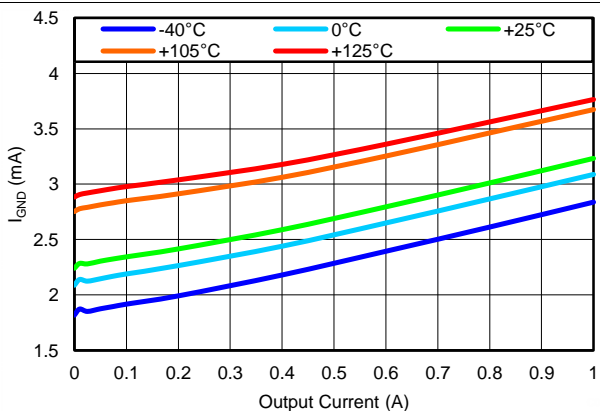
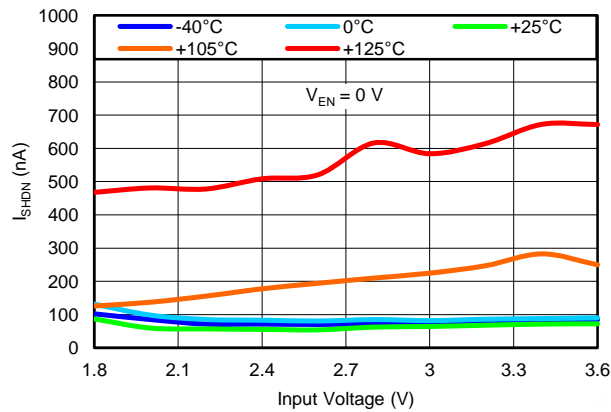


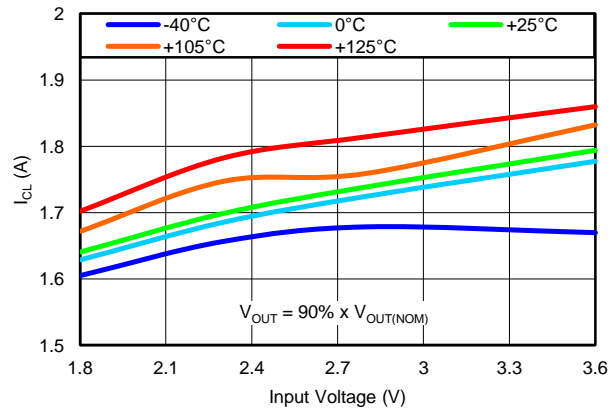
Figure 6. Ground Current vs Output Current

## Typical Characteristics (continued)

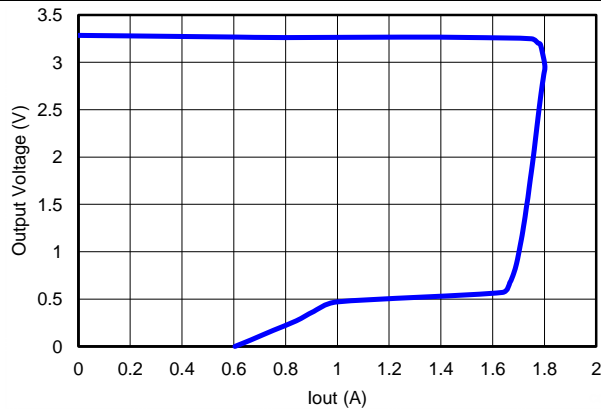
At  $V_{IN} = 3.6\text{ V}$ ,  $R_{NR} = \infty$  (not connected),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ , and  $C_{NR} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.



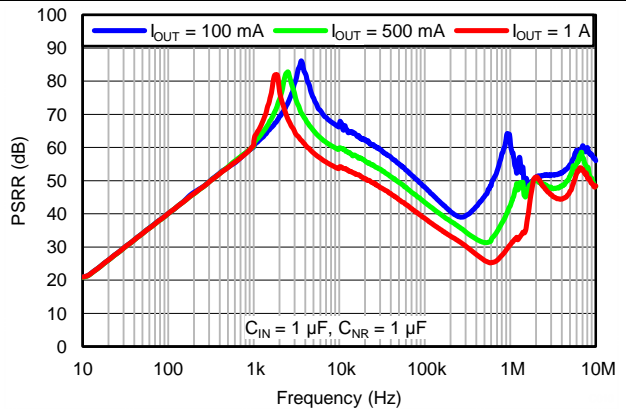
**Figure 7. Shutdown Current vs Input Voltage**



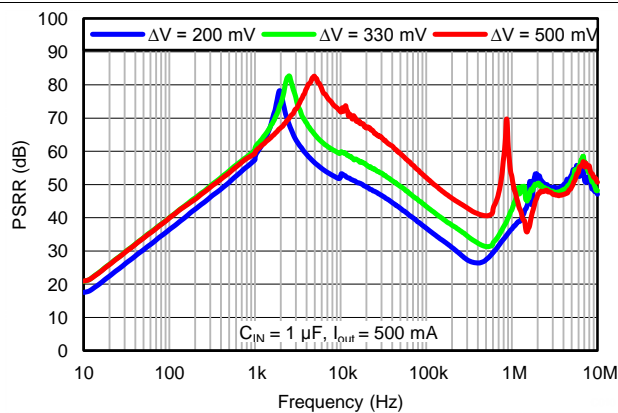
**Figure 8. Current Limit vs Input Voltage**



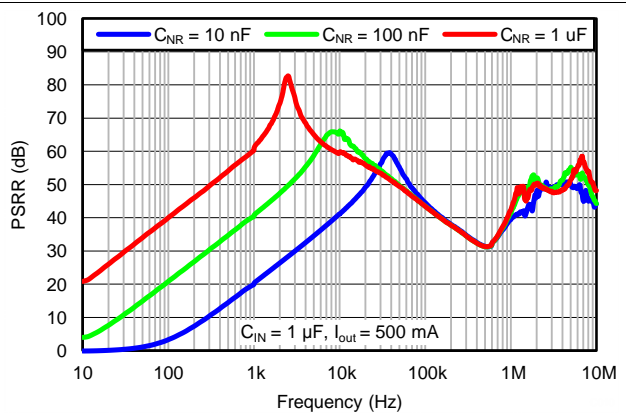
**Figure 9. Foldback Current Limit**



**Figure 10. Power-Supply Rejection Ratio vs Frequency**



**Figure 11. Power-Supply Rejection Ratio vs Frequency**

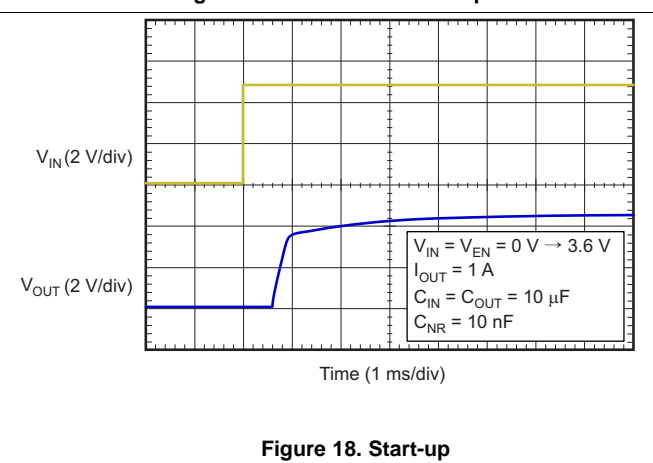
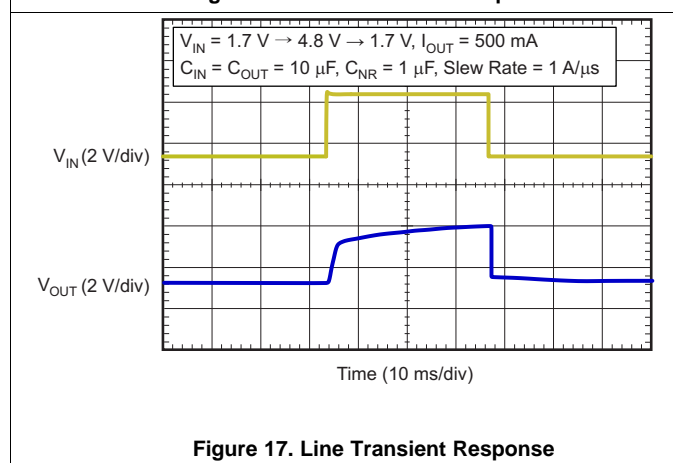
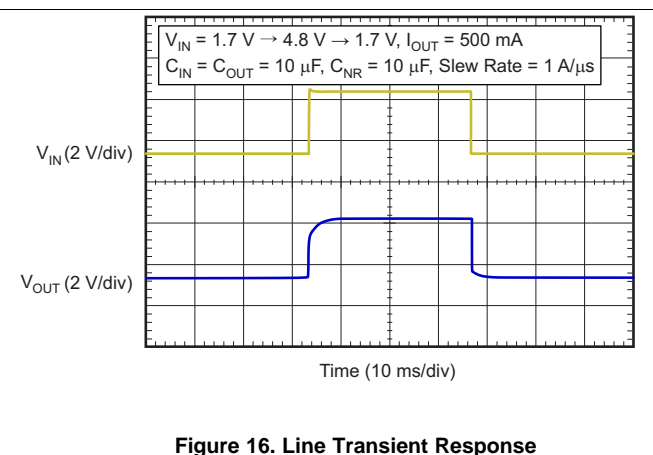
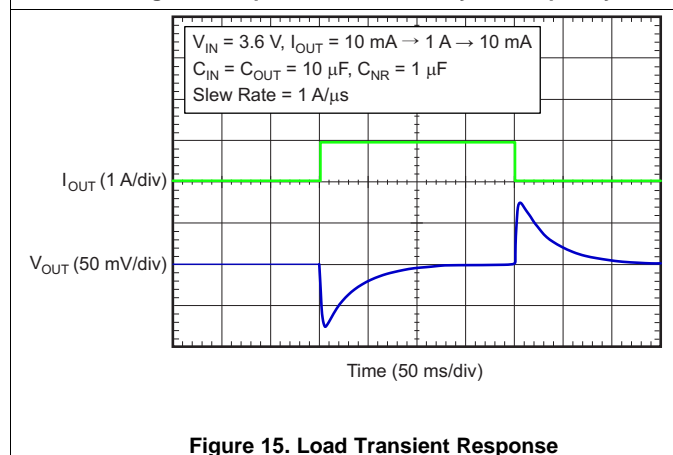
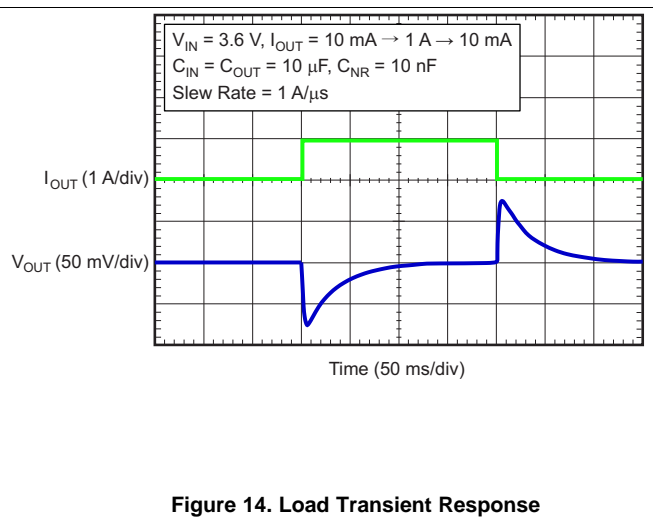
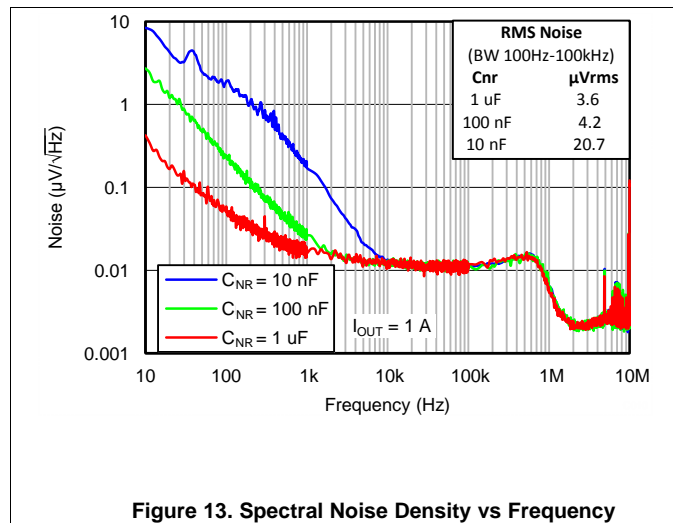


**Figure 12. Power-Supply Rejection Ratio vs Frequency**



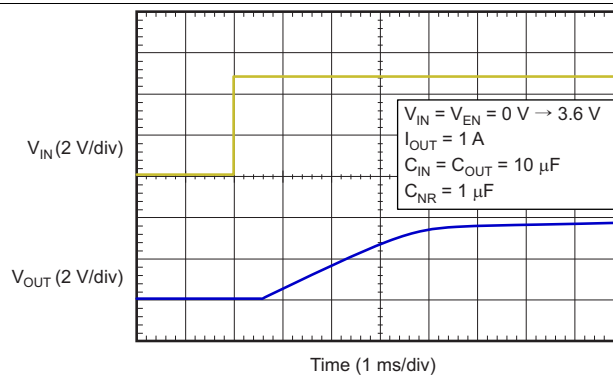
## Typical Characteristics (continued)

At  $V_{IN} = 3.6\text{ V}$ ,  $R_{NR} = \infty$  (not connected),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ , and  $C_{NR} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.



## Typical Characteristics (continued)

At  $V_{IN} = 3.6\text{ V}$ ,  $R_{NR} = \infty$  (not connected),  $I_{OUT} = 10\text{ mA}$ ,  $V_{EN} = V_{IN}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$ ,  $C_{IN} = 10\text{ }\mu\text{F}$ , and  $C_{NR} = 0.1\text{ }\mu\text{F}$ , unless otherwise noted.



**Figure 19. Start-up**

## 7 Detailed Description

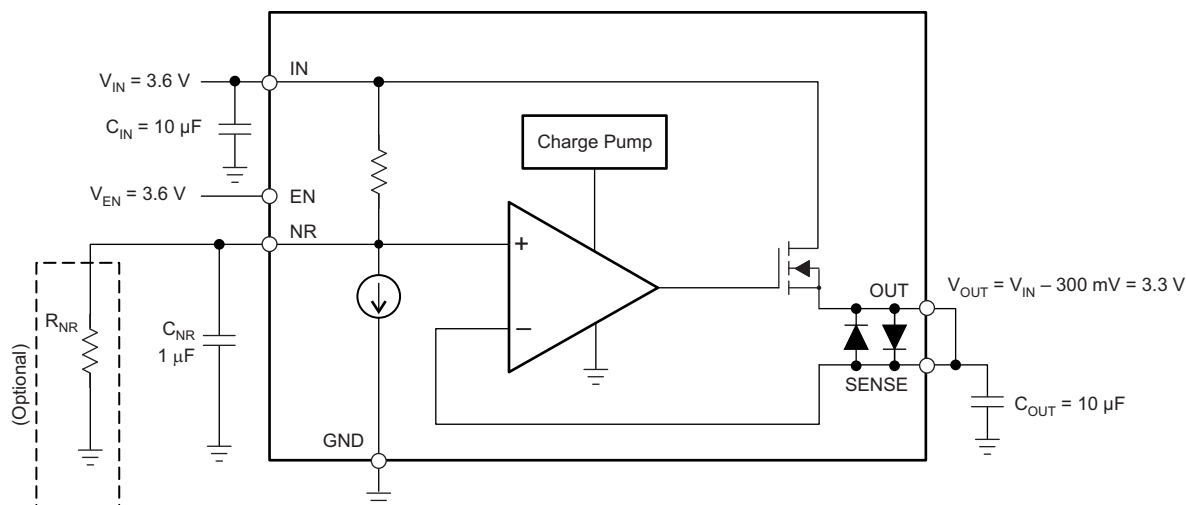
### 7.1 Overview

The TPS7A3501 is a positive-voltage, low-noise ( $3.8\text{-}\mu\text{V}_{\text{RMS}}$ ) power filter capable of sourcing a 1-A load. Power filters such as the TPS7A3501 provide voltage regulation across the input and output terminals with high accuracy and power-supply rejection ratio. The device is ideally suited as a noise filter for 4.5-V, 3.3-V, and 1.8-V supplies up to 1-A loads.

The input-to-output voltage drop is also user-programmable, from 200 mV up to 500 mV, with an external resistor. If no resistor is used, the TPS7A3501 provides 330 mV of input-to-output voltage regulation.

The TPS7A3501 is stable with 10- $\mu\text{F}$  ceramic input and output capacitors and a 10-nF ceramic noise-reduction capacitor. The device is fully specified over a wide temperature range of  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and is offered in a low thermal resistance, 2-mm  $\times$  2-mm, 6-pin WSON package.

### 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Power Filter Operation

A power filter is very similar to a low-dropout (LDO) regulator, except that instead of regulating output voltage relative to ground, the power filter regulates output voltage relative to  $V_{IN}$ . In other words, a power filter maintains a fixed  $\Delta V$  from input to output. The device is optimized for high PSRR with a low  $V_{IN}$ -to- $V_{OUT}$  delta, leading to a lower power dissipation than standard LDOs. Unlike a standard LDO, the bandgap and noise associated with the device are never gained up, resulting in low output noise regardless of  $V_{OUT}$ . The external noise capacitor on the power filter lets the user set the frequency at which the power filter starts to reject noise from the input. [Table 1](#) summarizes the differences between a power filter and a high-performance LDO.

**Table 1. Power Filter vs LDO Characteristics**

PARAMETER	POWER FILTER	LDO
Voltage regulation	Regulates input-to-output delta. Voltage delta can be set from 0.2 V to 0.5 V. Relies on the upstream power rail to set the output voltage.	Regulates the output voltage referenced to ground. Outputs any output voltage within the output voltage range (limited by power dissipation).
PSRR	High PSRR at typical switching frequencies of DC-DC converters with lower power dissipation. Lower PSRR at low frequencies.	High PSRR over broad bandwidth. Effective rejection of low-frequency noise and switching noise from DC-DC.
Noise	Lower noise, 3.8 $\mu V$ . Noise is not gained up when $V_{OUT}$ increases.	Low noise (typically in the range of 5 $\mu V_{RMS}$ to 20 $\mu V_{RMS}$ ). Noise is gained up when $V_{OUT}$ increases.
Power dissipation	High PSRR can be achieved with only 330 mV from $V_{IN}$ to $V_{OUT}$ .	Typically requires 750 mV to 1 V of $V_{IN}$ -to- $V_{OUT}$ delta to achieve high PSRR.

### 7.3.2 Minimum Load

The device is stable without an output load.

### 7.3.3 Shutdown

The enable pin (EN) is active high and compatible with standard and low-voltage TTL-CMOS levels. The enable pin voltage level is independent of input voltage and can be biased to a higher value than  $V_{IN}$  as long as EN is within the maximum specification. When shutdown capability is not required, EN can be connected to IN.

### 7.3.4 Internal Current Limit

The device has an internal foldback current limit that helps protect the power filter during fault conditions. The current supplied by the device is gradually reduced when the output voltage decreases. When the output is shorted to GND, the LDO supplies a typical current of 550 mA. When in current limit, the output voltage is not regulated and  $V_{OUT} = I_{OUT} \times R_{LOAD}$ . For reliable operation, do not operate the device in current limit for extended periods of time.

Because of the nature of the foldback current limit circuitry, if OUT is forced below 0 V before EN goes high, the device may not start up. To ensure proper start-up in applications that have both a positive and negative voltage rail, extra care must be taken to ensure that OUT is greater than or equal to 0 V. There are several ways to help ensure proper start-up for dual-rail applications:

- Enable the device before the negative rail and disable the device after the negative rail.
- Delaying the EN voltage with respect to IN voltage allows the internal pulldown resistor to discharge any residual voltage at OUT.
- If a faster discharge rate is required, or if EN is tied directly to IN, an external resistor from OUT to GND can be used.

### 7.3.5 Reverse Current

The TPS7A3501 has a built-in body diode that conducts current when the voltage at OUT exceeds the voltage at IN. This current is not internally limited, so if reverse voltage conditions are anticipated, external limiting is required.

If there are potential situations where reverse current is expected, place a diode from OUT to IN, as shown in [Figure 20](#).

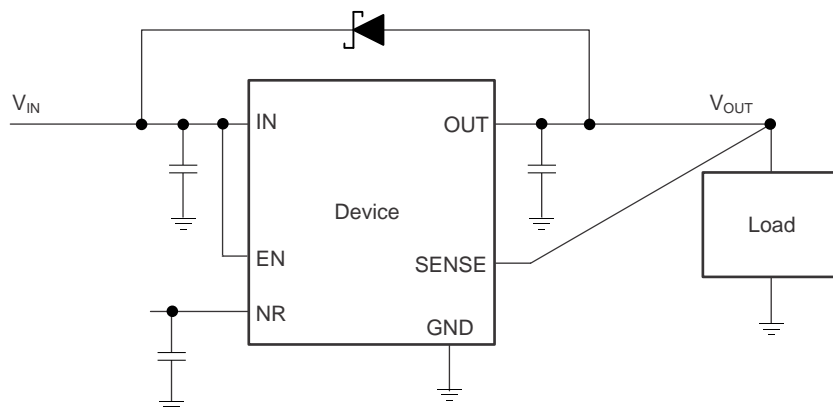


Figure 20. Reverse Current Protection Schematic

### 7.3.6 Undervoltage Lockout (UVLO)

The device uses an undervoltage lockout circuit to keep the output shut off until the internal circuitry is operating properly, ensuring a well-controlled start-up.

### 7.3.7 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits device power dissipation, thus protecting the device from damage resulting from overheating.

Any activation of the thermal protection circuit indicates excessive power dissipation or inadequate thermal dissipation on the PCB. For reliable operation, limit junction temperature to 125°C (maximum). To estimate the margin of safety in a complete design, increase the ambient temperature until the thermal protection is triggered using worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the application. This configuration produces a worst-case junction temperature of 125°C at the highest-expected ambient temperature and worst-case load.

The device internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heat-sinking or thermal dissipation on the PCB. Continuously running the device into thermal shutdown degrades device reliability.

## 7.4 Device Functional Modes

Table 2 provides a quick comparison between the normal, dropout, and disabled modes of operation.

Table 2. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V <sub>IN</sub>	EN	I <sub>OUT</sub>	T <sub>J</sub>
Normal	1.71 ≤ V <sub>IN</sub> ≤ 5	V <sub>EN</sub> > V <sub>EN(HI)</sub>	I <sub>OUT</sub> < I <sub>CL</sub>	T <sub>J</sub> < T <sub>sd</sub>
Disabled	—	V <sub>EN</sub> < V <sub>EN(LO)</sub>	—	T <sub>J</sub> > T <sub>sd</sub>

### 7.4.1 Normal Operation

The device functions as a fixed voltage drop filter under the following conditions:

- The input voltage is within the specified operating range of 1.71 V to 5 V.
- The enable voltage has previously exceeded the enable rising threshold voltage and not yet decreased below the enable falling threshold.
- The output current is less than the current limit (I<sub>OUT</sub> < I<sub>CL</sub>).
- The device junction temperature is less than the thermal shutdown temperature (T<sub>J</sub> < T<sub>sd</sub>).

#### 7.4.2 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature ( $T_J > T_{sd}$ ).

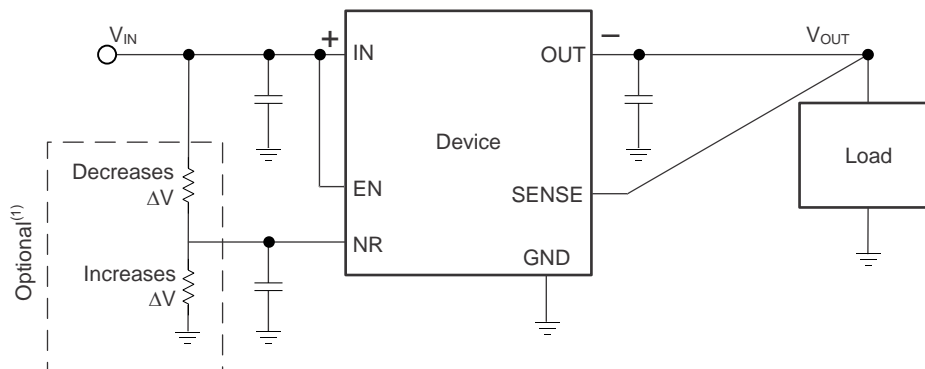
## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The TPS7A3501 is well-suited for use as a filter for switching power supplies. The high PSRR of the device significantly reduces the ripple caused by the switching frequency as well as the subsequent harmonic frequencies. [Figure 21](#) shows the basic circuit connections for the TPS7A3501. The IN pin should be connected to a well-regulated power source, typically a switching power supply.

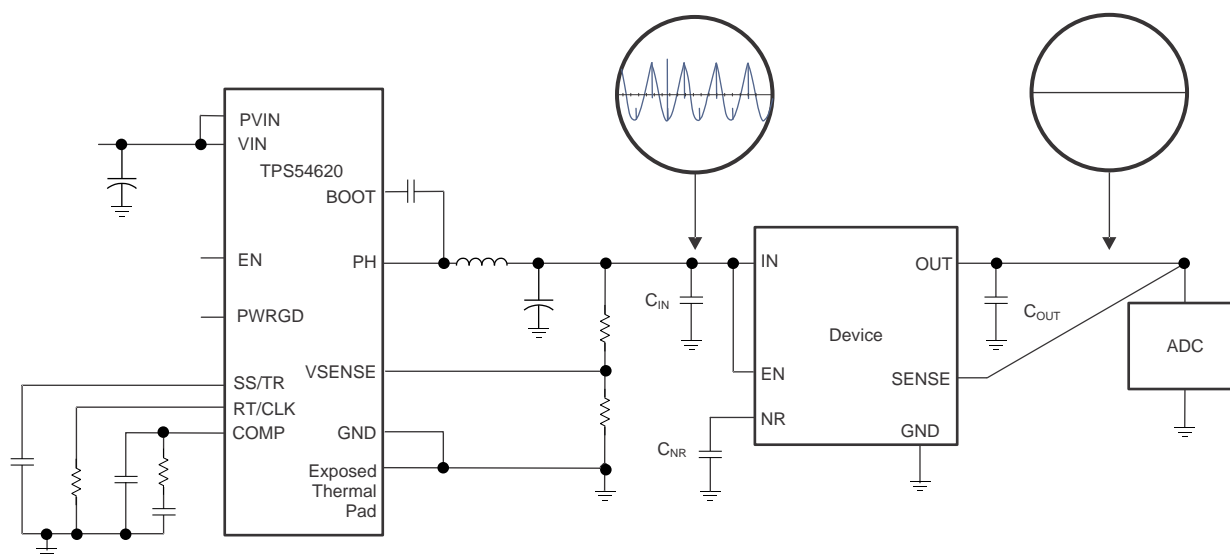


(1) Refer to [Table 4](#).

**Figure 21. Basic Circuit Connections**

### 8.2 Typical Application

[Figure 22](#) shows a schematic for filtering the output of a switching regulator using the TPS7A3501 to power an analog-to-digital converter (ADC).



**Figure 22. Typical Application Schematic**

## Typical Application (continued)

### 8.2.1 Design Requirements

Table 3 shows the design requirements.

**Table 3. Design Requirements**

PARAMETER	DESIGN REQUIREMENT
Input voltage	3.63 V
Output voltage	3.3 V
100-Hz to 100-kHz RMS noise	< 4 $\mu\text{V}_{\text{RMS}}$
Maximum output current	700 mA

### 8.2.2 Detailed Design Procedure

Select the input and output capacitors to be at least 10  $\mu\text{F}$  for stability. Select a value for  $R_{\text{NR}}$  to give the desired voltage drop. For this example of a 330-mV voltage drop, no external resistor on the NR pin is required. Pick a value for  $C_{\text{NR}}$  greater than 10 nF, but large enough to provide the required noise performance. Refer to Table 5 for guidelines on selecting  $C_{\text{NR}}$  for a desired RMS noise target. For this example, to achieve an RMS noise (100 Hz to 100 kHz) less than 4  $\mu\text{V}_{\text{RMS}}$ , the noise reduction capacitor must be at least 1  $\mu\text{F}$ .

#### 8.2.2.1 Adjustable Voltage Drop

In the TPS7A3501, the nominal voltage drop ( $\Delta\text{V}$ ) from IN to OUT is 330 mV.  $\Delta\text{V}$  can be adjusted from this nominal setting with an external resistor. By connecting a resistor from the NR pin to IN,  $\Delta\text{V}$  can be decreased to as low as 200 mV. By connecting a resistor from the NR pin to GND,  $\Delta\text{V}$  can be increased to as high as 500 mV. The ability to change  $\Delta\text{V}$  allows for the creation of standard voltage rails from higher voltage rails (for example, 2.5 V from 3 V, 1.5 V from 1.8 V, and so forth).

By connecting a resistor from the NR pin to IN,  $\Delta\text{V}$  can be decreased to as low as 200 mV. Use Equation 1 to determine the size of the resistor required to set  $\Delta\text{V}$ .

$$R = \Delta\text{V} / (0.33 - \Delta\text{V}) \times 150,000 \, \Omega \quad (1)$$

By connecting a resistor from the NR pin to GND,  $\Delta\text{V}$  can be increased to as high as 500 mV. Use Equation 2 to determine the size of the resistor required to set  $\Delta\text{V}$ .

$$R = V_{\text{OUT}} / (\Delta\text{V} - 0.33) \times 150,000 \, \Omega \quad (2)$$

Table 4 lists the standard external resistor values required for different input-to-output voltage drops.

**Table 4. Common Input-to-Output Voltage Drops**

$\Delta\text{V}$ (mV)	$V_{\text{OUT}}$	R TO $V_{\text{IN}}$	R TO GND
200	Any	240 k $\Omega$	Do not install
330	Any	Do not install	Do not install
400	3.3 V	Do not install	6.8 M $\Omega$
	2.5 V	Do not install	5.1 M $\Omega$
	1.8 V	Do not install	3.9 M $\Omega$
500	3.3 V	Do not install	3 M $\Omega$
	2.5 V	Do not install	2.2 M $\Omega$
	1.8 V	Do not install	1.6 M $\Omega$

#### 8.2.2.2 Input and Output Capacitor Requirements

Ceramic 10- $\mu\text{F}$  or larger input and output capacitors are required to assure proper device operation. This capacitor counteracts reactive source impedances, improving supply transient response and decreasing input ripple. Higher-value capacitors may be used if large, fast slew rate load transients are anticipated, or if the device is located several inches away from the power source. To assure correct device operation, there should be no more than 100  $\mu\text{F}$  of capacitance on the output of the device, including capacitance from downstream bypass capacitors.



TI recommends X5R- and X7R-type ceramic capacitors because these types of capacitors have minimal variation in value and equivalent series resistance (ESR) overtemperature. Other types of capacitors, such as electrolytic or tantalum, can make the device unstable.

### 8.2.2.3 Output Noise

A 10-nF, or higher, noise-reduction capacitor is required to assure stability. Using a 1-μF ceramic capacitor minimizes output noise (see [Figure 13](#)). To assure correct device operation, a maximum capacitor of 2.2 μF can be connected to NR.

### 8.2.2.4 Power-Supply Rejection Ratio (PSRR)

Unlike standard LDOs, the TPS7A3501 PSRR is significantly affected by the noise-reduction capacitor. The larger the noise-reduction capacitor, the higher the PSRR is for frequencies below 10 kHz. Using a 1-μF ceramic capacitor maximizes PSRR.

One of the most compelling features of the TPS7A3501 is its high PSRR capabilities. The rejection ratio for this device is lower than standard LDOs at frequencies below 1 kHz but becomes higher at higher frequencies. For better low-frequency PSRR performance, a larger noise-reduction capacitor can be used. TI recommends connecting a 1-μF ceramic capacitor to NR to maximize PSRR (see [Figure 12](#)). A higher input-to-output voltage difference also increases the device rejection ratio. Although the device maximizes rejection ratio at 500 mV, high rejection ratio can still be achieved with as little as a 330-mV input-to-output voltage differential, unlike most standard LDOs.

### 8.2.2.5 Start-up

Because adding a noise-reduction capacitor leads to the formation of an RC filter, start-up time and the rate at which the device tracks  $V_{IN}$  are increased. Thus, consider the tradeoff between start-up time, noise, and PSRR when selecting a noise-reduction capacitor to use with the TPS7A3501. Use [Equation 3](#) to calculate the typical start-up time.

$$T_{\text{startup}} = 250,000 \times C_{NR} \text{ (s)} \quad (3)$$

[Table 5](#) shows the effect of various noise-reduction capacitors on RMS noise (with a 100-Hz to 100-kHz bandwidth), PSRR (at 1 kHz), and start-up time.

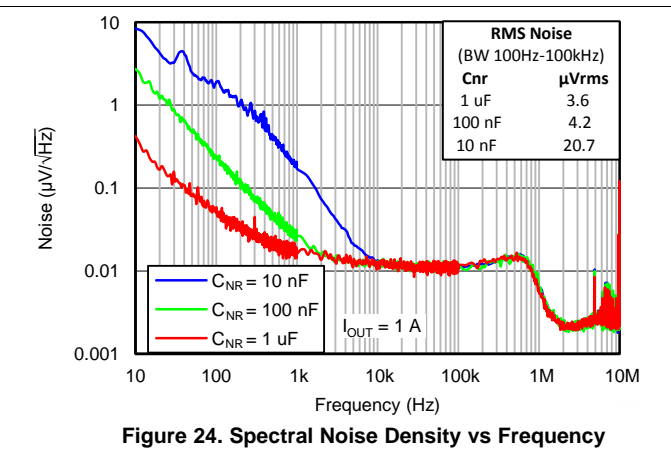
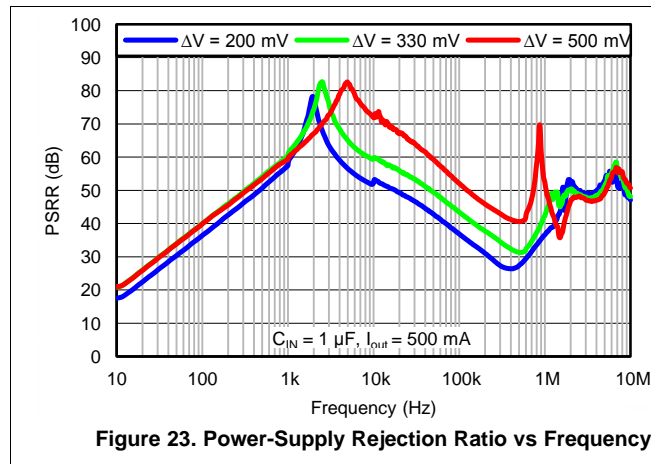
**Table 5. Effect of Various Filter Capacitors**

FILTER CAPACITOR	RMS NOISE (BW 100 Hz to 100 kHz)	PSRR (at 1 kHz)	START-UP TIME (EN to 90% of $V_{OUT}$ )
1 μF	3.62 μV	60 dB	250 ms
100 nF	4.21 μV	40 dB	25 ms
10 nF	20.70 μV	20 dB	3 ms

### 8.2.2.6 Transient Response

Increasing the size of the output capacitor reduces overshoot and undershoot magnitude during transients; however this size increase also slows the recovery from these transients.

## 8.2.3 Application Curves



## 8.3 Do's and Don'ts

Place at least 10-μF ceramic capacitors on both the IN and OUT pins of the device, as close as possible to the pins of the regulator.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Connect a 10-nF or greater, low-equivalent series resistance (ESR) capacitor across the NR pin and GND of the regulator. Larger capacitors provide lower noise performance.

Do not use a capacitor larger than 2.2 μF on the NR pin.

Do not exceed the absolute maximum ratings.

## 9 Power Supply Recommendations

For best performance, connect a low-output impedance power supply directly to the IN pin of the device. Inductive impedances between the input supply and the IN pin create significant voltage excursions at the IN pin.

## 10 Layout

### 10.1 Layout Guidelines

Input and output capacitors should be placed as close to the device pins as possible. TI recommends that all components be on the same side of the printed-circuit-board (PCB) as the device. Using long, thin traces or vias to connect the device to external components is highly discouraged because this practice leads to parasitic inductances, which in turn degrade noise, PSRR, and transient response. For an example layout, refer to the *TPS7A3501EVM-547 Evaluation Module User Guide* ( [SLVU921](#)).

### 10.2 Layout Example

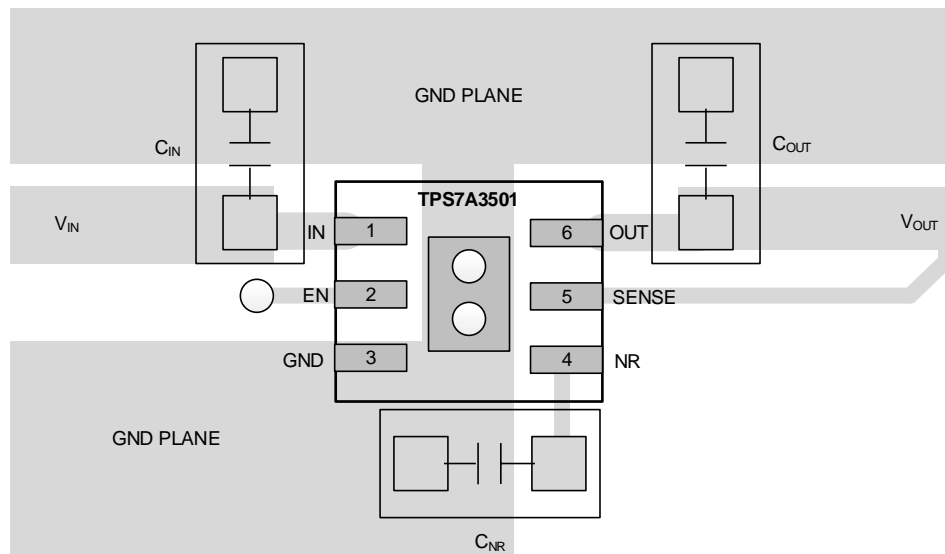


Figure 25. PCB Layout Example (DRV Package)

### 10.3 Power Dissipation

Knowing the device power dissipation and proper sizing of the thermal plane connected to the tab or pad is critical to avoiding thermal shutdown and ensuring reliable operation. Device power dissipation depends on input voltage and load conditions and can be calculated with [Equation 4](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (4)$$

Power dissipation can be minimized and greater efficiency can be achieved by using the lowest available voltage drop option of 200 mV. However, keep in mind that higher voltage drops result in better PSRR performance.

On the WSON (DRV) package, the primary conduction path for heat is through the exposed power pad to the PCB. To ensure the device does not overheat, connect the pad to ground with an appropriate amount of copper PCB area through vias.

The maximum power dissipation determines the maximum allowable junction temperature ( $T_J$ ) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ( $\theta_{JA}$ ) of the combined PCB and device package and the temperature of the ambient air ( $T_A$ ), according to [Equation 5](#):

$$T_J = T_A + (\theta_{JA} \times P_D) \quad (5)$$

Unfortunately, this thermal resistance ( $\theta_{JA}$ ) is highly dependent on the heat-spreading capability of the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The  $\theta_{JA}$  recorded in the table is determined by the JEDEC standard for PCB and copper-spreading area and is to be used only as a relative measure of package thermal performance. For a well-designed thermal layout,  $\theta_{JA}$  is actually the sum of the package junction-to-case (bottom) thermal resistance ( $\theta_{JCBot}$ ) plus the thermal resistance contribution by the PCB copper.

## 10.4 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi ( $\Psi$ ) thermal metrics to estimate the junction temperatures of the power filter on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of copper-spreading area. The key thermal metrics ( $\Psi_{JT}$  and  $\Psi_{JB}$ ) are given in the table and are used in accordance with [Equation 6](#).

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D$$

where:

- $P_D$  is the power dissipated as explained in [Equation 4](#),
- $T_T$  is the temperature at the center-top of the device package, and
- $T_B$  is the PCB surface temperature measured 1 mm from the device package and centered on the package edge.

(6)

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A3501. The [TPS7A3501EVM-547 evaluation module](#) (and [related user guide](#)) can be requested at the Texas Instruments website through the product folder or purchased directly from [the TI eStore](#).

##### 11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A3501 is available through the product folder under *Tools & Software*.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

- [TPS7A3501EVM-547 User's Guide, SLVU921](#).

### 11.3 Trademarks

PowerPAD is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 11.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3501DRVR	ACTIVE	WSO	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIQ	<a href="#">Samples</a>
TPS7A3501DRVT	ACTIVE	WSO	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	SIQ	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3501DRVR	WSO	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS7A3501DRV	WSO	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2



## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3501DRVR	WSN	DRV	6	3000	210.0	185.0	35.0
TPS7A3501DRV	WSN	DRV	6	250	210.0	185.0	35.0



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

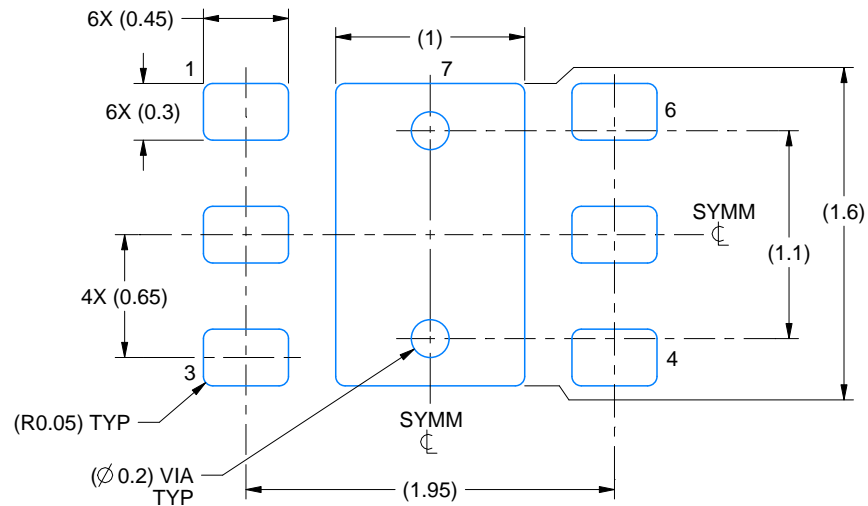


# EXAMPLE BOARD LAYOUT

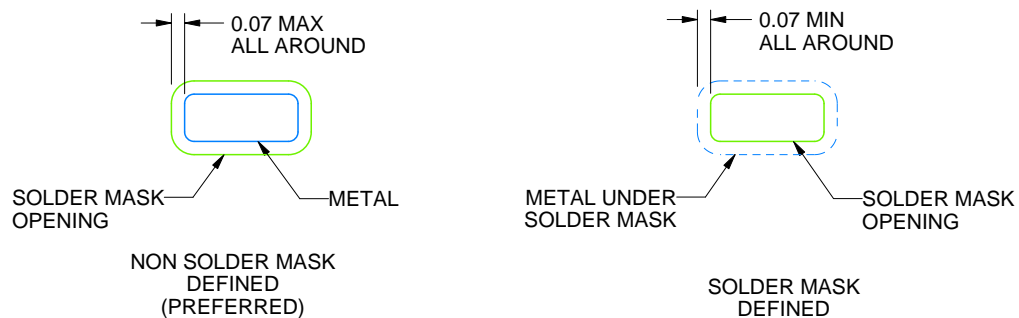
DRV0006A

WSN - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:25X



SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

# EXAMPLE STENCIL DESIGN

DRV0006A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7  
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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