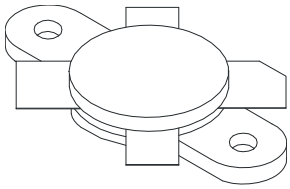
SD2933

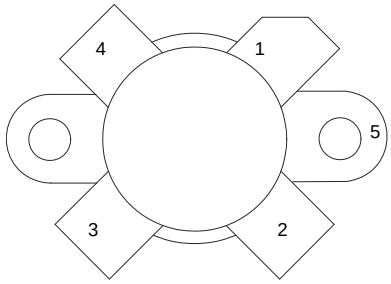
HF/VHF/UHF RF power N-channel MOSFETs

Datasheet - production data



M177 Epoxy sealed

Figure 1. Pin connection



1. Drain
2. Source
3. Gate
4, 5. Source

Features

- Gold metalization
- Excellent thermal stability
- Common source configuration
- P_{OUT} = 300 W min. with 20 dB gain @ 30 MHz
- Thermally enhanced packaging for lower junction temperatures

Description

The SD2933 is a gold metalized N-channel MOS field-effect RF power transistor, intended for use in 50 V dc large signal applications up to 150 MHz. Its special low thermal resistance package makes it ideal for ISM applications, where reliability and ruggedness are critical factors.

Table 1. Device summary

Order code	Marking	Package	Packaging
SD2933W	SD2933(1)	M177	Plastic tray

1. For more details please refer to *Chapter 6: Marking, packing and shipping specifications*.

Contents

1 Electrical data

1.1 Maximum rating

T_{CASE} = 25 °C

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{(BR)DSS}$	Drain source voltage	125	V
V_{DGR}	Drain-gate voltage (R_{GS} = 1MΩ)	125	V
V_{GS}	Gate-source voltage	±40	V
I_D	Drain current	40	A
P_{DISS}	Power dissipation	648	W
E_{AS}	Avalanche energy, single pulse (I_D = 53 A, 800 µH coil)	1100	mJ
E_{AR}(1)	Avalanche energy, repetitive	50	mJ
T_J	Max. operating junction temperature	200	°C
T_{STG}	Storage temperature	-65 to +150	°C

1. Repetitive rating: Pulse width limited by maximum junction temperature / repetitive avalanche causes additional power losses that can be calculated as: $P_{AV} = E_{AR} * f$

1.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJ\text{-}C}$	Junction to case thermal resistance	0.27	°C/W

2 Electrical characteristics

T_{CASE} = 25 °C

Table 4. Static

Symbol	Test conditions			Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	V_{GS} = 0 V	I_{DS} = 200 mA		125			V
I_{DSS}	V_{GS} = 0 V	V_{DS} = 50 V				100	µA
I_{GSS}	V_{GS} = 20 V	V_{DS} = 0 V				500	nA
$V_{GS(Q)}$(1)	V_{DS} = 10 V	I_D = 250 mA		1.5		4	V
$V_{DS(ON)}$	V_{GS} = 10 V	I_D = 20 A				3.0	V
G_{FS}(1)	V_{DS} = 10 V	I_D = 10 A		see *Table 5: G_{FS} sort*			mho
C_{ISS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		1000		pF
C_{OSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		372		pF
C_{RSS}	V_{GS} = 0 V	V_{DS} = 50 V	f = 1 MHz		29		pF

1. $V_{GS(Q)}$ and G_{FS} sorted with alpha/numeric code marked on unit.

Table 5. G_{FS} sort

G_{FS} sort	Value
A	10 - 10.99
B	11 - 11.99
C	12 - 12.99
D	13 - 13.99
E	14 - 14.99
F	15 - 15.99
G	16 - 16.99
H	17 - 18

Table 6. Dynamic

Symbol	Test Conditions	Min.	Typ.	Max.	Unit
P_{OUT}	V_{DD} = 50 V I_{DQ} = 250 mA f = 30 MHz	300	400		W
G_{PS}	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 300 W f = 30 MHz	20	23.5		dB
η_D	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 150 W f = 30 MHz	50	65		%
Load mismatch	V_{DD} = 50 V I_{DQ} = 250 mA P_{OUT} = 300 W f = 30 MHz all phase angles	3:1			VSWR

3 Impedance

Figure 2. Impedance data schematic

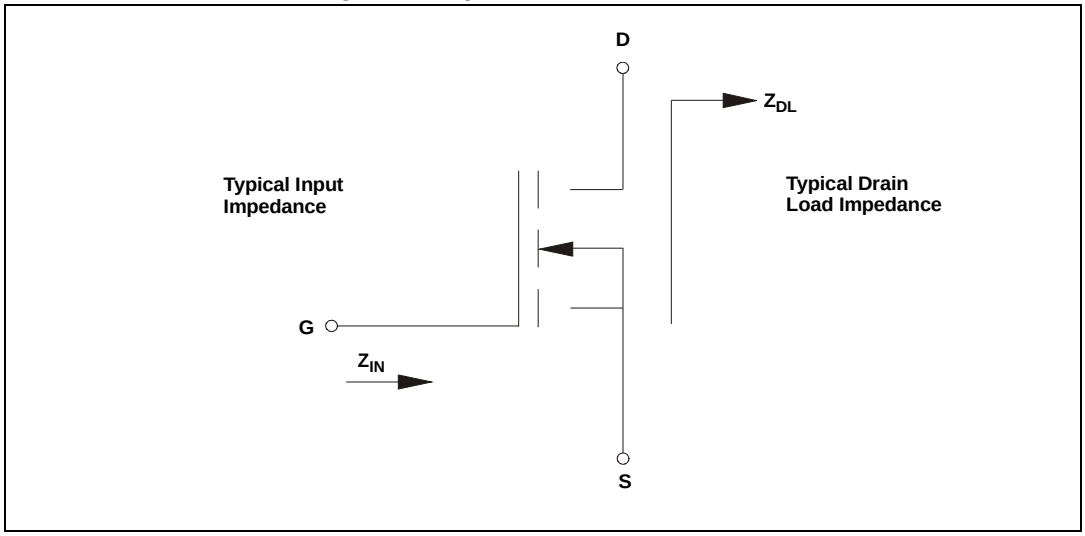


Table 7. Impedance data

f	Z_{IN} (Ω)	Z_{DL} (Ω)
30 MHz	1.8 - j 0.2	2.8 + j 2.3
108 MHz	1.9 + j 0.2	1.6 + j 1.4
175 MHz	1.9 + j 0.3	1.5 + j 1.6

4 Typical performance (30 MHz)

Figure 3. Capacitance vs. drain voltage

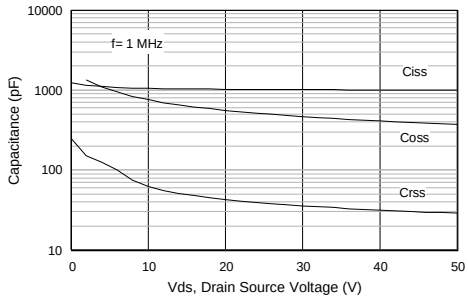


Figure 4. Drain current vs. gate voltage

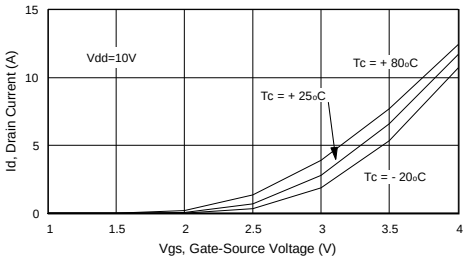


Figure 5. Gate-source voltage vs. case temperature

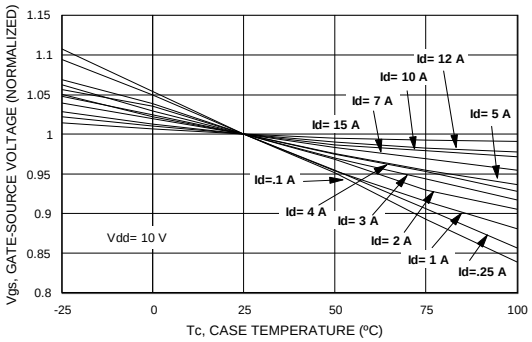


Figure 6. Maximum thermal resistance vs. case temperature

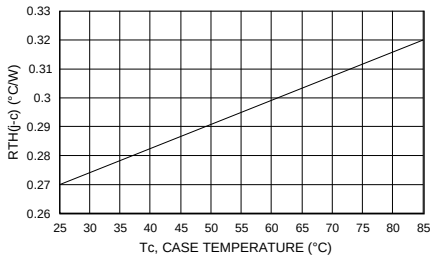


Figure 7. Transient thermal impedance

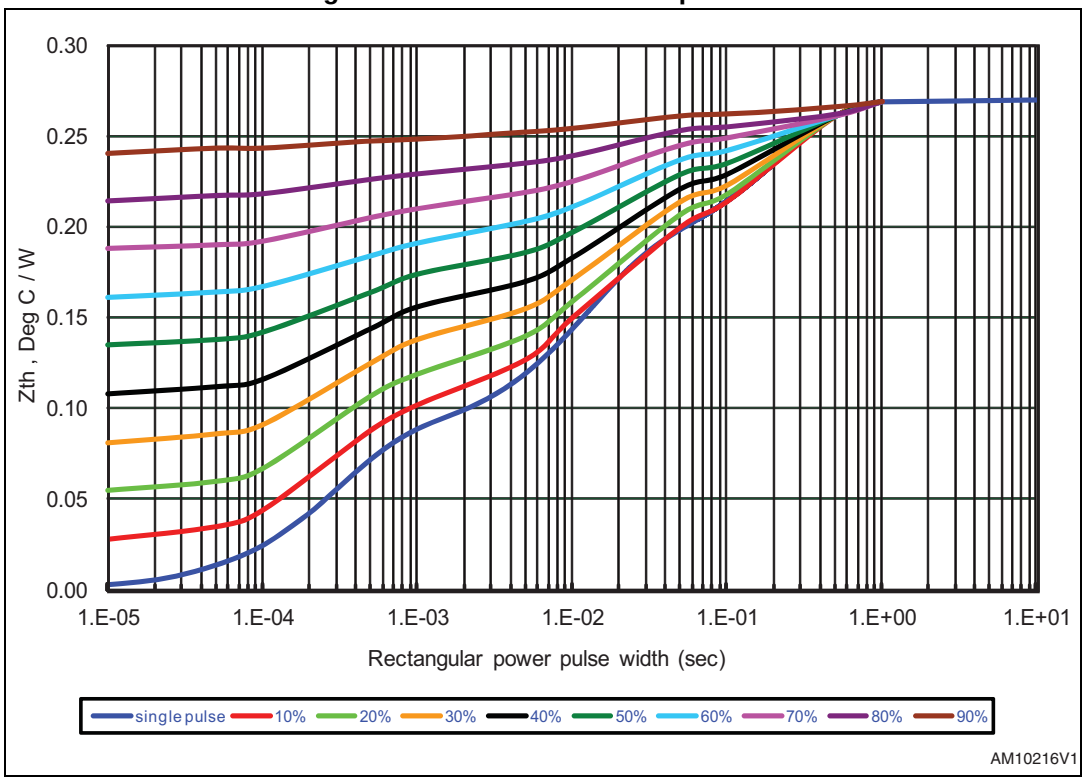


Figure 8. Transient thermal impedance model

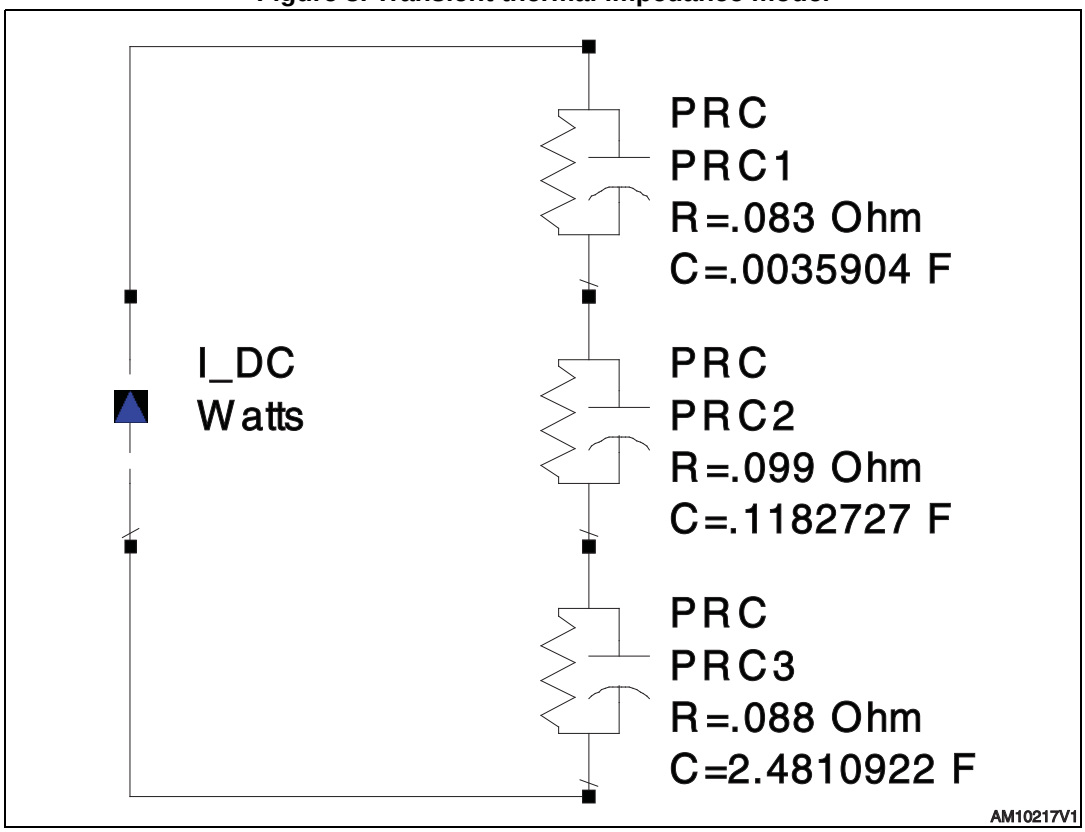


Figure 9. Output power vs. input power

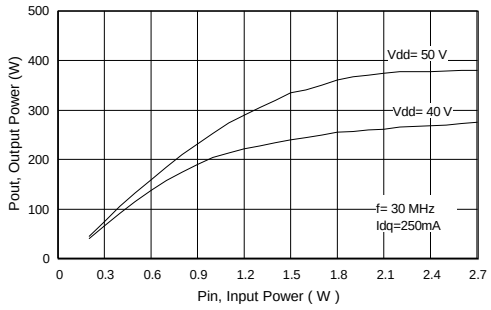


Figure 10. Output power vs. input power (at different temperature)

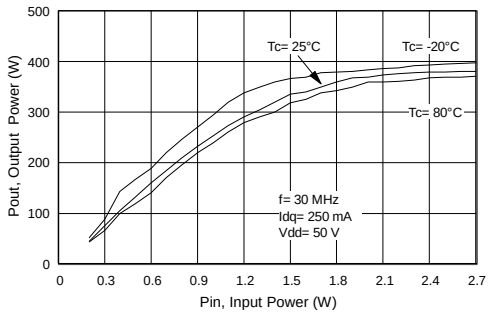


Figure 11. Power gain vs. output power

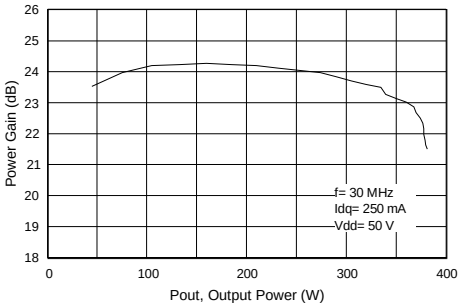


Figure 12. Efficiency vs. output power

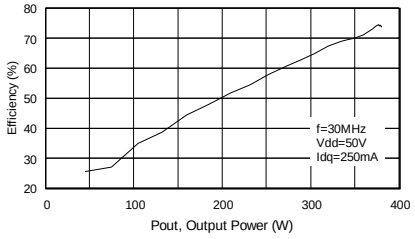


Figure 13. Output power vs. supply voltage

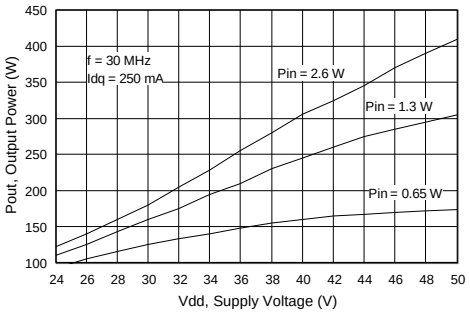
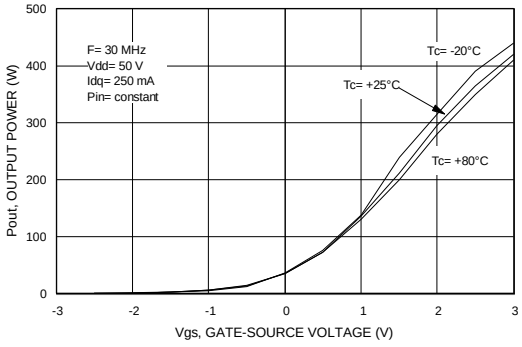


Figure 14. Output power vs. gate voltage



4.1 Test circuit (30 MHz)

Figure 15. 30 MHz test circuit schematic

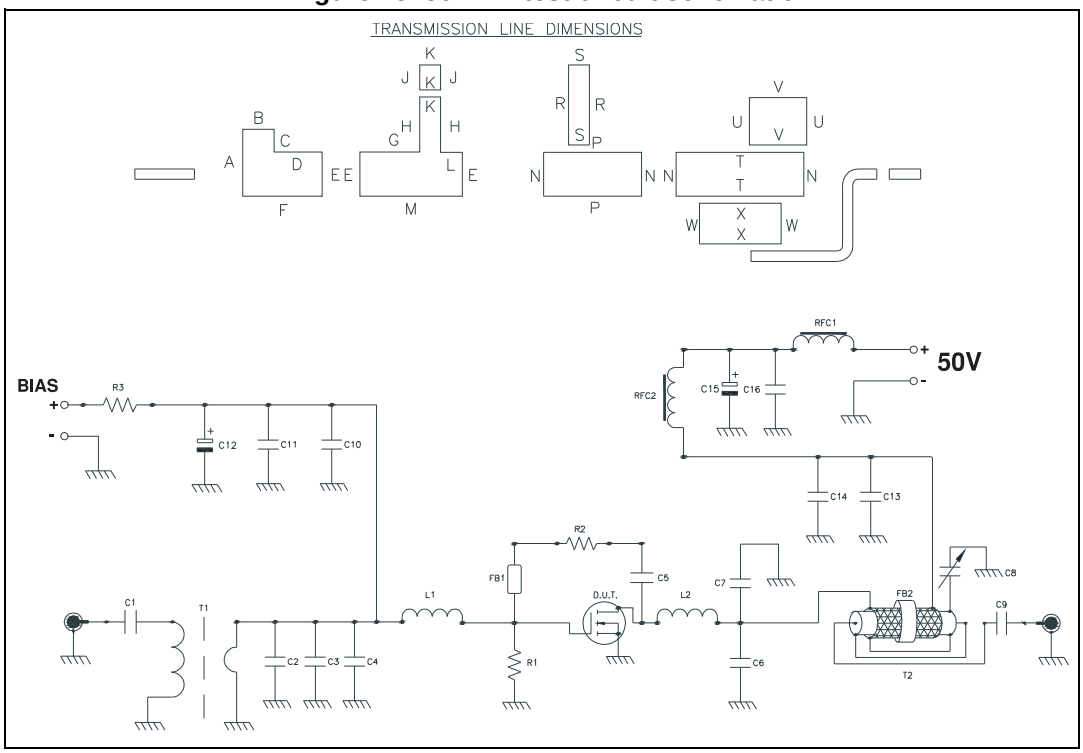


Table 8. Transmission line dimensions

Dim.	Inch	mm
A	0.532	13.51
B	0.250	6.35
C	0.181	4.59
D	0.383	9.37
E	0.351	8.91
F	0.633	16.08
G	0.477	12.12
H	0.438	11.12
J	0.200	5.08
K	0.164	4.16
L	0.174	4.42
M	0.817	20.75
N	0.350	8.89
P	0.779	19.79
R	0.639	16.23

Table 8. Transmission line dimensions (continued)

Dim.	Inch	mm
S	0.165	4.19
T	1.017	25.84
U	0.375	9.52
V	0.456	11.58
W	0.325	8.24
X	0.650	16.50

Table 9. 30 MHz test circuit part list

Component	Description
C1,C9	0.01 µF / 500 V surface mount ceramic chip capacitor
C2, C3	750 pF ATC 700B surface mount ceramic chip capacitor
C4	300 pF ATC 700B surface mount ceramic chip capacitor
C5,C10,C11,C14,C16	10000 pF ATC 200B surface mount ceramic chip capacitor
C6	510 pF ATC 700B surface mount ceramic chip capacitor
C7	300 pF ATC 700B surface mount ceramic chip capacitor
C8	175-680 pF type 46 standard trimmer capacitor
C12	47 µF / 63 V aluminum electrolytic radial lead capacitor
C13	1200 pF ATC 700B surface mount ceramic chip capacitor
C15	100 µF / 63 V aluminum electrolytic radial lead capacitor
R1,R3	1 K OHM 1 W surface mount chip resistor
R2	560 OHM 2 W wire-wound axis lead resistor
T1	HF 2-30 MHz surface mount 9:1 transformer
T2	RG - 142B/U 50 OHM coaxial cable OD = 0.165[4.18] L 15”[381.00] covered with 15”[381.00] tinned copper tubular brand 13/65” [5.1] width
L1	1 3/4 turn air-wound 16 AWG ID = 0.219 [5.56] poly-coated magnet wire
L2	1 3/4 turn air-wound 12 AWG ID = 0.250 [6.34] bus bar wire
RFC1,RFC2	3 turns 14 AWG wire through ferrite toroid
FB1	Surface mount EMI shield bead
FB2	Toroid
PCB	ULTRALAM 2000. 0.030” THK, εr = 2.55, 2 Oz ED CU both sides

Figure 16. 30 MHz test circuit photomaster

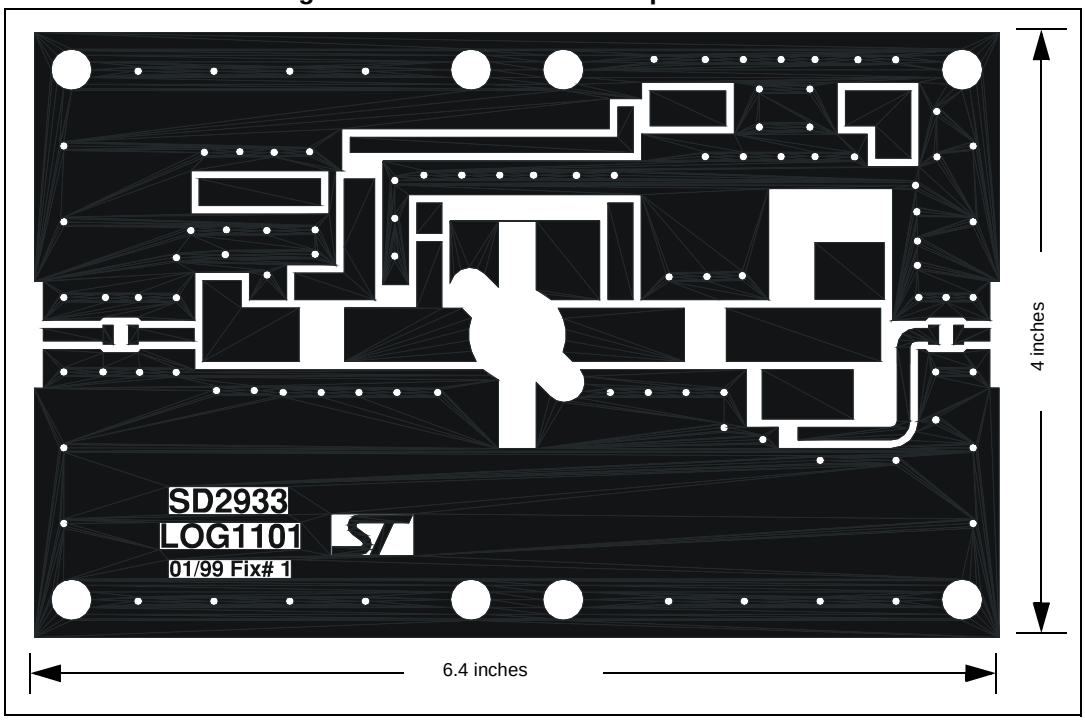
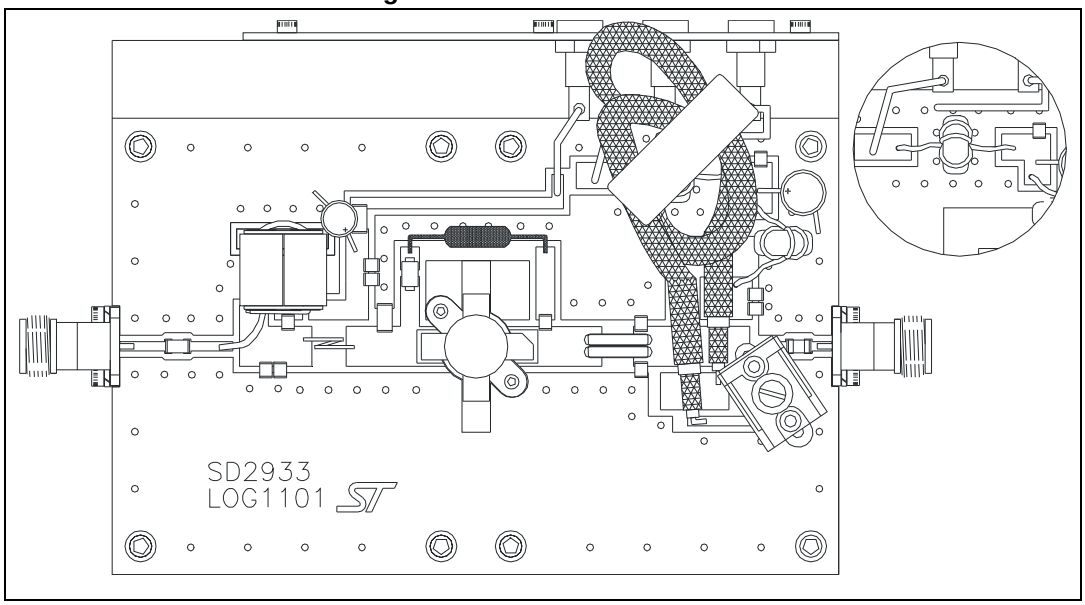


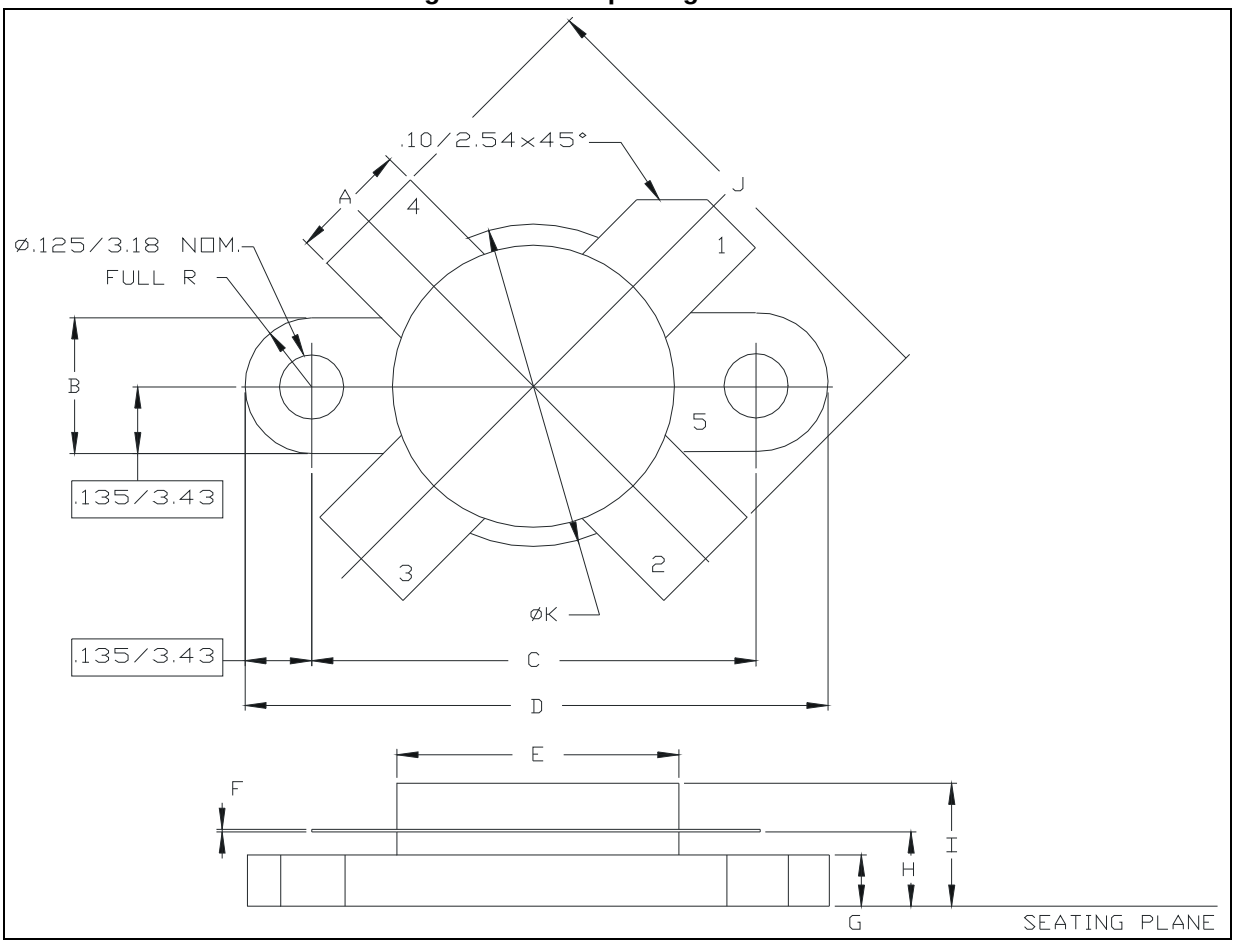
Figure 17. 30 MHz test circuit



5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 18. M177 package outline[a]



a. Controlling dimensions in inches.

Table 10. M177 (.500 dia 4/L N/HERM W/FLG) package mechanical data

Dim.	mm			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	5.72		5.97	0.225		0.235
B	6.73		6.96	0.265		0.275
C	21.84		22.10	0.860		0.870
D	28.70		28.96	1.130		1.140
E	13.84		14.10	0.545		0.555
F	0.08	-	0.18	0.003	-	0.007
G	2.49		2.74	0.098		0.108
H	3.81		4.32	0.150		0.170
I			7.11			0.280
J	27.43		28.45	1.080		1.120
K	15.88		16.13	0.625		0.635

6 Marking, packing and shipping specifications

Table 11. Packing and shipping specifications

Order code	Packaging	Pcs per tray	Dry pack humidity	GFS code	Lot code
SD2933W	Plastic tray	25	< 10%	Not mixed	Not mixed

Figure 19. Marking layout for SD2933W

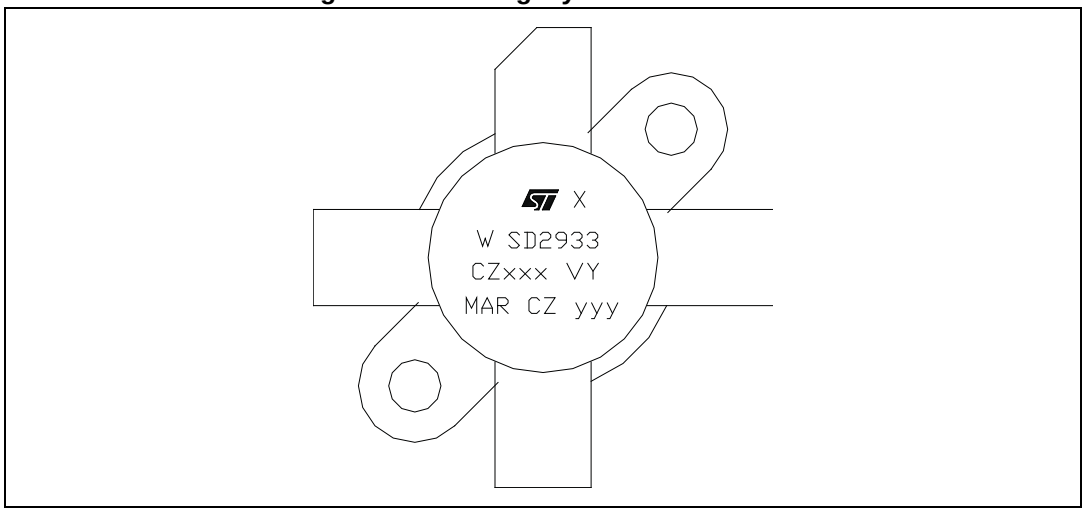


Table 12. Marking specifications

Symbol	Description
W	Wafer process code
X	G_{FS} sort
CZ	Assembly plant
xxx	Last 3 digits of diffusion lot
VY	Diffusion plant
MAR	Country of origin
CZ	Test and finishing plant
y	Assembly year
yy	Assembly week

7 Revision history

Table 13. Document revision history

Date	Revision	Changes
30-Jul-2004	9	
22-Sep-2011	10	Inserted *Section 6: Marking, packing and shipping specifications.* Updated EAS in *Table 2: Absolute maximum ratings*. Minor text changes to improve readability.
03-Oct-2011	11	Updated parameter Z_{IN} in *Table 7: Impedance data*.
17-Nov-2011	12	Inserted *Figure 7: Transient thermal impedance* and *Figure 8: Transient thermal impedance model*.
10-Jan-2012	13	Updated *Figure 7: Transient thermal impedance*.
30-Sep-2013	14	– Added row for “Avalanche energy, repetitive” and footnote to *Table 2: Absolute maximum ratings* – Minor text and formatting changes
14-Jul-2016	15	– Updated V_{GS} in *Table 2: Absolute maximum ratings*. – Minor text changes.