

CMOS Digital Integrated Circuit Silicon Monolithic

TC358771XBG/TC358772XBG

Mobile Peripheral Devices

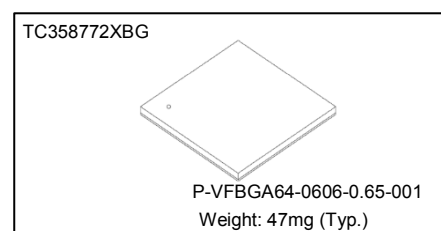
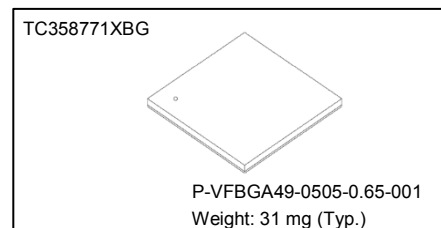
Overview

The TC358771XBG/TC358772XBG Functional Specification adds back light engine to function of TC358775XBG.

TC358771XBG/TC358772XBG is the follow-up chip of TC358774XBG/TC358775XBG, which:

1. Is pin compatible to TC358774XBG/TC358775XBG
2. Exhibit LVDS Tx block operates at 1.8V @135 MHz to reduce operation power
3. Back light engine controls the back light level automatically with ambient light and adjusts image contents.

The primary function of this chip is DSI-to-LVDS Bridge, enabling video streaming output over DSI link to drive LVDS-compatible display panels. The chip supports up to 1600x1200 24-bit pixel resolution for single-link LVDS and up to WUXGA (1920x1200 24-bit pixels) resolution for dual-link LVDS. As a secondary function, the chip also supports an I²C Master which is controlled by the DSI link; this may be used as an interface to any other control functions through I²C.



Features

● DSI Receiver

- ✧ Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
- ✧ Maximum bit rate of 1 Gbps/lane
- ✧ Video input data formats:
 - RGB565 16 bits per pixel
 - RGB666 18 bits per pixel
 - RGB666 loosely packed 24 bits per pixel
 - RGB888 24 bits per pixel
- ✧ Video frame size:
 - Up to 1600×1200 24-bit/pixel resolution to single-link LVDS display panel, limited by 135 MHz LVDS speed
 - Up to WUXGA resolutions (1920×1200 24-bit pixels) to dual-link LVDS display panel, limited by 4 Gbps DSI link speed
- ✧ Supports Video Stream packets for video data transmission.
- ✧ Supports generic long packets for accessing the chip's register set
- ✧ Supports the path for Host to control the on-chip I²C Master

● LVDS FPD Link Transmitter

- ✧ Supports single-link or dual-link
- ✧ Maximum pixel clock frequency of 135 MHz.
- ✧ Supports display up to 1600×1200 24-bit/pixel resolution for single-link, or up to 1920×1200 24-bit resolutions for dual-link

- ✧ Supports the following pixel formats:
 - RGB666 18 bits per pixel
 - RGB888 24 bits per pixel
- ✧ Features Toshiba Magic Square algorithm which enables a RGB666 display panel to produce a display quality almost equivalent to that of an RGB888 24-bit panel
- ✧ Flexible mapping of parallel data input bit ordering
- ✧ Supports programmable clock polarity
- ✧ Supports two power saving states
 - Sleep state, when receiving DSI ULPS signaling
 - Standby state, entered by STBY pin assertion

● Back Light Engine

- ✧ Provides a proper backlight parameter to the environment light

● System Operation

- ✧ Host configures the chip through DSI link
- ✧ Through DSI link, Host accesses the chip register set using Generic Write and Read packets. One Generic Long Write packet can write to multiple contiguous register addresses
- ✧ Includes an I²C Master function which is controlled by Host through DSI link (multi-master is not supported)
- ✧ Power management features to save power
- ✧ Configuration registers is also accessible through I²C Slave interface

- **Clock Source**

- ✧ LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK.
- ✧ A built-in PLL generates the high-speed LVDS serializing clock requiring no external components

- **Digital Input/Output Signals**

- ✧ All Digital Input signals are 3.3V tolerant
- ✧ All Digital Output signals can output ranging from 1.8V to 3.3V depending on IO supply voltage

- **Power supply**

- ✧ MIPI DSI D-PHY: 1.2 V
- ✧ LVDS PHY: 1.8 V
- ✧ I/O: 1.8 V - 3.3V (all IO supply pins must be same level)
- ✧ Digital Core: 1.2 V

- **Power Consumption (Typical Condition)**

- ✧ Evaluation image data: color bar
- ✧ Power Down State is achieved by:
 1. Reset asserted
 2. EXTCLK not toggling
 3. STBY = 0
 4. DSI in ULPS Drive

- **Packaging Information**

- ✧ BGA64 (0.65mm ball pitch)
 - Supports DSI-RX 4-data-lanes + Dual-Link LVDS-TX
 - 6.0mm × 6.0mm × 1.0mm
- ✧ BGA49 (0.65mm ball pitch)
 - Supports DSI-RX 4-data-lanes + Single-Link LVDS-TX
 - 5.0mm × 5.0mm × 1.0mm

Table of contents

REFERENCE	6
1. Introduction.....	8
1.1. Scope.....	8
1.2. Purpose	8
2. Device Overview	9
3. Features	10
4. Pin Layout	12
4.1. TC358772XBG BGA64 Pin-out Description.....	13
4.2. TC358772XBG BGA64 Pin Count Summary.....	14
4.3. TC358771XBG BGA49 Pin-out Description.....	15
4.4. TC358771XBG BGA49 Pin Count Summary.....	16
5. Package	17
6. Electrical characteristics.....	19
6.1. Absolute Maximum Ratings.....	19
6.2. Operating Conditions.....	19
7. Revision History	20
RESTRICTIONS ON PRODUCT USE.....	21

List of Figures

Figure 4.1 TC358772XBG Pin Layout (BGA64 – Top View).....	12
Figure 4.2 TC358771XBG Chip Pin Layout (BGA49 – Top View)	12
Figure 5.1 P-VFBGA64-0606-0.65-001 (TC358772XBG) Package Drawing.....	17
Figure 5.2 P-VFBGA49-0505-0.65-001 (TC358771XBG) Package Drawing.....	18

List of Tables

Table 4.1 TC358772XBG BGA64 Pin Count Summary	14
Table 4.2 TC358771XBG BGA49 Pin Count Summary	16
Table 5.1 Information Summary.....	18
Table 6.1 Absolute Maximum Ratings	19
Table 6.2 Operating Conditions	19
Table 7.1 Revision History	20

- MIPI is registered trademark of MIPI Alliance, Inc.

1 NOTICE OF DISCLAIMER

2 The material contained herein is not a license, either expressly or impliedly, to any IPR owned or controlled
3 by any of the authors or developers of this material or MIPI. The material contained herein is provided on
4 an "AS IS" basis and to the maximum extent permitted by applicable law, this material is provided AS IS
5 AND WITH ALL FAULTS, and the authors and developers of this material and MIPI hereby disclaim all
6 other warranties and conditions, either express, implied or statutory, including, but not limited to, any (if
7 any) implied warranties, duties or conditions of merchantability, of fitness for a particular purpose, of
8 accuracy or completeness of responses, of results, of workmanlike effort, of lack of viruses, and of lack of
9 negligence.

10 All materials contained herein are protected by copyright laws, and may not be reproduced, republished,
11 distributed, transmitted, displayed, broadcast or otherwise exploited in any manner without the express
12 prior written permission of MIPI Alliance. MIPI, MIPI Alliance and the dotted rainbow arch and all related
13 trademarks, tradenames, and other intellectual property are the exclusive property of MIPI Alliance and
14 cannot be used without its express prior written permission.

15 ALSO, THERE IS NO WARRANTY OF CONDITION OF TITLE, QUIET ENJOYMENT, QUIET
16 POSSESSION, CORRESPONDENCE TO DESCRIPTION OR NON-INFRINGEMENT WITH REGARD
17 TO THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT. IN NO EVENT WILL ANY
18 AUTHOR OR DEVELOPER OF THIS MATERIAL OR THE CONTENTS OF THIS DOCUMENT OR
19 MIPI BE LIABLE TO ANY OTHER PARTY FOR THE COST OF PROCURING SUBSTITUTE
20 GOODS OR SERVICES, LOST PROFITS, LOSS OF USE, LOSS OF DATA, OR ANY INCIDENTAL,
21 CONSEQUENTIAL, DIRECT, INDIRECT, OR SPECIAL DAMAGES WHETHER UNDER
22 CONTRACT, TORT, WARRANTY, OR OTHERWISE, ARISING IN ANY WAY OUT OF THIS OR
23 ANY OTHER AGREEMENT, SPECIFICATION OR DOCUMENT RELATING TO THIS MATERIAL,
24 WHETHER OR NOT SUCH PARTY HAD ADVANCE NOTICE OF THE POSSIBILITY OF SUCH
25 DAMAGES.

26 Without limiting the generality of this Disclaimer stated above, the user of the contents of this Document is
27 further notified that MIPI: (a) does not evaluate, test or verify the accuracy, soundness or credibility of the
28 contents of this Document; (b) does not monitor or enforce compliance with the contents of this Document;
29 and (c) does not certify, test, or in any manner investigate products or services or any claims of compliance
30 with the contents of this Document. The use or implementation of the contents of this Document may
31 involve or require the use of intellectual property rights ("IPR") including (but not limited to) patents,
32 patent applications, or copyrights owned by one or more parties, whether or not Members of MIPI. MIPI
33 does not make any search or investigation for IPR, nor does MIPI require or request the disclosure of any
34 IPR or claims of IPR as respects the contents of this Document or otherwise.

35 Questions pertaining to this document, or the terms or conditions of its provision, should be addressed to:

36 MIPI Alliance, Inc.
37 c/o IEEE-ISTO
38 445 Hoes Lane
39 Piscataway, NJ 08854
40 Attn: Board Secretary

This Notice of Disclaimer applies to all DSI input and processing paths related descriptions throughout this document.

REFERENCE

1. MIPI D-PHY, "MIPI_D-PHY_specification_v01-00-00, May 14, 2009"
2. MIPI Alliance Specification for DSI version 1.01, Feb 2008
3. MIPI Alliance Specification for DPI version 2.0, Sep, 2005
4. An Introduction to FPD-Link, AN-1032, Application Note, National Semiconductor 2009
5. DS90C383/DS90CF384 LVDS Transmitter 24-Bit FPD Link, Data Sheet, National Semiconductor 2000
6. THC63LVD823 Single/Dual Link LVDS Transmitter, Data Sheet, Thine Electronics, 2000-2003.
7. SN75LVDS83 FlatLink Transmitter, Data Sheet, Texas Instrument, 1997-2009.

Precautions and Usage Considerations Specific to Application Specific Standard Products and General-Purpose Linear Ics

Design

CAUTION

Use an appropriate power supply fuse to ensure that a large current does not continuously flow in case of over current and/or IC failure. The IC will fully break down when used under conditions that exceed its absolute maximum ratings, when the wiring is routed improperly or when an abnormal pulse noise occurs from the wiring or load, causing a large current to continuously flow and the breakdown can lead smoke or ignition. To minimize the effects of the flow of a large current in case of breakdown, appropriate settings, such as fuse capacity, fusing time and insertion circuit location, are required.

If your design includes an inductive load such as a motor coil, incorporate a protection circuit into the design to prevent device malfunction or breakdown caused by the current resulting from the inrush current at power ON or the negative current resulting from the back electromotive force at power OFF. For details on how to connect a protection circuit such as a current limiting resistor or back electromotive force adsorption diode, refer to individual IC datasheets or the IC databook. IC breakdown may cause injury, smoke or ignition.

Use a stable power supply with ICs with built-in protection functions. If the power supply is unstable, the protection function may not operate, causing IC breakdown. IC breakdown may cause injury, smoke or ignition.

Carefully select external components (such as inputs and negative feedback capacitors) and load components (such as speakers), for example, power amp and regulator.

If there is a large amount of leakage current such as input or negative feedback condenser, the IC output DC voltage will increase. If this output voltage is connected to a speaker with low input withstand voltage, overcurrent or IC failure can cause smoke or ignition. (The over current can cause smoke or ignition from the IC itself.) In particular, please pay attention when using a Bridge Tied Load (BTL) connection type IC that inputs output DC voltage to a speaker directly.

Over current Protection Circuit

Over current protection circuits (referred to as current limiter circuits) do not necessarily protect ICs under all circumstances. If the Over current protection circuits operate against the over current, clear the over current status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the over current protection circuit to not operate properly or IC breakdown before operation. In addition, depending on the method of use and usage conditions, if over current continues to flow for a long time after operation, the IC may generate heat resulting in breakdown.

Thermal Shutdown Circuit

Thermal shutdown circuits do not necessarily protect ICs under all circumstances. If the Thermal shutdown circuits operate against the over temperature, clear the heat generation status immediately.

Depending on the method of use and usage conditions, such as exceeding absolute maximum ratings can cause the thermal shutdown circuit to not operate properly or IC breakdown before operation.

Heat Radiation Design

When using an IC with large current flow such as power amp, regulator or driver, please design the device so that heat is appropriately radiated, not to exceed the specified junction temperature (T_J) at any time and condition. These ICs generate heat even during normal use. An inadequate IC heat radiation design can lead to decrease in IC life, deterioration of IC characteristics or IC breakdown. In addition, please design the device taking into consideration the effect of IC heat radiation with peripheral components.

Mounting

Installation to Heat Sink

Please install the power IC to the heat sink not to apply excessive mechanical stress to the IC. Excessive mechanical stress can lead to package cracks, resulting in a reduction in reliability or breakdown of internal IC chip. In addition, depending on the IC, the use of silicon rubber may be prohibited. Check whether the use of silicon rubber is prohibited for the IC you intend to use, or not. For details of power IC heat radiation design and heat sink installation, refer to individual technical datasheets or IC databooks.

Also please refer to "RESTRICTIONS ON PRODUCT USE".

1. Introduction

The TC358771XBG/TC358772XBG Functional Specification adds back light engine to function of 775XBG. TC358771XBG/TC358772XBG is the follow-up chip of TC358774XBG/TC358775XBG, which:

1. Is pin compatible to TC358774XBG/TC358775XBG
2. Exhibit LVDS Tx block operates at 1.8V @135 MHz to reduce operation power
3. Back light engine controls the back light level automatically with ambient light and adjusts image contents.

The primary function of this chip is DSI-to-LVDS Bridge, enabling video streaming output over DSI link to drive LVDS-compatible display panels. The chip supports up to 1600×1200 24-bit pixel resolution for single-link LVDS and up to WUXGA (1920×1200 24-bit pixels) resolution for dual-link LVDS. As a secondary function, the chip also supports an I²C Master which is controlled by the DSI link; this may be used as an interface to any other control functions through I²C.

The chip can be configured through the DSI link by sending write register commands through DSI Generic Long Write-packets. It can also be configured through the I²C Slave interface. I²C slave address of TC358771XBG/TC358772XBG is 8'b0001_111X, where X = 0/1 for write/read to/from TC358771XBG/TC358772XBG operation.

This specification provides description of two product versions:

TC358771XBG-49: In BGA49 package, it supports DSI-RX with up to 4 data lanes, and outputs to Single-Link LVDS.

TC358772XBG-64: In BGA64 package, it supports DSI-RX with up to 4 data lanes, and outputs to Single-Link and Dual-Link LVDS.

1.1. Scope

This document details the operation of the chip, description of each major function that the chip supports, description of the configuration register set, and includes pinout, package, and electrical characteristics information.

1.2. Purpose

This document serves as the vehicle for exchanging detailed technical information of the TC358771XBG/TC358772XBG and its usage within the target application systems at the customer side. It also serves as the chip functional specification for design implementation and verification.

2. Device Overview

The TC358771XBG/TC358772XBG chip functions primarily as a DSI-to-LVDS communication protocol bridge, enabling video streaming from a Host processor over DSI link to drive LVDS-compatible display panels. In other words, the chip receives video stream input through its DSI receiver (DSI-RX), buffers the received pixel data in a buffer, and then re-transmits the video stream out through the LVDS transmitter.

As a secondary function, the chip also ports an I²C Master which is controlled by the DSI link; this may be used as a programming interface to other peripherals in the system.

As a 3rd function, automatically control the back light level and adjust image contents based on ambient light.

The chip is configured through the DSI link. Alternatively, it can optionally be configured through the I²C Slave interface; in such case, the I²C Master function would be disabled.

The reference video pixel clock for the LVDS link is sourced either from an external clock via input pin EXTCLK or derived from DSICLK. The chip integrates a PLL which synthesizes the high-speed clock for use solely to serialize video data over the LVDS link.

The DSI-RX receiver supports from 1- to 4-Lane configurations at bit rate up to 1 Gbps per lane. Host can transmit video in video mode. In video mode, Host controls video timing by sending video frame and line sync events together with video pixel data; video data transmission can be burst or non-burst. Since the chip integrates only 1024-pixel of video buffer, Host still has to take care of transmitting pixel data at appropriate video line time in order to avoid buffer overflow (or underflow).

The LVDS transmitter supports a clock frequency of up to 135 MHz for either single- or dual-link.

The chip supports power management to conserve power when its functions are not in use. Host manages the chip's power consumption states by using ULPS signaling over DSI link and/or STBY pin.

3. Features

- **DSI Receiver**

- ✧ Configurable 1- up to 4-Data-Lane DSI Link with bi-directional support on Data Lane 0
- ✧ Maximum bit rate of 1 Gbps/lane
- ✧ Video input data formats:
 - RGB565 16 bits per pixel
 - RGB666 18 bits per pixel
 - RGB666 loosely packed 24 bits per pixel
 - RGB888 24 bits per pixel.
- ✧ Video frame size:
 - Up to 1600x1200 24-bit/pixel resolution to single-link LVDS display panel, limited by 135 MHz LVDS speed
 - Up to WUXGA resolutions (1920x1200 24-bit pixels) to dual-link LVDS display panel, limited by 4 Gbps DSI link speed
- ✧ Supports Video Stream packets for video data transmission.
- ✧ Supports generic long packets for accessing the chip's register set
- ✧ Supports the path for Host to control the on-chip I²C Master

- **LVDS FPD Link Transmitter**

- ✧ Supports single-link or dual-link
- ✧ Maximum pixel clock frequency of 135 MHz.
- ✧ Supports display up to 1600×1200 24-bit/pixel resolution for single-link, or up to 1920×1200 24-bit resolutions for dual-link
- ✧ Supports the following pixel formats:
 - RGB666 18 bits per pixel
 - RGB888 24 bits per pixel
- ✧ Features Toshiba Magic Square algorithm which enables a RGB666 display panel to produce a display quality almost equivalent to that of an RGB888 24-bit panel
- ✧ Flexible mapping of parallel data input bit ordering
- ✧ Supports programmable clock polarity
- ✧ Supports two power saving states
 - Sleep state, when receiving DSI ULPS signaling
 - Standby state, entered by STBY pin assertion

- **Back Light Engine**

- ✧ Provides a proper backlight parameter to the environment light

- **System Operation**

- ✧ Host configures the chip through DSI link
- ✧ Through DSI link, Host accesses the chip register set using Generic Write and Read packets. One Generic Long Write packet can write to multiple contiguous register addresses
- ✧ Includes an I²C Master function which is controlled by Host through DSI link (multi-master is not supported)
- ✧ Power management features to save power
- ✧ Configuration registers is also accessible through I²C Slave interface

• Clock Source

- ✧ LVDS pixel clock source is either from external clock EXTCLK or derived from DSICLK.
- ✧ A built-in PLL generates the high-speed LVDS serializing clock requiring no external components

• Digital Input/Output Signals

- ✧ All Digital Input signals are 3.3V tolerant
- ✧ All Digital Output signals can output ranging from 1.8V to 3.3V depending on IO supply voltage

• Power supply

- ✧ MIPI DSI D-PHY: 1.2 V
- ✧ LVDS PHY: 1.8 V
- ✧ I/O: 1.8 V - 3.3V (all IO supply pins must be same level)
- ✧ Digital Core: 1.2 V

• Power Consumption (Typical Condition)

- ✧ Evaluation image data : color bar
- ✧ Power Down State is achieved by:
 1. Reset asserted
 2. EXTCLK not toggling
 3. STBY=0
 4. DSI in ULPS Drive

Normal Mode									
	Condition		VDDC	VDDS	DSI	LVDS		TOTAL Power	Unit
	LVDS	DSI	VDDC	VDDIO	VDDMIPI	LVDS12	LVDS18		
			1.2	3.3	1.2	1.2	1.8		
1280x800x18 @60fps	75MHz	300MHz	29.6	0.08	13.6	7.4	16.1		mA
	Single link	4Lane	35.52	0.26	16.32	8.88	28.98	89.96	mW
1920x1080x18 @60fps	75MHz	450MHz	55.2	0.08	16.8	8.3	32.10		mA
	Dual link	4Lane	66.24	0.26	20.16	10.08	57.78	154.40	mW
Power Down	-	-	0.4	0.001	0.1	0.1	0.001		mA
	-	-	0.48	0.0033	0.12	0.12	0.0018	0.73	mW

• Packaging Information

- ✧ BGA64 (0.65mm ball pitch)
 - Supports DSI-RX 4-data-lanes + Dual-Link LVDS-TX
 - 6.0mm × 6.0mm × 1.0mm
- ✧ BGA49 (0.65mm ball pitch)
 - Supports DSI-RX 4-data-lanes + Single-Link LVDS-TX
 - 5.0mm × 5.0mm × 1.0mm

4. Pin Layout

A1 VSS_LVDS2_12	A2 LVTX2AN	A3 LVTX2BN	A4 LVTX2CN	A5 LVTX2DN	A6 LVTX2EN	A7 VSS_LVDS2_18	A8 VSS_LVDS1_12
B1 VDD_LVDS2_12	B2 LVTX2AP	B3 LVTX2BP	B4 LVTX2CP	B5 LVTX2DP	B6 LVTX2EP	B7 VDD_LVDS2_18	B8 VDD_LVDS1_12
C1 VSSIO	C2 VDDIO	C3 STBY	C4 PWM0	C5 VDD_LVDS2_18	C6 VSS_LVDS2_18	C7 LVTX1AP	C8 LVTX1AN
D1 EXTCLK	D2 GPIO2	D3 GPIO1	D4 RESX	D5 TM	D6 VDD_LVDS1_18	D7 LVTX1BP	D8 LVTX1BN
E1 VSSC	E2 VDDC	E3 GPIO0	E4 VDDC	E5 VSSC	E6 VSS_LVDS1_18	E7 LVTX1CP	E8 LVTX1CN
F1 VSSIO	F2 VDDIO	F3 VDD_MIPI	F4 VSS_MIPI	F5 VSS_MIPI	F6 VDD_MIPI	F7 LVTX1DP	F8 LVTX1DN
G1 I2C_SCL	G2 DSRXD0P	G3 DSRXD1P	G4 DSRXCP	G5 DSRXD2P	G6 DSRXD3P	G7 LVTX1EP	G8 LVTX1EN
H1 I2C_SDA	H2 DSRXD0M	H3 DSRXD1M	H4 DSRXCM	H5 DSRXD2M	H6 DSRXD3M	H7 VDD_LVDS1_18	H8 VSS_LVDS1_18

Figure 4.1 TC358772XBG Pin Layout (BGA64 – Top View)

A1 VSSIO	A2 VDDIO	A3 RESX	A4 GPIO0	A5 VSSC	A6 VDDC	A7 VSSC
B1 EXTCLK	B2 VDDC	B3 VSSC	B4 TM	B5 VDD_LVDS1_12	B6 LVTX1AP	B7 LVTX1AN
C1 I2C_SDA	C2 PWM0	C3 GPIO2	C4 GPIO1	C5 VSS_LVDS1_12	C6 LVTX1BP	C7 LVTX1BN
D1 I2C_SCL	D2 STBY	D3 VSS_MIPI	D4 VDD_MIPI	D5 VSS_LVDS1_18	D6 LVTX1CP	D7 LVTX1CN
E1 VDDIO	E2 VSSIO	E3 VSS_MIPI	E4 VDD_MIPI	E5 VDD_LVDS1_18	E6 LVTX1DP	E7 LVTX1DN
F1 DSRXD0P	F2 DSRXD1P	F3 DSRXCP	F4 DSRXD2P	F5 DSRXD3P	F6 LVTX1EP	F7 LVTX1EN
G1 DSRXD0M	G2 DSRXD1M	G3 DSRXCM	G4 DSRXD2M	G5 DSRXD3M	G6 VDD_LVDS1_18	G7 VSS_LVDS1_18

Figure 4.2 TC358771XBG Chip Pin Layout (BGA49 – Top View)

4.1. TC358772XBG BGA64 Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	State of pin at reset active	Power Supply Voltage
DSI-RX IF	DSRXCP	DSI-PHY	1	DSI clock signal - positive	Hi-z	1.2 V
	DSRXCM	DSI-PHY	1	DSI clock signal - negative	Hi-z	1.2 V
	DSRXD0P	DSI-PHY	1	DSI data lane 0 - positive	Hi-z	1.2 V
	DSRXD0M	DSI-PHY	1	DSI data lane 0 - negative	Hi-z	1.2 V
	DSRXD1P	DSI-PHY	1	DSI data lane 1 - positive	Hi-z	1.2 V
	DSRXD1M	DSI-PHY	1	DSI data lane 1 - negative	Hi-z	1.2 V
	DSRXD2P	DSI-PHY	1	DSI data lane 2 - positive	Hi-z	1.2 V
	DSRXD2M	DSI-PHY	1	DSI data lane 2 - negative	Hi-z	1.2 V
	DSRXD3P	DSI-PHY	1	DSI data lane 3 - positive	Hi-z	1.2 V
	DSRXD3M	DSI-PHY	1	DSI data lane 3 - negative	Hi-z	1.2 V
1st-Link LVDS-TX IF	VDD_MIPI	Power	2	MIPI Analog Power Supply	-	1.2 V
	VSS_MIPI	Ground	2	MIPI Analog Ground	-	GND
	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	Hi-z	1.8 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	Hi-z	1.8 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	Hi-z	1.8 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	Hi-z	1.8 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	Hi-z	1.8 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	Hi-z	1.8 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	Hi-z	1.8 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	Hi-z	1.8 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	Hi-z	1.8 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E - negative	Hi-z	1.8 V
	VDD_LVDS1_18	Power	2	First-link LVDS 1.8V Power Supply	-	1.8 V
	VSS_LVDS1_18	Ground	2	First-link LVDS 1.8V Ground	-	GND
2nd-Link LVDS-TX IF	VDD_LVDS1_12	Power	1	First-link LVDS 1.2V Power Supply	-	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2V Ground	-	GND
	LVTX2AP	LVDS-PHY	1	LVDS second-link data channel A - positive	Hi-z	1.8 V
	LVTX2AN	LVDS-PHY	1	LVDS second-link data channel A - negative	Hi-z	1.8 V
	LVTX2BP	LVDS-PHY	1	LVDS second-link data channel B - positive	Hi-z	1.8 V
	LVTX2BN	LVDS-PHY	1	LVDS second-link data channel B - negative	Hi-z	1.8 V
	LVTX2CP	LVDS-PHY	1	LVDS second-link data channel C - positive	Hi-z	1.8 V
	LVTX2CN	LVDS-PHY	1	LVDS second-link data channel C - negative	Hi-z	1.8 V
	LVTX2DP	LVDS-PHY	1	LVDS second-link data channel D (Clock) - positive	Hi-z	1.8 V
	LVTX2DN	LVDS-PHY	1	LVDS second-link data channel D (Clock) - negative	Hi-z	1.8 V
	LVTX2EP	LVDS-PHY	1	LVDS second-link data channel E - positive	Hi-z	1.8 V
	LVTX2EN	LVDS-PHY	1	LVDS second-link data channel E - negative	Hi-z	1.8 V
	VDD_LVDS2_18	Power	2	Second-link LVDS 1.8V Power Supply	-	1.8 V
	VSS_LVDS2_18	Ground	2	Second-link LVDS 1.8V Ground	-	GND
I ² C IF	VDD_LVDS2_12	Power	1	Second-link LVDS 1.2V Power Supply	-	1.2 V
	VSS_LVDS2_12	Ground	1	Second-link LVDS 1.2V Ground	-	GND
I ² C IF	I2C_SCL	S-OD	1	I ² C Master or Slave interface clock signal	Hi-z	1.8V-3.3V
I ² C IF	I2C_SDA	S-OD	1	I ² C Master or Slave interface data signal	Hi-z	1.8V-3.3V
GPIO	GPIO[2:0]	N _{PD}	3	GPIO bits 2-0	Hi-z	1.8V-3.3V
PWM	PWMO	N _{PD}	1	PWM Output / GPIO bit 3(Initial function)	Hi-z	1.8V-3.3V
SYSTEM	RESX	N _{PD}	1	Hardware reset, low active	Hi-z	1.8V-3.3V
	EXTCLK	N _{PD}	1	External pixel clock source	Hi-z	1.8V-3.3V
	STBY	N	1	Standby pin, low active	Hi-z	1.8V-3.3V
	TM	N _{PD}	1	Test mode select	Hi-z	1.8V-3.3V
	VDDIO	Power	2	IO Power Supply	-	1.8-3.3V
	VSSIO	Ground	2	IO Ground	-	GND
	VDDC	Power	2	Digital Core Power Supply	-	1.2 V
	VSSC	Ground	2	Digital Core Ground	-	GND

Buffer Type Abbreviation:

N:	Normal IO
N _{PD} :	Normal IO with weak Internal Pull-Down
N _{PU} :	Normal IO with weak Internal Pull-Up
S-OD:	Pseudo open-drain output, schmitt trigger input
SCHMIDTT:	Fail Safe schmitt trigger input buffer
DSI-PHY:	front-end analog IO for DSI
LVDS-PHY:	front-end analog IO for LVDS
A:	Analog pad

4.2. TC358772XBG BGA64 Pin Count Summary**Table 4.1 TC358772XBG BGA64 Pin Count Summary**

Group Name	Pin Count	Notes
DSI-RX IF	14	Include DSI Power & Ground
1st-Link LVDS-TX IF/ 2nd-Link LVDS-TX IF	32	Include LVDS Power & Ground
I ² C IF	2	-
GPIO	3	-
PWM	1	-
SYSTEM	12	Include Power & Ground
Total Pin Count	64	

4.3. TC358771XBG BGA49 Pin-out Description

Group	Pin Name	IO Type	Pin Cnt.	Description	State of pin at reset active	Power Supply Voltage
DSI-RX IF	DSRXCP	DSI-PHY	1	DSI clock signal - positive	Hi-z	DSICP
	DSRXCM	DSI-PHY	1	DSI clock signal - negative	Hi-z	DSICM
	DSRXD0P	DSI-PHY	1	DSI data lane 0 - positive	Hi-z	1.2 V
	DSRXD0M	DSI-PHY	1	DSI data lane 0 - negative	Hi-z	1.2 V
	DSRXD1P	DSI-PHY	1	DSI data lane 1 - positive	Hi-z	1.2 V
	DSRXD1M	DSI-PHY	1	DSI data lane 1 - negative	Hi-z	1.2 V
	DSRXD2P	DSI-PHY	1	DSI data lane 2 - positive	Hi-z	1.2 V
	DSRXD2M	DSI-PHY	1	DSI data lane 2 - negative	Hi-z	1.2 V
	DSRXD3P	DSI-PHY	1	DSI data lane 3 - positive	Hi-z	1.2 V
	DSRXD3M	DSI-PHY	1	DSI data lane 3 - negative	Hi-z	1.2 V
	VDD_MIPI	Power	2	MIPI Analog Power Supply	-	1.2 V
	VSS_MIPI	Ground	2	MIPI Analog Ground	-	GND
LVDS-TX IF	LVTX1AP	LVDS-PHY	1	LVDS first-link data channel A - positive	Hi-z	1.8 V
	LVTX1AN	LVDS-PHY	1	LVDS first-link data channel A - negative	Hi-z	1.8 V
	LVTX1BP	LVDS-PHY	1	LVDS first-link data channel B - positive	Hi-z	1.8 V
	LVTX1BN	LVDS-PHY	1	LVDS first-link data channel B - negative	Hi-z	1.8 V
	LVTX1CP	LVDS-PHY	1	LVDS first-link data channel C - positive	Hi-z	1.8 V
	LVTX1CN	LVDS-PHY	1	LVDS first-link data channel C - negative	Hi-z	1.8 V
	LVTX1DP	LVDS-PHY	1	LVDS first-link data channel D (Clock) - positive	Hi-z	1.8 V
	LVTX1DN	LVDS-PHY	1	LVDS first-link data channel D (Clock) - negative	Hi-z	1.8 V
	LVTX1EP	LVDS-PHY	1	LVDS first-link data channel E - positive	Hi-z	1.8 V
	LVTX1EN	LVDS-PHY	1	LVDS first-link data channel E - negative	Hi-z	1.8 V
	VDD_LVDS1_18	Power	2	First-link LVDS 1.8V Power Supply	-	1.8 V
	VSS_LVDS1_18	Ground	2	First-link LVDS 1.8V Ground	-	GND
	VDD_LVDS1_12	Power	1	First-link LVDS 1.2V Power Supply	-	1.2 V
	VSS_LVDS1_12	Ground	1	First-link LVDS 1.2V Ground	-	GND
I ² C IF	I2C_SCL	S-OD	1	I ² C Master or Slave interface clock signal	Hi-z	1.8V-3.3V
	I2C_SDA	S-OD	1	I ² C Master or Slave interface data signal	Hi-z	1.8V-3.3V
GPIO	GPIO[3:0]	N _{PD}	4	GPIO bits 2-0	Hi-z	1.8V-3.3V
PWM	PWMO	N _{PD}	1	PWM Output / GPIO bit 3(Initial Function)	Hi-z	1.8V-3.3V
SYSTEM	RESX	N _{PD}	1	Hardware reset, low active	Hi-z	1.8V-3.3V
	EXTCLK	N _{PD}	1	External pixel clock source	Hi-z	1.8V-3.3V
	STBY	N	1	Standby pin, low active	Hi-z	1.8V-3.3V
	TM	N _{PD}	1	Test mode select	Hi-z	1.8V-3.3V
	VDDIO	Power	2	IO Power Supply	-	1.8-3.3V
	VSSIO	Ground	2	IO Ground	-	GND
	VDDC	Power	2	Digital Core Power Supply	-	1.2 V
	VSSC	Ground	3	Digital Core Ground	-	GND

Buffer Type Abbreviation:

N: Normal IO
 S-OD: Pseudo open-drain output, schmitt trigger input
 SCHMIDTT: Fail Safe schmitt trigger input buffer
 DSI-PHY: front-end analog IO for DSI
 LVDS-PHY: front-end analog IO for LVDS
 A: Analog pad

4.4. TC358771XBG BGA49 Pin Count Summary

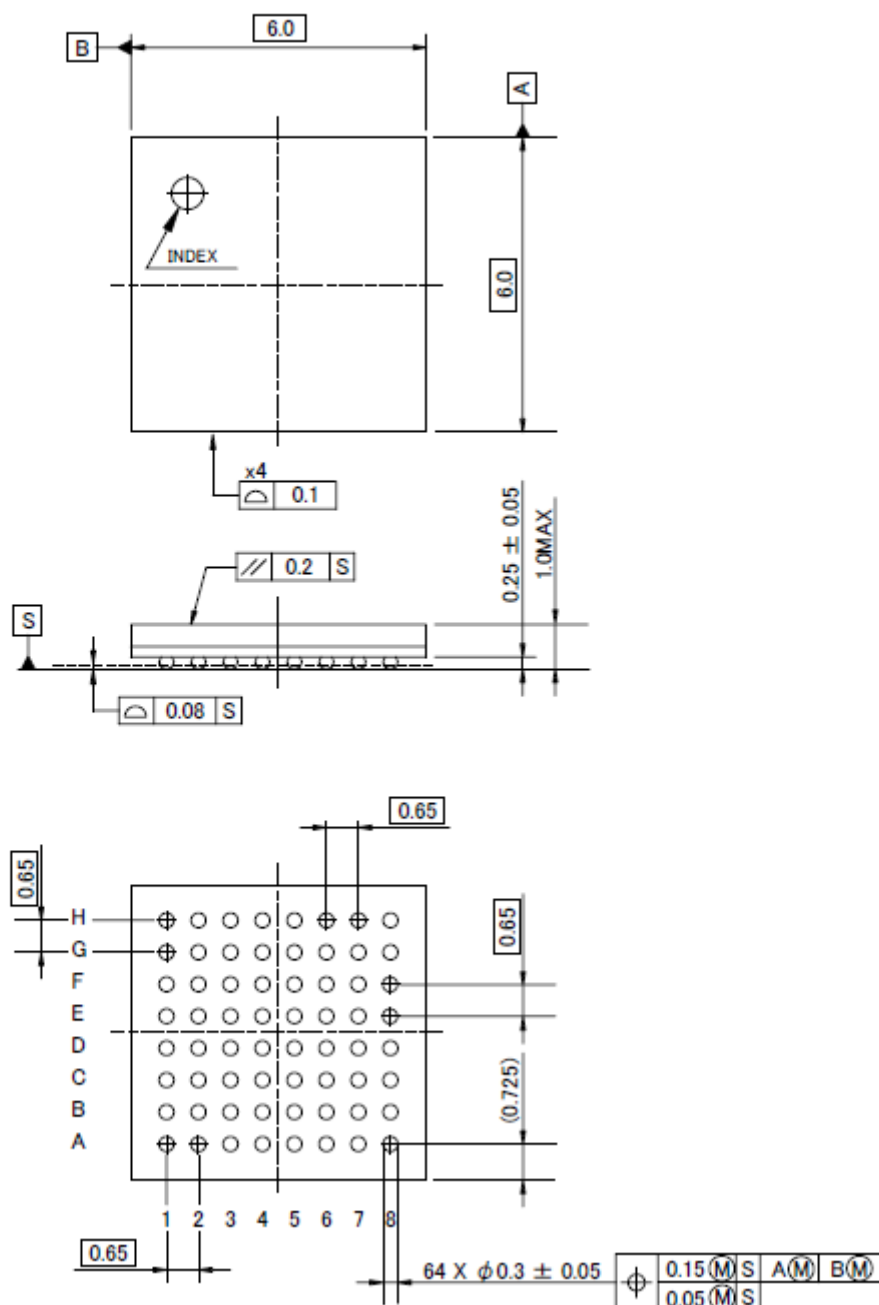
Table 4.2 TC358771XBG BGA49 Pin Count Summary

Group Name	Pin Count	Notes
DSI-RX IF	14	Include DSI Power & Ground
LVDS-TX IF	16	Include LVDS Power & Ground
I ² C IF	2	-
GPIO	3	-
PWM	1	-
SYSTEM	13	Include Power & Ground
Total Pin Count	49	

5. Package

P-VFBGA64-0606-0.65-001

"Unit : mm"

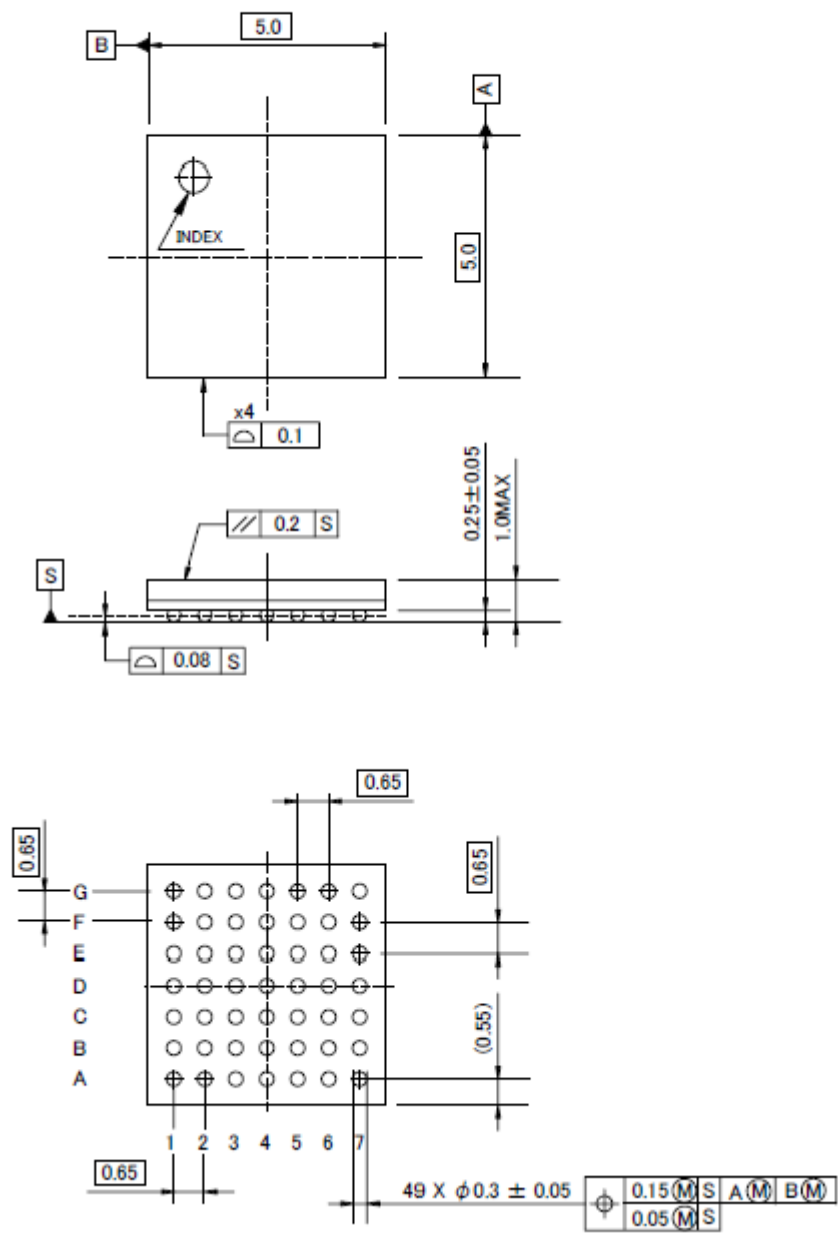


Weight: 47mg (Typ.)

Figure 5.1 P-VFBGA64-0606-0.65-001 (TC358772XBG) Package Drawing

P-VFBGA49-0505-0.65-001

Unit:mm



Weight: 31 mg (Typ.)

Figure 5.2 P-VFBGA49-0505-0.65-001 (TC358771XBG) Package Drawing

Table 5.1 Information Summary

	TC358772XBG Package	TC358771XBG Package
Package Type	VFBGA	VFBGA
Ball Diameter	0.3 mm	0.3mm
Ball Pitch	0.65 mm	0.65 mm
Body Size	6 mm × 6 mm	5 mm × 5 mm
Thickness	1 mm	1 mm

6. Electrical characteristics

6.1. Absolute Maximum Ratings

All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

Table 6.1 Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	-0.3 to +3.9	V
Supply voltage (1.2V – Digital Core)	VDDC	-0.3 to +1.8	V
Supply voltage (1.2V – MIPI DSI PHY)	VDD_MIPI	-0.3 to +1.8	V
Supply voltage (1.8V – LVDS PHY)	VDD_LVDS1_18, VDD_LVDS2_18	-0.3 to +3.9	V
Supply voltage (1.2V – LVDS PHY)	VDD_LVDS1_12 VDD_LVDS2_12	-0.3 to +1.8	V
Input voltage (DSI I/O)	V _{IN_DSI}	-0.3 to VDD_MIPI+0.3	V
Output voltage (DSI I/O)	V _{OUT_DSI}	-0.3 to VDD_MIPI+0.3	V
Input voltage (Digital IO)	V _{IN_IO}	-0.3 to VDDIO+0.3	V
Output voltage (Digital IO)	V _{OUT_IO}	-0.3 to VDDIO+0.3	V
Output voltage (LVDS Driver)	V _{OUT_LVDS}	-0.3 to VDD_LVDS_18+0.3	V
Input current	I _{in}	-10 to +10	mA
Storage temperature	T _{stg}	-40 to +125	°C

6.2. Operating Conditions

Table 6.2 Operating Conditions

Parameter	Symbol	Min	Typ.	Max	Unit
Supply voltage (1.8V – Digital IO)	VDDIO	1.7	1.8	1.9	V
Supply voltage (3.3V – Digital IO)	VDDIO	3.0	3.3	3.6	V
Supply voltage (1.2V – Digital Core)	VDDC	1.1	1.2	1.3	V
Supply voltage (1.2V – LVDS PHY)	VDD_LVDS_12	1.1	1.2	1.3	V
Supply voltage (1.8V – LVDS PHY)	VDD_LVDS_18	1.7	1.8	1.9	V
Supply voltage (1.2V – MIPI-DSI PHY)	VDD_MIPI	1.1	1.2	1.3	V
Operating internal frequency	fopr	-	-	150	MHz
Operating temperature (ambient temperature with voltage applied)	T _a	-30	+25	+85	°C

7. Revision History

Table 7.1 Revision History

Revision	Date	Description
0.31	2014-04-21	Newly released
0.312	2016-04-01	Package's weight is rounding up digits after the decimal point to form an integer.
1.0	2017-10-31	Added note to Table 4.1 and Table 4.2. Changed header, footer and the last page. Changed corporate name.

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as "TOSHIBA". Hardware, software and systems described in this document are collectively referred to as "Product".

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE").** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**