MachXO4 Family

Data Sheet

FPGA-DS-02125-1.0

December 2025

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Abbreviations in This Document

A list of abbreviations used in this document.

Abbreviation	Definition
AES	Advanced Encryption Standard
BGA	Ball Grid Array
caBGA	ChipArray Ball Grill Array
csfBGA	Chip Scale Flip-Chip Ball Grid Array
CE	Clock Enable
CLK	System clock
CMOS	Complementary Metal Oxide Semiconductor
DDR	Double Data Rate
EBR	Embedded Block RAM
ECDSA	Elliptic Curve Digital Signature Algorithm
ECLK	Edge Clock
FCIN	Fast Carry In
FCO	Fast Carry Out
I2C	Inter-Integrated Circuit
IP	Intellectual Property
I/O	Input/Output
JTAG	Joint Test Action Group
LED	Light-emitting Diode
LSR	Local Set/Reset
LUT	Look-Up Table
LVCMOS	Low-Voltage CMOS
LVDS	Low-Voltage Differential Signaling
LVPECL	Low-Voltage Positive/Pseudo Emitter-Coupled Logic
LVTTL	Low Voltage Transistor to Transistor Logic
MIPI	Mobile Industry Processor Interface
MLVDS	Multipoint Low-Voltage Differential Signaling
PCI	Peripheral Component Interconnect
PCLK	Primary Clock
PDPR	Pseudo Dual Port RAM
PFU	Programmable Functional Unit
PIC	Programmable Interface Controllers
PIO	Programmed Input/Output
PLD	Programmable Logic Device
PLL	Phase Locked Loop
RAM	Random Access Memory
ROM	Read-only Memory
SDR	Single Data Rate
SHA	Secure Hash Algorithm
SPI	Serial Peripheral Interface
SPR	Single Port Random Access Memory
SRAM	Static Random Access Memory
TransFR™	Transparent Field Reconfiguration
UFM	User Flash Memory
WLCSP	Wafer Level Chip Scale Package

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1. Introduction

The MachXO4™ family of ultra-low-density and low-power FPGAs support advanced programmable bridging and I/O expansion, making it ideal for a variety of applications in consumer electronics, computing and storage, wireless communications, industrial control, and automotive systems. It offers exceptional I/O density and a wide range of programmability options with integrated support for the latest industry-standard I/O interfaces.

The MachXO4 family consists of low-power, instant-on, non-volatile, and Flash-based FPGAs with six devices, featuring densities ranging from 896 to 9400 Look-Up Tables (LUTs). These devices include LUT-based programmable logic, Embedded Block RAM (EBR), Distributed RAM, User Flash Memory (UFM), Phase Locked Loops (PLLs), pre-engineered source synchronous I/O support, advanced configuration support including dual-boot capability, and hardened versions of commonly used functions such as SPI controller, I2C controller, and timer/counter.

Built on a 65 nm non-volatile low-power process, MachXO4 devices offer several architectural features to manage static and dynamic power consumption including programmable low swing differential I/O, the ability to turn off I/O banks, and dynamically controlled on-chip PLLs and oscillators.

The MachXO4 devices come in high-performance version, HC and HE. The high-performance devices are available in two speed grades, –5 and –6, with –6 being faster. HC devices have an internal linear voltage regulator supporting external VCC supply voltages of 3.3 V or 2.5 V, while HE devices accept only 1.2 V as the external VCC supply voltage. All HC and HE parts are functionally and pin-compatible.

These FPGAs are available in a range of advanced halogen-free packages, from the compact 2.5 x 2.5 mm WLCSP to the 20 x 20 mm TQFP, supporting density migration within the same package. Table 1.2 shows the logic densities, package, and I/O options, along with other key parameters.

The MachXO4 devices also provide enhanced I/O features such as drive strength control, slew rate control, PCI compatibility, bus-keeper latches, pull-up resistors, pull-down resistors, open drain outputs, and hot socketing. Pull-up, pull-down, and bus-keeper features are controllable on a per-pin basis.

Additionally, a user-programmable internal oscillator is included in MachXO4 devices. The clock output from this oscillator may be divisible by the timer/counter and can be used as a clock input in functions such as LED control, keyboard scanning, and similar state machines.

These devices also offer flexible, reliable, and secure configuration from on-chip Flash with encryption and authentication options. They can configure themselves from external SPI Flash or be configured by an external master through the JTAG test access port or the SPI/I2C port. Moreover, MachXO4 devices support dual-boot capability using external Flash memory and remote field upgrade TransFR capability.

Meanwhile, Lattice Radiant™ design software allows large complex user designs to be efficiently implemented on the MachXO4 FPGA family. Synthesis library support for these devices is available for popular logic synthesis tools. Radiant tools use the synthesis tool output along with constraints from its floor planning tools, to place and route the user design in a MachXO4 device. The tools extract timing from the routing and back-annotate it into the design for timing verification. Lattice Semiconductor provides many pre-engineered Intellectual Property (IP) modules for the MachXO4 family. By using these configurable soft IP cores as standardized blocks, designers can concentrate on the unique aspects of their design, increasing productivity.

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Table 1.1. Specification Status for MachXO4 Family Devices

Device	Variant	Package	Grade	Status
LFMXO4-010	HC	TSG100, BSG132, and TSG144	Commercial/Industrial/Automotive	Production
	HE	TSG100, BSG132, and TSG144	Commercial/Industrial/Automotive	Production
LFMXO4-015	HC	TSG100, BSG132, TSG144, BBG256, and BFG256	Commercial/Industrial/Automotive	Production
	HE	TSG100, BSG132, TSG144, BBG256, BFG256, and UUG36	Commercial/Industrial/Automotive	Production
LFMXO4-025	HC	TSG100, BSG132, TSG144, BBG256, and BFG256	Commercial/Industrial/Automotive	Production
	HE	TSG100, BSG132, TSG144, BBG256, BFG256, and UUG49	Commercial/Industrial/Automotive	Production
LFMXO4-050	HC	BSG132, TSG144, BBG256, BBG400, and BFG256	Commercial/Industrial/Automotive	Production
	HE	BSG132, TSG144, BBG256, BBG400, BFG256, and UUG81	Commercial/Industrial/Automotive	Production
LFMXO4-080	HC	BBG256 and BBG400	Commercial/Industrial	Production
	HE	BBG256 and BBG400	Commercial/Industrial	Production
LFMXO4-110	HC	BBG256, BBG400, and BBG484	Commercial/Industrial	Production
	HE	BBG256, BBG400, and BBG484	Commercial/Industrial	Production

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1.1. Features

1.1.1. Low Power and Programmable Architecture

- Logic density ranging from 896 to 9.4k LUT4
- 64 to 432 kb of Embedded Block Memory (EBR)
- Up to 54 kb of Distributed RAM
- Dedicated FIFO control logic
- Advanced 65 nm low power process
- Programmable low swing differential I/O
- Stand-by mode and other power-saving options

1.1.2. High Performance, Flexible I/O Buffer

- Programmable sysI/O™ buffer supports a wide range of interfaces:
  - LVCMOS 3.3/2.5/1.8/1.5/1.2/1.0
  - LVTTL
  - LVDS, Bus-LVDS, MLVDS, LVPECL
  - MIPI D-PHY Emulated
  - Schmitt trigger inputs, up to 0.5 V hysteresis
- I/O support hot socketing
- On-chip differential termination
- Programmable pull-up or pull-down mode

1.1.3. Pre-Engineered Source Synchronous I/O

- DDR registers in I/O cells
- Dedicated gearing logic
- 7:1 Gearing for Display I/O
- Generic DDR, DDRx2, DDRx4

1.1.4. Broad Range of Advanced Packaging

- Compact packages with high I/O-to-LUT ratio up to 382 I/O pins
- 0.4 mm pitch: 1280 to 4320 LUTs in very small footprint WLCSP (2.5 × 2.5 mm to 3.8 × 3.8 mm) with 27 to 62 I/O
- 0.5 mm pitch: 896 to 4320 LUTs in 8 x 8 mm BGA to 20 x 20 mm TQFP packages with up to 112 I/O
- 0.8 mm pitch: 1280 to 9400 LUTs in 14 x 14 mm to 19 x 19 mm BGA packages with up to 382 I/O
- 1.0 mm pitch: 1280 to 4320 LUTs in 17 x 17 mm BGA package with 204 I/O

1.1.5. Non-volatile, Multi-time Reconfigurable

- Instant-on; Powers up in milliseconds
- Optional dual boot with external SPI memory
- Single-chip, secure solution
- Programmable through JTAG, SPI or I2C
- Reconfigurable Flash up to 100,000 write/erase cycles for commercial/industrial devices and 10,000 write/erase cycles for automotive devices
- Supports background programming of non-volatile memory
- In-field logic update while I/O holds the system state through TransFR reconfiguration

1.1.6. Optimizable On-Chip Clocking

- On-chip oscillator with 5.5% accuracy for commercial/industrial devices
- Eight primary clocks
- Up to two edge clocks for high-speed I/O interfaces, top and bottom sides only
- Up to two analog PLLs per device with fractional-n frequency synthesis
- Wide input frequency range, 7 MHz to 400 MHz

1.1.7. Enhanced System-Level Support

- On-chip hardened functions: SPI, I2C, and timer/counter
- Unique TraceID for system tracking
- Single power supply with extended operating range
- IEEE Standard 1149.1 boundary scan
- IEEE 1532 compliant in-system programming

1.1.8. State-of-the-Art Design Software

- MachXO4 device is supported in Lattice Radiant
- Industry-leading RTL language support for VHDL, VHDL-2008, Verilog, and SystemVerilog
- Advanced scripting capability on command-line and TCL design flow
- One-click compilation flow and cross-probing between analysis tools
- Embedded timing and logic analyzer

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Table 1.2. MachXO4 Family Selection Guide

Features		LFMXO4-010	LFMXO4-015	LFMXO4-025	LFMXO4-050	LFMXO4-080	LFMXO4-110
LUTs		896	1280	2112	4320	6864[4]	9400[4]
Logic Cells		1100	1600	2600	5200	8300	11300
Distributed RAM (kb)		10	10	16	34	54	73
Embedded RAM (kb)		64	64	74	92	240	432
Embedded RAM (M9k Blocks)		7	7	8	10	26	48
User Flash Memory (kb)		64	64	80	96	256	448
Device Options	HC[1]	Yes	Yes	Yes	Yes	Yes	Yes
	HE[2]	Yes	Yes	Yes	Yes	Yes	Yes
Number of PLLs		1	1	1	2	2	2
Hardened Functions	I2C	2	2	2	2	2	2
	SPI	1	1	1	1	1	1
	Timer/Counter	1	1	1	1	1	1
	Oscillator	1	1	1	1	1	1
MIPI D-PHY Support		Yes	Yes	Yes	Yes	Yes	Yes
Automotive Qualified		Yes	Yes	Yes	Yes	No	No

Packages	Total I/O Count					
36-ball WLCSP[3] (2.5 mm x 2.5 mm, 0.4 mm)		27				
49-ball WLCSP[3] (3.2 mm x 3.2 mm, 0.4 mm)			37			
81-ball WLCSP[3] (3.8 mm x 3.8 mm, 0.4 mm)				62		
100-pin TQFP (14 mm x 14 mm, 0.5 mm)	78[5]	78[5]	78[5]			
132-ball csBGA (8 mm x 8 mm, 0.5 mm)	102[5]	102[5]	102[5]	102[5]		
144-pin TQFP (20 mm x 20 mm, 0.5 mm)	105	105	109	112		
256-ball caBGA (14 mm x 14 mm, 0.8 mm)		204[5]	204[5]	204[5]	204	204
400-ball caBGA (17 mm x 17 mm, 0.8 mm)				333	333	333
484-ball caBGA (19 mm x 19 mm, 0.8 mm)						382
256-ball ftBGA (17 mm x 17 mm, 1.0 mm)		204	204	204		

Notes:

1. High performance with regulator, VCC = 2.5 V/3.3 V.
2. High performance without regulator, VCC = 1.2 V.
3. Package is only available for E = 1.2 V devices.
4. Refer to Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409) for determination of safe ambient operating conditions.
5. Package is available for automotive devices, HC and HE variants.

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2. Architecture

2.1. Architecture Overview

The MachXO4 family architecture contains an array of logic blocks surrounded by Programmable I/O (PIO). All logic density devices in this family have sysCLOCK™ PLLs and blocks of sysMEM Embedded Block RAM (EBRs). Figure 2.1 and Figure 2.2 show the block diagrams of the various family members.

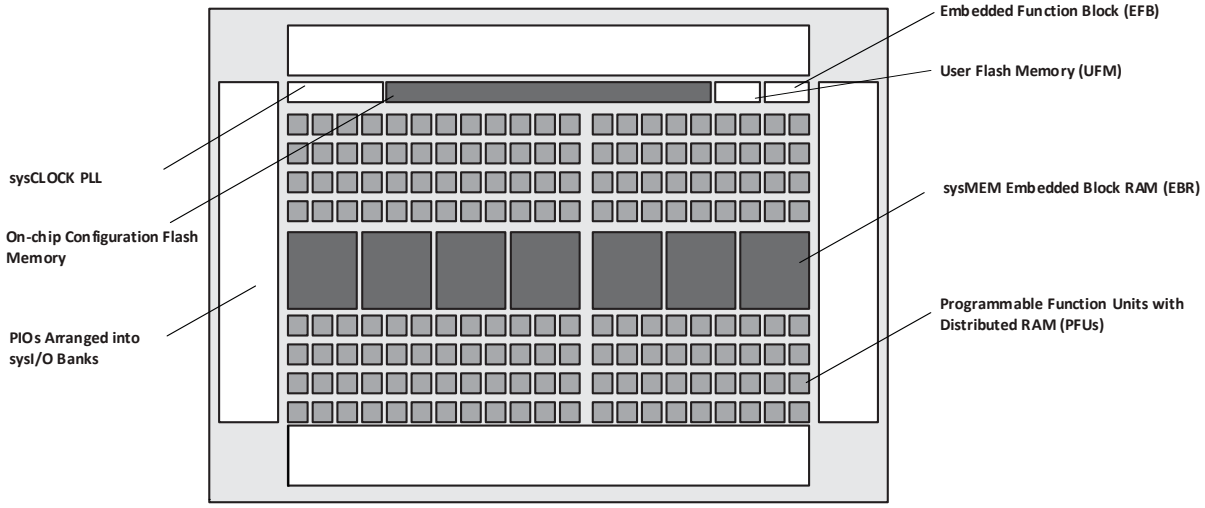
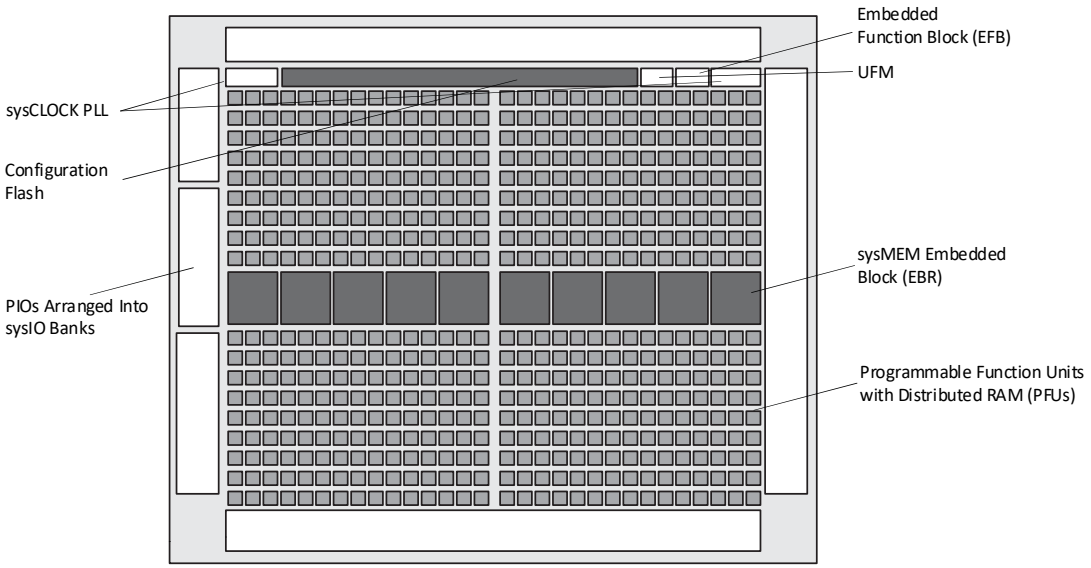


Figure 2.1. Top View of the LFMXO4-015 Part

Notes:

- LFMXO4-010 part is similar to LFMXO4-015 part.
- LFMXO4-010 has a lower LUT count.



Notes:
• MachXO4-025, MachXO4-080 and MachXO4-110 are similar to MachXO4-050. MachXO4-025 has a lower LUT count, one PLL, and eight EBR blocks.
• MachXO4-080 has a higher LUT count, two PLLs, and 26 EBR blocks. MachXO4-110 has a higher LUT count, two PLLs, and 48 EBR blocks.

Figure 2.2. Top View of the LFMXO4-050 Part

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The logic blocks, Programmable Functional Unit (PFU) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each row has either the logic blocks or the EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PFU contains the building blocks for logic, arithmetic, RAM, ROM, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysI/O buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the MachXO4 family, the number of sysI/O banks varies by device. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO. FIFO support includes dedicated FIFO pointer and flag “hard” control logic to minimize LUT usage.

The MachXO4 registers in PFU and sysI/O can be configured to be SET or RESET. After power up and device is configured, the device enters into user mode with these registers SET/RESET according to the configuration set-ting, allowing device entering to a known state for predictable system function.

The MachXO4 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. These blocks are located at the ends of the on-chip Flash block. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

MachXO4 devices provide commonly used hardened functions such as SPI controller, I^2C controller and timer/ counter.

MachXO4 devices also provide User Flash Memory (UFM). These hardened functions and the UFM interface to the core logic and routing through a WISHBONE interface. The UFM can also be accessed through the SPI, I^2C and JTAG ports.

Every device in the family has a JTAG port that supports programming and configuration of the device as well as access to the user logic. The MachXO4 devices are available for operation from 3.3 V, 2.5 V and 1.2 V power supplies, providing easy integration into the overall system.

2.2. PFU Blocks

The core of the MachXO4 device consists of PFU blocks, which can be programmed to perform logic, arithmetic, distributed RAM and distributed ROM functions. Each PFU block consists of four interconnected slices numbered 0 to 3 as shown in Figure 2.3. Each slice contains two LUTs and two registers. There are 53 inputs and 25 outputs associated with each PFU block.

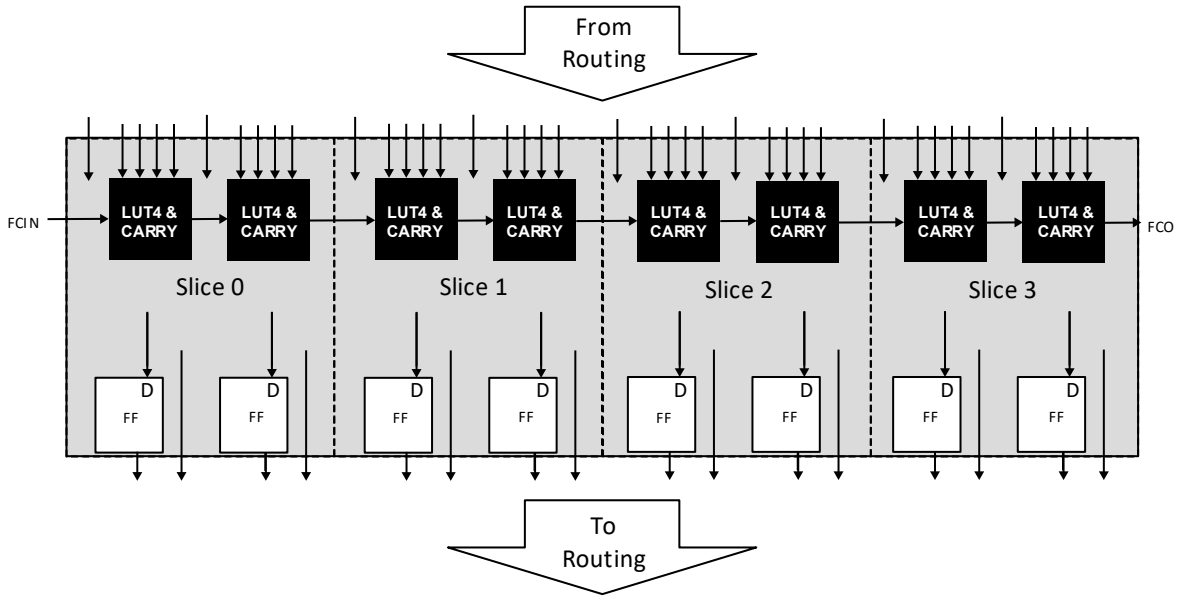

Figure 2.3. PFU Block Diagram

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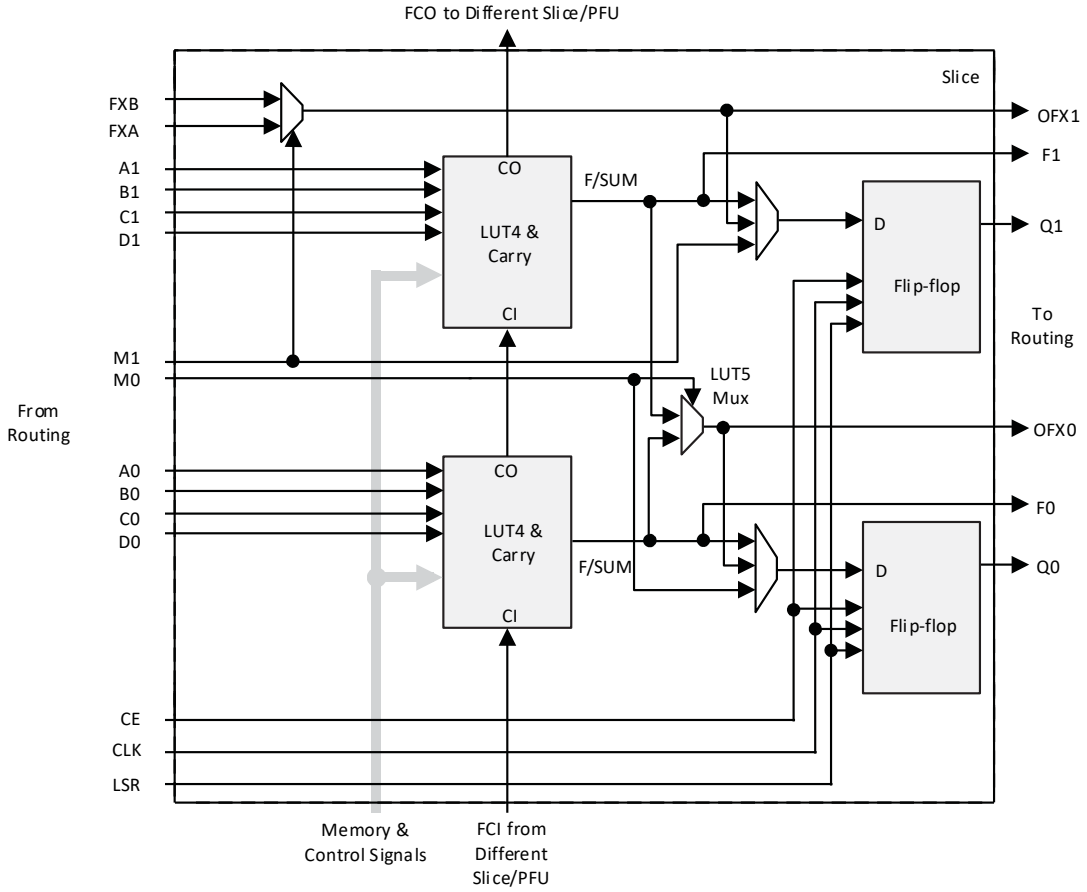
2.2.1. Slices

Slices 0-3 contain two LUT4s feeding two registers. Slices 0-2 can be configured as distributed memory. Table 2.1 shows the capability of the slices in PFU blocks along with the operation modes they enable. The control logic performs set/reset functions (programmable as synchronous/ asynchronous), clock select, chip select and wider RAM/ROM functions.

Table 2.1. Resources and Modes Available per Slice

Slice	PFU Block	
	Resources	Modes
Slice 0	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 1	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 2	2 LUT4s and 2 Registers	Logic, Ripple, RAM, ROM
Slice 3	2 LUT4s and 2 Registers	Logic, Ripple, ROM

Figure 2.4 shows an overview of the internal logic of the slice. The registers in the slice can be configured for positive/ negative and edge triggered or level sensitive clocks. All slices have 15 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six for routing and one to carry-chain (to the adjacent PFU). Table 2.2 lists the signals associated with Slices 0-3.



For Slices 0 and 1, memory control signals are generated from Slice 2 as follows:

- WCK is CLK
- WRE is from LSR
- DI [3:2] for Slice 1 and DI [1:0] for Slice 0 data from Slice 2
- WAD [A:D] is a 4-bit address from slice 2 LUT input

Figure 2.4. Slice Diagram

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Table 2.2. Slice Signal Descriptions

Function	Type	Signal Names	Description
Input	Data signal	A0, B0, C0, D0	Inputs to LUT4
Input	Data signal	A1, B1, C1, D1	Inputs to LUT4
Input	Multi-purpose	M0/M1	Multi-purpose input
Input	Control signal	CE	Clock enable
Input	Control signal	LSR	Local set/reset
Input	Control signal	CLK	System clock
Input	Inter-PFU signal	FCIN	Fast carry in[1]
Output	Data signals	F0, F1	LUT4 output register bypass signals
Output	Data signals	Q0, Q1	Register outputs
Output	Data signals	OFX0	Output of a LUT5 MUX
Output	Data signals	OFX1	Output of a LUT6, LUT7, LUT8[2] MUX depending on the slice
Output	Inter-PFU signal	FCO	Fast carry out[1]

Notes:
1. See Figure 2.3 for connection details.
2. Requires two PFUs.

2.2.2. Modes of Operation

Each slice has up to four potential modes of operation: Logic, Ripple, RAM and ROM.

2.2.2.1. Logic Mode

In this mode, the LUTs in each slice are configured as 4-input combinatorial lookup tables. A LUT4 can have 16 possible input combinations. Any four input logic functions can be generated by programming this lookup table. Since there are two LUT4s per slice, a LUT5 can be constructed within one slice. Larger look-up tables such as LUT6, LUT7 and LUT8 can be constructed by concatenating other slices. Note LUT8 requires more than four slices.

2.2.2.2. Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. In Ripple mode, the following functions can be implemented by each slice:

- Addition 2-bit
- Subtraction 2-bit
- Add/subtract 2-bit using dynamic control
- Up counter 2-bit
- Down counter 2-bit
- Up/down counter with asynchronous clear
- Up/down counter with preload (sync)
- Ripple mode multiplier building block
- Multiplier support
- Comparator functions of A and B inputs
- A greater-than-or-equal-to B
- A not-equal-to B
- A less-than-or-equal-to B

Ripple mode includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2 mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per-slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

2.2.3. RAM Mode

In this mode, a 16x4-bit distributed single port RAM (SPR) can be constructed by using each LUT block in Slice 0 and Slice 1 as a 16x1-bit memory. Slice 2 is used to provide memory address and control signals.

MachXO4 devices support distributed memory initialization.

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The Lattice design tools support the creation of a variety of different size memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.3 shows the number of slices required to implement different distributed RAM primitives. For more information about using RAM in MachXO4 devices, see MachXO4 Memory User Guide (FPGA-TN-02402).

Table 2.3. Number of Slices Required For Implementing Distributed RAM

	SPR 16 x 4	PDPR 16 x 4
Number of slices	3	3

Note: SPR = Single Pot RAM, PDPR = Pseudo Dual Port RAM

2.2.4. ROM Mode

ROM mode uses the LUT logic; hence, slices 0-3 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information on the RAM and ROM modes, refer to MachXO4 Memory User Guide (FPGA-TN-02402).

2.3. Routing

There are many resources provided in the MachXO4 devices to route signals individually or as buses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PFU connections are made with three different types of routing resources: x1 (spans two PFUs), x2 (spans three PFUs) and x6 (spans seven PFUs). The x1, x2, and x6 connections provide fast and efficient connections in the horizontal and vertical directions.

The design tools take the output of the synthesis tool and places and routes the design. Generally, the place and route tool is completely automatic, although an interactive routing editor is available to optimize the design.

2.4. Clock/Control Distribution Network

Each MachXO4 device has eight clock inputs (PCLK [T, C] [Banknum]_[2..0]) – three pins on the left side, two pins each on the bottom and top sides and one pin on the right side. These clock inputs drive the clock nets. These eight inputs can be differential or single-ended and may be used as general purpose I/O if they are not used to drive the clock nets. When using a single-ended clock input, only the PCLKT input can drive the clock tree directly.

The MachXO4 architecture has three types of clocking resources: edge clocks, primary clocks and secondary high fanout nets. MachXO4 devices have two edge clocks each on the top and bottom edges. Edge clocks are used to clock I/O registers and have low injection time and skew. Edge clock inputs are from PLL outputs, primary clock pads, edge clock bridge outputs and CIB sources.

The eight primary clock lines in the primary clock network drive throughout the entire device and can provide clocks for all resources within the device including PFUs, EBRs and PICs. In addition to the primary clock signals, MachXO4 devices also have eight secondary high fanout signals which can be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, etc. Internal logic can drive the global clock network for internally-generated global clocks and control signals.

The maximum frequency for the primary clock network is shown in the MachXO4 External Switching Characteristics table.

Primary clock signals for the LFMXO4-015 part and larger devices are generated from eight 27:1 muxes The available clock sources include eight I/O sources, 11 routing inputs, eight clock divider inputs and up to eight sysCLOCK PLL outputs.

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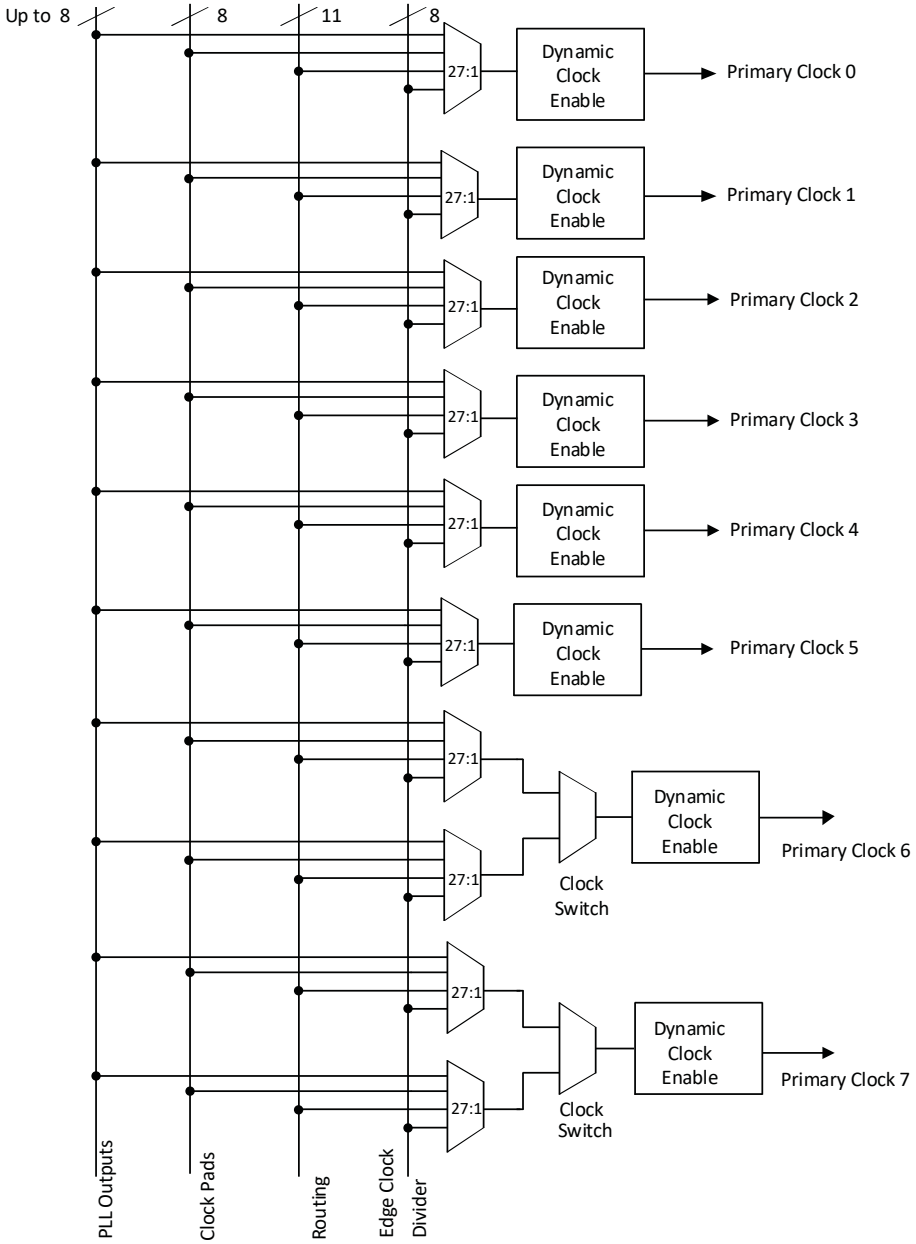

Figure 2.5. Primary Clocks for MachXO4 Devices

Eight secondary high fanout nets are generated from eight 8:1 muxes as shown in Figure 2.6. One of the eight inputs to the secondary high fanout net input mux comes from dual function clock pins and the remaining seven come from internal routing. The maximum frequency for the secondary clock network is shown in MachXO4 External Switching Characteristics table.

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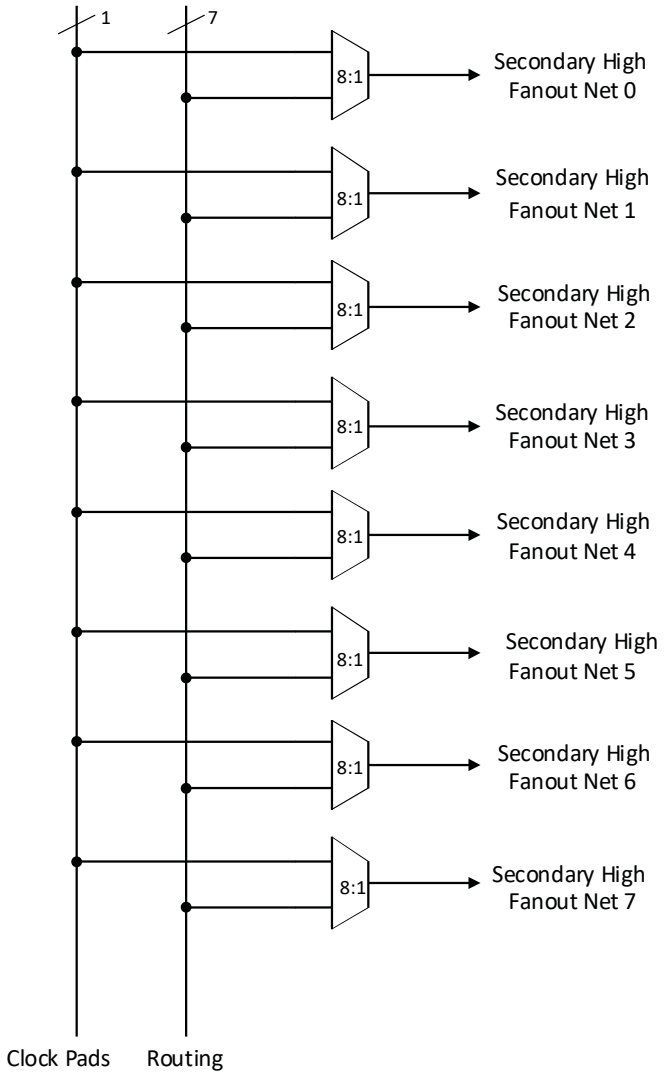

Figure 2.6. Secondary High Fanout Nets for MachXO4 Devices

2.4.1. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. All MachXO4 devices have one or more sysCLOCK PLL. CLKI is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. CLKFB is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The MachXO4 sysCLOCK PLLs support high resolution (16-bit) fractional-N synthesis. Fractional-N frequency synthesis allows the user to generate an output clock which is a non-integer multiple of the input frequency. For more information about using the PLL with Fractional-N synthesis, see MachXO4 sysCLOCK PLL Design User Guide (FPGA-TN-02391).

Each output has its own output divider, thus allowing the PLL to generate different frequencies for each output. The output dividers can have a value from 1 to 128. The output dividers may also be cascaded together to generate low frequency clocks. The CLKOP, CLKOS, CLKOS2, and CLKOS3 outputs can all be used to drive the MachXO4 clock distribution network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2.7.

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The setup and hold times of the device can be improved by programming a phase shift into the CLKOS, CLKOS2, and CLKOS3 output clocks which advance or delay the output clock with reference to the CLKOP output clock.

This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the t_{LOCK} parameter has been satisfied.

The MachXO4 also has a feature that allows the user to select between two different reference clock sources dynamically. This feature is implemented using the PLLREFCS primitive. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

The MachXO4 PLL contains a WISHBONE port feature that allows the PLL settings, including divider values, to be dynamically changed from the user logic. When using this feature the EFB block must also be instantiated in the design to allow access to the WISHBONE ports. Similar to the dynamic phase adjustment, when PLL settings are updated through the WISHBONE port the PLL may lose lock and not relock until the tLOCK parameter has been satisfied. The timing parameters for the PLL are shown in the sysCLOCK PLL Timing table.

For more details on the PLL and the WISHBONE interface, see MachXO4 sysCLOCK PLL Design User Guide (FPGA-TN-02391).

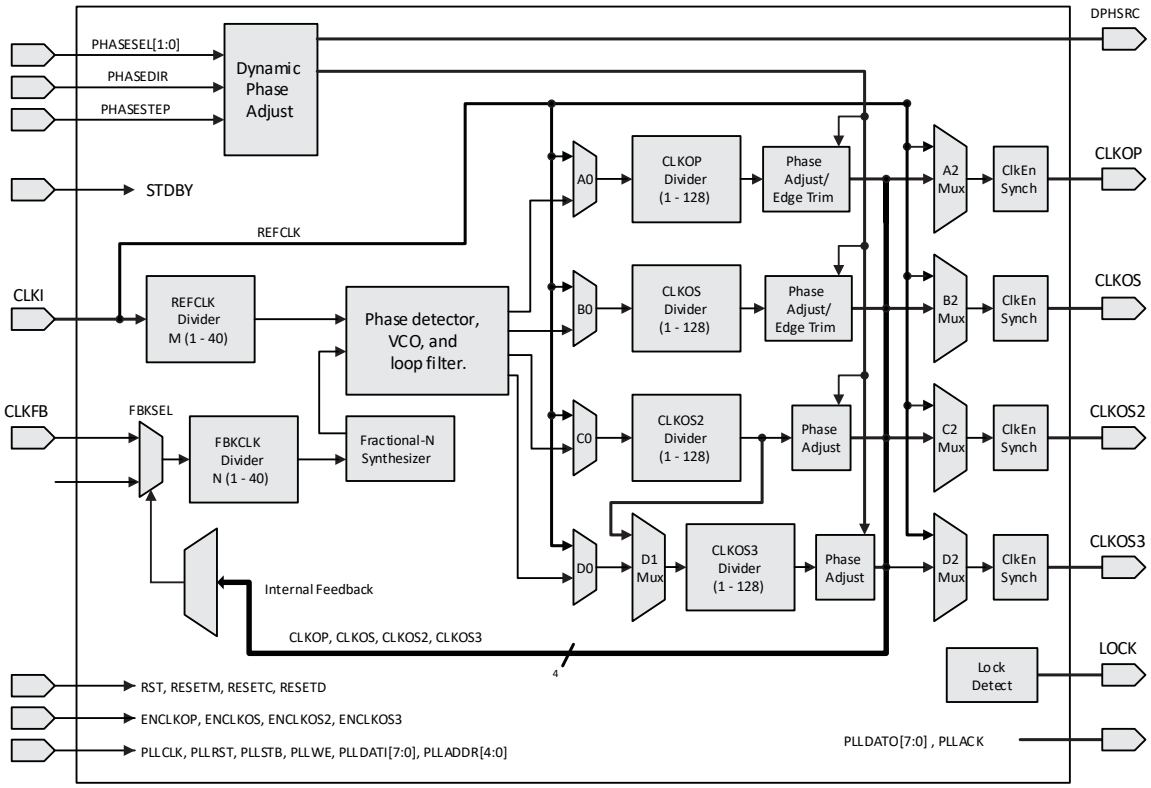

Figure 2.7. PLL Diagram

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Table 2.4 provides signal descriptions of the PLL block.

Table 2.4. PLL Signal Descriptions

Port Name	I/O	Description
CLKI	I	Input clock to PLL
CLKFB	I	Feedback clock
PHASESEL[1:0]	I	Select which output is affected by Dynamic Phase adjustment ports
PHASEDIR	I	Dynamic Phase adjustment direction
PHASESTEP	I	Dynamic Phase step – toggle shifts VCO phase adjust by one step.
CLKOP	O	Primary PLL output clock (with phase shift adjustment)
CLKOS	O	Secondary PLL output clock (with phase shift adjust)
CLKOS2	O	Secondary PLL output clock2 (with phase shift adjust)
CLKOS3	O	Secondary PLL output clock3 (with phrase shift adjust)
LOCK	O	PLL LOCK, asynchronous signal. Active high indicates PLL is locked to input and feedback signals.
DPHSRC	O	Dynamic Phase source – ports or WISHBONE is active
STDBY	I	Stand-by signal to power down the PLL
RST	I	PLL reset without resetting the M-driver. Active high reset.
RESETM	I	PLL rest – includes resetting the M-divider. Active high reset.
RESETC	I	Reset for CLKOS2 output divider only. Active high reset.
RESETD	I	Reset for CLKOS3 output divider only. Active high reset.
ENCLKOP	I	Enable PLL output CLKOP
ENCLKOS	I	Enable PLL output CLKOS when port is active
ENCLKOS2	I	Enable PLL output CLKOS2 when port is active
ENCLKOS3	I	Enable PLL output CLKOS3 when port is active
PLLCLK	I	PLL data bus clock input signal
PLLRST	I	PLL data bus reset. This resets only the data bus not any register values.
PLLSTB	I	PLL data bus strobe signal
PLLWE	I	PLL data bus write enable signal
PLLADDR [4:0]	I	PLL data bus address
PLLDATI [7:0]	I	PLL data bus data input
PLLDATO [7:0]	O	PLL data bus data output
PLLACK	O	PLL data bus acknowledge signal

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2.5. sysMEM Embedded Block RAM Memory

The MachXO4 devices contain sysMEM Embedded Block RAMs (EBRs). The EBR consists of a 9-Kbit RAM, with dedicated input and output registers. This memory can be used for a wide variety of purposes including data buffering, PROM for the soft processor and FIFO.

2.5.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port, pseudo dual port, or FIFO memories. Each block can be used in a variety of depths and widths as shown in Table 2.5.

Table 2.5. sysMEM Block Configurations

Memory Mode	Configurations
Single Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
True Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9
Pseudo Dual Port	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18
FIFO	8,192 x 1 4,096 x 2 2,048 x 4 1,024 x 9 512 x 18

2.5.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports. The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. EBR initialization data can be loaded from the Configuration Flash.

MachXO4 EBR initialization data can also be loaded from the UFM. To maximize the number of UFM bits, initialize the EBRs used in your design to an all-zero pattern. Initializing to an all-zero pattern does not use up UFM bits. MachXO4 devices have been designed such that multiple EBRs share the same initialization memory space if they are initialized to the same pattern.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

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2.5.5. Single, Dual, Pseudo-Dual Port and FIFO Modes

Figure 2.8 shows the five basic memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the memory array output.

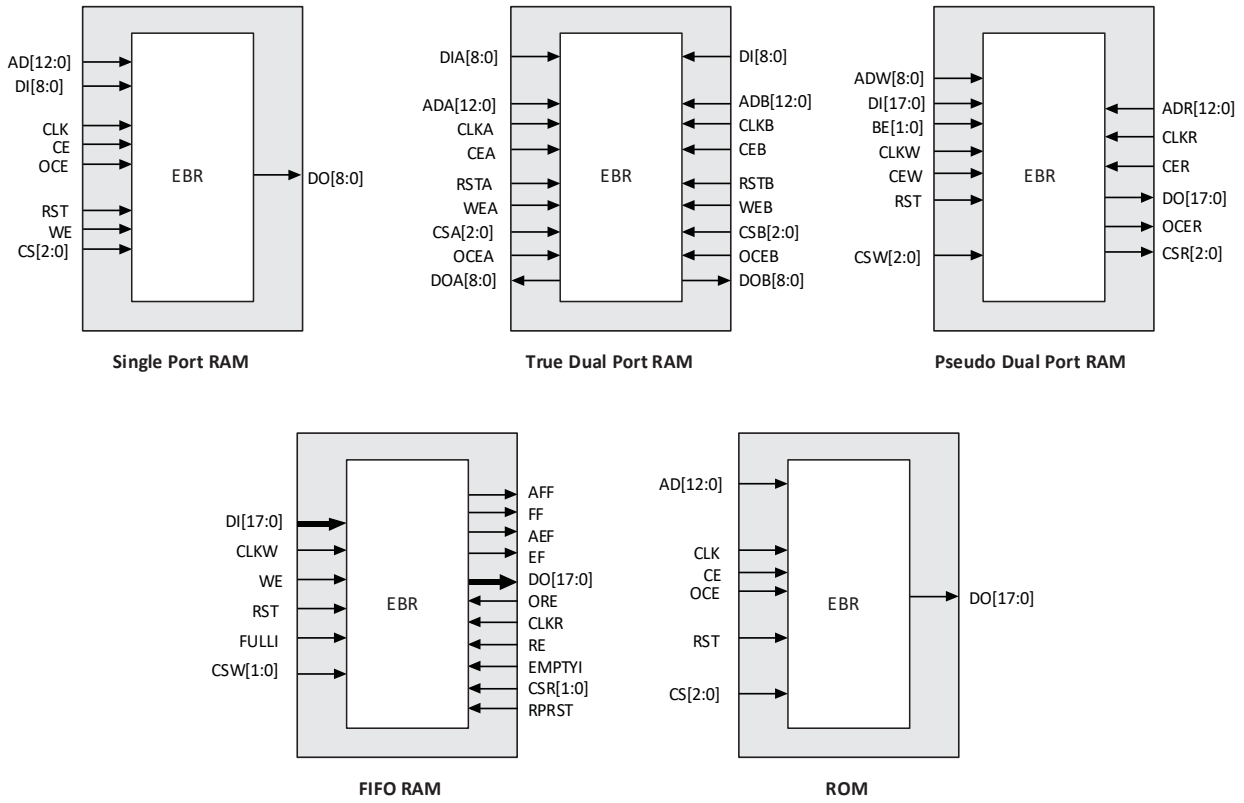

Figure 2.8. sysMEM Memory Primitives

Table 2.6. EBR Signal Descriptions

Port Name	Description	Active State
CLK	Clock	Rising Clock Edge
CE	Clock Enable	Active High
OCE1	Output Clock Enable	Active High
RST	Reset	Active High
BE1	Byte Enable	Active High
WE	Write Enable	Active High
AD	Address Bus	—
DI	Data In	—
DO	Data Out	—
CS	Chip Select	Active High
AFF	FIFO RAM Almost Full Flag	—
FF	FIFO RAM Full Flag	—
AEF	FIFO RAM Almost Empty Flag	—
EF	FIFO RAM Empty Flag	—
RPRST	FIFO RAM Read Pointer Reset	—

Notes:

1. Optional signals.

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2. For dual port EBR primitives a trailing ‘A’ or ‘B’ in the signal name specifies the EBR port A or port B respectively.
3. For FIFO RAM mode primitive, a trailing ‘R’ or ‘W’ in the signal name specifies the FIFO read port or write port respectively.
4. For FIFO RAM mode primitive, FULLI has the same function as CSW(2) and EMPTYI has the same function as CSR(2).
5. In FIFO mode, CLKW is the write port clock, CSW is the write port chip select, CLKR is the read port clock, CSR is the read port chip select, ORE is the output read enable.

The EBR memory supports three forms of write behavior for single or dual port operation:

- Normal – Data on the output appears only during the read cycle. During a write cycle, the data (at the current address) does not appear on the output. This mode is supported for all data widths.
- Write Through – A copy of the input data appears at the output of the same port. This mode is supported for all data widths.
- Read-Before-Write – When new data is being written, the old contents of the address appears at the output.

2.5.6. FIFO Configuration

The FIFO has a write port with data-in, CEW, WE and CLKW signals. There is a separate read port with data-out, RCE, RE and CLKR signals. The FIFO internally generates Almost Full, Full, Almost Empty and Empty Flags. The Full and Almost Full flags are registered with CLKW. The Empty and Almost Empty flags are registered with CLKR. Table 2.7 shows the range of programming values for these flags.

Table 2.7. Programmable FIFO Flag Ranges

Flag Name	Programming Range
Full (FF)	1 to max (up to 2^N-1)
Almost Full (AF)	1 to Full-1
Almost Empty (AE)	1 to Full-1
Empty (EF)	0

N = Address bit width.

The FIFO state machine supports two types of reset signals: RST and RPRST. The RST signal is a global reset that clears the contents of the FIFO by resetting the read/write pointer and puts the FIFO flags in their initial reset state. The RPRST signal is used to reset the read pointer. The purpose of this reset is to retransmit the data that is in the FIFO. In these applications it is important to keep careful track of when a packet is written into or read from the FIFO.

2.5.7. Memory Core Reset

The memory core contains data output latches for ports A and B. These are simple latches that can be reset synchronously or asynchronously. RSTA and RSTB are local signals, which reset the output latches associated with port A and port B respectively. The Global Reset (GSRN) signal resets both ports. The output data latches and associated resets for both ports are as shown in Figure 2.9.

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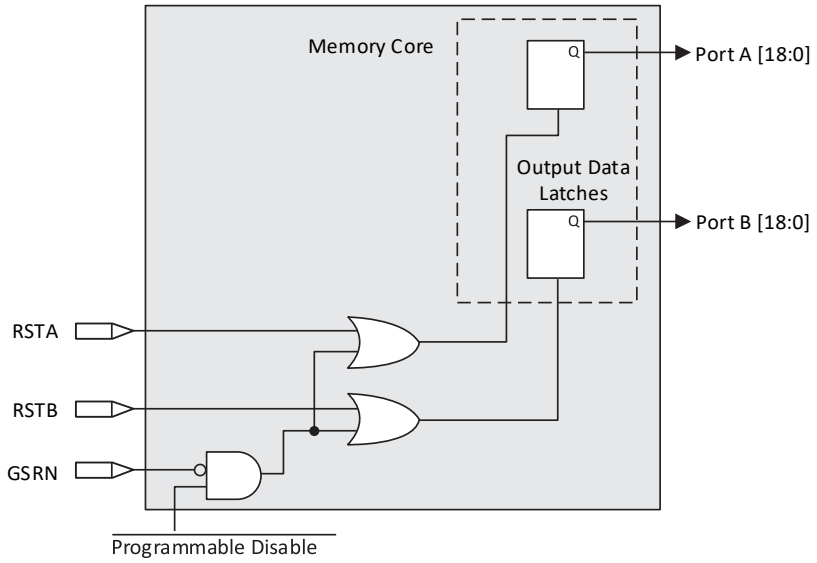

Figure 2.9. Memory Core Reset

For further information on the sysMEM EBR block, refer to MachXO4 Memory User Guide (FPGA-TN-02402).

2.5.8. EBR Asynchronous Reset

EBR asynchronous reset or GSR (if used) can only be applied if all clock enables are low for a clock cycle before the reset is applied and released a clock cycle after the reset is released, as shown in Figure 2.10. The GSR input to the EBR is always asynchronous.

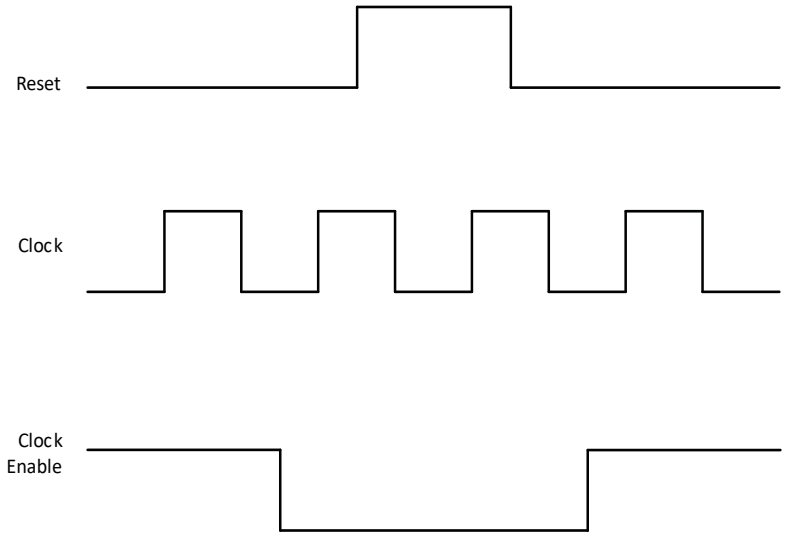

Figure 2.10. EBR Asynchronous Reset (Including GSR) Timing Diagram

If all clock enables remain enabled, the EBR asynchronous reset or GSR may only be applied and released after the EBR read and write clock inputs are in a steady state condition for a minimum of $1/f_{MAX}$ (EBR clock). The reset release must adhere to the EBR synchronous reset setup time before the next active read or write clock edge.

If an EBR is pre-loaded during configuration, the GSR input must be disabled or the release of the GSR during device wake up must occur before the release of the device I/O becoming active.

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These instructions apply to all EBR RAM, ROM and FIFO implementations. For the EBR FIFO mode, the GSR signal is always enabled and the WE and RE signals act like the clock enable signals in Figure 2.10. The reset timing rules apply to the RPReset input versus the RE input and the RST input versus the WE and RE inputs. Both RST and RPReset are always asynchronous EBR inputs. For more details refer to MachXO4 Memory User Guide (FPGA-TN-02402).

Note that there are no reset restrictions if the EBR synchronous reset is used and the EBR GSR input is disabled.

2.6. Programmable I/O Cells (PIC)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. On the MachXO4 devices, the PIO cells are assembled into groups of four PIO cells called a Programmable I/O Cell or PIC. The PICs are placed on all four sides of the device.

On all the MachXO4 devices, two adjacent PIOs can be combined to provide a complementary output driver pair.

All PIO pairs can implement differential receivers. Half of the PIO pairs on the top edge of these devices can be configured as true LVDS transmit pairs. The PIO pairs on the bottom edge of these devices have on-chip differential termination.

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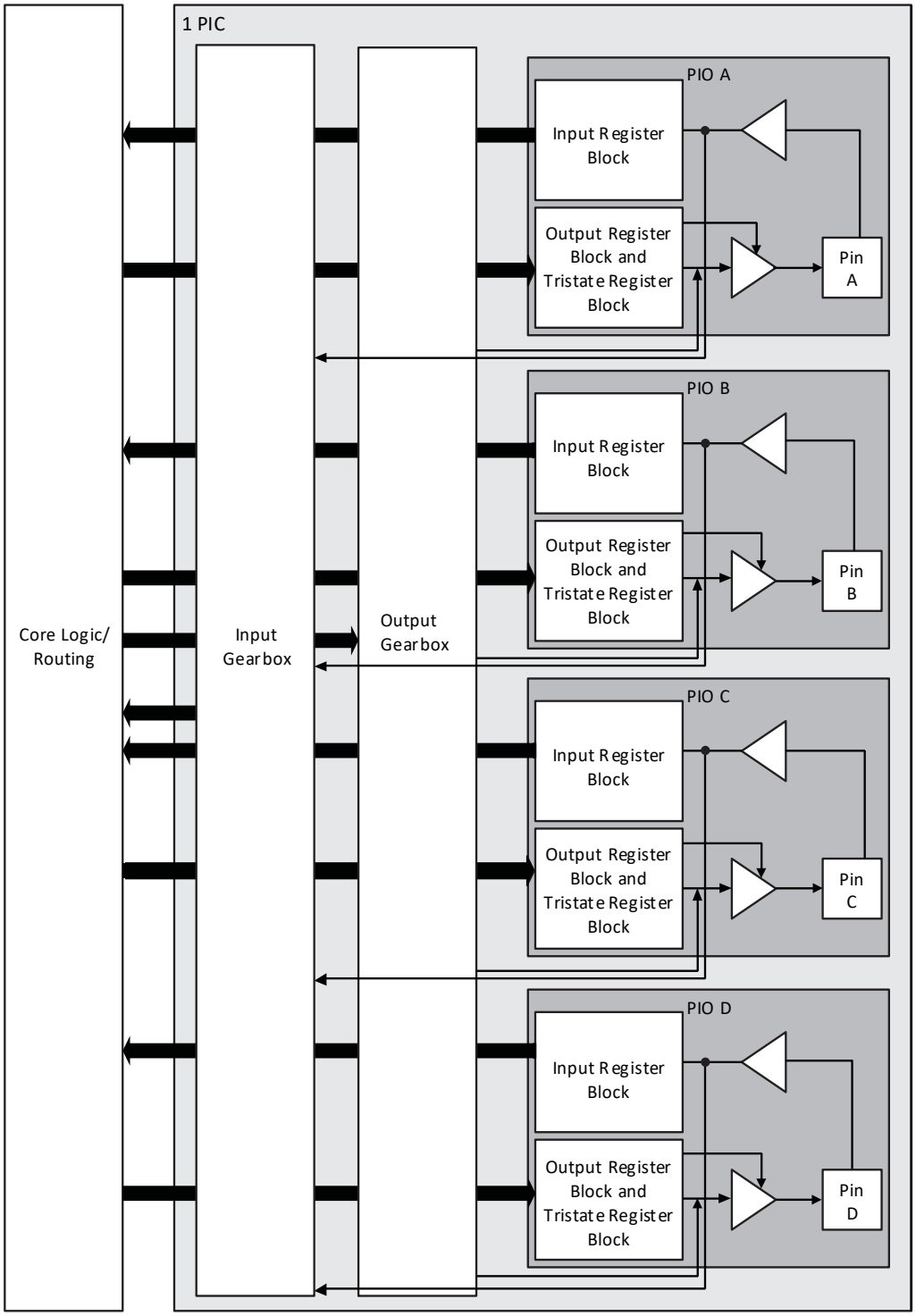

Figure 2.11. Group of Four Programmable I/O Cells

2.7. PIO

The PIO contains three blocks: an input register block, output register block and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic.

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Table 2.8. PIO Signal List

Pin Name	I/O Type	Description
CE	Input	Clock Enable
D	Input	Pin input from sysI/O buffer
INDD	Output	Register bypassed input
INCK	Output	Clock input
Q0	Output	DDR positive edge input
Q1	Output	Registered input/DDR negative edge input
D0	Input	Output signal from the core (SDR and DDR)
D1	Input	Output signal from the core (DDR)
TD	Input	Tri-state signal from the core
Q	Output	Data output signals to sysI/O Buffer
TQ	Output	Tri-state output signals to sysI/O Buffer
SCLK	Input	System clock for input and output/tri-state blocks
RST	Input	Local set reset signal

2.7.1. Input Register Block

The input register blocks for the PIOs on all edges contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core.

2.7.1.1. Left, Top, Bottom Edges

Input signals are fed from the sysI/O buffer to the input register block (as signal D). If desired, the input signal can bypass the register and delay elements and be used directly as a combinatorial signal (INDD), and a clock (INCK). If an input delay is desired, users can select a fixed delay. I/O on the bottom edge also have a dynamic delay, DEL[4:0]. The delay, if selected, reduces input register hold time requirements when using a global clock. The input block allows two modes of operation. In single data rate (SDR) the data is registered with the system clock (SCLK) by one of the registers in the single data rate sync register block. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock (SCLK) signal, creating two data streams.

2.7.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

2.7.2.1. Left, Top, Bottom Edges

In SDR mode, D0 feeds one of the flip-flops that then feeds the output.

In DDR generic mode, D0 and D1 inputs are fed into registers on the positive edge of the clock. At the next falling edge the registered D1 input is registered into the register Q1. A multiplexer running off the same clock is used to switch the mux between the outputs of registers Q0 and Q1 that then feed the output.

Figure 2.12 shows the output register block on the left, top and bottom edges.

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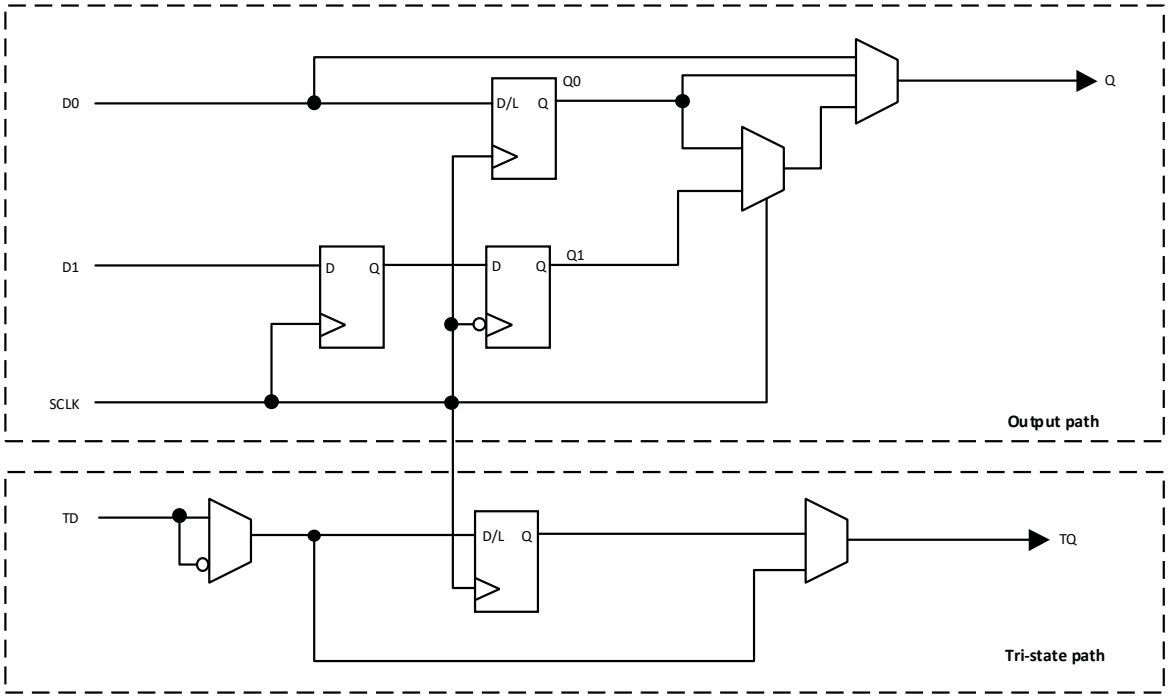

Figure 2.12. Output Register Block Diagram (PIO on the Left, Top and Bottom Edges)

2.7.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, TD input feeds one of the flip-flops that then feeds the output.

2.8. Input Gearbox

Each PIC on the bottom edge has a built-in 1:8 input gearbox. Each of these input gearboxes may be programmed as a 1:7 de-serializer or as one IDDRX4 (1:8) gearbox or as two IDDRX2 (1:4) gearboxes. Table 2.9 shows the gearbox signals.

Table 2.9. Input Gearbox Signal List

Name	I/O Type	Description
D	Input	High-speed data input after programmable delay in PIO A input register block
ALIGNWD	Input	Data alignment signal from device core
SCLK	Input	Slow-speed system clock
ECLK[1:0]	Input	High-speed edge clock
RST	Input	Reset
Q[7:0]	Output	Low-speed data to device core: Video RX(1:7): Q[6:0] GDDRX4(1:8): Q[7:0] GDDRX2(1:4)(IOL-A): Q4, Q5, Q6, Q7 GDDRX2(1:4)(IOL-C): Q0, Q1, Q2, Q3

Note:

These gearboxes have three stage pipeline registers. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals UPDATE and SEL0 from the control block. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. Figure 2.13 shows a block diagram of the input gearbox.

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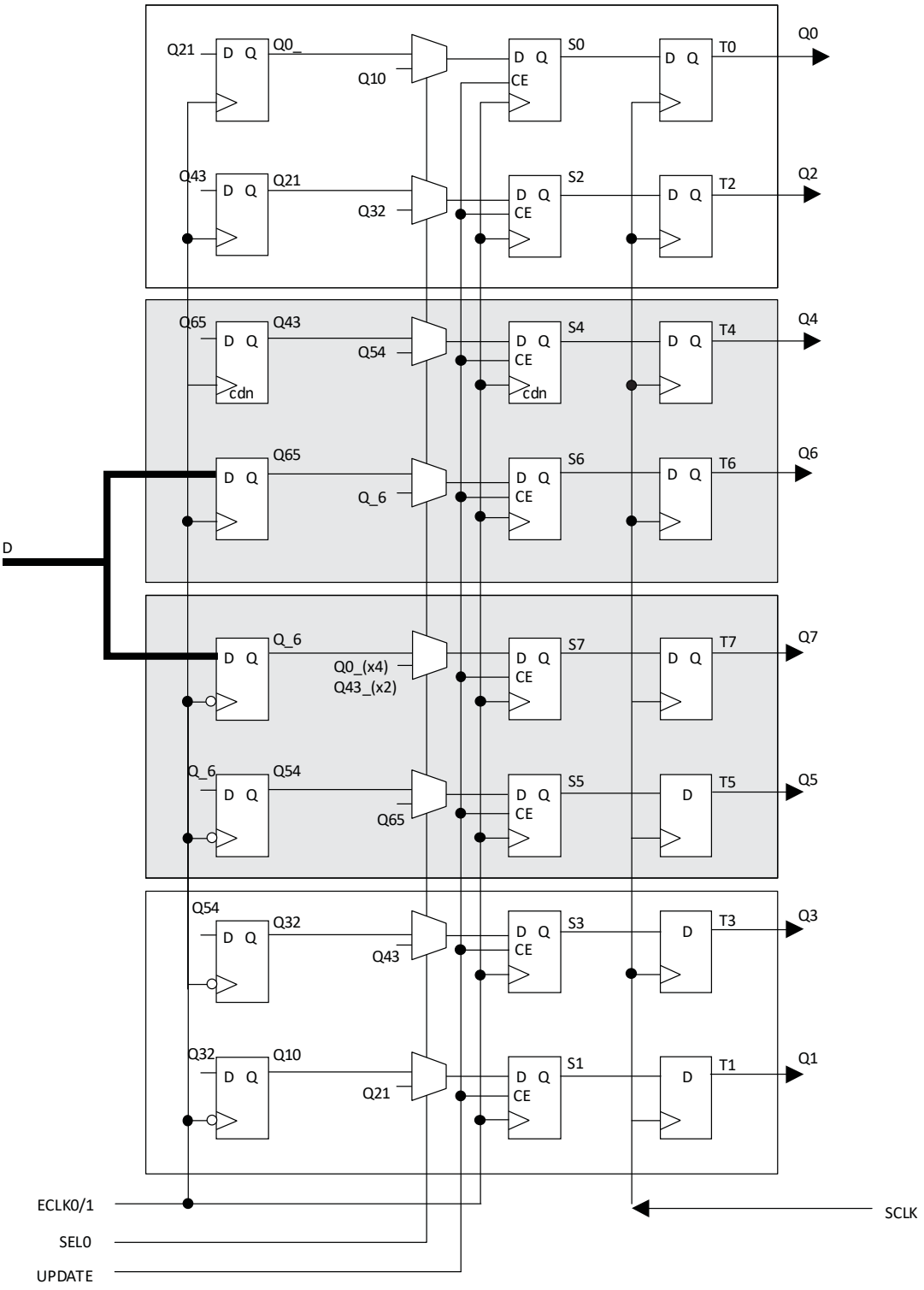

Figure 2.13. Input Gearbox

More information on the input gearbox is available in Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410).

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2.9. Output Gearbox

Each PIC on the top edge has a built-in 8:1 output gearbox. Each of these output gearboxes may be programmed as a 7:1 serializer or as one ODDRX4 (8:1) gearbox or as two ODDRX2 (4:1) gearboxes. Table 2.10 shows the gearbox signals.

Table 2.10. Output Gearbox Signal List

Name	I/O Type	Description
Q	Output	High-speed data output
D[7:0]	Input	Low-speed data from device core
Video TX(7:1): D[6:0]	—	—
GDDRX4(8:1): D[7:0]	—	—
GDDRX2(4:1)(IOL-A): D[3:0]	—	—
GDDRX2(4:1)(IOL-C): D[7:4]	—	—
SCLK	Input	Slow-speed system clock
ECLK [1:0]	Input	High-speed edge clock
RST	Input	Reset

The gearboxes have three stage pipeline registers. The first stage registers sample the low-speed input data on the low-speed system clock. The second stage registers transfer data from the low-speed clock registers to the high-speed clock registers. The third stage pipeline registers controlled by high-speed edge clock shift and mux the high-speed data out to the sysI/O buffer. Figure 2.14 shows the output gearbox block diagram.

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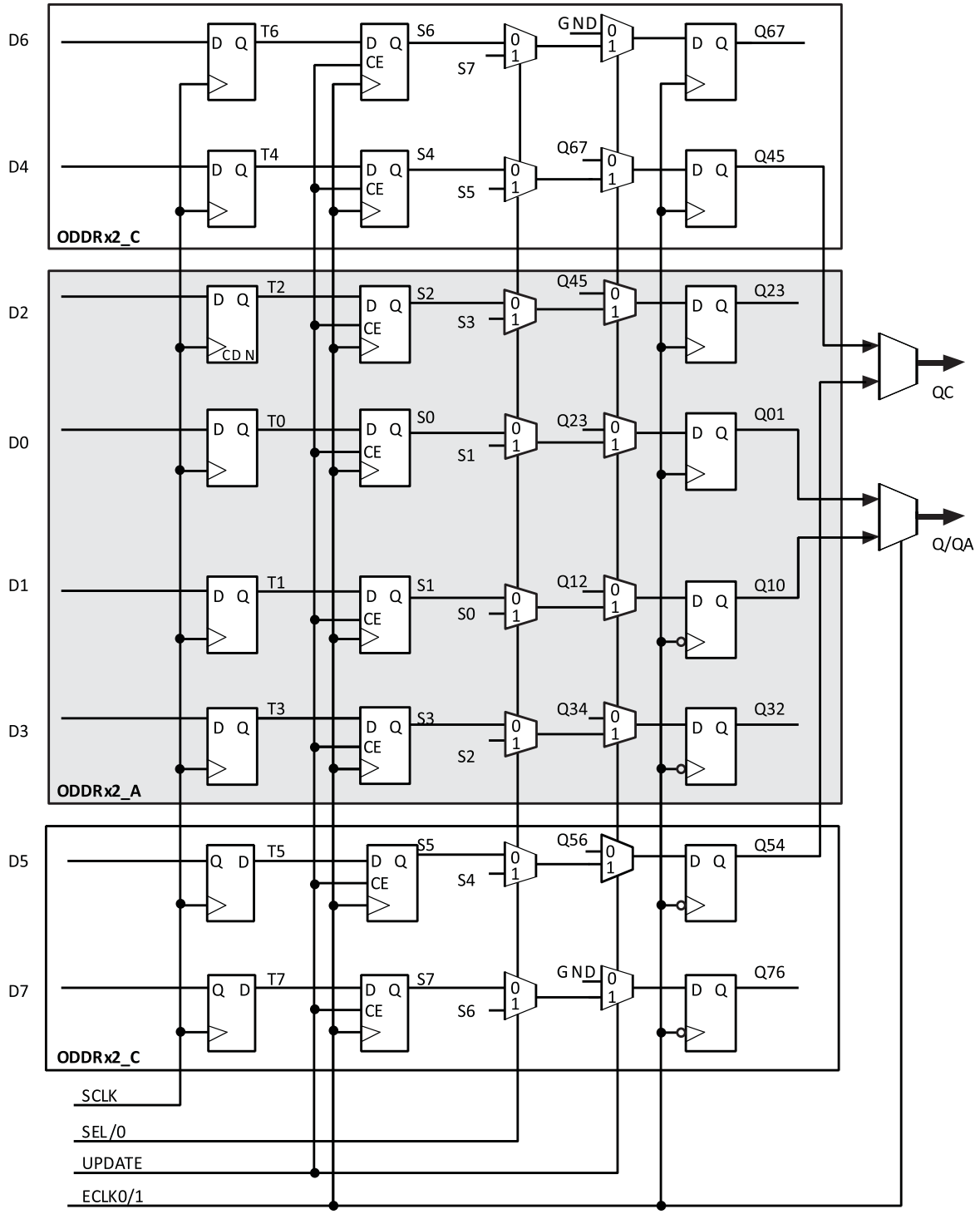

Figure 2.14. Output Gearbox

More information on the output gearbox is available in Implementing High-Speed Interfaces with MachXO4 Devices (FPGA-TN-02410).

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2.10. sysI/O Buffer

Each I/O is associated with a flexible buffer referred to as a sysI/O buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow you to implement a wide variety of standards that are found in today's systems including LVCMOS, TTL, LVDS, BLVDS, MLVDS, and LVPECL.

Each bank is capable of supporting multiple I/O standards. In the MachXO4 devices, single-ended output buffers, ratioed input buffers (LVTTL and LVCMOS), and differential (LVDS) input buffers are powered using I/O supply voltage (V_{CCIO}). Each sysI/O bank has its own V_{CCIO}.

MachXO4 devices contain three types of sysI/O buffer pairs.

- Left and Right sysI/O Buffer Pairs

  The sysI/O buffer pairs in the left and right banks of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the left and right of the devices also have differential input buffers.
- Bottom sysI/O Buffer Pairs

  The sysI/O buffer pairs in the bottom bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the bottom also have differential input buffers.
- Top sysI/O Buffer Pairs

  The sysI/O buffer pairs in the top bank of the device consist of two single-ended output drivers and two single-ended input buffers (for ratioed inputs such as LVCMOS and LVTTL). The I/O pairs on the top also have differential I/O buffers. Half of the sysI/O buffer pairs on the top edge have true differential outputs. The sysI/O buffer pair comprising of the A and B PIOs in every PIC on the top edge have a differential output driver.

2.10.1. Typical I/O Behavior during Power-up

The internal power-on-reset (POR) signal is deactivated when V_{CC} and V_{CCIO0} have reached VPORUP level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a blank device is tri-state with a weak pull-down to GND (some pins such as PROGRAMN and the JTAG pins have weak pull-up to V_{CCIO} as the default functionality). The I/O pins maintain the blank configuration until V_{CC} and V_{CCIO} (for I/O banks containing configuration I/O) have reached VPORUP levels at which time the I/O takes on the user-configured settings only after a proper download/configuration.

2.10.2. Supported Standards

The MachXO4 sysI/O buffer supports both single-ended and differential standards. Single-ended standards can be further subdivided into LVCMOS and LVTTL. The buffer supports the LVTTL, LVCMOS 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V standards. In the LVCMOS and LVTTL modes, the buffer has individually configurable options for drive strength, bus maintenance (weak pull-up, weak pull-down, bus-keeper latch or none) and open drain. BLVDS, MLVDS and LVPECL output emulation is supported on all devices. The MachXO4 devices support on-chip LVDS output buffers on approximately 50% of the I/O on the top bank. Differential receivers for LVDS, BLVDS, MLVDS and LVPECL are supported on all banks of MachXO4 devices. PCI compatibility is supported in the bottom bank of the MachXO4 devices. PCI compatibility is provided by:

- Selecting the LVTTL33 buffer standard
- Enabling the clamp feature
- Setting 16 mA drive strength (PCI output only).

Table 2.11 shows the I/O standards (together with their supply and reference voltages) supported by the MachXO4 devices. For further information on utilizing the sysI/O buffer to support a variety of standards, see MachXO4 sysI/O User Guide (FPGA-TN-02398).

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Table 2.11. Supported Input Standards

	V_{CCIO} (Typ.)				
Input Standard	**3.3 V**	**2.5 V**	**1.8 V**	**1.5 V**	**1.2 V**
Single-Ended Interfaces					
LVTTL	Yes	Yes[2]	Yes[2]	Yes[2]	—
LVCMOS33	Yes	Yes[2]	Yes[2]	Yes[2]	—
LVCMOS25	Yes[2]	Yes	Yes[2]	Yes[2]	—
LVCMOS18	Yes[2]	Yes[2]	Yes	Yes[2]	—
LVCMOS15	Yes[2]	Yes[2]	Yes[2]	Yes	Yes[2]
LVCMOS12	Yes[2]	Yes[2]	Yes[2]	Yes[2]	Yes
Differential Interfaces					
LVDS	Yes	Yes	—	—	—
BLVDS, MLVDS, LVPECL	Yes	Yes	—	—	—
MIPI[1]	Yes	Yes	—	—	—
LVTTLD	Yes	—	—	—	—
LVCMOS33D	Yes	—	—	—	—
LVCMOS25D	—	Yes	—	—	—
LVCMOS18D	—	—	Yes	—	—

Notes:

1. These interfaces can be emulated with external resistors in all devices.
2. Reduced functionality. Refer to MachXO4 sysI/O User Guide (FPGA-TN-02398) for more details.

Table 2.12. Supported Output Standards

Output Standard	V_{CCIO} (Typ.)
Single-Ended Interfaces	
LVTTL	3.3
LVCMOS33	3.3
LVCMOS25	2.5
LVCMOS18	1.8
LVCMOS15	1.5
LVCMOS12	1.2
LVCMOS33, Open Drain	—
LVCMOS25, Open Drain	—
LVCMOS18, Open Drain	—
LVCMOS15, Open Drain	—
LVCMOS12, Open Drain	—
Differential Interfaces	
LVDS[1]	2.5, 3.3
BLVDS, MLVDS	2.5
LVPECL[1]	3.3
MIPI[1]	2.5
LVTTLD	3.3
LVCMOS33D	3.3
LVCMOS25D	2.5
LVCMOS18D	1.8

Note:

1. These interfaces can be emulated with external resistors in all devices.

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2.10.3. sysI/O Buffer Banks

The numbers of banks vary between the devices of this family. LFMXO4-015 in the 256 Ball packages and the LFMXO4-025 and higher density devices have six I/O banks (one bank on the top, right and bottom side and three banks on the left side). The LFMXO4-015 and lower density devices have four banks (one bank per side). Figure 2.15 and Figure 2.16 show the sysI/O banks and their associated supplies for all devices.

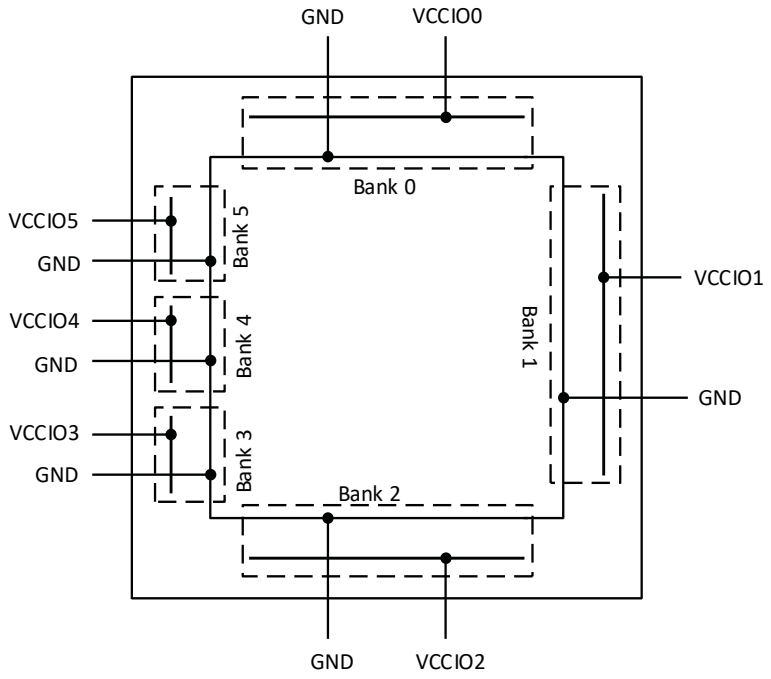

Figure 2.15. LFMXO4-015 in 256 Ball Packages, LFMXO4-025, LFMXO4-050, LFMXO4-080, and LFMXO4-110 I/O Banks

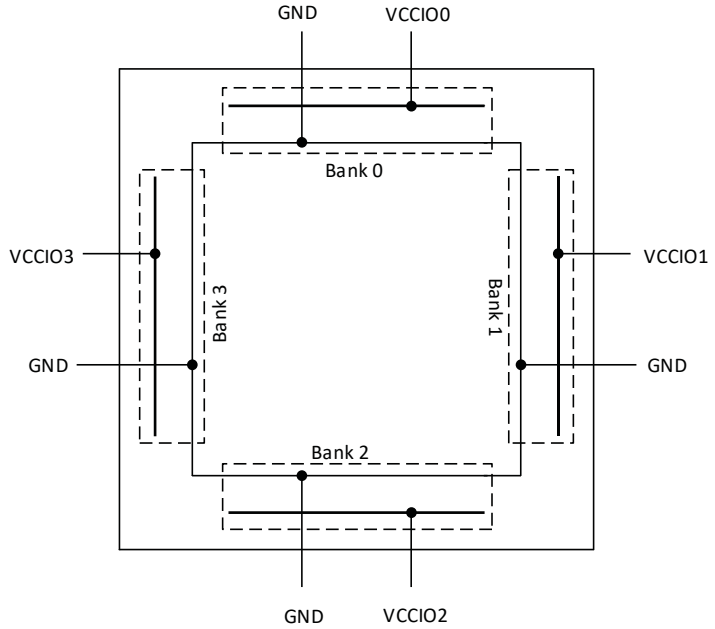

Figure 2.16.LFMXO4-010 and LFMXO4-015 in Non-256 Ball Packages I/O Banks

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2.11. Hot Socketing

The MachXO4 devices have been carefully designed to ensure predictable behavior during power-up and power-down. Leakage into I/O pins is controlled to within specified limits. This allows for easy integration with the rest of the system. These capabilities make the MachXO4 ideal for many multiple power supply and hot-swap applications.

2.12. On-chip Oscillator

Every MachXO4 device has an internal CMOS oscillator. The oscillator output can be routed as a clock to the clock tree or as a reference clock to the sysCLOCK PLL using general routing resources. The oscillator frequency can be divided by internal logic. There is a dedicated programming bit and a user input to enable/disable the oscillator. The oscillator frequency ranges from 2.08 MHz to 133 MHz. The software default value of the Master Clock (MCLK) is nominally 2.08 MHz. When a different MCLK is selected during the design process, the following sequence takes place:

Device powers up with a nominal MCLK frequency of 2.08 MHz.

During configuration, users select a different master clock frequency.

The MCLK frequency changes to the selected frequency once the clock configuration bits are received.

If the user does not select a master clock frequency, then the configuration bitstream defaults to the MCLK frequency of 2.08 MHz.

Table 2.13 lists all the available MCLK frequencies.

Table 2.13. Available MCLK Frequencies

MCLK (MHz, Nominal)	MCLK (MHz, Nominal)	MCLK (MHz, Nominal)
2.08 (default)	9.17	33.25
2.46	10.23	38
3.17	13.3	44.33
4.29	14.78	53.2
5.54	20.46	66.5
7	26.6	88.67
8.31	29.56	133

2.13. Embedded Hardened IP Functions

All MachXO4 devices provide embedded hardened functions such as SPI, I^2C and Timer/Counter. MachXO4 devices also provide User Flash Memory (UFM). These embedded blocks interface through the WISHBONE interface with routing as shown in Figure 2.17.

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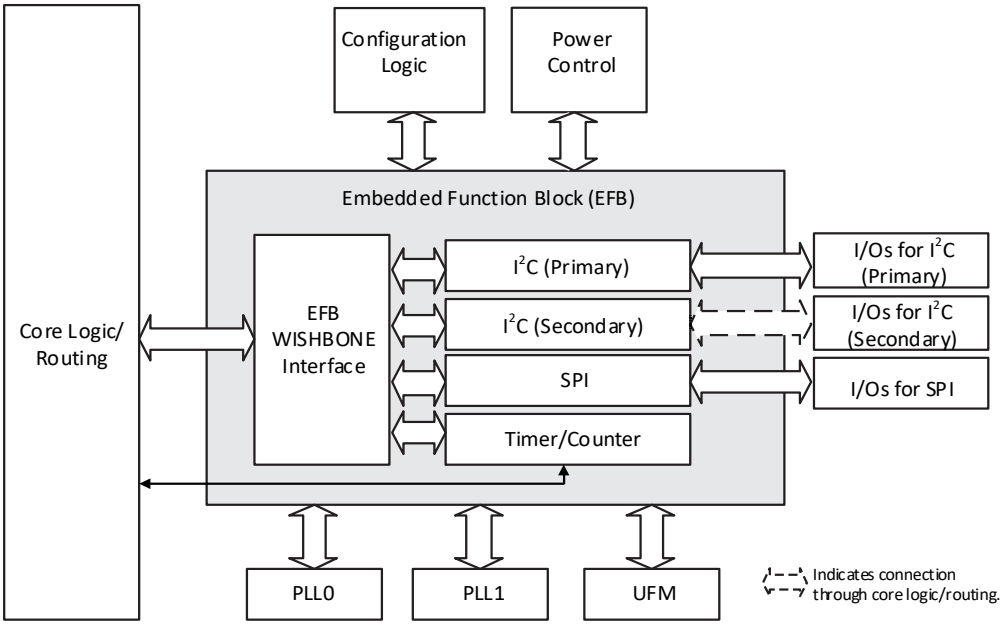

Figure 2.17. Embedded Function Block Interface

2.13.1. Hardened I2C IP Core

Every MachXO4 device contains two I2C IP cores. These are the primary and secondary I2C IP cores. Either of the two cores can be configured either as an I2C master or as an I2C slave. The only difference between the two IP cores is that the primary core has pre-assigned I/O pins whereas users can assign I/O pins for the secondary core.

When the IP core is configured as a master it is able to control other devices on the I2C bus through the interface. When the core is configured as the slave, the device is able to provide I/O expansion to an I2C Master. The I2C cores support the following functionality:

- Master and Slave operation
- 7-bit and 10-bit addressing
- Multi-master arbitration support
- Up to 400 kHz data transfer speed
- General call support
- Interface to custom logic through 8-bit WISHBONE interface

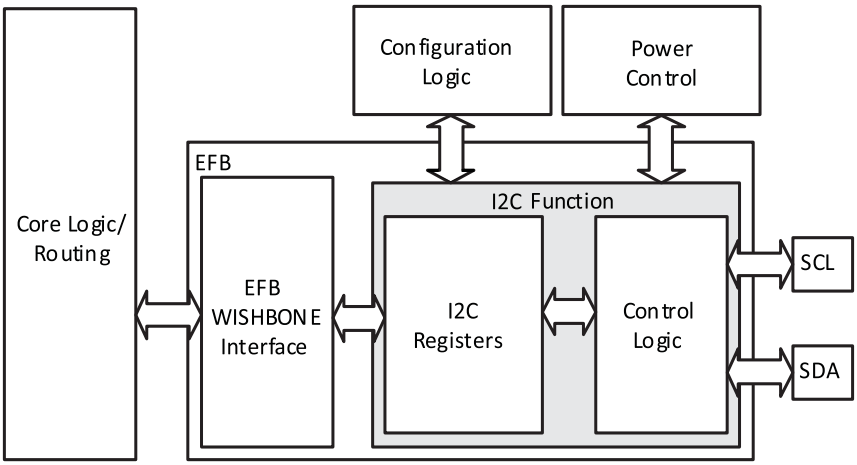

Figure 2.18. I2C Core Block Diagram

Table 2.14 describes the signals interfacing with the I2C cores.

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Table 2.14. I2C Core Signal Description

Signal Name	I/O	Description
i2c_scl	Bi-directional	Bi-directional clock line of the I2C core. The signal is an output if the I2C core is in master mode. The signal is an input if the I2C core is in slave mode. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I2C ports in each MachXO4 device.
i2c_sda	Bi-directional	Bi-directional data line of the I2C core. The signal is an output when data is transmitted from the I2C core. The signal is an input when data is received into the I2C core. MUST be routed directly to the pre-assigned I/O of the chip. Refer to the Pinout Information section of this document for detailed pad and pin locations of I2C ports in each MachXO4 device.
i2c_irqo	Output	Interrupt request output signal of the I2C core. The intended usage of this signal is for it to be connected to the WISHBONE master controller (for example, a microcontroller or state machine) and request an interrupt when a specific condition is met. These conditions are described with the I2C register definitions.
cfg_wake	Output	Wake-up signal – To be connected only to the power module of the MachXO4 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I2C Tab.
cfg_stdby	Output	Stand-by signal – To be connected only to the power module of the MachXO4 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, I2C Tab.

2.13.2. Hardened SPI IP Core

Every MachXO4 device has a hard SPI IP core that can be configured as a SPI master or slave. When the IP core is configured as a master it is able to control other SPI enabled chips connected to the SPI bus. When the core is configured as the slave, the device is able to interface to an external SPI master. The SPI IP core on MachXO4 devices supports the following functions:

- Configurable Master and Slave modes
- Full-Duplex data transfer
- Mode fault error flag with CPU interrupt capability
- Double-buffered data register
- Serial clock with programmable polarity and phase
- LSB First or MSB First Data Transfer
- Interface to custom logic through 8-bit WISHBONE interface

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There are some limitations on the use of the hardened user SPI. These are defined in the following technical notes:

- Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02198) (Appendix B)
- MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403)

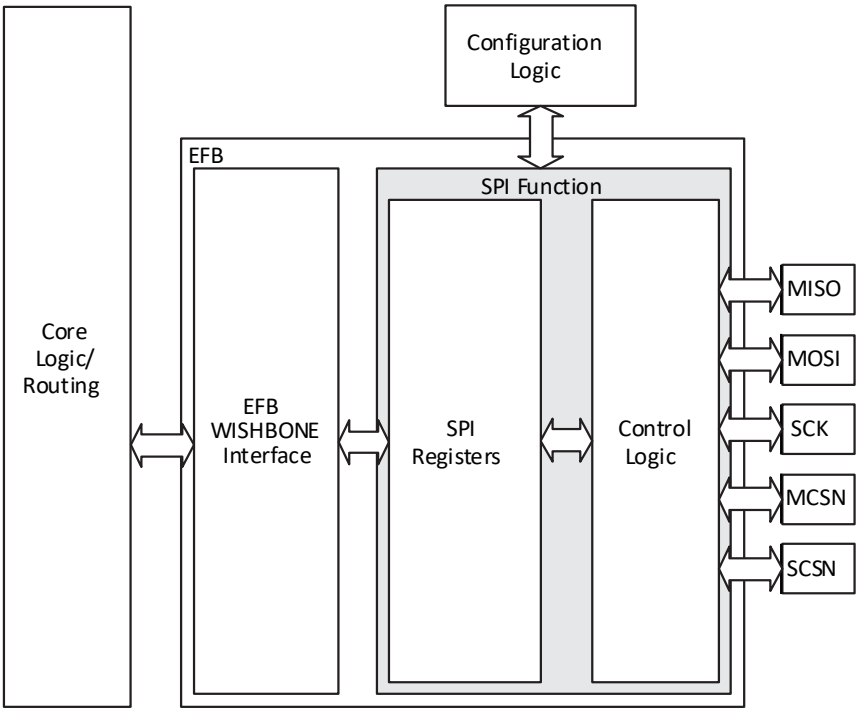

Figure 2.19. SPI Core Block Diagram

Table 2.15 describes the signals interfacing with the SPI cores.

Table 2.15. SPI Core Signal Description

Signal Name	I/O	Master/Slave	Description
spi_csn[0]	O	Master	SPI master chip-select output
spi_csn[1..7]	O	Master	Additional SPI chip-select outputs (total up to eight slaves)
spi_scsn	I	Slave	SPI slave chip-select input
spi_irq	O	Master/Slave	Interrupt request
spi_clk	I/O	Master/Slave	SPI clock. Output in master mode. Input in slave mode.
spi_miso	I/O	Master/Slave	SPI data. Input in master mode. Output in slave mode.
spi_mosi	I/O	Master/Slave	SPI data. Output in master mode. Input in slave mode.
sn	I	Slave	Configuration Slave Chip Select (active low), dedicated for selecting the Configuration Logic.
cfg_stdby	O	Master/Slave	Stand-by signal – To be connected only to the power module of the MachXO4 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.
cfg_wake	O	Master/Slave	Wake-up signal – To be connected only to the power module of the MachXO4 device. The signal is enabled only if the “Wakeup Enable” feature has been set within the EFB GUI, SPI Tab.

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2.13.3. Hardened Timer/Counter

MachXO4 devices provide a hard Timer/Counter IP core. This Timer/Counter is a general purpose, bidirectional, 16-bit timer/counter module with independent output compare units and PWM support. The Timer/Counter supports the following functions:

- Supports the following modes of operation:
- Watchdog timer
- Clear timer on compare match
- Fast PWM
- Phase and Frequency Correct PWM
- Programmable clock input source
- Programmable input clock prescaler
- One static interrupt output to routing
- One wake-up interrupt to on-chip stand-by mode controller
- Three independent interrupt sources: overflow, output compare match, and input capture
- Auto reload
- Time-stamping support on the input capture unit
- Waveform generation on the output
- Glitch-free PWM waveform generation with variable PWM period
- Internal WISHBONE bus access to the control and status registers
- Stand-alone mode with preloaded control registers and direct reset input

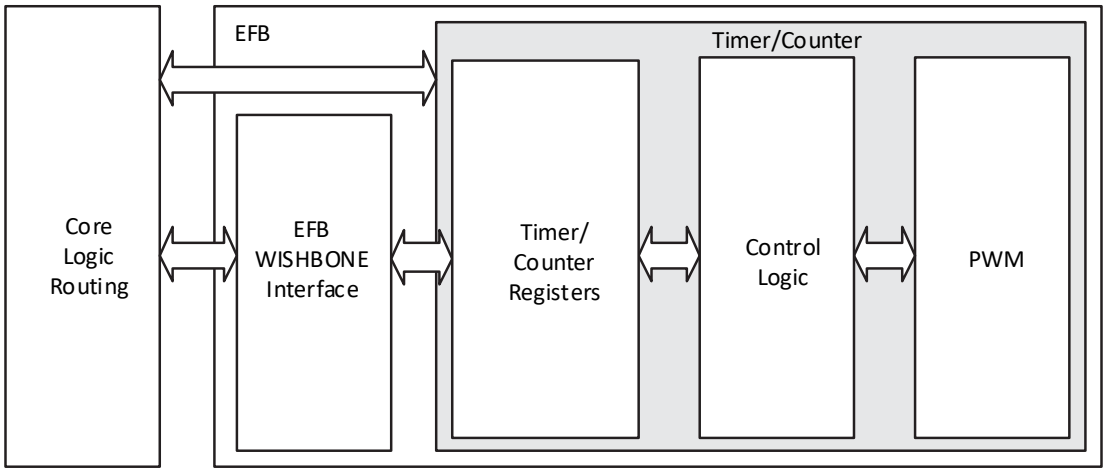

Figure 2.20. Timer/Counter Block Diagram

Table 2.16. Timer/Counter Signal Description

Port	I/O	Description
tc_clki	I	Timer/Counter input clock signal
tc_rstn	I	Register tc_rstn_ena is preloaded by configuration to always keep this pin enabled.
tc_ic	I	Input capture trigger event, applicable for non-pwm modes with WISHBONE interface. If enabled, a rising edge of this signal is detected and synchronized to capture tc_cnt value into tc_icr for time-stamping.
tc_int	O	Without WISHBONE – Can be used as overflow flag With WISHBONE – Controlled by three IRQ registers.
tc_oc	O	Timer counter output signal

For more details on these embedded functions, refer to MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403).

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2.14. User Flash Memory (UFM)

MachXO4 devices provide a User Flash Memory block, which can be used for a variety of applications including storing a portion of the configuration image, initializing EBRs, to store PROM data or, as a general purpose user Flash memory. The UFM block connects to the device core through the embedded function block WISHBONE interface. Users can also access the UFM block through the JTAG, I2C and SPI interfaces of the device. The UFM block offers the following features:

- Non-volatile storage up to 448 kbits
- 100,000 write/erase cycles for commercial/industrial devices and 10,000 for automotive devices
- Write access is performed page-wise; each page has 128 bits (16 bytes)
- Auto-increment addressing
- WISHBONE interface

For more information on the UFM, refer to MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403).

2.15. Stand-by Mode and Power Saving Options

MachXO4 devices are available in two options for maximum flexibility: HC and HE devices. The HC devices have a built-in voltage regulator to allow for 2.5 V VCC and 3.3 V VCC while the HE devices operate at 1.2 V VCC.

MachXO4 devices have been designed with features that allow users to meet the static and dynamic power requirements of their applications by controlling various device subsystems such as the bandgap, power-on-reset circuitry, I/O bank controllers, power guard, on-chip oscillator, PLLs, etc. In order to maximize power savings, MachXO4 devices support a low power stand-by mode.

In the stand-by mode, the MachXO4 devices are powered on and configured. Internal logic, I/O and memories are switched on and remain operational, as the user logic waits for an external input. The device enters this mode when the stand-by input of the stand-by controller is toggled or when an appropriate I2C or JTAG instruction is issued by an external master. Various subsystems in the device such as the band gap, power-on-reset circuitry can be configured such that they are automatically turned “off” or go into a low power consumption state to save power when the device enters this state. Note that the MachXO4 devices are powered on when in stand-by mode and all power supplies should remain in the Recommended Operating Conditions.

Table 2.17. MachXO4 Power Saving Features Description

Device Subsystem	Feature Description
Bandgap	The bandgap can be turned off in stand-by mode. When the Bandgap is turned off, analog circuitry such as the POR, PLLs, on-chip oscillator, and differential I/O buffers are also turned off. Bandgap can only be turned off for 1.2 V devices.
Power-On-Reset (POR)	The POR can be turned off in stand-by mode. This monitors VCC levels. In the event of unsafe VCC drops, this circuit reconfigures the device. When the POR circuitry is turned off, limited power detector circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable.
On-Chip Oscillator	The on-chip oscillator has two power saving features. It may be switched off if it is not needed in your design. It can also be turned off in stand-by mode.
PLL	Similar to the on-chip oscillator, the PLL also has two power saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in stand-by mode. The PLL waits until all output clocks from the PLL are driven low before powering off.
I/O Bank Controller	Differential I/O buffers (used to implement standards such as LVDS) consume more than ratioed single-ended I/O such as LVCMOS and LVTTL. The I/O bank controller allows the user to turn these I/O off dynamically on a per bank selection.
Dynamic Clock Enable for Primary Clock Nets	Each primary clock net can be dynamically disabled to save power.

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Device Subsystem	Feature Description
Power Guard	Power Guard is a feature implemented in input buffers. This feature allows users to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is that in the stand-by mode it can be used to switch off clock inputs that are distributed using general routing resources.

For more details on the stand-by mode, refer to Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409).

2.16. Power On Reset

MachXO4 devices have power-on reset circuitry to monitor V_{CCINT} and V_{CCIO} voltage levels during power-up and operation. At power-up, the POR circuitry monitors V_{CCINT} and V_{CCIO0} (controls configuration) voltage levels. It then triggers download from the on-chip configuration Flash memory after reaching the VPORUP level specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. For "E" devices without voltage regulators, V_{CCINT} is the same as the V_{CC} supply voltage. For "C" devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage. From this voltage reference, the time taken for configuration and entry into user mode is specified as Flash Download Time ($t_{REFRESH}$) in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/O are held in tri-state. I/O are released to user functionality once the device has finished configuration. Note that for "C" devices, a separate POR circuit monitors external V_{CC} voltage in addition to the POR circuit that monitors the internal post-regulated power supply voltage level.

Once the device enters into user mode, the POR circuitry can optionally continue to monitor V_{CCINT} levels. If V_{CCINT} drops below $V_{PORDNBG}$ level (with the bandgap circuitry switched on) or below $V_{PORDNSRAM}$ level (with the bandgap circuitry switched off to conserve power) device functionality cannot be guaranteed. In such a situation the POR issues a reset and begins monitoring the V_{CCINT} and V_{CCIO} voltage levels. $V_{PORDNBG}$ and $V_{PORDNSRAM}$ are both specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet.

Note that once an "E" device enters user mode, users can switch off the bandgap to conserve power. When the bandgap circuitry is switched off, the POR circuitry also shuts down. The device is designed such that a minimal, low power POR circuit is still operational (this corresponds to the $V_{PORDNSRAM}$ reset point described in the paragraph above). However this circuit is not as accurate as the one that operates when the bandgap is switched on. The low power POR circuit emulates an SRAM cell and is biased to trip before the vast majority of SRAM cells flip. If users are concerned about the V_{CC} supply dropping below V_{CC} (min), they should not shut down the bandgap or POR circuit.

2.17. Configuration and Testing

This section describes the configuration and testing features of the MachXO4 family.

2.17.1. IEEE 1149.1-Compliant Boundary Scan Testability

All MachXO4 devices have boundary scan cells that are accessed through an IEEE 1149.1 compliant test access port (TAP). This allows functional testing of the circuit board, on which the device is mounted, through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK and TMS. The test access port shares its power supply with V_{CCIO} Bank 0 and can operate with LVCMOS3.3, 2.5, 1.8, 1.5, and 1.2 standards.

For more details on boundary scan test, see Boundary Scan Testability with Lattice sysI/O Capability (AN8066) and Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02198).

2.17.2. Device Configuration

All MachXO4 devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration and the sysCONFIG port which supports serial configuration through I2C or SPI. The TAP supports both the IEEE Standard 1149.1 Boundary Scan specification and the IEEE Standard 1532 In-System Configuration specification. There are various ways to configure a MachXO4 device:

- Internal Flash Download

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- JTAG
- Standard Serial Peripheral Interface (Master SPI mode) – interface to boot PROM memory
- System microprocessor to drive a serial slave SPI port (SSPI mode)
- Standard I2C Interface to system microprocessor

Upon power-up, the configuration SRAM is ready to be configured using the selected sysCONFIG port. Once a configuration port is selected, it remains active throughout that configuration cycle. The IEEE 1149.1 port can be activated any time after power-up by sending the appropriate command through the TAP port. Optionally, the device can run a CRC check upon entering the user mode. This ensures that the device is configured correctly.

The sysCONFIG port has 10 dual-function pins which can be used as general purpose I/O if they are not required for configuration. See MachXO4 Programming and Configuration User Guide (FPGA-TN-02393) for more information about using the dual-use pins as general purpose I/O.

Lattice design software uses proprietary compression technology to compress bit-streams for use in MachXO4 devices. Use of this technology allows Lattice to provide a lower cost solution. In the unlikely event that this technology is unable to compress bitstreams to fit into the amount of on-chip Flash, there are a variety of techniques that can be utilized to allow the bitstream to fit in the on-chip Flash. For more details, refer to MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

The Test Access Port (TAP) has five dual purpose pins (TDI, TDO, TMS, TCK and JTAGENB). These pins are dual function pins - TDI, TDO, TMS and TCK can be used as general purpose I/O if desired. For more details, refer to MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

2.17.2.1. TransFR (Transparent Field Reconfiguration)

TransFR is a unique Lattice technology that allows users to update their logic in the field without interrupting system operation using a simple push-button solution. For more details, refer to Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02198) for details.

2.17.2.2. Security and One-Time Programmable Mode (OTP)

For applications where security is important, the lack of an external bitstream provides a solution that is inherently more secure than SRAM-based FPGAs. This is further enhanced by device locking. MachXO4 devices contain security bits that, when set, prevent the readback of the SRAM configuration and Flash spaces. The device can be in one of two modes:

- Unlocked – Readback of the SRAM configuration and Flash spaces is allowed.
- Permanently Locked – The device is permanently locked.

Once set, the only way to clear the security bits is to erase the device. To further complement the security of the device, a One Time Programmable (OTP) mode is available. Once the device is set in this mode it is not possible to erase or re-program the Flash and SRAM OTP portions of the device. For more details, refer to MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

2.17.2.3. Password

The MachXO4 supports a password-based security access feature also known as Flash Protect Key. Optionally, the MachXO4 device can be ordered with a custom specification (c-spec) to support this feature. The Flash Protect Key feature provides a method of controlling access to the Configuration and Programming modes of the device. When enabled, the Configuration and Programming edit mode operations (including Write, Verify and Erase operations) are allowed only when coupled with a Flash Protect Key which matches that expected by the device. Without a valid Flash Protect Key, the user can perform only rudimentary non-configuration operations such as Read Device ID. For more details, refer to Using Password Security with MachXO4 Devices (FPGA-TN-02408).

2.17.2.4. Dual Boot

MachXO4 devices can optionally boot from two patterns, a primary bitstream and a golden bitstream. If the primary bitstream is found to be corrupt while being downloaded into the SRAM, the device shall then automatically re-boot from the golden bitstream. Note that the primary bitstream must reside in the external SPI Flash. The golden image MUST reside in an on-chip Flash. For more details, refer to MachXO4 Programming and Configuration User Guide (FPGA-TN-02393).

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2.17.2.5. Soft Error Detection

The SED feature is a CRC check of the SRAM cells after the device is configured. This check ensures that the SRAM cells were configured successfully. This feature is enabled by a configuration bit option. The Soft Error Detection can also be initiated in user mode via an input to the fabric. The clock for the Soft Error Detection circuit is generated using a dedicated divider. The undivided clock from the on-chip oscillator is the input to this divider. For low power applications users can switch off the Soft Error Detection circuit. For more details, refer to MachXO4 Soft Error Detection (SED)/Correction (SEC) User Guide (FPGA-TN-02406).

2.17.2.6. Soft Error Correction

The MachXO4 device supports Soft Error Correction (SEC). When BACKGROUND_RECONFIG is enabled using the Lattice Radiant Software in a design, asserting the PROGRAMN pin or issuing the REFRESH sysConfig command refreshes the SRAM array from configuration memory. Only the detected error bit is corrected. No other SRAM cells are changed, allowing the user design to function uninterrupted.

During the project design phase, if the overall system cannot guarantee containment of the error or its subsequent effects on downstream data or control paths, Lattice recommends using SED only. The MachXO4 can be then be soft-reset by asserting PROGRAMN or issuing the Refresh command over a sysConfig port in response to SED. Soft-reset additionally erases the SRAM array prior to the SRAM refresh, and asserts internal Reset circuitry to guarantee a known state. For more details, refer to MachXO4 Soft Error Detection (SED)/Correction (SEC) User Guide (FPGA-TN-02406).

2.18. TraceID

Each MachXO4 device contains a unique (per device), TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the EFB WISHBONE interface and can also be accessed through the SPI, I2C, or JTAG interfaces.

2.19. Density Shifting

The MachXO4 family has been designed to enable density migration within the same package. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a lower utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likely success in each case. When migrating from lower to higher density or higher to lower density, ensure to review all the power supplies and NC pins of the chosen devices.

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3. DC and Switching Characteristics

3.1. Absolute Maximum Rating

Table 3.1. Absolute Maximum Rating[1, 2, 3]

	MachXO4 E (1.2 V)	MachXO4 C (2.5 V/3.3 V)[6]
Supply Voltage V_{CC}	–0.5 V to 1.32 V	–0.5 V to 3.75 V
Output Supply Voltage V_{CCIO}	–0.5 V to 3.75 V	–0.5 V to 3.75 V
I/O Tri-state Voltage Applied[4, 5]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Dedicated Input Voltage Applied[4]	–0.5 V to 3.75 V	–0.5 V to 3.75 V
Storage Temperature (Ambient)	–55 °C to 125 °C	–55 °C to 125 °C
Junction Temperature (T_J)	–40 °C to 125 °C	–40 °C to 125 °C

Notes:
1. Stress above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice Thermal Management document is required.
3. All voltages referenced to GND.
4. Overshoot and undershoot of –2 V to (VIHMAX + 2) volts is permitted for a duration of <20 ns.
5. The dual function I2C pins SCL and SDA are limited to –0.25 V to 3.75 V or to –0.3 V with a duration of <20 ns.
6. Refer to Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409) for determination of safe ambient operating conditions.

3.2. Recommended Operating Conditions

Table 3.2. Recommended Operating Conditions[1]

Symbol	Parameter	Min.	Max.	Unit
V_{CC}[1]	Core Supply Voltage for 1.2 V Devices	1.14	1.26	V
	Core Supply Voltage for 2.5 V/3.3 V Devices	2.375	3.465	V
V_{CCIO}[1, 2, 3]	I/O Driver Supply Voltage	1.14	3.465	V
t_{JCOM}	Junction Temperature Commercial Operation	0	85	°C
t_{JIND}	Junction Temperature Industrial Operation	–40	100	°C
t_{JAUTO}	Junction Temperature Automotive Operation	–40	125	°C

Notes:
1. Like power supplies must be tied together. For example, if V_{CCIO} and V_{CC} are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3. V_{CCIO} pins of unused I/O banks should be connected to the V_{CC} power supply on boards.

3.3. Power Supply Ramp Rates

Table 3.3. Power Supply Ramp Rates

Symbol		Parameter	Min.	Typ.	Max.	Unit
t_{RAMP}	Commercial/Industrial	Power supply ramp rates for all power supplies.	0.01	—	100	V/ms
	Automotive		0.01	—	40	V/ms

Note: Assumes monotonic ramp rates.

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3.4. Power-On-Reset Voltage Levels

Table 3.4. Power-On Reset Voltage Levels

Symbol	Parameter	Commercial/Industrial			Automotive			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{PORUP}	Power-On-Reset ramp up trip point (band gap based circuit monitoring V_{CCINT} and V_{CCIO0})	0.9	—	1.06	0.9	—	1.06	V
$V_{PORUPEXT}$	Power-On-Reset ramp up trip point (band gap based circuit monitoring external V_{CC} power supply)	1.5	—	2.1	1.5	—	2.1	V
$V_{PORDNBG}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CCINT})	0.75	—	0.93	0.75	—	1.06	V
$V_{PORDNBGEXT}$	Power-On-Reset ramp down trip point (band gap based circuit monitoring V_{CC})	0.98	—	1.33	0.98	—	1.47	V
$V_{PORDNSRAM}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CCINT})	—	0.6	—	—	0.84	—	V
$V_{PORDNSRAMEXT}$	Power-On-Reset ramp down trip point (SRAM based circuit monitoring V_{CC})	—	0.96	—	—	1.16	—	V

Notes:

- These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.
- For devices without voltage regulators V_{CCINT} is the same as the V_{CC} supply voltage. For devices with voltage regulators, V_{CCINT} is regulated from the V_{CC} supply voltage.
- Note that V_{PORUP} (min.) and $V_{PORDNBG}$ (max.) are in different process corners. For any given process corner $V_{PORDNBG}$ (max.) is always 12.0 mV below V_{PORUP} (min.).
- $V_{PORUPEXT}$ is for HC devices only. In these devices, a separate POR circuit monitors the external V_{CC} power supply.
- V_{CCIO0} does not have a Power-On-Reset ramp down trip point. V_{CCIO0} must remain within the Recommended Operating Conditions to ensure proper operation.

3.5. Hot Socketing Specifications

Table 3.5. Hot Socketing Specifications

Symbol	Parameter	Condition	Commercial/Industrial	Automotive	Unit
			Max.		
I_{DK}	Input or I/O leakage Current	$0 < V_{IN} < V_{IH}$ (MAX)	±350	±400	µA

Notes:

1. Insensitive to sequence of V_{CC} and V_{CCIO}. However, assumes monotonic rise/fall rates for V_{CC} and V_{CCIO}.
2. $0 < V_{CC} < V_{CC}$ (MAX), $0 < V_{CCIO} < V_{CCIO}$ (MAX).
3. IDK is additive to IPU, IPD or IBH.
4. Clamp option is set to OFF

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3.6. Programming/Erase Specifications

Table 3.6. Programming/Erase Specifications

Symbol	Parameter	Commercial/Industrial		Automotive		Unit
		Min.	Max.[1]	Min.	Max.[1]	
$N_{PROGCYC}$	Flash Programming cycles per $t_{RETENTION}$	—	10,000	—	1,000	Cycle
	Flash Write/Erase cycles[2]	—	100,000	—	10,000	
$t_{RETENTION}$	Data retention at 125 °C junction temperature	—	—	2	—	Year
	Data retention at 100 °C junction temperature	10	—	10	—	
	Data retention at 85 °C junction temperature	20	—	20	—	

Notes:

1. Maximum Flash memory reads are limited to 7.5E13 cycles over the lifetime of the product.
2. A Write/Erase cycle is defined as any number of writes over time followed by any erase cycle.

3.7. ESD Performance

Refer to the MachXO4 Product Family Qualification Summary for complete qualification data, including ESD performance. The MachXO4 Family Qualification Summary can be requested from Lattice Semiconductor Quality and Reliability Team.

3.8. DC Electrical Characteristics

Over recommended operating conditions.

Table 3.7. DC Electrical Characteristics

Symbol	Parameter	Condition	Commercial/Industrial			Automotive			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
I_{IL}, I_{IH}[1, 4]	Input or I/O Leakage	Clamp OFF and $V_{CCIO} < V_{IN} < V_{IH}$ (MAX)	—	—	+175	—	—	+175	µA
		Clamp OFF and $V_{IN} = V_{CCIO}$	–10	—	10	–10	—	11	µA
		Clamp OFF and V_{CCIO} - 0.97 V < $V_{IN} < V_{CCIO}$	–175	—	—	–175	—	—	µA
		Clamp OFF and 0 V < V_{IN} < V_{CCIO} – 0.97 V	—	—	10	—	—	10	µA
		Clamp OFF and V_{IN} = GND	—	—	10	—	—	10	µA
		Clamp ON and 0 V < V_{IN} < V_{CCIO}	—	—	10	—	—	11	µA
I_{PU}	I/O Active Pull-up Current	0 < V_{IN} < 0.7 V_{CCIO}	–309	—	–26	–309	—	–26	µA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX) < $V_{IN} < V_{CCIO}$	30	—	305	30	—	305	µA
I_{BHLS}	Bus Hold Low sustaining current	$V_{IN} = V_{IL}$ (MAX)	30	—	—	30	—	—	µA
I_{BHHS}	Bus Hold High sustaining current	$V_{IN} = 0.7V_{CCIO}$	–30	—	—	–27	—	—	µA
I_{BHLO}	Bus Hold Low Overdrive current	$0 \le V_{IN} \le V_{CCIO}$	—	—	305	—	—	305	µA
I_{BHHO}	Bus Hold High Overdrive current	$0 \le V_{IN} \le V_{CCIO}$	—	—	–309	—	—	–309	µA
V_{BHT}[3]	Bus Hold Trip Points	—	V_{IL} (MAX)	—	V_{IH} (MIN)	V_{IL} (MAX)	—	V_{IH} (MIN)	V

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Symbol	Parameter	Condition	Commercial/Industrial			Automotive			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
C1	I/O Capacitance[2]	V_{CCIO} = 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V V_{CC} = Typ., V_{IO} = 0 to V_{IH} (MAX)	3	5	9	3	5	9	pf
V_{HYST}	Hysteresis for Schmitt Trigger Inputs[5]	V_{CCIO} = 3.3 V, Hysteresis = Large	—	450	—	—	450	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Large	—	250	—	—	250	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Large	—	125	—	—	125	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Large	—	100	—	—	100	—	mV
		V_{CCIO} = 3.3 V, Hysteresis = Small	—	250	—	—	250	—	mV
		V_{CCIO} = 2.5 V, Hysteresis = Small	—	150	—	—	150	—	mV
		V_{CCIO} = 1.8 V, Hysteresis = Small	—	60	—	—	60	—	mV
		V_{CCIO} = 1.5 V, Hysteresis = Small	—	40	—	—	40	—	mV

Notes:

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Bus maintenance circuits are disabled.
2. T_A 25 °C, f = 1.0 MHz.
3. Refer to V_{IL} and V_{IH} in the sysI/O Single-Ended DC Electrical Characteristics table of this document.
4. When V_{IH} is higher than V_{CCIO}, a transient current typically of 30 ns in duration or less with a peak current of 6 mA can occur on the high-to-low transition. For true LVDS output pins in MachXO4 devices, V_{IH} must be less than or equal to V_{CCIO}.
5. With bus keeper circuit turned on. For more details, refer to MachXO4 sysI/O User Guide (FPGA-TN-02398).

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3.9. Static Supply Current – HC/HE Devices

Table 3.8. Static Supply Current – HC/HE Devices[1, 2, 3, 6]

Symbol	Parameter	Device	Typ.[4]	Unit
I_{CC}	Core Power Supply	LFMXO4-010HC	3.49	mA
		LFMXO4-015HC	3.49	mA
		LFMXO4-015HC 256 Ball Package	4.8	mA
		LFMXO4-025HC	4.8	mA
		LFMXO4-050HC	8.45	mA
		LFMXO4-050HC 400 Ball Package	12.87	mA
		LFMXO4-080HC	12.87	mA
		LFMXO4-110HC	17.86	mA
		LFMXO4-010HE	1.00	mA
		LFMXO4-015HE	1.00	mA
		LFMXO4-015HE 256 Ball Package	1.39	mA
		LFMXO4-025HE	1.39	mA
		LFMXO4-050HE	2.55	mA
		LFMXO4-050HE 400 Ball Package	4.06	mA
		LFMXO4-080HE	4.06	mA
		LFMXO4-110HE	5.66	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

Notes:

1. For further information on supply current, refer to Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409).
2. Assumes a test pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at V_{CCIO} or GND, on-chip oscillator is off, on-chip PLL is off.
3. Frequency = 0 MHz.
4. TJ = 25 °C, power supplies at nominal voltage.
5. Does not include pull-up/pull-down.
6. To determine the MachXO4 peak start-up current data, use the Power Calculator tool.

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3.10. Programming and Erase Supply Current – HC/HE Devices

Table 3.9. Programming and Erase Supply Current – HC/HE Devices[1, 2, 3, 4]

Symbol	Parameter	Device	Typ.[4]	Unit
I_{CC}	Core Power Supply	LFMXO4-010HC	18.8	mA
		LFMXO4-015HC	18.8	mA
		LFMXO4-015HC 256 Ball Package	22.1	mA
		LFMXO4-025HC	22.1	mA
		LFMXO4-050HC	26.8	mA
		LFMXO4-050HC 400 Ball Package	33.2	mA
		LFMXO4-080HC	33.2	mA
		LFMXO4-110HC	39.6	mA
		LFMXO4-010HE	17.7	mA
		LFMXO4-015HE	17.7	mA
		LFMXO4-015HE 256 Ball Package	18.3	mA
		LFMXO4-025HE	18.3	mA
		LFMXO4-050HE	20.4	mA
		LFMXO4-050HE 400 Ball Package	23.9	mA
		LFMXO4-080HE	23.9	mA
		LFMXO4-110HE	28.5	mA
I_{CCIO}	Bank Power Supply[5] V_{CCIO} = 2.5 V	All devices	0	mA

Notes:

1. For further information on supply current, refer to Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409).
2. Assumes all inputs are held at V_{CCIO} or GND and all outputs are tri-stated.
3. Typical user pattern.
4. JTAG programming is at 25 MHz.
5. T_J = 25 °C, power supplies at nominal voltage.
6. Per bank. V_{CCIO} = 2.5 V. Does not include pull-up/pull-down.

3.11. sysI/O Recommended Operating Conditions

Table 3.10. sysI/O Recommended Operating Conditions

Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS 3.3	3.135	3.3	3.465	—	—	—
LVCMOS 2.5	2.375	2.5	2.625	—	—	—
LVCMOS 1.8	1.71	1.8	1.89	—	—	—
LVCMOS 1.5	1.425	1.5	1.575	—	—	—
LVCMOS 1.2	1.14	1.2	1.26	—	—	—
LVTTL	3.135	3.3	3.465	—	—	—
LVDS25[1, 2]	2.375	2.5	2.625	—	—	—
LVDS33[1, 2]	3.135	3.3	3.465	—	—	—
LVPECL[1]	3.135	3.3	3.465	—	—	—
BLVDS[1]	2.375	2.5	2.625	—	—	—
MIPI[3]	2.375	2.5	2.625	—	—	—
MIPI_LP[3]	1.14	1.2	1.26	—	—	—
LVCMOS25R33	3.135	3.3	3.6	1.1	1.25	1.4
LVCMOS18R33	3.135	3.3	3.6	0.75	0.9	1.05
LVCMOS18R25	2.375	2.5	2.625	0.75	0.9	1.05

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Standard	V_{CCIO} (V)			V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVCMOS15R33	3.135	3.3	3.6	0.6	0.75	0.9
LVCMOS15R25	2.375	2.5	2.625	0.6	0.75	0.9
LVCMOS12R33	3.135	3.3	3.6	0.45	0.6	0.75
LVCMOS12R25	2.375	2.5	2.625	0.45	0.6	0.75
LVCMOS10R33	3.135	3.3	3.6	0.35	0.5	0.65
LVCMOS10R25	2.375	2.5	2.625	0.35	0.5	0.65

Notes:

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.
2. For the dedicated LVDS buffers.
3. Requires the addition of external resistors.

3.12. sysI/O Single-Ended DC Electrical Characteristics

Table 3.11. sysI/O Single-Ended DC Electrical Charateristics[1, 2, 4]

Standard	VIL		VIH		VOL Max. (V)	VOH Min. (V)	IOL Max.[5] (mA)	IOH Max.[5] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS 3.3 LVTTL	–0.3	0.8	2.0	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
							12	–12
							16	–16
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 2.5	–0.3	0.7	1.7	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
							12	–12
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 1.8	–0.3	0.35 VCCIO	0.65 VCCIO	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
							12	–12
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 1.5	–0.3	0.35 VCCIO	0.65 VCCIO	3.6	0.4	VCCIO – 0.4	4	–4
							8	–8
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS 1.2	–0.3	0.35 VCCIO	0.65 VCCIO	3.6	0.4	VCCIO – 0.4	4	–2
							8	–6
					0.2	VCCIO – 0.2	0.1	–0.1
LVCMOS25R33	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R33	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS18R25	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R33	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS15R25	–0.3	VREF – 0.1	VREF+0.1	3.6	NA	NA	NA	NA
LVCMOS12R33	–0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain
LVCMOS12R25	–0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain
LVCMOS10R33	–0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	24, 16, 12, 8, 4	NA Open Drain

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Standard	VIL		VIH		VOL Max. (V)	VOH Min. (V)	IOL Max.[5] (mA)	IOH Max.[5] (mA)
	Min. (V)[3]	Max. (V)	Min. (V)	Max. (V)				
LVCMOS10R25	-0.3	VREF – 0.1	VREF+0.1	3.6	0.40	NA Open Drain	16, 12, 8, 4	NA Open Drain

Notes:

1. MachXO4 devices allow LVCMOS inputs to be placed in I/O banks where V_{CCIO} is different from what is specified in the applicable JEDEC specification. This is referred to as a ratioed input buffer. In a majority of cases this operation follows or exceeds the applicable JEDEC specification. The cases where MachXO4 devices do not meet the relevant JEDEC specification are documented in the table below.
2. MachXO4 devices allow for LVCMOS referenced I/O, which follow applicable JEDEC specifications. For more details about mixed mode operation please refer to MachXO4 sysI/O User Guide (FPGA-TN-02398).
3. The dual function I2C pins SCL and SDA are limited to a VIL min of –0.25 V or to –0.3 V with a duration of <10 ns.
4. For I/O with mixed voltage support, V_{OH} follows respective sysI/O bank V_{CCIO} supply voltage, and V_{IL} / V_{IH} follows the I/O signaling standard.
5. For electromigration, the average DC current sourced or sinked by I/O pads between two consecutive V_{CCIO} or GND pad connections, or between the last V_{CCIO} or GND in an I/O bank and the end of an I/O bank, shall not exceed a maximum of n * 8 mA. “n” is the number of I/O pads between the two consecutive bank V_{CCIO} or GND connections or between the last V_{CCIO} and GND in a bank and the end of a bank. I/O Grouping can be found in the Data Sheet Pin Tables, which can also be generated from the Lattice Radiant software.

3.13. sysI/O Differential Electrical Characteristics

The LVDS differential output buffers are available on the top side of the MachXO4 PLD family.

3.13.1. LVDS

Over recommended operating conditions.

Table 3.12. LVDS

Parameter Symbol	Parameter Description	Test Condition	Min.	Typ.	Max.	Unit
V_{INP}, V_{INM}	Input Voltage (Commercial/Industrial)	V_{CCIO} = 3.3 V	0	—	2.605	V
		V_{CCIO} = 2.5 V	0	—	2.05	V
	Input Voltage (Automotive)	V_{CCIO} = 3.3 V	0	—	2.6	V
		V_{CCIO} = 2.5 V	0	—	2.0	V
V_{THD}	Differential Input Threshold	—	±100	—	—	mV
V_{CM}	Input Common Mode Voltage	V_{CCIO} = 3.3 V	0.05	—	2.6	V
		V_{CCIO} = 2.5 V	0.05	—	2.0	V
I_{IN}	Input current	Power on	—	—	±10	µA
V_{OH}	Output high voltage for V_{OP} or V_{OM}	R_T = 100 Ω	—	1.375	—	V
V_{OL}	Output low voltage for V_{OP} or V_{OM}	R_T = 100 Ω	0.90	1.025	—	V
V_{OD}	Output voltage differential	(V_{OP} - V_{OM}), R_T = 100 Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} between high and low	—	—	—	50	mV
V_{OS}	Output voltage offset (Commercial/Industrial)	(V_{OP} - V_{OM})/2, R_T = 100 Ω	1.125	1.20	1.395	V
	Output voltage offset (Automotive)	(V_{OP} - V_{OM})/2, R_T = 100 Ω	1.10	1.20	1.395	V
ΔV_{OS}	Change in V_{OS} between H and L	—	—	—	50	mV
I_{OSD}	Output short circuit current	V_{OD} = 0 V driver outputs shorted	—	—	24	mA

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3.13.2. LVDS Emulation

MachXO4 devices can support LVDS outputs via emulation (LVDS25E). The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3.1 is one possible solution for LVDS standard implementation. Resistor values in Figure 3.1 are industry standard values for 1% resistors.

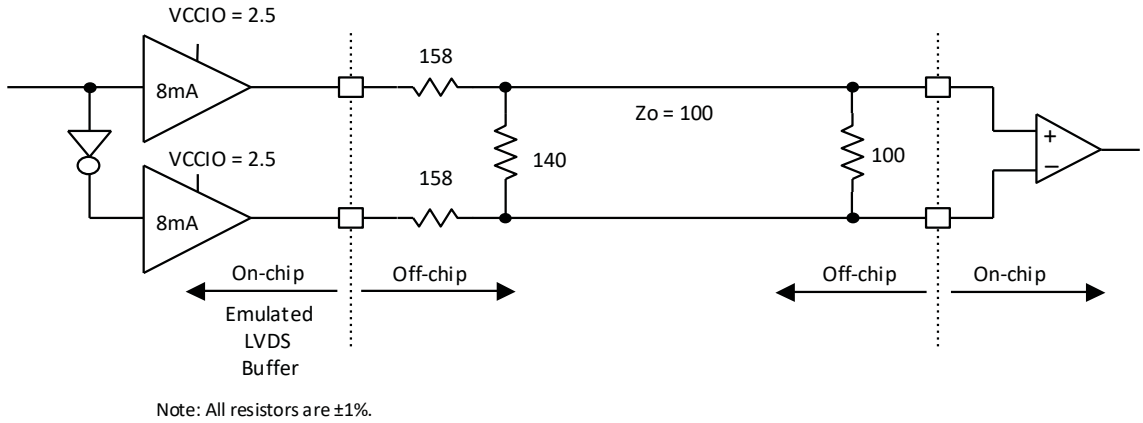

Figure 3.1. LVDS Using External Resistors (LVDS25E)

Over recommended operating conditions.

Table 3.13. LVDS25E DC Conditions

Parameter	Description	Typ.	Unit
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	158	Ω
R_P	Driver parallel resistor	140	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	1.43	V
V_{OL}	Output low voltage	1.07	V
V_{OD}	Output differential voltage	0.35	V
V_{CM}	Output common mode voltage	1.25	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	6.03	mA

3.13.3. BLVDS

The MachXO4 family supports the BLVDS standard through emulation. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs. The input standard is supported by the LVDS differential input buffer. BLVDS is intended for use when multi-drop and bi-directional multi-point differential signaling is required. The scheme shown in Figure 3.2 is one possible solution for bi-directional multi-point differential signals.

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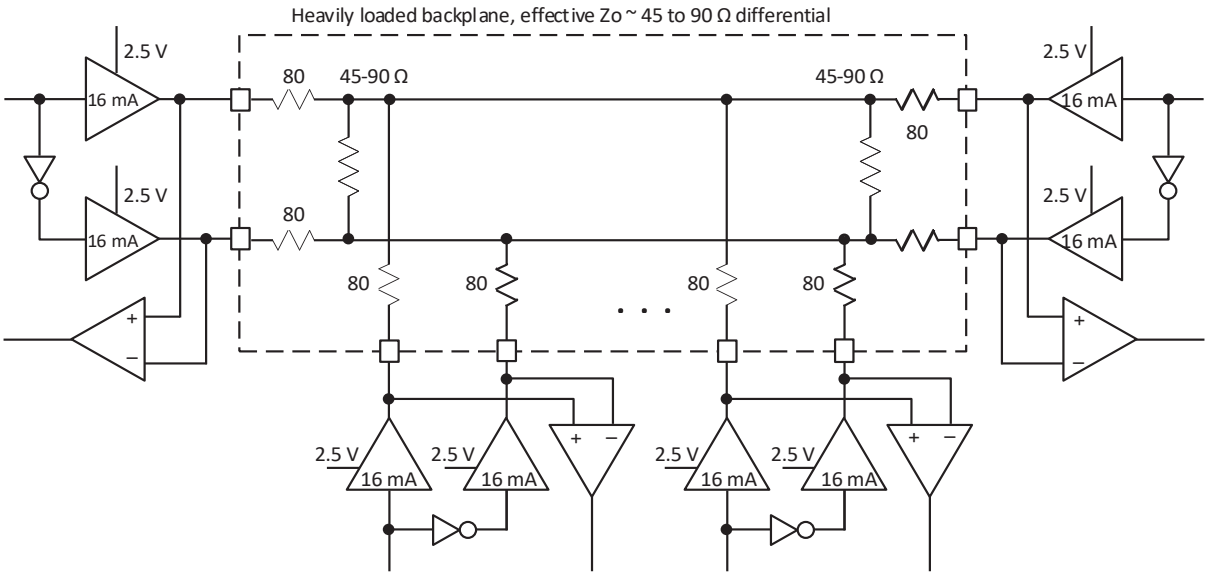

Figure 3.2. BLVDS Multi-point-Output Example

Over recommended operating conditions.

Table 3.14. BLVDS DC Condition

Symbol	Description	Nominal		Unit
		Zo = 45	Zo = 90	
Z_{OUT}	Output impedance	20	20	Ω
R_S	Driver series resistance	80	80	Ω
R_{TLEFT}	Left end termination	45	90	Ω
R_{TRIGHT}	Right end termination	45	90	Ω
V_{OH}	Output high voltage	1.376	1.480	V
V_{OL}	Output low voltage	1.124	1.020	V
V_{OD}	Output differential voltage	0.253	0.459	V
V_{CM}	Output common mode voltage	1.250	1.250	V
I_{DC}	DC output current	11.236	10.204	mA

Note: For input buffer, see LVDS table.

3.13.4. LVPECL

The MachXO4 family supports the differential LVPECL standard through emulation. This output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all the devices. The LVPECL input standard is supported by the LVDS differential input buffer. The scheme shown in Differential LVPECL is one possible solution for point-to-point signals.

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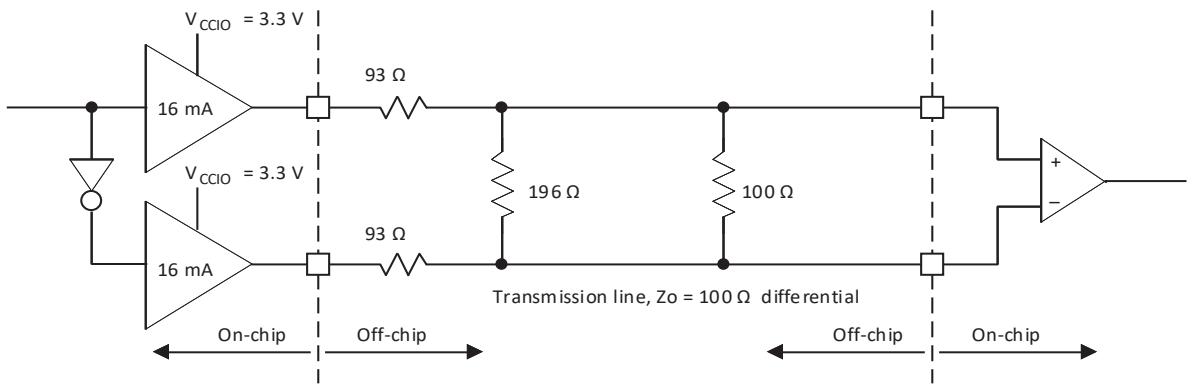

Figure 3.3. Differential LVPECL

Over recommended operating conditions.

Table 3.15. LVPECL DC Conditions

Symbol	Description	Nominal	Unit
Z_{OUT}	Output impedance	20	Ω
R_S	Driver series resistor	93	Ω
R_P	Driver parallel resistor	196	Ω
R_T	Receiver termination	100	Ω
V_{OH}	Output high voltage	2.05	V
V_{OL}	Output low voltage	1.25	V
V_{OD}	Output differential voltage	0.80	V
V_{CM}	Output common mode voltage	1.65	V
Z_{BACK}	Back impedance	100.5	Ω
I_{DC}	DC output current	12.11	mA

Note: For input buffer, see LVDS table.

For further information on LVPECL, BLVDS and other differential interfaces, see details of additional technical documentation at the end of the data sheet.

3.13.5. MIPI D-PHY Emulation

MachXO4 devices can support MIPI D-PHY unidirectional HS (High Speed) and bidirectional LP (Low Power) inputs and outputs via emulation. In conjunction with external resistors High Speed I/O use the LVDS25E buffer and Low Power I/O use the LVCMOS buffers. The scheme shown in Figure 3.4 is one possible solution for MIPI D-PHY Receiver implementation. The scheme shown in Figure 3.5 is one possible solution for MIPI D-PHY Transmitter implementation.

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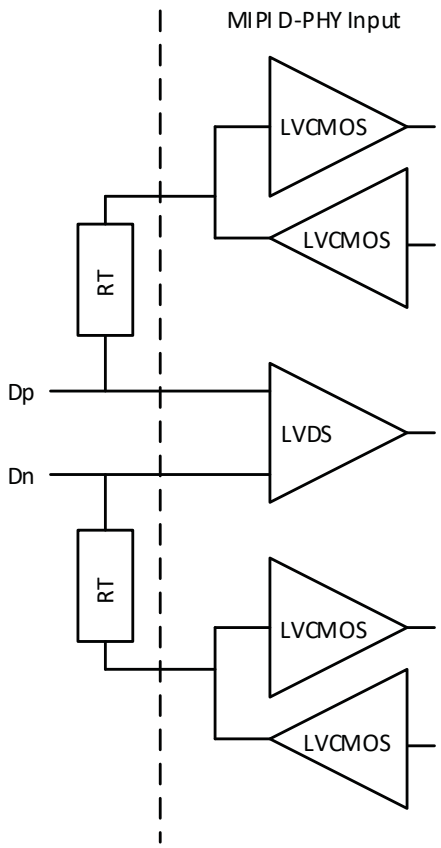

Figure 3.4. MIPI D-PHY Input Using External Resistors

Over recommended operating conditions.

Table 3.16. MIPI DC Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
Receiver					
External Termination					
RT	1% external resistor with V_{CCIO}=2.5 V	—	50	—	Ω
	1% external resistor with V_{CCIO}=3.3 V	—	50	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated input buffer	—	3.3	—	V
V_{CMRX}	Common-mode voltage HS receive mode	150	200	250	mV
V_{IDTH}	Differential input high threshold	—	—	100	mV
V_{IDTL}	Differential input low threshold	–100	—	—	mV
V_{IHHS}	Single-ended input high voltage	—	—	400	mV
V_{ILHS}	Single-ended input low voltage	0	—	—	mV
ZID	Differential input impedance	80	100	120	Ω
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{IH}	Logic 1 input voltage	—	—	0.88	V
V_{IL}	Logic 0 input voltage, not in ULP State	0.55	—	—	V
V_{HYST}	Input hysteresis	25	—	—	mV

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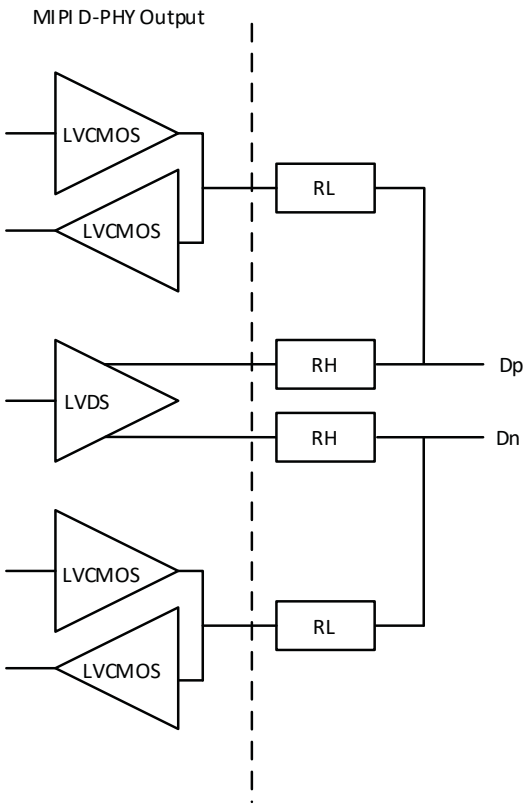

Figure 3.5. MIPI D-PHY Output Using External Resistors

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Over recommended operating conditions.

Table 3.17. MIPI D-PHY Output DC Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
Transmitter					
External Termination					
R_L	1% external resistor with V_{CCIO} = 2.5 V	—	50	—	Ω
	1% external resistor with V_{CCIO} = 3.3 V	—	50	—	
R_H	1% external resistor with performance up to 800 Mbps or with performance up 900 Mbps when V_{CCIO} = 2.5 V	—	330	—	Ω
	1% external resistor with performance between 800 Mbps to 900 Mbps when V_{CCIO} = 3.3 V	—	464	—	Ω
High Speed					
V_{CCIO}	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	2.5	—	V
	V_{CCIO} of the Bank with LVDS Emulated output buffer	—	3.3	—	V
V_{CMTX}	HS transmit static common mode voltage	150	200	250	mV
V_{OD}	HS transmit differential voltage	140	200	270	mV
V_{OHHS}	HS output high voltage	—	—	360	mV
ZOS	Single ended output impedance	—	50	—	Ω
ΔZOS	Single ended output impedance mismatch	—	—	10	%
Low Power					
V_{CCIO}	V_{CCIO} of the Bank with LVCMOS12D 6 mA drive bidirectional I/O buffer	—	1.2	—	V
V_{OH}	Output high level	1.1	1.2	1.3	V
V_{OL}	Output low level	–50	0	50	mV
ZOLP	Output impedance of LP transmitter	110	—	—	Ω

3.13.6. Comparator Function

MachXO4 devices can support a limited comparator function using the 3.3 V referenced input buffers. The scheme is shown in Figure 3.6.

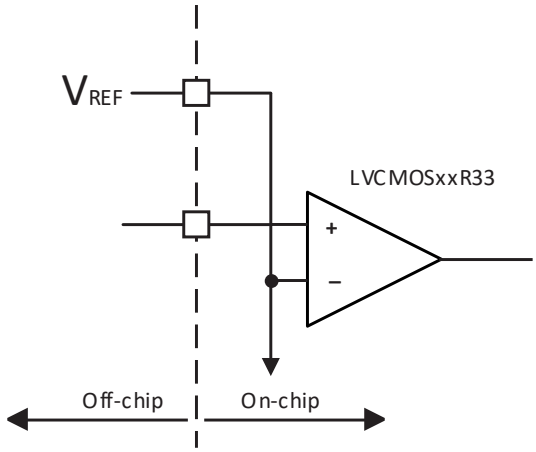

Figure 3.6. Comparator Function Using Referenced Input Buffers

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Over recommended operating conditions.

Table 3.18. Comparator Specifications[1]

Parameter	Description	Test Condition	–6/–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	
V_{IH}	Single-Ended input	V_{CCIO} = 3.3 V	V_{REF} + 0.1	3.6	V_{REF} + 0.1	3.6	V
V_{IL}			–0.3	V_{REF} – 0.1	–0.3	V_{REF} – 0.1	
V_{ref}	Voltage Ref input	V_{CCIO} = 3.3 V	0.05	2.605	0.05	2.605	V
t_{W_PRI}	Propagation Delay	V_{CCIO} = 3.3 V	—	10	—	10	ns
V_{OS}	Input Offset Voltage	V_{CCIO} = 3.3 V	–100	100	–105	105	mV

Note:

1. Comparator function supported for 3.3 V Referenced Input Buffer types LVCMOS25R33, LVCMOS18R33, LVCMOS15R33, LVCMOS12R33, and LVCMOS10R33.

3.14. Typical Building Block Function Performance – HC/HE Devices

3.14.1. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Table 3.19. Pin-to-Pin Performance (LVCMOS25 12 mA Drive)

Function	–6 Timing	Unit
Basic Functions		
16-bit decoder	8.9	ns
4:1 MUX	7.5	ns
16:1 MUX	8.3	ns

3.14.2. Register-to-Register Performance

Table 3.20. Register-to-Register Performance

Function	–6 Timing	Unit
Basic Functions		
16:1 MUX	412	MHz
16-bit adder	297	MHz
16-bit counter	324	MHz
64-bit counter	161	MHz
Embedded Memory Functions		
1024x9 True-Dual Port RAM (Write Through or Normal, EBR output registers)	183	MHz
Distributed Memory Functions		
16x4 Pseudo-Dual Port RAM (one PFU)	500	MHz

Note: The above timing numbers are generated using the Radiant design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Radiant software.

3.15. Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

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3.16. Maximum sysI/O Buffer Performance

Table 3.21. Maximum sysI/O Buffer Performance

I/O Standard	Max. Speed (Commercial/Industrial)	Max. Speed (Automotive)	Unit
MIPI	450	—	MHz
LVDS25	400	—	MHz
LVDS25E	150	—	MHz
BLVDS25	150	—	MHz
BLVDS25E	150	—	MHz
MLVDS25	150	—	MHz
MLVDS25E	150	—	MHz
LVPECL33	150	—	MHz
LVPECL33E	150	—	MHz
LVTTL33	150	—	MHz
LVTTL33D	150	—	MHz
LVCMOS33	150	—	MHz
LVCMOS33D	150	—	MHz
LVCMOS25	150	—	MHz
LVCMOS25D	150	—	MHz
LVCMOS18	150	—	MHz
LVCMOS18D	150	—	MHz
LVCMOS15	150	—	MHz
LVCMOS15D	150	—	MHz
LVCMOS12	91	—	MHz
LVCMOS12D	91	—	MHz

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3.17. External Switching Characteristics – HC/HE Devices

Over recommended operating conditions.

Table 3.22. MachXO4 External Switching Characteristics – HC/HE Devices[1, 2, 3, 4, 5, 6, 10]

Parameter	Description	Device	–6 (Commercial/Industrial)		–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Clocks									
Primary Clocks									
f_{MAX_PRI}[7]	Frequency for Primary Clock Tree	All MachXO4 devices	—	388	—	323	—	323	MHz
t_{W_PRI}	Clock Pulse Width for Primary Clock	All MachXO4 devices	0.5	—	0.6	—	0.6	—	ns
t_{SKEW_PRI}	Primary Clock Skew Within a Device	LFMXO4-010 HC/HE	—	867	—	897	—	952	ps
		LFMXO4-015 HC/HE	—	867	—	897	—	952	ps
		LFMXO4-025 HC/HE	—	867	—	897	—	952	ps
		LFMXO4-050 HC/HE	—	865	—	892	—	986	ps
		LFMXO4-080 HC/HE	—	902	—	942	—	—	ps
		LFMXO4-110 HC/HE	—	908	—	950	—	—	ps
Edge Clock									
f_{MAX_EDGE}[7]	Frequency for Edge Clock	All MachXO4 devices	—	400	—	333	—	333	MHz
Pin-LUT-Pin Propagation Delay									
t_{PD}	Best case propagation delay through one LUT-4	All MachXO4 devices	—	6.72	—	6.96	—	6.96	ns
General I/O Pin Parameters (Using Primary Clock without PLL)									
t_{CO}	Clock to Output – PIO Output Register	LFMXO4-010 HC/HE	—	7.46	—	7.66	—	7.66	ns
		LFMXO4-015 HC/HE	—	7.46	—	7.66	—	7.66	ns
		LFMXO4-025 HC/HE	—	7.46	—	7.66	—	7.66	ns
		LFMXO4-050 HC/HE	—	7.51	—	7.71	—	7.71	ns
		LFMXO4-080 HC/HE	—	7.54	—	7.75	—	—	ns
		LFMXO4-110 HC/HE	—	7.53	—	7.83	—	—	ns
t_{SU}	Clock to Data Setup – PIO Input Register	LFMXO4-010 HC/HE	–0.20	—	–0.20	—	–0.20	—	ns
		LFMXO4-015 HC/HE	–0.20	—	–0.20	—	–0.20	—	ns
		LFMXO4-025 HC/HE	–0.20	—	–0.20	—	–0.20	—	ns
		LFMXO4-050 HC/HE	–0.23	—	–0.23	—	–0.23	—	ns
		LFMXO4-080 HC/HE	–0.23	—	–0.23	—	—	—	ns
		LFMXO4-110 HC/HE	–0.24	—	–0.24	—	—	—	ns
t_H	Clock to Data Hold – PIO Input Register	LFMXO4-010 HC/HE	1.89	—	2.13	—	2.58	—	ns
		LFMXO4-015 HC/HE	1.89	—	2.13	—	2.58	—	ns
		LFMXO4-025 HC/HE	1.89	—	2.13	—	2.58	—	ns
		LFMXO4-050 HC/HE	1.94	—	2.18	—	2.49	—	ns
		LFMXO4-080 HC/HE	1.98	—	2.23	—	—	—	ns
		LFMXO4-110 HC/HE	1.99	—	2.24	—	—	—	ns
t_{SU_DEL}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFMXO4-010 HC/HE	1.61	—	1.76	—	1.76	—	ns
		LFMXO4-015 HC/HE	1.61	—	1.76	—	1.76	—	ns
		LFMXO4-025 HC/HE	1.61	—	1.76	—	1.76	—	ns
		LFMXO4-050 HC/HE	1.66	—	1.81	—	1.81	—	ns
		LFMXO4-080 HC/HE	1.53	—	1.67	—	—	—	ns
		LFMXO4-110 HC/HE	1.65	—	1.80	—	—	—	ns

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Parameter	Description	Device	–6 (Commercial/Industrial)		–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{H_DEL}	Clock to Data Hold – PIO Input Register with Input Data Delay	LFMXO4-010 HC/HE	–0.23	—	–0.23	—	–0.19	—	ns
		LFMXO4-015 HC/HE	–0.23	—	–0.23	—	–0.19	—	ns
		LFMXO4-025 HC/HE	–0.23	—	–0.23	—	–0.19	—	ns
		LFMXO4-050 HC/HE	–0.25	—	–0.25	—	–0.22	—	ns
		LFMXO4-080 HC/HE	–0.21	—	–0.21	—	—	—	ns
		LFMXO4-110 HC/HE	–0.24	—	–0.24	—	—	—	ns
$f_{MAX_I/O}$	Clock Frequency of I/O and PFU Register	All MachXO4 devices	—	388	—	323	—	323	MHz
General I/O Pin Parameters (Using Edge Clock without PLL)									
t_{COE}	Clock to Output – PIO Output Register	LFMXO4-010 HC/HE	—	7.53	—	7.76	—	7.76	ns
		LFMXO4-015 HC/HE	—	7.53	—	7.76	—	7.76	ns
		LFMXO4-025 HC/HE	—	7.53	—	7.76	—	7.76	ns
		LFMXO4-050 HC/HE	—	7.45	—	7.68	—	7.68	ns
		LFMXO4-080 HC/HE	—	7.53	—	7.76	—	—	ns
		LFMXO4-110 HC/HE	—	8.93	—	9.35	—	—	ns
t_{SUE}	Clock to Data Setup – PIO Input Register	LFMXO4-010 HC/HE	–0.19	—	–0.19	—	–0.19	—	ns
		LFMXO4-015 HC/HE	–0.19	—	–0.19	—	–0.19	—	ns
		LFMXO4-025 HC/HE	–0.19	—	–0.19	—	–0.19	—	ns
		LFMXO4-050 HC/HE	–0.16	—	–0.16	—	–0.16	—	ns
		LFMXO4-080 HC/HE	–0.19	—	–0.19	—	—	—	ns
		LFMXO4-110 HC/HE	–0.20	—	–0.20	—	—	—	ns
t_{HE}	Clock to Data Hold – PIO Input Register	LFMXO4-010 HC/HE	1.97	—	2.24	—	2.24	—	ns
		LFMXO4-015 HC/HE	1.97	—	2.24	—	2.24	—	ns
		LFMXO4-025 HC/HE	1.97	—	2.24	—	2.24	—	ns
		LFMXO4-050 HC/HE	1.89	—	2.16	—	2.16	—	ns
		LFMXO4-080 HC/HE	1.97	—	2.24	—	—	—	ns
		LFMXO4-110 HC/HE	1.98	—	2.25	—	—	—	ns
t_{SU_DELE}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFMXO4-010 HC/HE	1.56	—	1.69	—	1.69	—	ns
		LFMXO4-015 HC/HE	1.56	—	1.69	—	1.69	—	ns
		LFMXO4-025 HC/HE	1.56	—	1.69	—	1.69	—	ns
		LFMXO4-050 HC/HE	1.74	—	1.88	—	1.88	—	ns
		LFMXO4-080 HC/HE	1.66	—	1.81	—	—	—	ns
		LFMXO4-110 HC/HE	1.71	—	1.85	—	—	—	ns
t_{H_DELE}	Clock to Data Hold – PIO Input Register with Input Data Delay	LFMXO4-010 HC/HE	–0.23	—	–0.23	—	–0.23	—	ns
		LFMXO4-015 HC/HE	–0.23	—	–0.23	—	–0.23	—	ns
		LFMXO4-025 HC/HE	–0.23	—	–0.23	—	–0.23	—	ns
		LFMXO4-050 HC/HE	–0.34	—	–0.34	—	–0.34	—	ns
		LFMXO4-080 HC/HE	–0.29	—	–0.29	—	—	—	ns
		LFMXO4-110 HC/HE	–0.30	—	–0.30	—	—	—	ns
General I/O Pin Parameters (Using Primary Clock with PLL)									
t_{COPLL}	Clock to Output – PIO Output Register	LFMXO4-010 HC/HE	—	5.98	—	6.01	—	6.01	ns
		LFMXO4-015 HC/HE	—	5.98	—	6.01	—	6.01	ns
		LFMXO4-025 HC/HE	—	5.98	—	6.01	—	6.01	ns
		LFMXO4-050 HC/HE	—	5.99	—	6.02	—	6.02	ns
		LFMXO4-080 HC/HE	—	6.02	—	6.06	—	—	ns
		LFMXO4-110 HC/HE	—	5.55	—	6.13	—	—	ns

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Parameter	Description	Device	–6 (Commercial/Industrial)		–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
t_{SUPLL}	Clock to Data Setup – PIO Input Register	LFMXO4-010 HC/HE	0.36	—	0.36	—	0.36	—	ns
		LFMXO4-015 HC/HE	0.36	—	0.36	—	0.36	—	ns
		LFMXO4-025 HC/HE	0.36	—	0.36	—	0.36	—	ns
		LFMXO4-050 HC/HE	0.35	—	0.35	—	0.42	—	ns
		LFMXO4-080 HC/HE	0.34	—	0.34	—	—	—	ns
		LFMXO4-110 HC/HE	0.33	—	0.33	—	—	—	ns
t_{HPLL}	Clock to Data Hold – PIO Input Register	LFMXO4-110 HC/HE	0.42	—	0.49	—	0.49	—	ns
		LFMXO4-015 HC/HE	0.42	—	0.49	—	0.49	—	ns
		LFMXO4-025 HC/HE	0.42	—	0.49	—	0.49	—	ns
		LFMXO4-050 HC/HE	0.43	—	0.50	—	0.51	—	ns
		LFMXO4-080 HC/HE	0.46	—	0.54	—	—	—	ns
		LFMXO4-110 HC/HE	0.47	—	0.55	—	—	—	ns
t_{SU_DELPLL}	Clock to Data Setup – PIO Input Register with Data Input Delay	LFMXO4-010 HC/HE	2.87	—	3.18	—	3.38	—	ns
		LFMXO4-015 HC/HE	2.87	—	3.18	—	3.38	—	ns
		LFMXO4-025 HC/HE	2.87	—	3.18	—	3.38	—	ns
		LFMXO4-050 HC/HE	2.96	—	3.28	—	3.66	—	ns
		LFMXO4-080 HC/HE	3.05	—	3.35	—	—	—	ns
		LFMXO4-110 HC/HE	3.06	—	3.37	—	—	—	ns
t_{H_DELPLL}	Clock to Data Hold – PIO Input Register with Input Data Delay	LFMXO4-010 HC/HE	–0.83	—	–0.83	—	–0.83	—	ns
		LFMXO4-015 HC/HE	–0.83	—	–0.83	—	–0.83	—	ns
		LFMXO4-025 HC/HE	–0.83	—	–0.83	—	–0.83	—	ns
		LFMXO4-050 HC/HE	–0.87	—	–0.87	—	–0.87	—	ns
		LFMXO4-080 HC/HE	–0.91	—	–0.91	—	—	—	ns
		LFMXO4-110 HC/HE	–0.93	—	–0.93	—	—	—	ns
Generic DDRX1 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Aligned[8, 9]									
t_{DVA}	Input Data Valid After CLK	All MachXO4 devices, all sides	—	0.317	—	0.344	—	0.344	UI
t_{DVE}	Input Data Hold After CLK		0.742	—	0.702	—	0.702	—	UI
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	125	MHz
Generic DDRX1 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_RX.SCLK.Centered[8, 9]									
t_{SU}	Input Data Setup Before CLK	All MachXO4 devices, all sides	0.566	—	0.565	—	0.565	—	Ns
t_{HO}	Input Data Hold After CLK		0.778	—	0.879	—	0.879	—	ns
f_{DATA}	DDRX1 Input Data Speed		—	300	—	250	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency		—	150	—	125	—	125	MHz

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Parameter	Description	Device	–6 (Commercial/Industrial)		–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Aligned[8, 9]									
t_{DVA}	Input Data Valid After CLK	MachXO4 devices, bottom side only	—	0.316	—	0.342	—	0.342	UI
t_{DVE}	Input Data Hold After CLK		0.710	—	0.675	—	0.675	—	UI
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz
Generic DDRX2 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_RX.ECLK.Centered[8, 9]									
t_{SU}	Input Data Setup Before CLK	MachXO4 devices, bottom side only	0.233	—	0.233	—	0.233	—	ns
t_{HO}	Input Data Hold After CLK		0.287	—	0.287	—	0.287	—	ns
f_{DATA}	DDRX2 Serial Input Data Speed		—	664	—	554	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency		—	332	—	277	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz
Generic DDR4 Inputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Aligned[8]									
t_{DVA}	Input Data Valid After ECLK	MachXO4 devices, bottom side only	—	0.307	—	0.320	—	0.320	UI
t_{DVE}	Input Data Hold After ECLK		0.782	—	0.699	—	0.699	—	UI
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz
Generic DDR4 Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_RX.ECLK.Centered[8]									
t_{SU}	Input Data Setup Before ECLK	MachXO4 devices, bottom side only	0.233	—	0.233	—	0.233	—	ns
t_{HO}	Input Data Hold After ECLK		0.287	—	0.287	—	0.287	—	ns
f_{DATA}	DDRX4 Serial Input Data Speed		—	800	—	630	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz

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Parameter	Description	Device	–6 (Commercial/Industrial)		–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
7:1 LVDS Inputs (GDDR71_RX.ECLK.7:1)[9]									
t_{DVA}	Input Data Valid After ECLK	MachXO4 devices, bottom side only	—	0.290	—	0.320	—	0.257	UI
t_{DVE}	Input Data Hold After ECLK		0.739	—	0.699	—	0.699	—	UI
f_{DATA}	DDR71 Serial Input Data Speed		—	756	—	630	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	315	MHz
f_{CLKIN}	7:1 Input Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	90	MHz
MIPI D-PHY Inputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input - GDDRX4_RX.ECLK.Centered[10, 11, 12]									
t_{SU}[15]	Input Data Setup Before ECLK	All MachXO4 devices, bottom side only	0.200	—	0.200	—	0.295	—	UI
t_{HO}[15]	Input Data Hold After ECLK		0.200	—	0.200	—	0.312	—	UI
f_{DATA}[14]	MIPI D-PHY Input Data Speed		—	900	—	900	—	900	Mbps
f_{DDRX4}[14]	MIPI D-PHY ECLK Frequency		—	450	—	450	—	450	MHz
f_{SCLK}[14]	SCLK Frequency		—	112.5	—	112.5	—	112.5	MHz
Generic DDR Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Aligned[8]									
t_{DIA}	Output Data Invalid After CLK Output	All MachXO4 devices, all sides	—	0.520	—	0.550	—	0.550	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.520	—	0.550	—	0.550	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK frequency		—	150	—	125	—	125	MHz
Generic DDR Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX1_TX.SCLK.Centered[8]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO4 devices, all sides	1.210	—	1.510	—	1.510	—	ns
t_{DVA}	Output Data Valid After CLK Output		1.210	—	1.510	—	1.510	—	ns
f_{DATA}	DDRX1 Output Data Speed		—	300	—	250	—	250	Mbps
f_{DDRX1}	DDRX1 SCLK Frequency (minimum limited by PLL)		—	150	—	125	—	125	MHz

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Parameter	Description	Device	–6 (Commercial/Industrial)		–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Generic DDRX2 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Aligned[8]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO4 devices, top side only	—	0.200	—	0.215	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.215	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK frequency		—	332	—	277	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz
Generic DDRX2 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX2_TX.ECLK.Centered[8, 9]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO4 devices, top side only	0.535	—	0.670	—	0.670	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.535	—	0.670	—	0.658	—	ns
f_{DATA}	DDRX2 Serial Output Data Speed		—	664	—	554	—	554	Mbps
f_{DDRX2}	DDRX2 ECLK Frequency (minimum limited by PLL)		—	332	—	277	—	277	MHz
f_{SCLK}	SCLK Frequency		—	166	—	139	—	139	MHz
Generic DDRX4 Outputs with Clock and Data Aligned at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Aligned[8, 9]									
t_{DIA}	Output Data Invalid After CLK Output	MachXO4 devices, top side only	—	0.200	—	0.215	—	0.215	ns
t_{DIB}	Output Data Invalid Before CLK Output		—	0.200	—	0.215	—	0.215	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency		—	400	—	315	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz
Generic DDRX4 Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[8, 9]									
t_{DVB}	Output Data Valid Before CLK Output	MachXO4 devices, top side only	0.455	—	0.570	—	0.570	—	ns
t_{DVA}	Output Data Valid After CLK Output		0.455	—	0.570	—	0.549	—	ns
f_{DATA}	DDRX4 Serial Output Data Speed		—	800	—	630	—	630	Mbps
f_{DDRX4}	DDRX4 ECLK Frequency (minimum limited by PLL)		—	400	—	315	—	315	MHz
f_{SCLK}	SCLK Frequency		—	100	—	79	—	79	MHz

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Parameter	Description	Device	–6 (Commercial/Industrial)		–5 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
7:1 LVDS Outputs – GDDR71_TX.ECLK.7:1[8, 9]									
t_{DIB}	Output Data Invalid Before CLK Output	MachXO4 devices, top side only	—	0.160	—	0.180	—	0.180	ns
t_{DIA}	Output Data Invalid After CLK Output		—	0.160	—	0.180	—	0.201	ns
f_{DATA}	DDR71 Serial Output Data Speed		—	756	—	630	—	630	Mbps
f_{DDR71}	DDR71 ECLK Frequency		—	378	—	315	—	315	MHz
f_{CLKOUT}	7:1 Output Clock Frequency (SCLK) (minimum limited by PLL)		—	108	—	90	—	90	MHz
MIPI D-PHY Outputs with Clock and Data Centered at Pin Using PCLK Pin for Clock Input – GDDRX4_TX.ECLK.Centered[10, 11, 12]									
t_{DVB}	Output Data Valid Before CLK Output	All MachXO4 devices, top side only	0.200	—	0.200	—	0.200	—	UI
t_{DVA}	Output Data Valid After CLK Output		0.200	—	0.200	—	0.200	—	UI
f_{DATA}	MIPI D-PHY Output Data Speed		—	900	—	900	—	900	Mbps
F_{DDRX4}	MIPI D-PHY ECLK Frequency (minimum limited by PLL)		—	450	—	450	—	450	MHz
f_{SCLK}	SCLK Frequency		—	112.5	—	112.5	—	112.5	MHz

Notes:

1. Exact performance may vary with device and design implementation. Commercial timing numbers are shown at 85 °C and 1.14 V. Other operating conditions, including industrial, can be extracted from the Radiant software.
2. General I/O timing numbers based on LVCMOS 2.5, 8 mA, 0pf load, fast slew rate.
3. Generic DDR timing numbers based on LVDS I/O (for input, output, and clock ports).
4. 7:1 LVDS (GDDR71) uses the LVDS I/O standard (for input, output, and clock ports).
5. For Generic DDRX1 mode tSU = tHO = (tDVE - tDVA - 0.03 ns)/2.
6. The tSU_DEL and tH_DEL values use the SCLK_ZERHOLD default step size. Each step is 105 ps (–6), 113 ps (–5), 120 ps (–4).
7. This number for general purpose usage. Duty cycle tolerance is +/–10%.
8. Duty cycle is +/– 5% for system usage.
9. Performance is calculated with 0.225 UI.
10. Performance is calculated with 0.20 UI.
11. Performance for Industrial devices are only supported with VCC between 1.16 V to 1.24 V.
12. Performance for Industrial devices and –5 devices are not modeled in the Radiant design tool.
13. The above timing numbers are generated using the Radiant design tool. Exact performance may vary with the device selected.
14. Above 800 Mbps is only supported with WLCSP and csfBGA packages.
15. Between 800 Mbps to 900 Mbps:
    - VIDTH exceeds the MIPI D-PHY Input DC Conditions (Table 3.16) and can be calculated with the equation t_{SU} or t_H = –0.0005*VIDTH + 0.3284
    - Example calculations:
    - t_{SU} and t_{HO} = 0.28 with VIDTH = 100 mV
    - t_{SU} and t_{HO} = 0.25 with VIDTH = 170 mV
    - t_{SU} and t_{HO} = 0.20 with VIDTH = 270 mV

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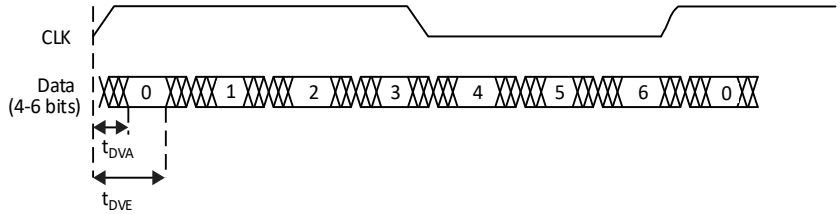

Figure 3.7.Receiver GDDR71_RX. Waveforms

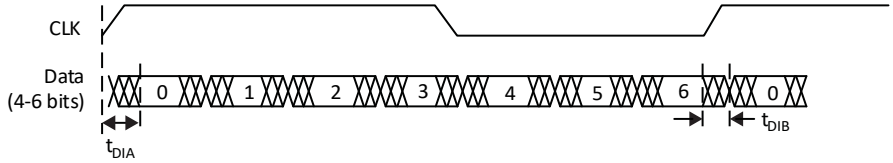

Figure 3.8. Transmitter GDDR71_TX. Waveforms

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3.18. sysCLOCK PLL Timing

Over recommended operating conditions.

Table 3.23. sysCLOCK PLL Timing

Parameter	Descriptions	Condition	–6 (Commercial/Industrial)		–5 (Automotive)		Unit
			Min.	Max.	Min.	Max.	
f_{IN}	Input Clock Frequency (CLKI, CLKFB)	—	7	400	7	400	MHz
f_{OUT}	Output Clock Frequency (CLKOP, CLKOS, CLKOS2)	—	1.5625	400	1.5625	400	MHz
f_{OUT2}	Output Frequency (CLKOS3 cascaded from CLKOS2)	—	0.0122	400	0.0122	400	MHz
f_{VCO}	PLL VCO Frequency	—	200	800	200	800	MHz
f_{PFD}	Phase Detector Input Frequency	—	7	400	7	400	MHz
AC Characteristics							
t_{DT}	Output Clock Duty Cycle	Without duty trim selected[3]	45	55	45	55	%
t_{DT_TRIM}[7]	Edge Duty Trim Accuracy	—	–75	75	N/A	N/A	%
t_{PH}[4]	Output Phase Accuracy	—	–6	6	–6	6	%
t_{OPJIT}[1, 8]	Output Clock Period Jitter	fOUT > 100 MHz	—	150	—	150	ps p-p
		fOUT < 100 MHz	—	0.007	—	0.010	UIPP
	Output Clock Cycle-to-cycle Jitter	fOUT > 100 MHz	—	180	—	180	ps p-p
		fOUT < 100 MHz	—	0.009	—	0.015	UIPP
	Output Clock Phase Jitter	fPFD > 100 MHz	—	160	—	160	ps p-p
		fPFD < 100 MHz	—	0.011	—	0.011	UIPP
	Output Clock Period Jitter (Fractional-N)	fOUT > 100 MHz	—	230	—	TBD	ps p-p
		fOUT < 100 MHz	—	0.12	—	TBD	UIPP
	Output Clock Cycle-to-cycle Jitter (Fractional-N)	fOUT > 100 MHz	—	230	—	TBD	ps p-p
		fOUT < 100 MHz	—	0.12	—	TBD	UIPP
t_{SPO}	Static Phase Offset	Divider ratio = integer	–120	120	–141	141	ps
t_W	Output Clock Pulse Width	At 90% or 10%[3]	0.9	—	—	—	ns
t_{LOCK}[2, 5]	PLL Lock-in Time	—	—	15	—	17.5	ms
t_{UNLOCK}	PLL Unlock Time	—	—	50	—	50	ns
t_{IPJIT}[6]	Input Clock Period Jitter	fPFD ≥ 20 MHz	—	1,000	—	1,000	ps p-p
		fPFD < 20 MHz	—	0.02	0.8	0.02	UIPP
t_{HI}	Input Clock High Time	90% to 90%	0.5	—	0.8	—	ns
t_{LO}	Input Clock Low Time	10% to 10%	0.5	—	0.5	—	ns
t_{STABLE}[5]	STANDBY High to PLL Stable	—	—	15	—	15	ms
t_{RST}	RST/RESETM Pulse Width	—	1	—	1	—	ns
t_{RSTREC}	RST Recovery Time	—	1	—	2.46	—	ns
t_{RST_DIV}	RESETC/D Pulse Width	—	10	—	10	—	ns
t_{RSTREC_DIV}	RESETC/D Recovery Time	—	1	—	2.33	—	ns
$t_{ROTATE\text{-}SETUP}$	PHASESTEP Setup Time	—	10	—	10	—	ns
t_{ROTATE_WD}	PHASESTEP Pulse Width	—	4	—	4	—	VCO Cycles

Notes:

1. Period jitter sample is taken over 10,000 samples of the primary PLL output with a clean reference clock. Cycle-to-cycle jitter is taken over 1000 cycles. Phase jitter is taken over 2000 cycles. All values per JESD65B.
2. Output clock is valid after t_{LOCK} for PLL reset and dynamic delay adjustment.

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3. Using LVDS output buffers.
4. CLKOS as compared to CLKOP output for one phase step at the maximum VCO frequency. See MachXO4 sysCLOCK PLL Design User Guide (FPGA-TN-02391) for more details.
5. At minimum fPFD. As the fPFD increases the time decreases to approximately 60% the value listed.
6. Maximum allowed jitter on an input clock. PLL unlock may occur if the input jitter exceeds this specification. Jitter on the input clock may be transferred to the output clocks, resulting in jitter measurements outside the output specifications listed in this table.
7. Edge Duty Trim Accuracy is a percentage of the setting value. Settings available are 70 ps, 140 ps, and 280 ps in addition to the default value of none.
   Edge Duty Trim Accuracy does not apply to Automotive.
8. Jitter values measured with the internal oscillator operating. The jitter values increase with loading of the PLD fabric and in the presence of SSO noise.

3.19. Oscillator Output Frequency

Table 3.24. Oscillator Output Frequency

Symbol	Parameter	–6 (Commercial/Industrial)			–5 (Automotive)			Unit
		Min.	Typ.	Max	Min.	Typ.	Max	
f_{MAX}	Oscillator Output Frequency (Commercial Grade Devices, 0 to 85°C)	125.685	133	140.315	—	—	—	MHz
	Oscillator Output Frequency (Industrial Grade Devices, –40 °C to 100 °C)	124.355	133	141.645	—	—	—	MHz
	Oscillator Output Frequency (Automotive Grade Devices, -40 to 125°C)	—	—	—	122.360	133	143.640	MHz
t_{DT}	Output Clock Duty Cycle	43	50	57	43	50	57	%
t_{OPJIT}	Output Clock Period Jitter	—	—	0.02	—	—	0.02	UIPP
$t_{STABLEOSC}$	STDBY Low to Oscillator Stable	—	—	0.1	—	—	0.1	µs

Note: Output Clock Period Jitter specified at 133 MHz. The values for lower frequencies are smaller UIPP. The typical value for 133 MHz is 95 ps and for 2.08 MHz the typical value is 1.54 ns.

3.20. Flash Download Time

Table 3.25. Flash Download Time

Symbol	Parameter	Device	Typ.	Unit
$t_{REFRESH}$	POR to Device I/O Active	LFMXO4-010	1.9	ms
		LFMXO4-015	1.9	ms
		LFMXO4-015 256-Ball Package	1.4	ms
		LFMXO4-025	1.4	ms
		LFMXO4-050	2.4	ms
		LFMXO4-050 400-Ball Package	3.8	ms
		LFMXO4-080	3.8	ms
		LFMXO4-110C	5.2	ms

Notes:
- Assumes sysMEM EBR initialized to an all zero pattern if they are used.
- The Flash download time is measured starting from the maximum voltage of POR trip point.
- The worst case can be up to 1.75 times the Typ value.

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3.21. JTAG Port Timing Specifications

Table 3.26. JTAG Port Timing Specifications

Symbol	Parameter	Commercial/Industrial		Automotive		Unit
		Min.	Max.	Min.	Max.	
f_{MAX}	TCK clock frequency	—	25	—	25	MHz
t_{BTCPH}	TCK [BSCAN] clock pulse width high	20	—	20	—	ns
t_{BTCPL}	TCK [BSCAN] clock pulse width low	20	—	20	—	ns
t_{BTS}	TCK [BSCAN] setup time	10	—	10	—	ns
t_{BTH}	TCK [BSCAN] hold time	8	—	10	—	ns
t_{BTCO}	TAP controller falling edge of clock to valid output	—	10	—	10	ns
$t_{BTCODIS}$	TAP controller falling edge of clock to valid disable	—	10	—	12	ns
t_{BTCOEN}	TAP controller falling edge of clock to valid enable	—	10	—	12	ns
t_{BTCRS}	BSCAN test capture register setup time	8	—	8	—	ns
t_{BTCRH}	BSCAN test capture register hold time	20	—	20	—	ns
t_{BUTCO}	BSCAN test update register, falling edge of clock to valid output	—	25	—	25	ns
$t_{BTUODIS}$	BSCAN test update register, falling edge of clock to valid disable	—	25	—	27	ns
$t_{BTUPOEN}$	BSCAN test update register, falling edge of clock to valid enable	—	25	—	25	ns

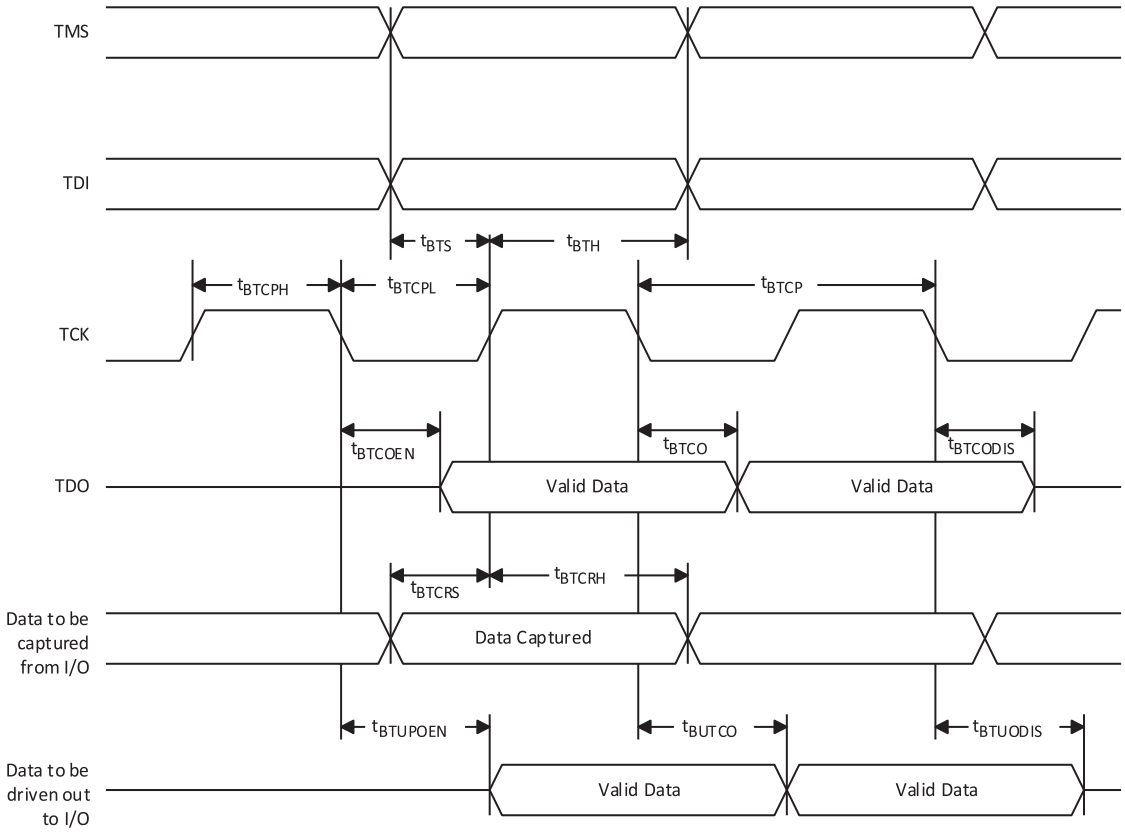

Figure 3.9. JTAG Port Timing Waveforms

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3.22. sysCONFIG Port Timing Specifications

Table 3.27. sysCONFIG Port Timing Specifications

Symbol	Parameter		Commercial/Industrial		Automotive		Unit
			Min.	Max.	Min.	Max.	
All Configuration Modes							
t_{PRGM}	PROGRAMN low pulse accept		55	—	55	—	ns
t_{PRGMJ}	PROGRAMN low pulse rejection		—	25	—	25	ns
t_{INITL}	INITN low time	LCMXO4-010/ LCMXO4-015	—	55	—	93	us
		LCMXO4-015 256-Ball Package/ LCMXO4-025	—	70	—	93	us
		LCMXO4-050	—	105	—	130	us
		LCMXO4-050 400-Ball Package/LCMXO4-080	—	130	—	—	us
		LCMXO4-110C	—	175	—	—	us
$t_{DPPINIT}$	PROGRAMN low to INITN low		—	150	—	150	ns
$t_{DPPDONE}$	PROGRAMN low to DONE low		—	150	—	150	ns
t_{IODISS}	PROGRAMN low to I/O disable		—	120	—	120	ns
Slave SPI							
f_{MAX}	CCLK clock frequency		—	66	—	66	MHz
t_{CCLKH}	CCLK clock pulse width high		7.5	—	7.5	—	ns
t_{CCLKL}	CCLK clock pulse width low		7.5	—	7.5	—	ns
t_{STSU}	CCLK setup time		2	—	2	—	ns
t_{STH}	CCLK hold time		0	—	0	—	ns
t_{STCO}	CCLK falling edge to valid output		—	10	—	14	ns
t_{STOZ}	CCLK falling edge to valid disable		—	10	—	12	ns
t_{STOV}	CCLK falling edge to valid enable		—	10	—	14	ns
t_{SCS}	Chip select high time		25	—	25	—	ns
t_{SCSS}	Chip select setup time		3	—	3	—	ns
t_{SCSH}	Chip select hold time		3	—	3	—	ns
Master SPI							
f_{MAX}	MCLK clock frequency		—	133	—	66	MHz
t_{MCLKH}	MCLK clock pulse width high		3.75	—	7.5	—	ns
t_{MCLKL}	MCLK clock pulse width low		3.75	—	7.5	—	ns
t_{STSU}	MCLK setup time		5	—	6	—	ns
t_{STH}	MCLK hold time		1	—	3	—	ns
t_{CSSPI}	INITN high to chip select low		100	200	100	200	ns
t_{MCLK}	INITN high to first MCLK edge		0.75	1	0.75	1	us

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3.23. I2C Port Timing Specifications

Table 3.28. I2C Port Timing Specification

Symbol	Parameter	Min.	Max.	Unit
f_{MAX}	Maximum SCL clock frequency	—	400	kHz

Notes:

- MachXO4 supports the following modes:
  - Standard-mode (Sm), with a bit rate up to 100 kb/s (user and configuration mode)
  - Fast-mode (Fm), with a bit rate up to 400 kb/s (user and configuration mode)
- Refer to the I2C specification for timing requirements.

3.24. SPI Port Timing Specifications

Table 3.29. SPI Port Timing Specifications

Symbol	Parameter	Min.	Max.	Units
f_{MAX}	Maximum SCK clock frequency	—	45	MHz

Note: Applies to user mode only. For configuration mode timing specifications, refer to sysCONFIG Port Timing Specifications table in this data sheet.

3.25. Switching Test Conditions

Figure 3.9 shows the output test load used for AC testing. The specific values for resistance, capacitance, voltage, and other test conditions are shown in Table 3.29.

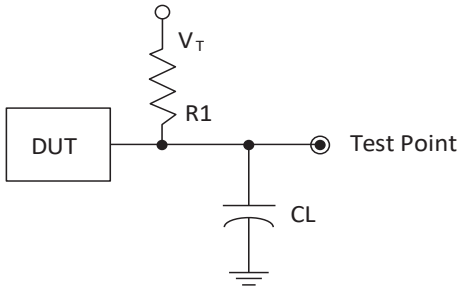

Figure 3.10. Output Test Load, LVTTL and LVCMOS Standards

Table 3.30. Test Fixture Required Components, Non-Terminated Interfaces

Test Condition	R1	CL	Timing Ref.	VT
LVTTL and LVCMOS settings (L -> H, H -> L)	∞	0 pF	LVTTL, LVCMOS 3.3 = 1.5 V	—
			LVCMOS 2.5 = VCCIO/2	—
			LVCMOS 1.8 = VCCIO/2	—
			LVCMOS 1.5 = VCCIO/2	—
			LVCMOS 1.2 = VCCIO/2	—
LVTTL and LVCMOS 3.3 (Z -> H)	188	0 pF	1.5	V_{OL}
LVTTL and LVCMOS 3.3 (Z -> L)			1.5	V_{OH}
Other LVCMOS (Z -> H)			VCCIO/2	V_{OL}
Other LVCMOS (Z -> L)			VCCIO/2	V_{OH}
LVTTL + LVCMOS (H -> Z)			VOH – 0.15	V_{OL}
LVTTL + LVCMOS (L -> Z)			VOL – 0.15	V_{OH}

Note: Output test conditions for all other interfaces are determined by the respective standards.

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4. Signal Descriptions

Table 4.1. Signal Descriptions

Signal Name	I/O	Description
General Purpose		
P[Edge] [Row/Column Number]_[A/B/C/D]	I/O	[Edge] indicates the edge of the device on which the pad is located. Valid edge designations are L (Left), B (Bottom), R (Right), T (Top). [Row/Column Number] indicates the PFU row or the column of the device on which the PIO Group exists. When Edge is T (Top) or (Bottom), only need to specify Row Number. When Edge is L (Left) or R (Right), only need to specify Column Number. [A/B/C/D] indicates the PIO within the group to which the pad is connected. Some of these user-programmable pins are shared with special function pins. When not used as special function pins, these pins can be programmed as I/O for user logic. During configuration of the user-programmable I/O, the user has an option to tri-state the I/O and enable an internal pull-up, pull-down or buskeeper resistor. This option also applies to unused pins (or those not bonded to a package pin). The default during configuration is for user-programmable I/O to be tri-stated with an internal pull-down resistor enabled. When the device is erased, I/O is tri-stated with an internal pull-down resistor enabled. Some pins, such as PROGRAMN and JTAG pins, default to tri-stated I/O with pull-up resistors enabled when the device is erased.
NC	—	No connect.
GND	—	GND – Ground. Dedicated pins. It is recommended that all GNDs are tied together.
V_{CC}	—	V_{CC} – The power supply pins for core logic. Dedicated pins. It is recommended that all V_{CC}s are tied to the same supply.
V_{CCIO}x	—	V_{CCIO} – The power supply pins for I/O Bank x. Dedicated pins. It is recommended that all V_{CCIO}s located in the same bank are tied to the same supply.
PLL and Clock Functions (Used as user-programmable I/O pins when not used for PLL or clock pins)		
[LOC]_GPLL[T, C]_IN	—	Reference Clock (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
[LOC]_GPLL[T, C]_FB	—	Optional Feedback (PLL) input pads: [LOC] indicates location. Valid designations are L (Left PLL) and R (Right PLL). T = true and C = complement.
PCLK [n]_[2:0]	—	Primary Clock pads. One to three clock pads per side.
Test and Programming (Dual function pins used for test access port and during sysCONFIG™)		
TMS	I	Test Mode Select input pin, used to control the 1149.1 state machine.
TCK	I	Test Clock input pin, used to clock the 1149.1 state machine.
TDI	I	Test Data input pin, used to load data into the device using an 1149.1 state machine.
TDO	O	Output pin – Test Data output pin used to shift data out of the device using 1149.1.
JTAGENB	I	Optionally controls behavior of TDI, TDO, TMS, TCK. If the device is configured to use the JTAG pins (TDI, TDO, TMS, TCK) as general purpose I/O, then: If JTAGENB is low: TDI, TDO, TMS and TCK can function a general purpose I/O. If JTAGENB is high: TDI, TDO, TMS and TCK function as JTAG pins. For more details, refer to MachXO4 Programming and Configuration Usage Guide (FPGA-TN-02393).
Configuration (Dual function pins used during sysCONFIG)		
PROGRAMN	I	Initiates configuration sequence when asserted low. This pin is single-ended and always has an active pull-up.
INITN	I/O	Open Drain pin. Indicates the FPGA is ready to be configured. During configuration, a pull-up is enabled. This pin is single-ended.
DONE	I/O	Open Drain pin. Indicates that the configuration sequence is complete, and the start-up sequence is in progress. This pin is single-ended.
MCLK/CCLK	I/O	Input Configuration Clock for configuring an FPGA in Slave SPI mode. Output Configuration Clock for configuring an FPGA in SPI and SPIm configuration modes.
SN	I	Slave SPI active low chip select input.
CSSPIN	I/O	Master SPI active low chip select output.

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Signal Name	I/O	Description
SI/SPISI	I/O	Slave SPI serial data input and master SPI serial data output.
SO/SPISO	I/O	Slave SPI serial data output and master SPI serial data input.
SCL	I/O	Slave I2C clock input and master I2C clock output.
SDA	I/O	Slave I2C data input and master I2C data output.

4.1. Pin Information Summary

Table 4.2. LFMXO4-010 and LFMXO4-015 Pin Summary

	LFMXO4-010			LFMXO4-015					
	TSG100	BSG132	TSG144	UUG36	TSG100	BSG132	TSG144	BBG256	BFG256
General Purpose I/O per Bank									
Bank 0	18	24	26	15	18	24	26	49	49
Bank 1	21	26	26	0	21	26	26	52	52
Bank 2	20	28	28	9	20	28	28	52	52
Bank 3	20	25	26	4	20	25	26	16	16
Bank 4	0	0	0	0	0	0	0	16	16
Bank 5	0	0	0	0	0	0	0	20	20
Total General Purpose Single Ended I/O	79	103	106	28	79	103	106	205	205
Minimum Reserved for Configuration*	1	1	1	1	1	1	1	1	1
Maximum Programmable Single Ended I/O	78	102	105	27	78	102	105	204	204
Differential I/O per Bank									
Bank 0	8	11	12	7	8	11	12	23	23
Bank 1	10	13	13	0	10	13	13	26	26
Bank 2	10	14	14	4	10	14	14	26	26
Bank 3	10	12	13	2	10	12	13	8	8
Bank 4	0	0	0	0	0	0	0	8	8
Bank 5	0	0	0	0	0	0	0	10	10
Total General Purpose Differential I/O	38	50	52	13	38	50	52	101	101
Dual Function I/O	31	33	33	25	31	33	33	33	33

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	LFMXO4-010			LFMXO4-015					
	TSG100	BSG132	TSG144	UUG36	TSG100	BSG132	TSG144	BBG256	BFG256
Number 7:1 or 8:1 Gearboxes									
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	3	5	5	2	3	5	5	12	12
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	5	7	7	2	5	7	7	14	14
High-speed Differential Outputs									
Bank 0	3	5	5	2	3	5	5	12	12
VCCIO Pins									
Bank 0	3	4	4	2	3	4	4	5	5
Bank 1	2	3	3	0	2	3	3	4	4
Bank 2	2	3	3	1	2	3	3	4	4
Bank 3	3	3	3	1	3	3	3	1	1
Bank 4	0	0	0	0	0	0	0	2	2
Bank 5	0	0	0	0	0	0	0	1	1
VCC	2	4	4	2	2	4	4	8	8
GND	8	11	13	2	8	11	13	25	25
NC	1	1	8	0	1	1	8	1	1
Total Count of Bonded Pins	100	132	144	36	100	132	144	256	256

***Note:** One pin for JTAGENB or four pins for JTAG.

Table 4.3. LFMXO4-025 Pin Summary

	LFMXO4-025					
	UUG49	TSG100	BSG132	TSG144	BBG256	BFG256
General Purpose I/O per Bank						
Bank 0	19	18	24	26	49	49
Bank 1	0	21	26	28	52	52
Bank 2	13	20	28	28	52	52
Bank 3	0	6	7	8	16	16
Bank 4	0	6	8	10	16	16
Bank 5	6	8	10	10	20	20
Total General Purpose Single Ended I/O	38	79	103	110	205	205
Minimum Reserved for Configuration*	1	1	1	1	1	1
Maximum Programmable Single Ended I/O	37	78	102	109	204	204

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	LFMXO4-025					
	UUG49	TSG100	BSG132	TSG144	BBG256	BFG256
Differential I/O per Bank						
Bank 0	9	8	11	12	23	23
Bank 1	0	10	13	14	26	26
Bank 2	6	10	14	14	26	26
Bank 3	0	3	3	4	8	8
Bank 4	0	3	4	5	8	8
Bank 5	3	4	5	5	10	10
Total General Purpose Differential I/O	18	38	50	54	101	101
Dual Function I/O	25	31	33	33	33	33
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	4	3	6	7	12	12
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	6	10	14	14	14	14
High-speed Differential Outputs						
Bank 0	4	3	6	7	12	12
VCCIO Pins						
Bank 0	2	3	4	4	5	5
Bank 1	0	2	3	3	4	4
Bank 2	1	2	3	3	4	4
Bank 3	0	1	1	1	1	1
Bank 4	0	1	1	1	2	2
Bank 5	1	1	1	1	1	1
VCC	2	2	4	4	8	8
GND	5	8	11	13	25	25
NC	0	1	1	4	1	1
Total Count of Bonded Pins	49	100	132	144	256	256

***Note:** One pin for JTAGENB or four pins for JTAG.

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Table 4.4. LFMXO4-050 Pin Summary

	LFMXO4-050					
	UUG81	**BSG132**	**TSG144**	**BBG256**	**BFG256**	**BBG400**
General Purpose I/O per Bank						
Bank 0	28	24	26	49	49	82
Bank 1	0	26	29	52	52	84
Bank 2	20	28	29	52	52	84
Bank 3	7	7	9	16	16	28
Bank 4	0	8	10	16	16	24
Bank 5	7	10	10	20	20	32
Total General Purpose Single Ended I/O	62	103	113	205	205	334
Minimum Reserved for Configuration*	1	1	1	1	1	1
Maximum Programmable Single Ended I/O	61	102	112	204	204	333
Differential I/O per Bank						
Bank 0	13	11	12	23	23	40
Bank 1	0	13	14	26	26	42
Bank 2	10	14	14	26	26	42
Bank 3	3	3	4	8	8	14
Bank 4	0	4	5	8	8	12
Bank 5	3	5	5	10	10	16
Total General Purpose Differential I/O	29	50	54	101	101	166
Dual Function I/O	25	37	37	37	37	37
Number 7:1 or 8:1 Gearboxes						
Number of 7:1 or 8:1 Output Gearboxes Available (Bank 0)	8	6	7	16	16	19
Number of 7:1 or 8:1 Input Gearboxes Available (Bank 2)	10	14	14	18	18	21
High-speed Differential Outputs						
Bank 0	8	6	7	16	16	19
VCCIO Pins						
Bank 0	4	4	4	5	5	6
Bank 1	0	3	3	4	4	5
Bank 2	2	3	3	4	4	5
Bank 3	1	1	1	1	1	2
Bank 4	0	1	1	2	2	2
Bank 5	1	1	1	1	1	2
VCC	4	4	4	8	8	10
GND	7	11	13	25	25	34
NC	0	1	1	1	1	0
Total Count of Bonded Pins	81	132	144	256	256	400

***Note:** One pin for JTAGENB or four pins for JTAG.

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Table 4.5. LFMXO4-080 Pin Summary

	LFMXO4-080	
	BBG256	**BBG400**
General Purpose I/O per Bank		
Bank 0	49	82
Bank 1	52	84
Bank 2	52	84
Bank 3	16	28
Bank 4	16	24
Bank 5	20	32
Total General Purpose Single Ended I/O	205	334
Minimum Reserved for Configuration*	1	1
Maximum Programmable Single Ended I/O	204	333
Differential I/O per Bank		
Bank 0	23	40
Bank 1	26	42
Bank 2	26	42
Bank 3	8	14
Bank 4	8	12
Bank 5	10	16
Total General Purpose Differential I/O	101	166
Dual Function I/O	37	37
Number 7:1 or 8:1 Gearboxes		
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	18	19
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	21
High-speed Differential Outputs		
Bank 0	18	19
VCCIO Pins		
Bank 0	5	6
Bank 1	4	5
Bank 2	4	5
Bank 3	1	2
Bank 4	2	2
Bank 5	1	2
VCC	8	10
GND	25	34
NC	1	0
Total Count of Bonded Pins	256	400

***Note:** One pin for JTAGENB or four pins for JTAG.

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Table 4.6. LFMXO4-110 Pin Summary

	LFMXO4-110		
	BBG256	**BBG400**	**BBG484**
General Purpose I/O per Bank			
Bank 0	49	82	94
Bank 1	52	84	96
Bank 2	52	84	96
Bank 3	16	28	36
Bank 4	16	24	24
Bank 5	20	32	36
Total General Purpose Single Ended I/O	205	334	382
Minimum Reserved for Configuration*	1	1	1
Maximum Programmable Single Ended I/O	204	333	381
Differential I/O per Bank			
Bank 0	23	40	46
Bank 1	26	42	48
Bank 2	26	42	48
Bank 3	8	14	18
Bank 4	8	12	12
Bank 5	10	16	18
Total General Purpose Differential I/O	101	166	190
Dual Function I/O	37	37	45
Number 7:1 or 8:1 Gearboxes			
Number of 7:1 or 8:1 Output Gearbox Available (Bank 0)	18	20	22
Number of 7:1 or 8:1 Input Gearbox Available (Bank 2)	20	22	24
High-speed Differential Outputs			
Bank 0	18	20	22
VCCIO Pins			
Bank 0	5	6	10
Bank 1	4	5	9
Bank 2	4	5	9
Bank 3	1	2	3
Bank 4	2	2	3
Bank 5	1	2	3
VCC	8	10	12
GND	25	34	53
NC	1	0	0
Total Count of Bonded Pins	256	400	484

***Note:** One pin for JTAGENB or four pins for JTAG.

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5. MachXO4 Part Number Description

LFMXO4 – XXX X X – X XXXXXX X XX

Device Family:
MachXO4 FPGA

Logic Capacity:
010 = 896 LUTs
015 = 1280 LUTs
025 = 2112 LUTs
050 = 4320 LUTs
080 = 6864 LUTs
110 = 9400 LUTs

Power/Performance:
H = High Performance

Supply Voltage:
C = 2.5 V / 3.3 V
E = 1.2 V

Speed:
5 = Slow
6 = Fast
} High Performance

Shipping Method:
Blank = Trays
TR = Tape and Reel
TR1K = 1000 parts per reel

Grade:
C = Commercial
I = Industrial
A = Automotive

Package:
UUG36 = 36-Ball WLCSP (0.4 mm pitch)
UUG49 = 49-Ball WLCSP (0.4 mm pitch)
UUG81 = 81-Ball WLCSP (0.4 mm pitch)
TSG100 = 100-Pin TQFP (0.5 mm pitch)
BSG132 = 132-Ball csBGA (0.5 mm pitch)
TSG144 = 144-Pin TQFP (0.5 mm pitch)
BBG256 = 256-Ball caBGA (0.8 mm pitch)
BBG400 = 400-Ball caBGA (0.8 mm pitch)
BBG484 = 484-Ball caBGA (0.8 mm pitch)
BFG256 = 256-Ball ftBGA (1.0 mm pitch)

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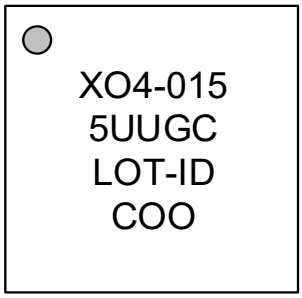
6. Ordering Information

- For all MachXO4 devices in 100-TQFP and 132-csBGA packages, the top-side marking below is used.

- For all MachXO4 devices in WLCSP packages, the markings are abbreviated and adhered to the sample format shown below.



- Other MachXO4 devices have a topside marking format as shown below.

6.1. MachXO4 High Performance Commercial Grade Devices, Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-010HE-5TSG100C	896	1.2 V	5	TSG100	100	COM
LFMXO4-010HE-6TSG100C	896	1.2 V	6	TSG100	100	COM
LFMXO4-010HE-5BSG132C	896	1.2 V	5	BSG132	132	COM
LFMXO4-010HE-6BSG132C	896	1.2 V	6	BSG132	132	COM
LFMXO4-010HE-5TSG144C	896	1.2 V	5	TSG144	144	COM
LFMXO4-010HE-6TSG144C	896	1.2 V	6	TSG144	144	COM

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Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-010HC-5TSG100C	896	2.5 V / 3.3 V	5	TSG100	100	COM
LFMXO4-010HC-6TSG100C	896	2.5 V / 3.3 V	6	TSG100	100	COM
LFMXO4-010HC-5BSG132C	896	2.5 V / 3.3 V	5	BSG132	132	COM
LFMXO4-010HC-6BSG132C	896	2.5 V / 3.3 V	6	BSG132	132	COM
LFMXO4-010HC-5TSG144C	896	2.5 V / 3.3 V	5	TSG144	144	com
LFMXO4-010HC-6TSG144C	896	2.5 V / 3.3 V	6	TSG144	144	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-015HE-5UUG36C	1280	1.2 V	5	UUG36	36	COM
LFMXO4-015HE-5UUG36CTR1K	1280	1.2 V	5	UUG36	36	COM
LFMXO4-015HE-5TSG100C	1280	1.2 V	5	TSG100	100	COM
LFMXO4-015HE-6TSG100C	1280	1.2 V	6	TSG100	100	COM
LFMXO4-015HE-5BSG132C	1280	1.2 V	5	BSG132	132	COM
LFMXO4-015HE-6BSG132C	1280	1.2 V	6	BSG132	132	COM
LFMXO4-015HE-5TSG144C	1280	1.2 V	5	TSG144	144	COM
LFMXO4-015HE-6TSG144C	1280	1.2 V	6	TSG144	144	COM
LFMXO4-015HE-5BBG256C	1280	1.2 V	5	BBG256	256	COM
LFMXO4-015HE-6BBG256C	1280	1.2 V	6	BBG256	256	COM
LFMXO4-015HE-5BFG256C	1280	1.2 V	5	BFG256	256	COM
LFMXO4-015HE-6BFG256C	1280	1.2 V	6	BFG256	256	COM
LFMXO4-015HC-5TSG100C	1280	2.5 V / 3.3 V	5	TSG100	100	COM
LFMXO4-015HC-6TSG100C	1280	2.5 V / 3.3 V	6	TSG100	100	COM
LFMXO4-015HC-5BSG132C	1280	2.5 V / 3.3 V	5	BSG132	132	COM
LFMXO4-015HC-6BSG132C	1280	2.5 V / 3.3 V	6	BSG132	132	COM
LFMXO4-015HC-5TSG144C	1280	2.5 V / 3.3 V	5	TSG144	144	COM
LFMXO4-015HC-6TSG144C	1280	2.5 V / 3.3 V	6	TSG144	144	COM
LFMXO4-015HC-5BBG256C	1280	2.5 V / 3.3 V	5	BBG256	256	COM
LFMXO4-015HC-6BBG256C	1280	2.5 V / 3.3 V	6	BBG256	256	COM
LFMXO4-015HC-5BFG256C	1280	2.5 V / 3.3 V	5	BFG256	256	COM
LFMXO4-015HC-6BFG256C	1280	2.5 V / 3.3 V	5	BFG256	256	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-025HE-5UUG49C	2112	1.2 V	5	UUG49	49	COM
LFMXO4-025HE-5UUG49CTR1K	2112	1.2 V	5	UUG49	49	COM
LFMXO4-025HE-5TSG100C	2112	1.2 V	5	TSG100	100	COM
LFMXO4-025HE-6TSG100C	2112	1.2 V	6	TSG100	100	COM
LFMXO4-025HE-5BSG132C	2112	1.2 V	5	BSG132	132	COM
LFMXO4-025HE-6BSG132C	2112	1.2 V	6	BSG132	132	COM
LFMXO4-025HE-5TSG144C	2112	1.2 V	5	TSG144	144	COM
LFMXO4-025HE-6TSG144C	2112	1.2 V	6	TSG144	144	COM
LFMXO4-025HE-5BBG256C	2112	1.2 V	5	BBG256	256	COM
LFMXO4-025HE-6BBG256C	2112	1.2 V	6	BBG256	256	COM
LFMXO4-025HE-5BFG256C	2112	1.2 V	5	BFG256	256	COM
LFMXO4-025HE-6BFG256C	2112	1.2 V	6	BFG256	256	COM
LFMXO4-025HC-5TSG100C	2112	2.5 V / 3.3 V	5	TSG100	100	COM
LFMXO4-025HC-6TSG100C	2112	2.5 V / 3.3 V	6	TSG100	100	COM
LFMXO4-025HC-5BSG132C	2112	2.5 V / 3.3 V	5	BSG132	132	COM
LFMXO4-025HC-6BSG132C	2112	2.5 V / 3.3 V	6	BSG132	132	COM

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Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-025HC-5TSG144C	2112	2.5 V / 3.3 V	5	TSG144	144	COM
LFMXO4-025HC-6TSG144C	2112	2.5 V / 3.3 V	6	TSG144	144	COM
LFMXO4-025HC-5BBG256C	2112	2.5 V / 3.3 V	5	BBG256	256	COM
LFMXO4-025HC-6BBG256C	2112	2.5 V / 3.3 V	6	BBG256	256	COM
LFMXO4-025HC-5BFG256C	2112	2.5 V / 3.3 V	5	BFG256	256	COM
LFMXO4-025HC-6BFG256C	2112	2.5 V / 3.3 V	6	BFG256	256	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-050HE-5UUG81C	4320	1.2 V	5	UUG81	81	COM
LFMXO4-050HE-5UUG81CTR1K	4320	1.2 V	5	UUG81	81	COM
LFMXO4-050HE-5BSG132C	4320	1.2 V	5	BSG132	132	COM
LFMXO4-050HE-6BSG132C	4320	1.2 V	6	BSG132	132	COM
LFMXO4-050HE-5TSG144C	4320	1.2 V	5	TSG144	144	COM
LFMXO4-050HE-6TSG144C	4320	1.2 V	6	TSG144	144	COM
LFMXO4-050HE-5BBG256C	4320	1.2 V	5	BBG256	256	COM
LFMXO4-050HE-6BBG256C	4320	1.2 V	6	BBG256	256	COM
LFMXO4-050HE-5BBG400C	4320	1.2 V	5	BBG400	400	COM
LFMXO4-050HE-6BBG400C	4320	1.2 V	6	BBG400	400	COM
LFMXO4-050HE-5BFG256C	4320	1.2 V	5	BFG256	256	COM
LFMXO4-050HE-6BFG256C	4320	1.2 V	6	BFG256	256	COM
LFMXO4-050HC-5BSG132C	4320	2.5 V / 3.3 V	5	BSG132	132	COM
LFMXO4-050HC-6BSG132C	4320	2.5 V / 3.3 V	6	BSG132	132	COM
LFMXO4-050HC-5TSG144C	4320	2.5 V / 3.3 V	5	TSG144	144	COM
LFMXO4-050HC-6TSG144C	4320	2.5 V / 3.3 V	6	TSG144	144	COM
LFMXO4-050HC-5BBG256C	4320	2.5 V / 3.3 V	5	BBG256	256	COM
LFMXO4-050HC-6BBG256C	4320	2.5 V / 3.3 V	6	BBG256	256	COM
LFMXO4-050HC-5BBG400C	4320	2.5 V / 3.3 V	5	BBG400	400	COM
LFMXO4-050HC-6BBG400C	4320	2.5 V / 3.3 V	6	BBG400	400	COM
LFMXO4-050HC-5BFG256C	4320	2.5 V / 3.3 V	5	BFG256	256	COM
LFMXO4-050HC-6BFG256C	4320	2.5 V / 3.3 V	6	BFG256	256	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-080HE-5BBG256C	6864	1.2 V	5	BBG256	256	COM
LFMXO4-080HE-6BBG256C	6864	1.2 V	6	BBG256	256	COM
LFMXO4-080HE-5BBG400C	6864	1.2 V	5	BBG400	400	COM
LFMXO4-080HE-6BBG400C	6864	1.2 V	6	BBG400	400	COM
LFMXO4-080HC-5BBG256C	6864	2.5 V / 3.3 V	5	BBG256	256	COM
LFMXO4-080HC-6BBG256C	6864	2.5 V / 3.3 V	6	BBG256	256	COM
LFMXO4-080HC-5BBG400C	6864	2.5 V / 3.3 V	5	BBG400	400	COM
LFMXO4-080HC-6BBG400C	6864	2.5 V / 3.3 V	6	BBG400	400	COM

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-110HE-5BBG256C	9400	1.2 V	5	BBG256	256	COM
LFMXO4-110HE-6BBG256C	9400	1.2 V	6	BBG256	256	COM
LFMXO4-110HE-5BBG400C	9400	1.2 V	5	BBG400	400	COM
LFMXO4-110HE-6BBG400C	9400	1.2 V	6	BBG400	400	COM
LFMXO4-110HE-5BBG484C	9400	1.2 V	5	BBG484	484	COM
LFMXO4-110HE-6BBG484C	9400	1.2 V	6	BBG484	484	COM

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Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-110HC-5BBG256C	9400	2.5 V / 3.3 V	5	BBG256	256	COM
LFMXO4-110HC-6BBG256C	9400	2.5 V / 3.3 V	6	BBG256	256	COM
LFMXO4-110HC-5BBG400C	9400	2.5 V / 3.3 V	5	BBG400	400	COM
LFMXO4-110HC-6BBG400C	9400	2.5 V / 3.3 V	6	BBG400	400	COM
LFMXO4-110HC-5BBG484C	9400	2.5 V / 3.3 V	5	BBG484	484	COM
LFMXO4-110HC-6BBG484C	9400	2.5 V / 3.3 V	6	BBG484	484	COM

6.2. MachXO4 High Performance Industrial Grade Devices, Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-010HE-5TSG100I	896	1.2 V	5	TSG100	100	IND
LFMXO4-010HE-6TSG100I	896	1.2 V	6	TSG100	100	IND
LFMXO4-010HE-5BSG132I	896	1.2 V	5	BSG132	132	IND
LFMXO4-010HE-6BSG132I	896	1.2 V	6	BSG132	132	IND
LFMXO4-010HE-5TSG144I	896	1.2 V	5	TSG144	144	IND
LFMXO4-010HE-6TSG144I	896	1.2 V	6	TSG144	144	IND
LFMXO4-010HC-5TSG100I	896	2.5 V / 3.3 V	5	TSG100	100	IND
LFMXO4-010HC-6TSG100I	896	2.5 V / 3.3 V	6	TSG100	100	IND
LFMXO4-010HC-5BSG132I	896	2.5 V / 3.3 V	5	BSG132	132	IND
LFMXO4-010HC-6BSG132I	896	2.5 V / 3.3 V	6	BSG132	132	IND
LFMXO4-010HC-5TSG144I	896	2.5 V / 3.3 V	5	TSG144	144	IND
LFMXO4-010HC-6TSG144I	896	2.5 V / 3.3 V	6	TSG144	144	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-015HE-5UUG36I	1280	1.2 V	5	UUG36	36	IND
LFMXO4-015HE-5UUG36ITR1K	1280	1.2 V	5	UUG36	36	IND
LFMXO4-015HE-5TSG100I	1280	1.2 V	5	TSG100	100	IND
LFMXO4-015HE-6TSG100I	1280	1.2 V	6	TSG100	100	IND
LFMXO4-015HE-5BSG132I	1280	1.2 V	5	BSG132	132	IND
LFMXO4-015HE-6BSG132I	1280	1.2 V	6	BSG132	132	IND
LFMXO4-015HE-5TSG144I	1280	1.2 V	5	TSG144	144	IND
LFMXO4-015HE-6TSG144I	1280	1.2 V	6	TSG144	144	IND
LFMXO4-015HE-5BBG256I	1280	1.2 V	5	BBG256	256	IND
LFMXO4-015HE-6BBG256I	1280	1.2 V	6	BBG256	256	IND
LFMXO4-015HE-5BFG256I	1280	1.2 V	5	BFG256	256	IND
LFMXO4-015HE-6BFG256I	1280	1.2 V	6	BFG256	256	IND
LFMXO4-015HC-5TSG100I	1280	2.5 V / 3.3 V	5	TSG100	100	IND
LFMXO4-015HC-6TSG100I	1280	2.5 V / 3.3 V	6	TSG100	100	IND
LFMXO4-015HC-5BSG132I	1280	2.5 V / 3.3 V	5	BSG132	132	IND
LFMXO4-015HC-6BSG132I	1280	2.5 V / 3.3 V	6	BSG132	132	IND
LFMXO4-015HC-5TSG144I	1280	2.5 V / 3.3 V	5	TSG144	144	IND
LFMXO4-015HC-6TSG144I	1280	2.5 V / 3.3 V	6	TSG144	144	IND
LFMXO4-015HC-5BBG256I	1280	2.5 V / 3.3 V	5	BBG256	256	IND
LFMXO4-015HC-6BBG256I	1280	2.5 V / 3.3 V	6	BBG256	256	IND
LFMXO4-015HC-5BFG256I	1280	2.5 V / 3.3 V	5	BFG256	256	IND
LFMXO4-015HC-6BFG256I	1280	2.5 V / 3.3 V	6	BFG256	256	IND

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Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-025HE-5UUG49I	2112	1.2 V	5	UUG49	49	IND
LFMXO4-025HE-5UUG49ITR1K	2112	1.2 V	5	UUG49	49	IND
LFMXO4-025HE-5TSG100I	2112	1.2 V	5	TSG100	100	IND
LFMXO4-025HE-6TSG100I	2112	1.2 V	6	TSG100	100	IND
LFMXO4-025HE-5BSG132I	2112	1.2 V	5	BSG132	132	IND
LFMXO4-025HE-6BSG132I	2112	1.2 V	6	BSG132	132	IND
LFMXO4-025HE-5TSG144I	2112	1.2 V	5	TSG144	144	IND
LFMXO4-025HE-6TSG144I	2112	1.2 V	6	TSG144	144	IND
LFMXO4-025HE-5BBG256I	2112	1.2 V	5	BBG256	256	IND
LFMXO4-025HE-6BBG256I	2112	1.2 V	6	BBG256	256	IND
LFMXO4-025HE-5BFG256I	2112	1.2 V	5	BFG256	256	IND
LFMXO4-025HE-6BFG256I	2112	1.2 V	6	BFG256	256	IND
LFMXO4-025HC-5TSG100I	2112	2.5 V / 3.3 V	5	TSG100	100	IND
LFMXO4-025HC-6TSG100I	2112	2.5 V / 3.3 V	6	TSG100	100	IND
LFMXO4-025HC-5BSG132I	2112	2.5 V / 3.3 V	5	BSG132	132	IND
LFMXO4-025HC-6BSG132I	2112	2.5 V / 3.3 V	6	BSG132	132	IND
LFMXO4-025HC-5TSG144I	2112	2.5 V / 3.3 V	5	TSG144	144	IND
LFMXO4-025HC-6TSG144I	2112	2.5 V / 3.3 V	6	TSG144	144	IND
LFMXO4-025HC-5BBG256I	2112	2.5 V / 3.3 V	5	BBG256	256	IND
LFMXO4-025HC-6BBG256I	2112	2.5 V / 3.3 V	6	BBG256	256	IND
LFMXO4-025HC-5BFG256I	2112	2.5 V / 3.3 V	5	BFG256	256	IND
LFMXO4-025HC-6BFG256I	2112	2.5 V / 3.3 V	6	BFG256	256	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-050HE-5UUG81I	4320	1.2 V	5	UUG81	81	IND
LFMXO4-050HE-5UUG81ITR1K	4320	1.2 V	5	UUG81	81	IND
LFMXO4-050HE-5BSG132I	4320	1.2 V	5	BSG132	132	IND
LFMXO4-050HE-6BSG132I	4320	1.2 V	6	BSG132	132	IND
LFMXO4-050HE-5TSG144I	4320	1.2 V	5	TSG144	144	IND
LFMXO4-050HE-6TSG144I	4320	1.2 V	6	TSG144	144	IND
LFMXO4-050HE-5BBG256I	4320	1.2 V	5	BBG256	256	IND
LFMXO4-050HE-6BBG256I	4320	1.2 V	6	BBG256	256	IND
LFMXO4-050HE-5BBG400I	4320	1.2 V	5	BBG400	400	IND
LFMXO4-050HE-6BBG400I	4320	1.2 V	6	BBG400	400	IND
LFMXO4-050HE-5BFG256I	4320	1.2 V	5	BFG256	256	IND
LFMXO4-050HE-6BFG256I	4320	1.2 V	6	BFG256	256	IND
LFMXO4-050HC-5BSG132I	4320	2.5 V / 3.3 V	5	BSG132	132	IND
LFMXO4-050HC-6BSG132I	4320	2.5 V / 3.3 V	6	BSG132	132	IND
LFMXO4-050HC-5TSG144I	4320	2.5 V / 3.3 V	5	TSG144	144	IND
LFMXO4-050HC-6TSG144I	4320	2.5 V / 3.3 V	6	TSG144	144	IND
LFMXO4-050HC-5BBG256I	4320	2.5 V / 3.3 V	5	BBG256	256	IND
LFMXO4-050HC-6BBG256I	4320	2.5 V / 3.3 V	6	BBG256	256	IND
LFMXO4-050HC-5BBG400I	4320	2.5 V / 3.3 V	5	BBG400	400	IND
LFMXO4-050HC-6BBG400I	4320	2.5 V / 3.3 V	6	BBG400	400	IND
LFMXO4-050HC-5BFG256I	4320	2.5 V / 3.3 V	5	BFG256	256	IND
LFMXO4-050HC-6BFG256I	4320	2.5 V / 3.3 V	6	BFG256	256	IND

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Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-080HE-5BBG256I	6864	1.2 V	5	BBG256	256	IND
LFMXO4-080HE-6BBG256I	6864	1.2 V	6	BBG256	256	IND
LFMXO4-080HE-5BBG400I	6864	1.2 V	5	BBG400	400	IND
LFMXO4-080HE-6BBG400I	6864	1.2 V	6	BBG400	400	IND
LFMXO4-080HC-5BBG256I	6864	2.5 V / 3.3 V	5	BBG256	256	IND
LFMXO4-080HC-6BBG256I	6864	2.5 V / 3.3 V	6	BBG256	256	IND
LFMXO4-080HC-5BBG400I	6864	2.5 V / 3.3 V	5	BBG400	400	IND
LFMXO4-080HC-6BBG400I	6864	2.5 V / 3.3 V	6	BBG400	400	IND

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-110HE-5BBG256I	9400	1.2 V	5	BBG256	256	IND
LFMXO4-110HE-6BBG256I	9400	1.2 V	6	BBG256	256	IND
LFMXO4-110HE-5BBG400I	9400	1.2 V	5	BBG400	400	IND
LFMXO4-110HE-6BBG400I	9400	1.2 V	6	BBG400	400	IND
LFMXO4-110HE-5BBG484I	9400	1.2 V	5	BBG484	484	IND
LFMXO4-110HE-6BBG484I	9400	1.2 V	6	BBG484	484	IND
LFMXO4-110HC-5BBG256I	9400	2.5 V / 3.3 V	5	BBG256	256	IND
LFMXO4-110HC-6BBG256I	9400	2.5 V / 3.3 V	6	BBG256	256	IND
LFMXO4-110HC-5BBG400I	9400	2.5 V / 3.3 V	5	BBG400	400	IND
LFMXO4-110HC-6BBG400I	9400	2.5 V / 3.3 V	6	BBG400	400	IND
LFMXO4-110HC-5BBG484I	9400	2.5 V / 3.3 V	5	BBG484	484	IND
LFMXO4-110HC-6BBG484I	9400	2.5 V / 3.3 V	6	BBG484	484	IND

6.3. MachXO4 High Performance Automotive Grade Devices, Packaging

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-010HE-5TSG100A	896	1.2 V	5	TSG100	100	AUTO
LFMXO4-010HE-5BSG132A	896	1.2 V	5	BSG132	132	AUTO
LFMXO4-010HC-5TSG100A	896	2.5 V/3.3 V	5	TSG100	100	AUTO
LFMXO4-010HC-5BSG132A	896	2.5 V/3.3 V	5	BSG132	132	AUTO

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-015HE-5TSG100A	1280	1.2 V	5	TSG100	100	AUTO
LFMXO4-015HE-5BSG132A	1280	1.2 V	5	BSG132	132	AUTO
LFMXO4-015HE-5BBG256A	1280	1.2 V	5	BBG256	256	AUTO
LFMXO4-015HC-5TSG100A	1280	2.5 V/3.3 V	5	TSG100	100	AUTO
LFMXO4-015HC-5BSG132A	1280	2.5 V/3.3 V	5	BSG132	132	AUTO
LFMXO4-015HC-5BBG256A	1280	2.5 V/3.3 V	5	BBG256	256	AUTO

Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-025HE-5TSG100A	2112	1.2 V	5	TSG100	100	AUTO
LFMXO4-025HE-5BSG132A	2112	1.2 V	5	BSG132	132	AUTO
LFMXO4-025HE-5BBG256A	2112	1.2 V	5	BBG256	256	AUTO
LFMXO4-025HC-5TSG100A	2112	2.5 V/3.3 V	5	TSG100	100	AUTO
LFMXO4-025HC-5BSG132A	2112	2.5 V/3.3 V	5	BSG132	132	AUTO
LFMXO4-025HC-5BBG256A	2112	2.5 V/3.3 V	5	BBG256	256	AUTO

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Part Number	LUTs	Supply Voltage	Speed	Package	Pins	Temp.
LFMXO4-050HE-5BSG132A	4320	1.2 V	5	BSG132	132	AUTO
LFMXO4-050HE-5BBG256A	4320	1.2 V	5	BBG256	256	AUTO
LFMXO4-050HC-5BSG132A	4320	2.5 V/3.3 V	5	BSG132	132	AUTO
LFMXO4-050HC-5BBG256A	4320	2.5 V/3.3 V	5	BBG256	256	AUTO

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References

- MachXO4 sysCLOCK PLL Design User Guide (FPGA-TN-02391)
- MachXO4 Implementing High-Speed I/O Interface User Guide (FPGA-TN-02410)
- MachXO4 sysI/O User Guide (FPGA-TN-02398)
- MachXO4 Programming and Configuration User Guide (FPGA-TN-02393)
- MachXO4 Hardened Control Functions User Guide (FPGA-TN-02403)
- MachXO4 Soft Error Detection (SED)/Correction (SEC) User Guide (FPGA-TN-02406)
- Using Password Security with MachXO4 Devices (FPGA-TN-02408)
- Power and Thermal Estimation and Management for MachXO4 Devices (FPGA-TN-02409)
- PCB Layout Recommendations for BGA Packages (FPGA-TN-02024)
- Minimizing System Interruption During Configuration Using TransFR Technology (FPGA-TN-02198)
- Boundary Scan Testability with Lattice sysI/O Capability (AN8066)
- MachXO4 Device Pinout Files
- Thermal Management (FPGA-TN-02044)
- Lattice Design Tools
- MachXO4 Family Web Page
- Boards, Demos, IP Cores and Reference Designs for MachXO4 Family Devices
- Lattice Insights for Training Series and Learning Plans

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Revision History

Revision 1.0, December 2025

Section	Change Summary

All	• Performed minor grammatical and typographical edits.
	• Provided URL to all the references in this document.
	• Removed NVCM globally.
	• Made the following global changes:
	  • from MachXO4-010 to LFMXO4-010;
	  • from MachXO4-015 to LFMXO4-015;
	  • from MachXO4-020 to LFMXO4-020;
	  • from MachXO4-050 to LFMXO4-050;
	  • from MachXO4-080 to LFMXO4-080;
	  • from MachXO4-110 to LFMXO4-110.

Introduction	• Updated to *The MachXO4 family consists of low-power, instant-on, non-volatile, and Flash-based FPGAs with six devices* in the description.
	• Removed –1 speed grade from the description.
	• Updated to *milliseconds* in Non-volatile, Multi-time Reconfigurable of the Features section.
	• Newly added Table 1.1. Specification Status for MachXO4 Family Devices.
	• Table 1.2. MachXO4 Family Selection Guide:
	  • added note superscripts for LUTs for LFMXO4-080 and LFMXO4-110 parts;
	  • removed note superscripts from 256-ball caBGA (14 mm x 14 mm, 0.8 mm) of LFMXO4-080 and LFMXO4-110;
	  • changed Device Options HC for LFMXO4-110 part to *No*;
	  • updated Note 3 to the current;
	  • updated Note 6 adding HC and HE variants.

Architecture	• Updated Figure 2.1. Top View of the LFMXO4-015 and to Figure 2.2. Top View of the LFMXO4-050 Part the current. • Removed the mentioning of MachXO4 migration files from the Density Shifting section.

DC and Switching Characteristics	• Updated Table 3.5. Hot Socketing Specifications to the current.
	• Table 3.10. sysI/O Recommended Operating Conditions:
	removed the original Note 4.
	• Table 3.11. sysI/O Single-Ended DC Electrical Charateristics1, 2, 4:
	For LVCMO2.5 symbol:
	  • removed 16 from IOL Max (mA);
	  • removed –16 from IOH Max (mA).

Signal Description	Updated all the package information to the current in Table 4.2. LFMXO4-010 and LFMXO4-015 Pin Summary, Table 4.3. LFMXO4-025 Pin Summary, Table 4.4. LFMXO4-050 Pin Summary, Table 4.5. LFMXO4-080 Pin Summary, and Table 4.6. LFMXO4-110 Pin Summary.
MachXO4 Part Number Description	Updated the part number description to the current.
Ordering Information	• Updated the three marking diagrams to the current. • Newly added LFMXO4-015HE-5UUG36CTR1K, LFMXO4-025HE-5UUG49CTR1K, and LFMXO4-050HE-5UUG81CTR1K parts and their related information to the MachXO4 High Performance Commercial Grade Devices, Packaging section. • Newly added LFMXO4-015HE-5UUG36ITR1K, LFMXO4-050HE-5UUG81ITR1K, LFMXO4-050HE-5UUG81ITR1K parts and their related information to the MachXO4 High Performance Industrial Grade Devices, Packaging section.
References	Updated the document title of *MachXO4 Implementing High-Speed I/O Interface User Guide (FPGA-TN-02410)* to the current.

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Revision 0.80, June 2025

Section	Change Summary
All	Initial Preliminary release.
Introduction	Table 1.2. MachXO4 Family Selection Guide: Updated MIPI D-PHY Support for LFMXO4-080 and LFMXO4-110 parts to *No*.
DC and Switching Characteristics	Table 3.18. Comparator Specifications1: Updated the Unit to V for V_{IH} parameter.
MachXO4 Part Number Description	Updated the Slowest and the Highest Speed for High Performance parts.
Ordering Information	• MachXO4 Low Power Commercial Grade Devices, Packaging section: Adjusted LUTs for the following parts: LFMXO4-080ZC-1BBG256C LFMXO4-080ZC-2BBG256C LFMXO4-080ZC-3BBG256C LFMXO4-080ZC-1BBG400C LFMXO4-080ZC-2BBG400C LFMXO4-080ZC-3BBG400C • MachXO4 High Performance Industrial Grade Devices, Packaging section: Adjusted LUTs for the following parts: LFMXO4-025HE-5UUG49I LFMXO4-025HE-5TSG100I LFMXO4-025HE-6TSG100I LFMXO4-025HE-5BSG132I LFMXO4-025HE-6BSG132I LFMXO4-025HE-5TSG144I LFMXO4-025HE-6TSG144I LFMXO4-025HE-5BBG256I LFMXO4-025HE-6BBG256I LFMXO4-025HE-5BFG256I LFMXO4-025HE-6BFG256I LFMXO4-025HC-5TSG100I LFMXO4-025HC-6TSG100I LFMXO4-025HC-5BSG132I LFMXO4-025HC-6BSG132I LFMXO4-025HC-5TSG144I LFMXO4-025HC-6TSG144I LFMXO4-025HC-5BBG256I LFMXO4-025HC-6BBG256I LFMXO4-025HC-5BFG256I LFMXO4-025HC-6BFG256I

Revision 0.70, March 2025

Section	Change Summary
All	Initial Advance release.

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