7.5V to 15V, 2A Integrated MOSFET 1ch Synchronous Buck DC/DC Converter

BD95821MUV

●Description

BD95821MUV is a 1ch synchronous buck converter that can generate output voltage (0.8V to 5.5V) at the input voltage range (7.5V to 15V). Space-saving and high efficient switching regulator can be achieved due to built-in N-MOSFET power transistors. The IC also incorporates H^{3}Reg^{TM} technology, a Rohm proprietary constant ON TIME control mode which facilitates ultra-high transient response against changes in load without external compensation components. Fixed soft start function, power good function, and short circuit / over voltage protection with timer latch functions are incorporated. The BD95821MUV is designed for power supplies for Digital AV Equipment.

●Applications

- LCD TVs
- Set Top Boxes (STB)
- DVD/Blu-ray players/recorders
- Broadband Network and Communication Interface
- Amusement, other.

●Features

- Input Voltage Range: 7.5V to 15.0V
- Reference Voltage: 0.8V±1.5%
- Output Voltage Range: 0.8V to 5.5V
- Output Current: 2.0A (Max.)
- Switching Frequency: 500kHz to 800kHz
  (depend on input-output condition)
- Built-in Power MOS FET
  High-side Nch FET ON resistance: 120mΩ(typ.)
  Low-side Nch FET ON resistance: 65mΩ(typ.)
- Fast Transient Responses due to H^{3}Reg control
- Over Current Protection (OCP) – Cycle-by-Cycle
- Thermal Shut Down (TSD)
- Under-Voltage Lock-Out (UVLO)
- Short Circuit Protection (SCP)
- Over Voltage Protection (OVP)
- Fixed Soft Start (1msec ; typ)
- Power Good function

●Package

W(Typ.) x D(Typ.) x H(Max.)

- VQFN016V3030 3.0mm x 3.0mm x 1.0mm

●Typical Application

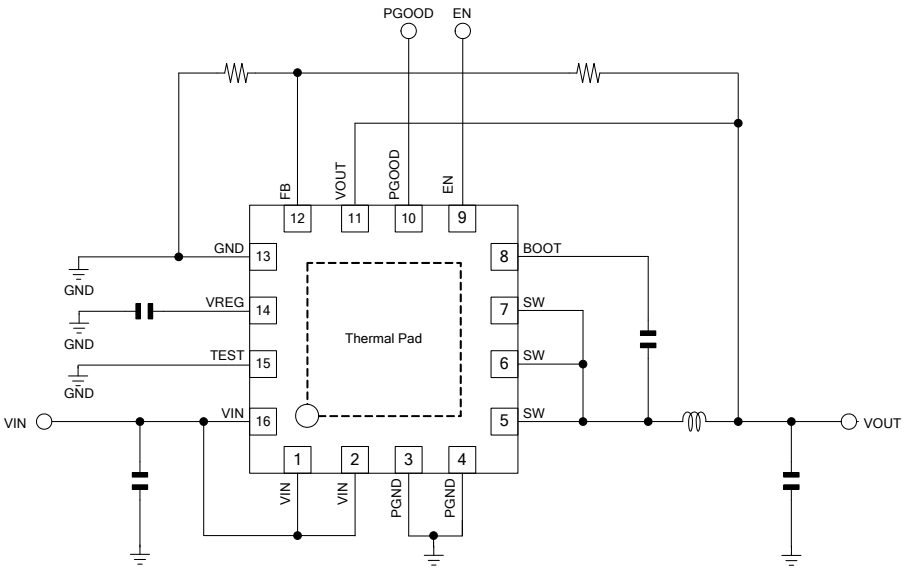


Figure 1. Typical Application Circuit

●Pin Configuration (TOP VIEW)

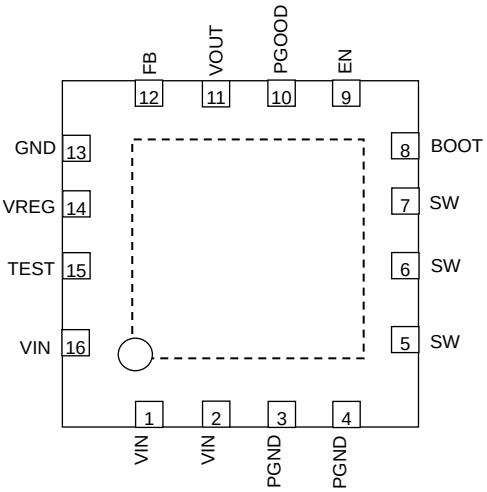


Figure 2 .Pin Configuration

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●Block Diagram

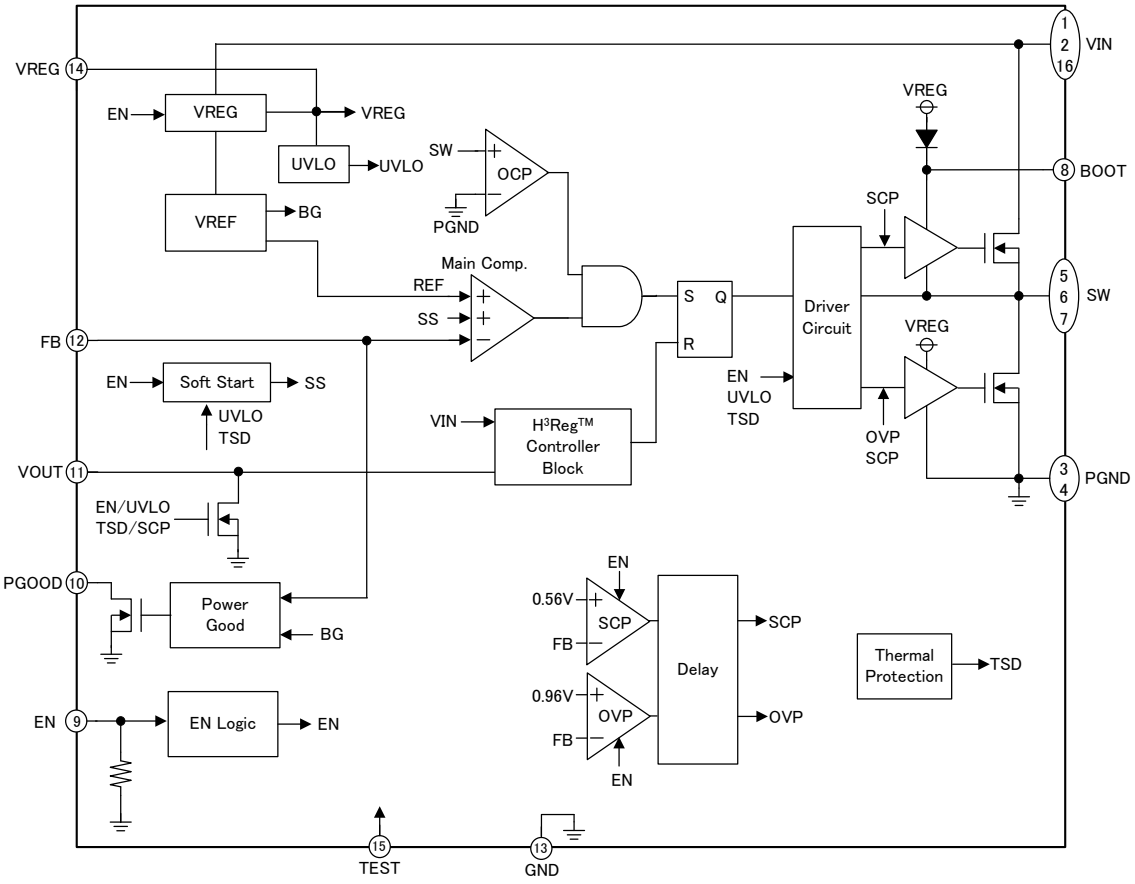


Figure 3. Block Diagram

●Pin Description

No.	Symbol	Description
1, 2, 16	VIN	Input Voltage Supply pin. The IC determines the duty cycles internally based on the input voltage. Therefore, variations of VIN pin can lead to unstable operation. This pin also acts as the input voltage to the internal switching regulator output block, and is sensitive to the impedance of the power supply. Connect over 10μF ceramic capacitors for the decoupling capacitors to PGND as near as these pins.
3, 4	PGND	Power ground pin connected to the source of the Low side FET.
5, 6, 7	SW	Switch node connection between High side FET source and Low side FET drain. Connect 0.01μF capacitor between BOOT and SW. This pin is also connected to inductor (L).
8	BOOT	High side FET Gate Driver Power Supply pin. Connect 0.01μF capacitor between BOOT and SW. BOOT voltage swings from VREG to (VIN + VREG) during normal switching operation.
9	EN	Enable Input pin. When the input voltage of the EN pin reaches at least 2.2V, the switching regulator becomes active. At the voltage less than 0.3 V, the IC becomes standby mode.
10	PGOOD	Open-drain Power Good Output pin. Due to the open-drain output, a 100kΩ pull-up resistor should be connected between this pin and VREG or other power supply. In the case of no use, this pin is opened or shortened to ground.

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●**Pin Description (Continued)**

No.	Symbol	Description
11	VOUT	Output Voltage Sense pin. Connect to output voltage directly. ONTIME is determined by monitoring the output voltage.
12	FB	Output Voltage Feedback pin. FB is compared with REF in the IC. Please set the output voltage in the feedback resistances of less than total 50kΩ. (Refer to page 15)
13	GND	Sense ground pin for all internal analog and digital power supplies.
14	VREG	Power supply output inside IC. When at least 2.2V is supplied to the EN pin, the VREG is active. This pin supplies 5.0V at up to 10mA. Insert a 0.022μF capacitor between this pin and ground pin.
15	TEST	TEST Pin. Connect to ground.
Thermal Pad	-	Exposed Thermal Pad. Connect to ground.

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●Absolute Maximum Ratings (Ta=25℃)

Parameter	Symbol	Limit	Unit	Comment
Input Voltage	VIN	15.2 *1	V	
BOOT Voltage	BOOT	21.5 *1	V	
BOOT-SW Voltage	BOOT-SW	7 *1	V	
Output Voltage	VOUT	7 *1	V	
SW Voltage	SW	15.2 *1	V	
Output Feedback Voltage	FB	VREG	V	
VREG Voltage	VREG	7 *1	V	
EN Input Voltage	EN	15.2 *1	V	
PGOOD Voltage	PGOOD	7 *1	V	
Power Dissipation 1	Pd1	0.27	W	Ta≧25°C (IC only), power dissipated at 2.2mW / °C.
Power Dissipation 2	Pd2	0.62	W	Ta≧25°C (70mm×70mm×1.6mm single-layer board, 6.28mm^2 copper heat dissipation pad), power dissipated at 5.0mW / °C.
Power Dissipation 3	Pd3	1.77	W	Ta≧25°C (70mm × 70mm × 1.6mm 4-layer board, 6.28 mm^2 copper heat dissipation pad on top and bottom layer, 5505 mm^2 pad on 2nd and 3rd layer), power dissipated at 14.1mW / °C.
Power Dissipation 4	Pd4	2.66	W	Ta≧25°C (70mm × 70mm × 1.6mm 4-layer board, all layers with 5505 mm^2 copper heat dissipation pads), power dissipated at 21.3mW / °C.
Operating Temperature Range	Topr	-20 to +100 *1	℃	
Storage Temperature Range	Tstg	-55 to +150	℃	
Junction Temperature	Tjmax	+150	℃	

*1 Not to exceed Pd.

●Operating Ratings (Ta= -20 to 100℃)

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
Input Voltage	VIN	7.5	12	15	V
VREG Voltage	VREG	4.5	5.0	5.5	V
BOOT Voltage	BOOT	4.5	-	21	V
SW Voltage	SW	-0.7	-	15	V
BOOT-SW Voltage	BOOT-SW	4.5	-	5.5	V
EN Input Voltage	EN	0	-	15	V
Output Voltage	VOUT *2	0.8	-	5.5	V
PGOOD Voltage	PGOOD	0	-	5.5	V
Minimum ON Time	Tonmin	-	-	200	nsec

*2 VOUT depends on Input Voltage (VIN) in some cases.

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●**Electrical Characteristics**

(Unless otherwise noted Ta=25℃, VIN=12V, EN=3V, VOUT=3.3V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
VIN Bias Current	I_{IN}	-	1.2	2.0	mA	
VIN Standby Current	I_{IN_STB}	-	2	15	μA	EN=0V
Enable Control						
EN Low Voltage	EN_{LOW}	GND	-	0.3	V	
EN High Voltage	EN_{HIGH}	2.2	-	15	V	
EN Bias Current	I_{EN}	-	3	10	μA	EN=3V
VREG Output Voltage						
VREG Standby Voltage	V_{REG_STB}	-	-	0.1	V	EN=0V
VREG Output Voltage	V_{REG}	4.5	5.0	5.5	V	I_{REG}=10mA
Maximum Output Current	I_{REG}	10	-	-	mA	
Power MOSFET						
High side FET ON Resistance	R_{ONH}	-	120	240	mΩ	
Low side FET ON Resistance	R_{ONL}	-	65	130	mΩ	
Reference Voltage						
FB threshold Voltage	V_{FB}	0.788	0.800	0.812	V	
FB Input Current	I_{FB}	-1	-	1	μA	
H^3Reg Control						
ON Time	T_{ON}	-	470	-	nsec	
Minimum OFF Time	T_{OFFMIN}	200	450	-	nsec	
Soft Start / Output Discharge						
Soft Start Time	T_{SOFT}	-	1.0	-	msec	
VOUT Discharge Current	I_{VOUT}	3	6.6	-	mA	VOUT=1V, EN=0V, V_{REG}=5V

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●**Electrical Characteristics (Continued)**

(Unless otherwise noted Ta=25℃, VIN=12V, EN=3V, VOUT=3.3V)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Over Current Protection						
Over Current Protection Current Limit	I_{OCP}	2.5	3.5	6.0	A	*3
SCP						
SCP Threshold Voltage	V_{SCP}	0.48	0.56	0.64	V	V_{FB}=0.8V → 0V
SCP delay time	T_{SCP}	-	1.0	-	msec	
OVP						
OVP Threshold Voltage	V_{OVP}	0.86	0.96	1.06	V	V_{FB}=0.8V → 2.0V
OVP delay time	T_{OVP}	-	1.0	-	msec	
UVLO						
VREG Threshold Voltage	V_{REG_UVLO}	3.75	4.20	4.65	V	VREG: Sweep up
VREG Hysteresis Voltage	dV_{REG_UVLO}	100	160	220	mV	VREG: Sweep down
Power Good						
V_{FB} Power Good Low Voltage	V_{FB_PL}	0.61	0.68	0.75	V	V_{FB}=0.8V → 0V
V_{FB} Power Good High Voltage	V_{FB_PH}	0.65	0.72	0.79	V	V_{FB}=0V → 0.8V

＊3 No tested on outgoing inspection.

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●**Typical Performance Curves (Unless otherwise noted Ta=25℃, VIN=12V)**

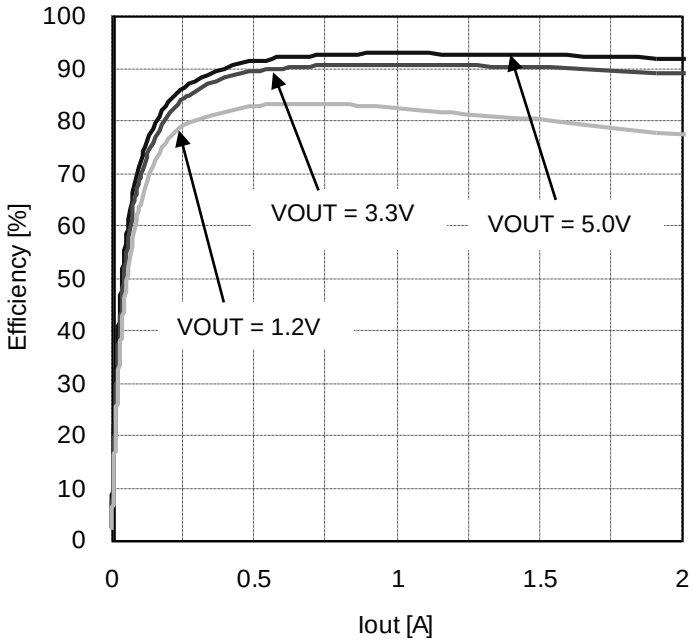


Figure 4. Efficiency
(VIN=12V, L=3.3μH)

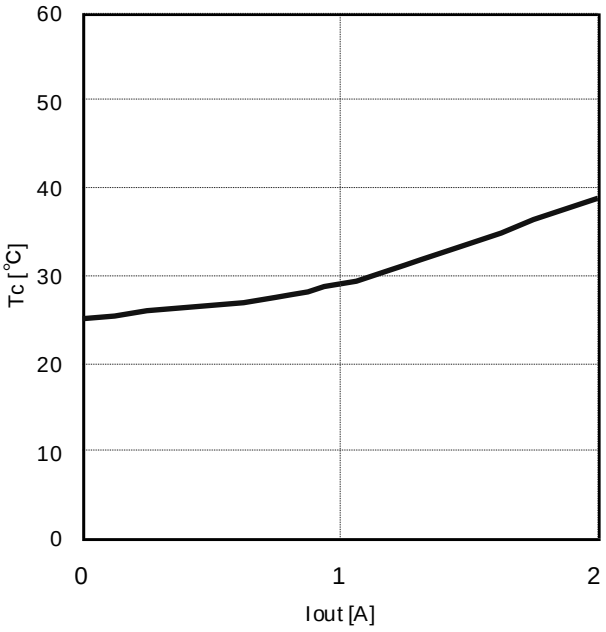


Figure 5. Tc – Iout
(VIN=12V, VOUT=3.3V, L=3.3μH)

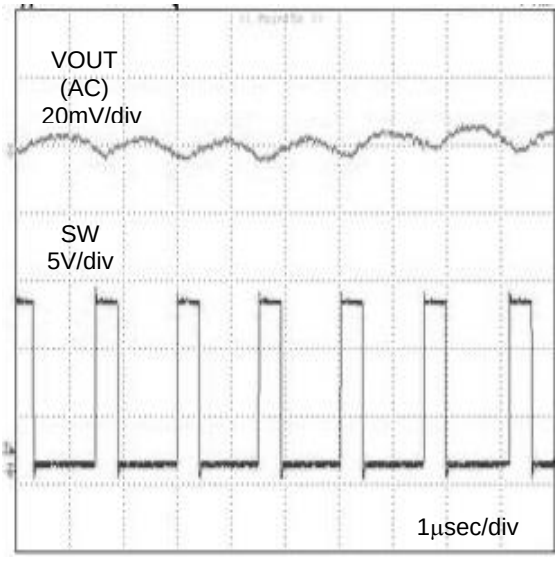


Figure 6. VOUT Ripple voltage
(VIN=12V, VOUT=3.3V, L=3.3μH, COUT=44μF, Iout=0A)

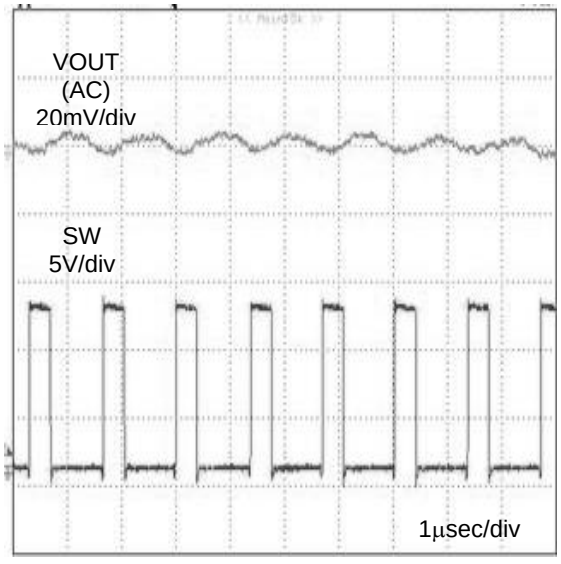


Figure 7. VOUT Ripple voltage
(VIN=12V, VOUT=3.3V, L=3.3μH, COUT=44μF, Iout=2A)

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●**Typical Performance Curves (Unless otherwise noted Ta=25℃, VIN=12V) (Continued)**

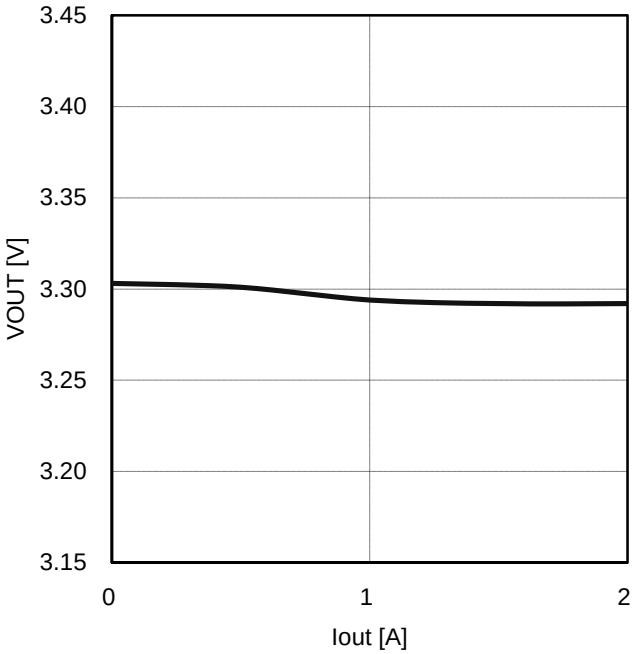


Figure 8. VOUT Load Regulation
(VIN=12V, VOUT=3.3V, L=3.3μH)

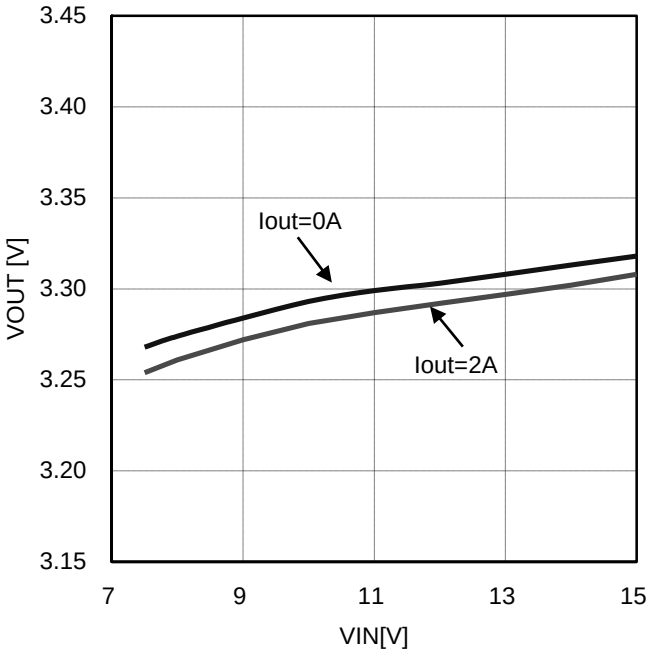


Figure 9. VOUT Line Regulation
(VOUT=3.3V, L=3.3μH, Iout=0A / 2A)

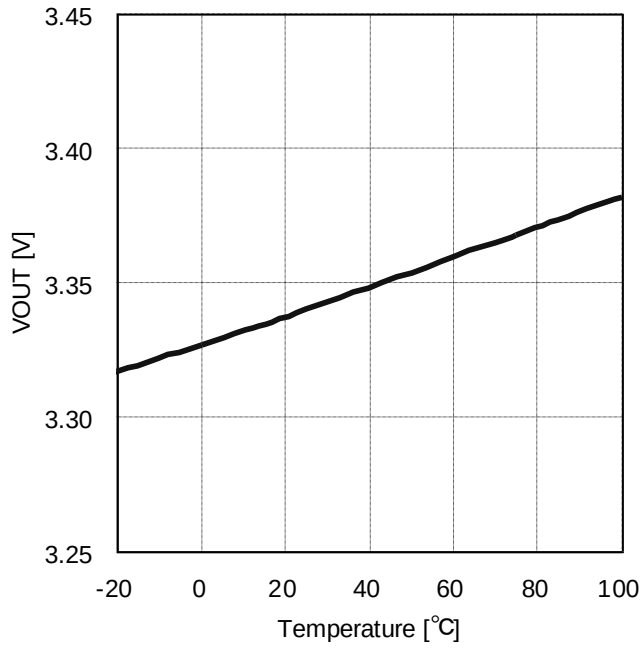


Figure 10. VOUT - Temperature
(VIN=12V, VOUT=3.3V, L=3.3μH, Iout=0A)

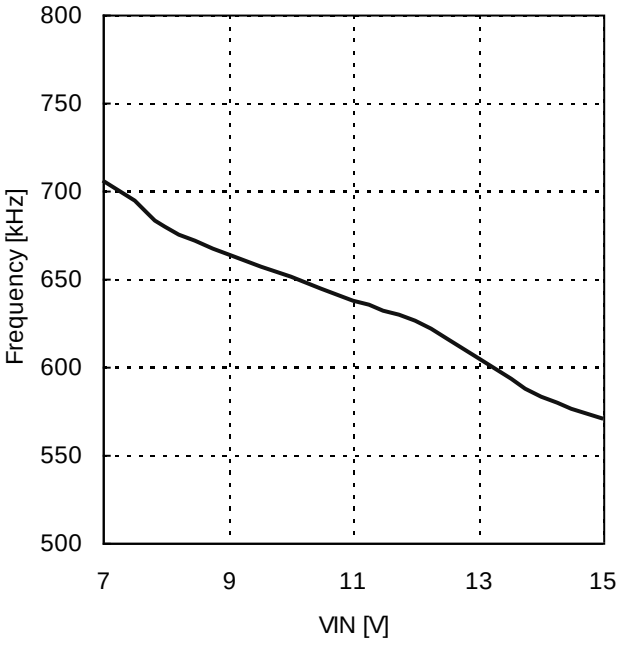


Figure 11. Frequency - VIN
(VIN=12V, VOUT=3.3V, L=3.3μH, Iout=0A)

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●**Typical Performance Curves (Unless otherwise noted Ta=25℃, VIN=12V) (Continued)**

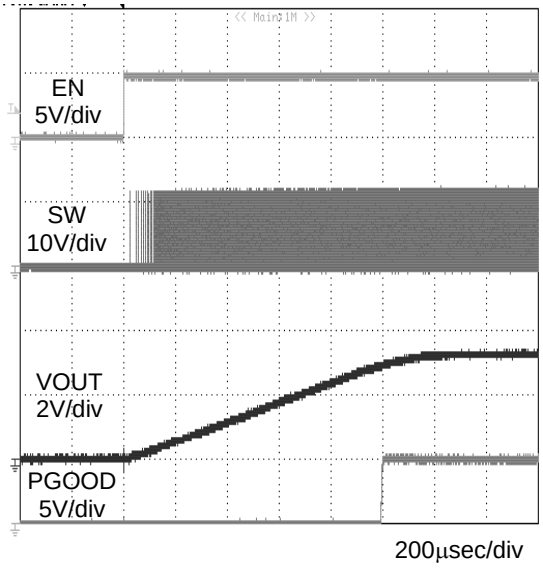


Figure 12. Start up with EN
(VIN=12V, VOUT=3.3V, L=3.3μH, COUT=44μF, Iout=0A)

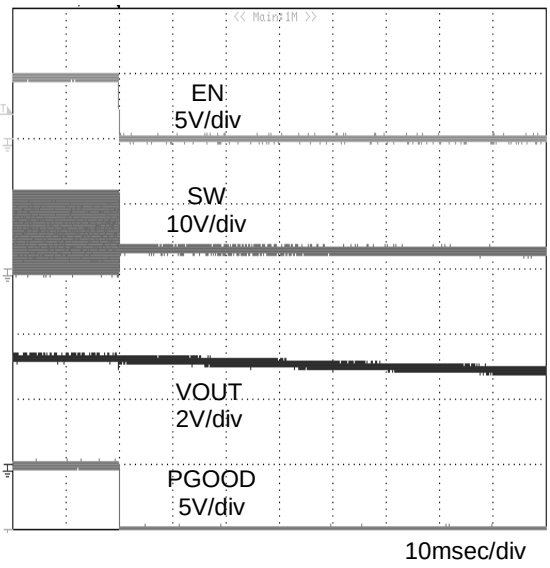


Figure 13. Power down with EN
(VIN=12V, VOUT=3.3V, L=3.3μH, COUT=44μF, Iout=0A)

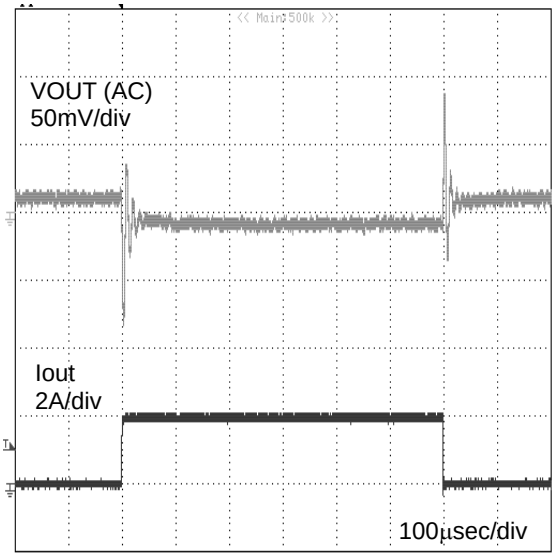


Figure 14. VOUT Transient Response
(VIN=12V, VOUT=3.3V, L=3.3μH, COUT=44μF)
Iout=0⇔2A (SR=1.0A/μsec)

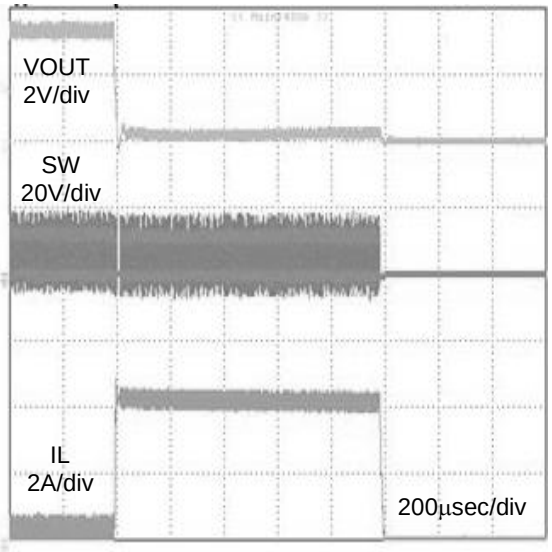


Figure 15. OCP function
(VIN=12V, VOUT=3.3V, L=3.3μH, COUT=44μF)
(VOUT is shorted to ground)

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●Explanation of Operation

The BD95821MUV is a 1ch synchronous buck converter incorporating ROHM's proprietary H³Reg™ CONTROLLA system. When VOUT drops due to a rapid load change, the system quickly restores VOUT by increasing the frequency.

1. H³Reg™ System

1-1. Normal Operation

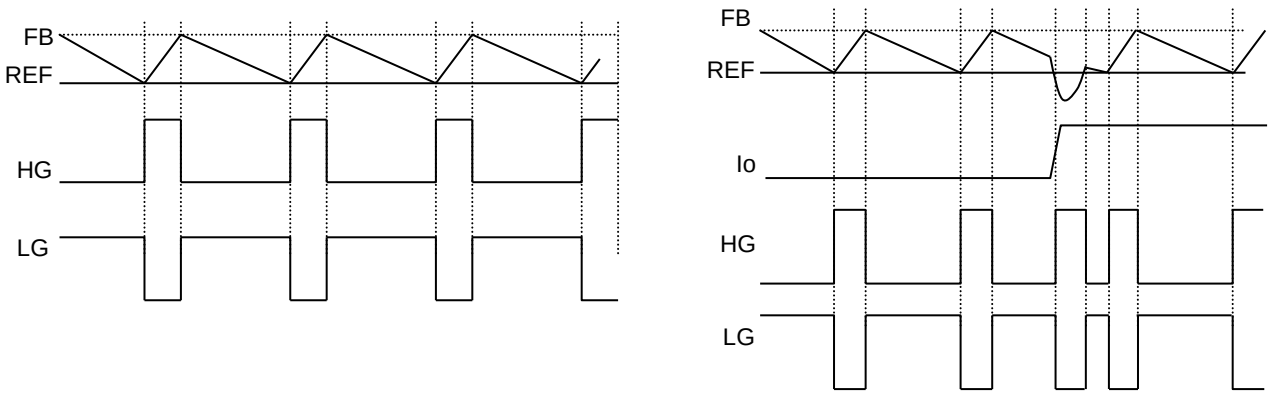
When FB falls below the threshold voltage (REF), a drop is detected, activating the H³Reg™ CONTROLLA system.

$$Ton = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f} \quad [sec] \qquad (1)$$

HG (Gate of High side MOSFET) output is determined by the formula (1). LG (Gate of Low side MOSFET) output operates until FB voltage falls below REF voltage after HG becomes OFF. OFF time is restricted by MIN OFF Time (typ.:450nsec). Hence, BD95821MUV runs with a constant on-time by using the input and output voltage to set the internal on-time timer.

1-2. VOUT drops due to a rapid load change

When FB (VOUT) drops due to a rapid load change and the voltage remains below REF, the system quickly restores VOUT by shortening OFF time of HG (increasing the frequency), improving transient response as shown Figure 16 (b).



(a) Normal operation (b) Rapid load change

Figure 16. H³REG System

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●Timing Chart

1. Soft Start Function

Soft start is utilized when the EN pin is set high. Current control takes effect at startup, enabling a moderate “ramping start” on the output voltage. Soft start time is 1.0msec (typ). Rush current is determined via formula (2) below.

$$I_{IN} = \frac{C_{OUT} \times V_{OUT}}{1.0msec} \quad [A] \quad (2)$$

C_{OUT}: All capacitors connected with V_{OUT}

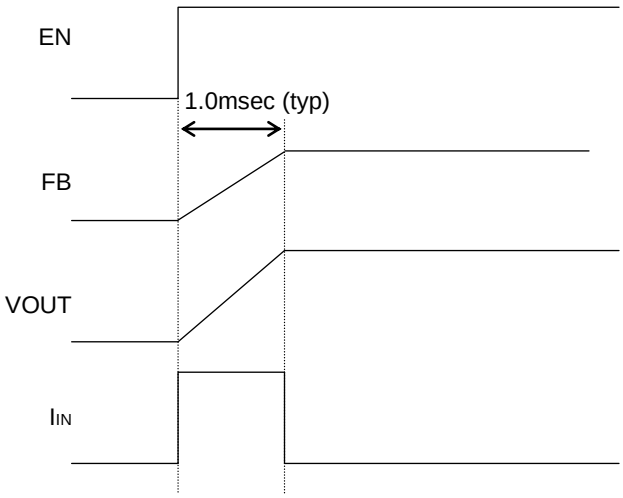


Figure 17. Soft Start Timing Chart

2. Power Good Function

When FB voltage is more than 0.72V (90%), the integrated open-drain NMOS is set to OFF, and PGOOD outputs High due to pull-up register. If FB voltage falls below 0.68V (85%), PGOOD becomes Low.

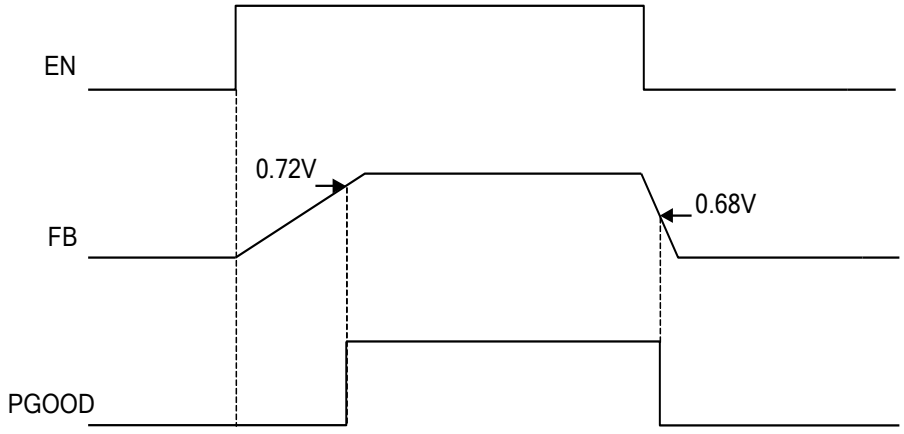


Figure 18. Power Good Timing Chart

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●Protection Operation

1. OCP Operation

Normally, when FB voltage falls below REF voltage, HG becomes high. However, if the current through the inductor (I_L) exceeds OCP current value (I_{OCP}) during LG=ON, HG does not become high and I_L is restricted by I_{OCP}. When I_L falls down below I_{OCP}, HG is stricken by the pulse width of Ton decided by formula (1). As the result, the output voltage can decrease as the frequency and duty are changed.

When OCP is released in the state that the output has decreased by OCP operation, the output voltage might rise up due to high-speed load response. Also OFF Latch is operated when FB voltage becomes below the SCP setting voltage during 1msec (typ.) (Refer to 2-1).

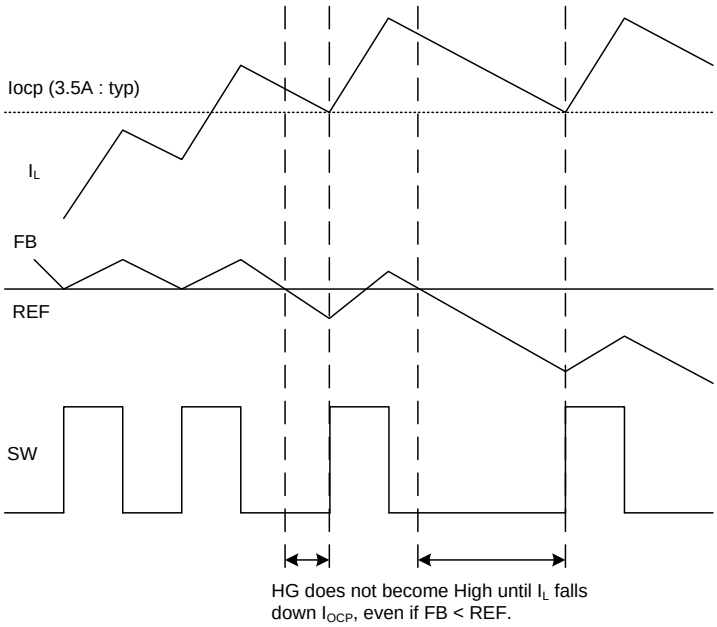


Figure 19. OCP Timing Chart

2. SCP Operation / OVP Operation (OFF Latch)

2-1. SCP Operation

SCP monitors FB voltage. When FB falls below 0.56V, after 1msec (typ.) later, the short circuit protection (SCP) operates, turning the high side MOSFET and low side MOSFET OFF, and performs OFF latch operation.

2-2. OVP Operation

OVP monitors FB voltage. When FB exceeds 0.96V, after 1msec (typ.) later, the output over voltage protection (OVP) operates, turning the high side FET OFF and the low side FET ON, and performs OFF latch operation.

2-3. Recovery from OFF Latch mode

Off latch is released by EN=OFF or UVLO operation, and then it returns to standard operation.

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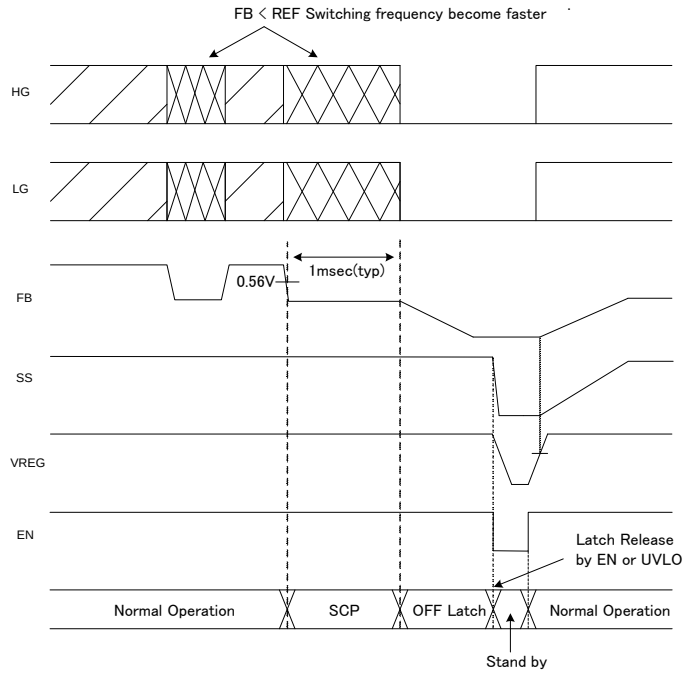


Figure 20. SCP Timing Chart

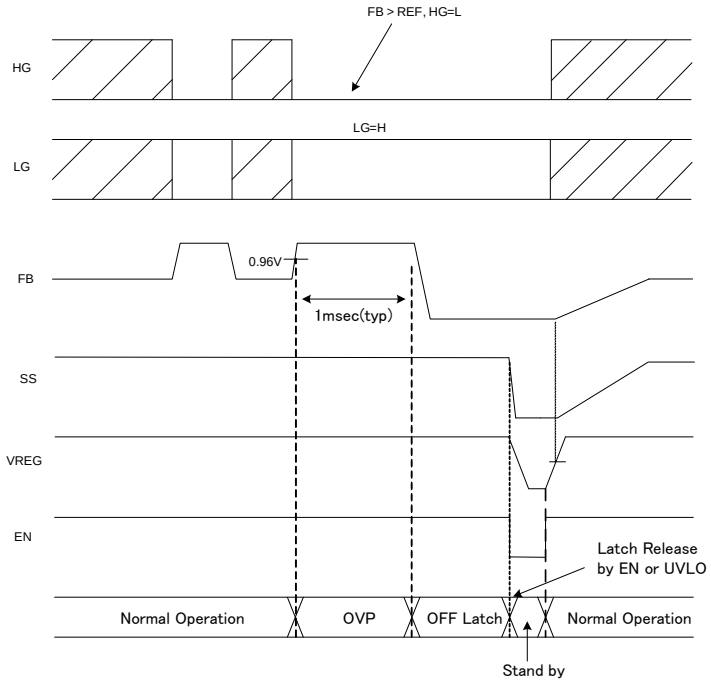


Figure 21. OVP Timing Chart

3. TSD Operation (Self Recovery)

TSD is self-activating. If the junction temperature exceeds Tj = 175℃, and HG, LG, PGOOD, and SS become Low.
The IC becomes standby when TSD operating.
When Tj falls below 150℃, it returns to standard operation.

4. UVLO Operation

UVLO operates when V_{REG} voltage falls below 4.05V, ad HG, LG, PGOOD and SS become Low.
The IC becomes standby when UVLO operating.
UVLO is released when V_{REG} goes up to 4.2V, and starts standard operation

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●Selection of Components Externally Connected

1. Output LC Filter Selection (Buck Converter)

1-1. Inductor (L) Selection

The Output LC filter is required to supply constant current to the output load. A larger value inductance at this filter results in less inductor ripple current (ΔI_L) and less output ripple voltage. However, the larger value inductors tend to have less fast load transient-response, a larger physical size, a lower saturation current and higher series resistance. A smaller value inductance has almost opposite characteristics above.
The recommended inductor values are shown in Table 1(Refer to page 18).

The value of ΔI_L is shown as formula (3).

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times f \times V_{IN}} \quad [A] \qquad (3)$$

For example, with V_{IN} = 12 V, V_{OUT} = 3.3 V, L = 3.3μH and the switching frequency f = 600 kHz, the calculated ripple current ΔI_L is 1.2A.
Then, the inductor saturation current must be larger than the sum of the maximum output current (I_{OUTMAX}) and 1/2 of the inductor ripple current (ΔI_L / 2). A larger current than the inductor's saturation current will cause magnetic saturation in the inductor, and decrease efficiency. When selecting an inductor, be sure to allow enough margins to assure that peak current does not exceed the inductor's saturation current value.
※To minimize loss of inductor and improve efficiency, choose a inductor with a low resistance (DCR, ACR).

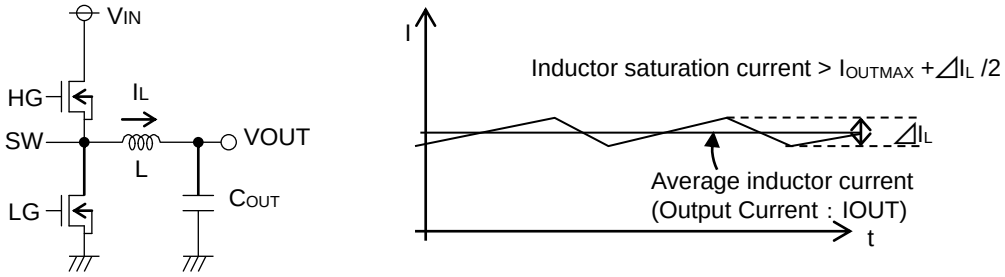


Figure 22. Inductor Ripple Current

1-2. Output Capacitor (C_{OUT}) Selection

Output Capacitor (C_{OUT}) has a considerable influence on output voltage regulation due to a rapid load change and smoothing output ripple voltage. Determine the capacitor by considering the value of capacity, the equivalent series resistance, and equivalent series inductance. Also, make sure the capacitor's voltage rating is high enough for the set output voltage (including ripple).
Output ripple voltage is determined as in formula (4) below.

$$\Delta VOUT = \Delta I_L / (8 \times C_{OUT} \times f) + ESR \times \Delta I_L + ESL \times \Delta I_L / Ton \quad [V] \qquad (4)$$

(ΔI_L Output ripple current、ESR: Equivalent series resistance、ESL: Equivalent series inductance)

Also, give consideration to the conditions in formula (5) below for output capacitance, bearing in mind that output rise time must be established within the fixed soft start time. As output capacitance, bypass capacitor will be also connected to output load side (C_{EXT}, Figure 23). Please set the over current detection value with regards to these capacitance.

$$C_{OUT} \leq \frac{1msec \times (I_{OCP} - I_{OUT})}{V_{OUT}} \quad [F] \qquad (5)$$

(I_{OCP} : OCP Current Limit, I_{OUT} : Output Current)

Note: an improper output capacitor may cause startup malfunctions.

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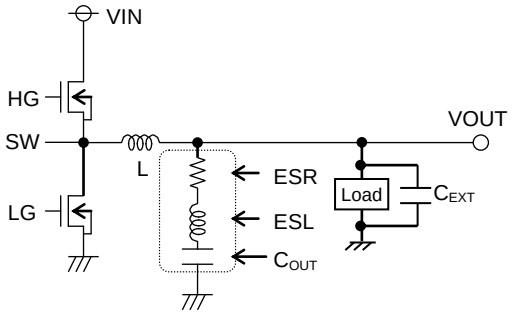


Figure 23. Output Capacitor

2. Input Capacitor (CIN) Selection

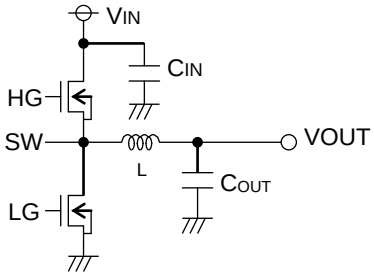


Figure 24. Input Capacitor

In order to prevent transient spikes in voltage, the input capacitor should have a low enough ESR resistance to fully support a large ripple current. The formula for ripple current I_{RMS} is given in equation (6) as below.

$$I_{RMS} = I_{OUT} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}} \quad [A] \quad (6)$$

Where $V_{IN} = 2 \times V_{OUT}$, $I_{RMS} = \frac{I_{OUT}}{2}$

A low ESR capacitor is recommended to reduce ESR loss and improve efficiency.

3. Output Voltage Setting

The IC controls output voltage as REF≒V_{FB}.
However, the actual output voltage will also reflect the average ripple voltage value.
The output voltage is set with a resistor divider from the output node to the FB pin. The formula for output voltage is given in (7) below:

$$\text{Output Voltage} = \frac{R1+R2}{R2} \times \text{REF} + \Delta VOUT \quad [V] \quad (7)$$

$$\text{REF} = V_{FB}(\text{TYP } 0.8V) + 0.02 - (\text{ON DUTY} \times 0.05) \quad [V] \quad (8)$$

$$\text{ON DUTY} = \frac{VOUT}{V_{IN}} \quad (9)$$

Please refer to eq. (4) regarding ΔVOUT.

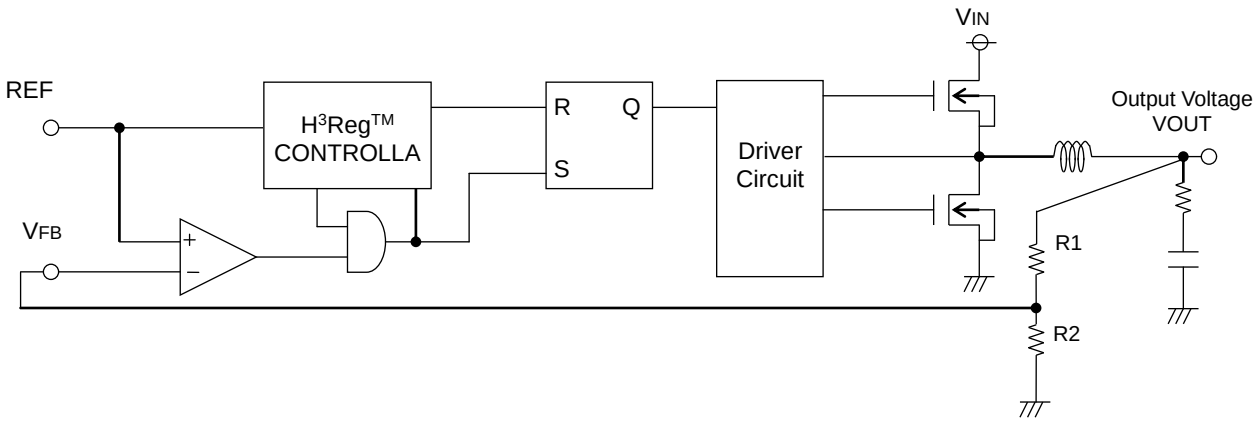


Figure 25. Output Voltage Setting

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4. Relationship between Output Voltage and ONTIME

BD95821MUV is a synchronous buck converter controlling constant ONTIME. The ONTIME (Ton) depends on the output voltage settings, as described by the formula (10).

$$Ton = 1770 \times \frac{V_{OUT}}{V_{IN}} - \frac{610}{V_{IN}} + 55 \quad [nsec] \quad (10)$$

The frequency of the application condition is determined by the formula (11) using the above Ton.

$$Frequency = \frac{VOUT}{V_{IN}} \times \frac{1}{Ton} \quad [kHz] \quad (11)$$

However with actual applications, there exists a rising and falling time of the SW due to the gate capacitance of the integrated MOSFET and the switching speed, which may vary the above parameters. Therefore please also verify those parameters experimentally.

5. Relationship between Output Current and Frequency

BD95821MUV is a constant ontime type of switching regulator. When the output current increases, the switching loss of the inductor, MOSFET, and output capacitor also increases. Hence the switching frequency speeds up.
The loss of the inductor, MOSFET, and output capacitor is determined as below.

① Loss of Inductor = $IOUT^2 \times DCR$

② Loss of MOSFET (High Side) = $IOUT^2 \times R_{ONH} \times \frac{VOUT}{VIN}$

③ Loss of MOSFET (Low Side) = $IOUT^2 \times R_{ONL} \times (1 - \frac{VOUT}{VIN})$

④ Loss of Output Capacitor = $IOUT^2 \times ESR$

(DCR : Inductor Equivalent series resistance、R_{ONH} : On resistance of High-side MOSFET、R_{ONL} : On resistance of Low-side MOSFET、ESR :COUT Equivalent series resistance)

Taking the above losses into the frequency equation, then T (=1/Freq) becomes

$$T\ (=1/Freq) = \frac{VIN \times IOUT \times Ton}{VOUT \times IOUT + ① + ② + ③ + ④} \quad [nsec] \quad (12)$$

However since the parasitic resistance of the PCB layout pattern exists in actual applications and affects the parameter, please also verify experimentally.

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●PCB Layout Guide

Two high pulsing current flowing loops exist in the buck regulator system.
The first loop, when FET is ON, starts from the input capacitors, to the VIN terminal, to the SW terminal, to the inductor, to the output capacitors, and then returns to the input capacitor through GND.
The second loop, when FET is OFF, starts from the low FET, to the inductor, to the output capacitor, and then returns to the low FET through GND.
To reduce the noise and improve the efficiency, please minimize these two loop area.
Especially input capacitor and output capacitor should be connected to GND (PGND) plain.
PCB Layout may affect the thermal performance, noise and efficiency greatly. So please take extra care when designing PCB Layout patterns.

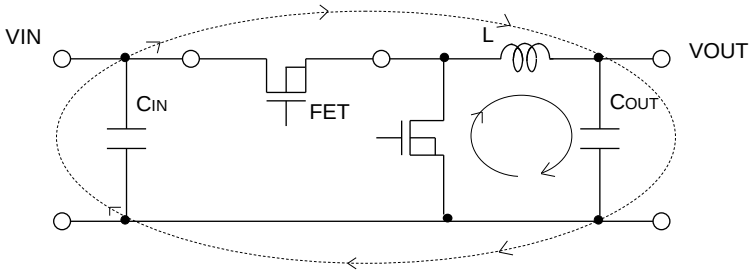


Figure 26. Current loop Buck regulator system

- The thermal Pad on the back side of IC has the great thermal conduction to the chip. So using the GND plain as broad and wide as possible can help thermal dissipation. And a lot of thermal via for helping the spread of heat to the different layer is also effective.
- The input capacitors should be connected to PGND as close as possible to the VIN terminal.
- The inductor and the output capacitors should be placed close to SW pin as much as possible.

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●List of Evaluation Board Components

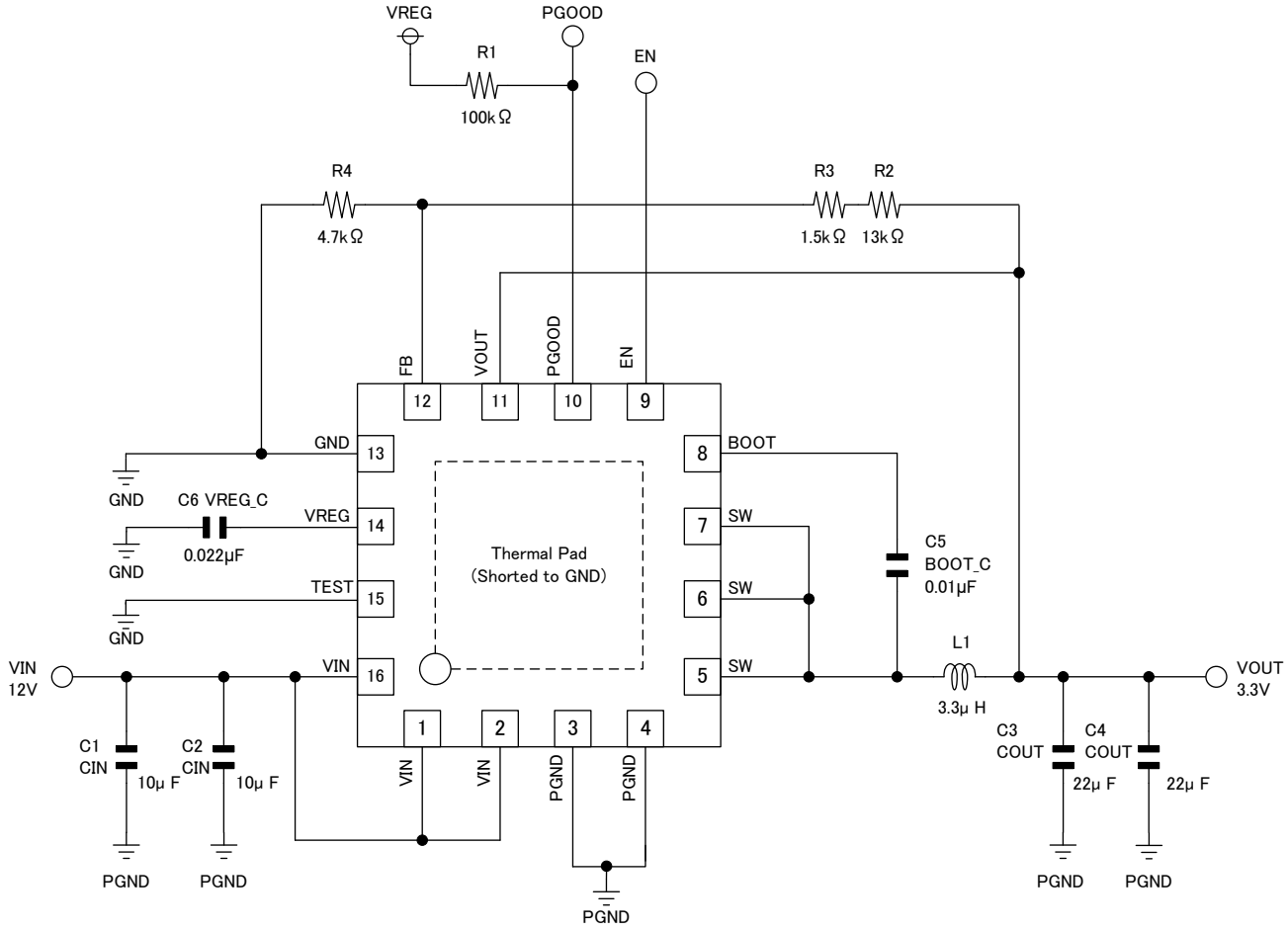


Figure 27. Typical Application Circuit (VOUT=3.3V)

Table 1. Recommended BOM List(VIN=12V)

Symbol	Part	Value	Manufacture	Series
L1	Coil	※	TOKO	FDVC0630 Series
			TDK	SPM6530 Series
CIN (C1, C2)	Ceramic capacitor	10μF / 25V	Murata	GRM31CR71E16KA12
COUT (C3, C4)	Ceramic capacitor	22μF / 16V	Murata	GRM31CB31C226ME15
BOOT_C (C5)	Ceramic capacitor	0.01μF / 50V	Murata	GRM18 Series
R1	Resistance	100kΩ	Rohm	MCR03 Series
R2	Resistance	※	Rohm	MCR03 Series
R3	Resistance	※	Rohm	MCR03 Series
R4	Resistance	※	Rohm	MCR03 Series
VREG_C (C6)	Ceramic capacitor	0.022μF / 50V	Murata	GRM18 Series

※

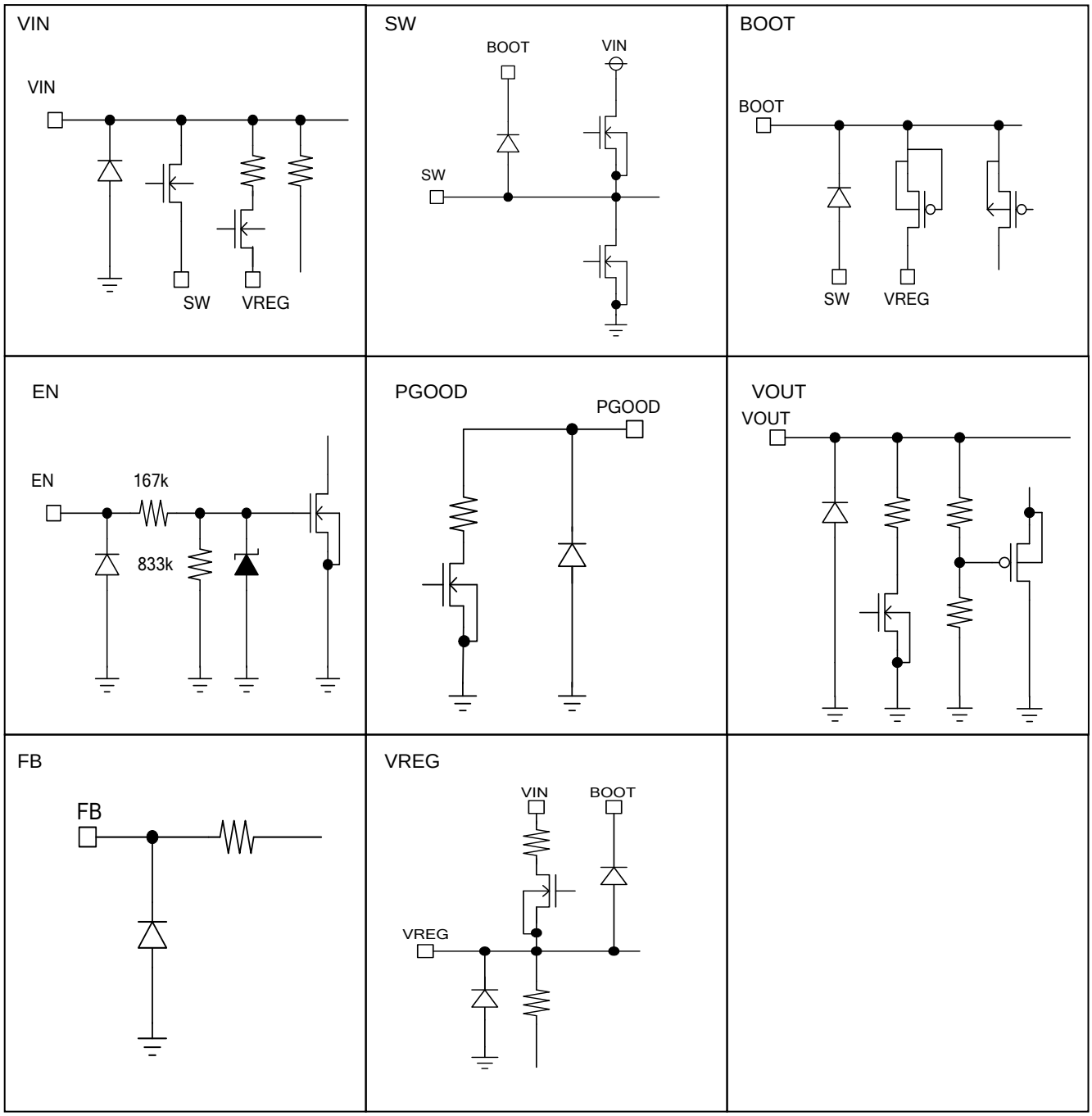
VOUT	R2	R3	R4	L1
1.0V	360Ω	130Ω	2.2kΩ	1.5μH
1.2V	2kΩ	220Ω	4.7kΩ	1.5μH
1.8V	5.6kΩ	110Ω	4.7kΩ	2.2μH
3.3V	13kΩ	1.5kΩ	4.7kΩ	3.3μH
5.0V	24kΩ	680Ω	4.7kΩ	3.3μH

The above components list is an example. Please check actual circuit characteristics on the application carefully before use.

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●I/O Equivalence circuit



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●Operational Notes

(1) Absolute Maximum Ratings
Use of the IC in excess of absolute maximum ratings may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

(2) GND voltage
The potential of the GND, PGND pin must be the minimum potential in the system in all operating conditions.

(3) Thermal design
Use a thermal design that allows for a sufficient margin for power dissipation (Pd) under actual operating conditions

(4) Inter-pin Shorts and Mounting Errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply and GND pins caused by poor soldering or foreign objects may result in damage to the IC.

(5) Operation in Strong Electromagnetic Fields
Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

(6) ASO (Area of Safe Operation)
When using the IC, ensure that operating conditions do not exceed absolute maximum ratings or ASO of the output transistors.

(7) Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(8) Electrical Characteristics
The electrical characteristics indicated in this datasheet may change upon the conditions of temperature, supply voltage, and external components. Please validate/verify your design at the worst case conditions.

(9) Not of a radiation-resistant design.

(10) Back Electromotive Force
If a large inductive load is connected at the output pin that might cause introducing back electromotive force at the start up and at the output disable, please insert protection diodes.

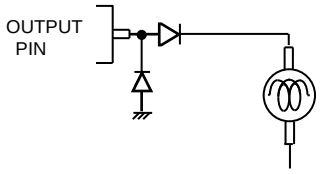


Figure 28. Back Electromotive Force

(11) Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the figure below):、

- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

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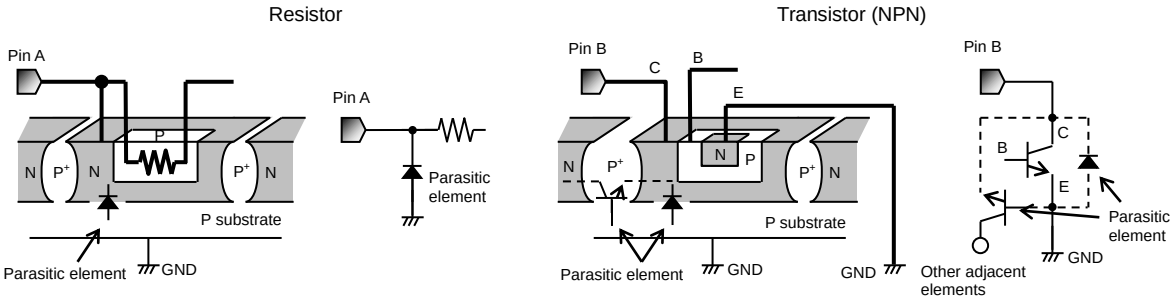


Figure 29. Example of IC structure

(12) Ground Wiring Pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage.

(13) Operating Condition

The electrical characteristics indicated in this datasheet are not guaranteed for the whole operational and temperature ranges, however these characteristics do not significantly fluctuate within the operational and temperature ranges.

(14) Thermal shutdown (TSD) circuit

The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed. If the thermal shutdown is activated while the load current exists, the output may possibly be latched off at the release of the thermal shutdown.

TSD ON Temp.[℃] (typ.)	Hysteresis Temp[℃] (typ.)
175	25

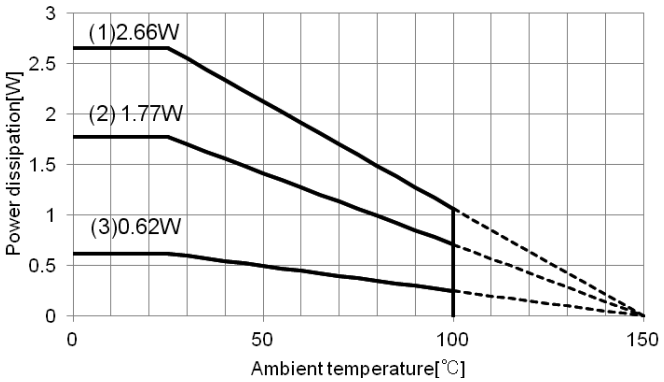
(15) Heat Sink (FIN)

The heat sink (FIN) is connected to the substrate. Please connect it to GND.

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●Thermal Derating Curves



(1) 4 layer board
(All layers with 5505 mm^2 copper heat dissipation pads)
θ j-a=47.0℃/W
(2) 4 layer board
(6.28 mm^2 copper heat dissipation pad on top and bottom layer, 5505 mm^2 pad on 2nd and 3rd layer)
θ j-a=70.62℃/W
(3) 1 layer board (6.28 mm^2 copper heat dissipation pad)
θ j-a=201.6℃/W

Figure 30. Thermal derating curve
(VQFN016V3030)

●Ordering Information

B D 9 5 8 2 1 M U V - E 2

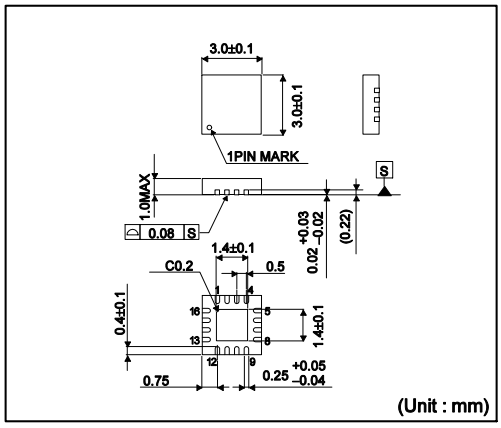
Part Number

Package
MUV: VQFN016V3030

Packaging and forming specification
E2: Embossed tape and reel

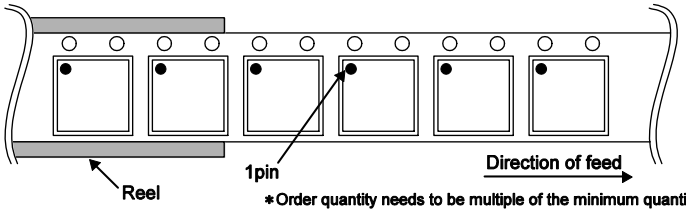
●Physical Dimension Tape and Reel Information

VQFN016V3030



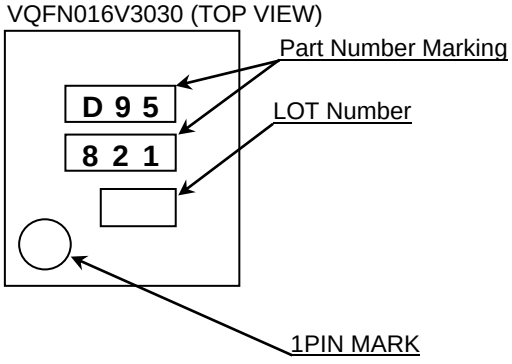
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram



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●**Revision History**

Date	Revision	Changes
6.Aug.2012	001	New Release
24.Aug.2012	002	Revised the General Description
18.Mar.2013	003	Revised the General Description
27.Dec.2023	004	Update the revision according to revising the JP version

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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