

MOSFET – P-Channel 1.8 V Specified POWERTRENCH®

FDN304P

General Description

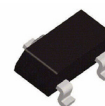
This P-Channel 1.8 V specified MOSFET uses onsemi's advanced low voltage POWERTRENCH process. It has been optimized for battery power management applications.

Features

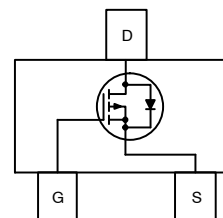
- -2.4 A, -20 V
 - ♦ $R_{DS(ON)} = 52 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$
 - ♦ $R_{DS(ON)} = 70 \text{ m}\Omega$ @ $V_{GS} = -2.5 \text{ V}$
 - ♦ $R_{DS(ON)} = 100 \text{ m}\Omega$ @ $V_{GS} = -1.8 \text{ V}$
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SUPERSOT™ -23 provides Low $R_{DS(ON)}$ and 30% Higher Power Handling Capability than SOT23 in the same Footprint
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Applications

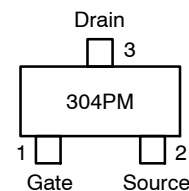
- Battery Management
- Load Switch
- Battery Protection



SOT-23/SUPERSOT-23, 3 LEAD, 1.4x2.9
CASE 527AG



MARKING DIAGRAM



304P = Specific Device Code
M = Date Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

ABSOLUTE MAXIMUM RATINGST_A = 25°C unless otherwise noted

Symbol	Parameter	Ratings	Unit
V _{DSS}	Drain–Source Voltage	–20	V
V _{GSS}	Gate–Source Voltage	±8	V
I _D	Drain Current Continuous (Note 1a) Pulsed	–2.4 –10	A
P _D	Maximum Power Dissipation (Note 1a) (Note 1b)	0.5 0.46	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
R _{θJA}	Thermal Resistance, Junction–to–Ambient (Note 1a)	250	°C/W
R _{θJC}	Thermal Resistance, Junction–to–Case (Note 1)	75	°C/W

ELECTRICAL CHARACTERISTICST_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain–Source Breakdown Voltage	V _{GS} = 0 V, I _D = –250 μA	–20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C		–13		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = –16 V, V _{GS} = 0 V			–1	μA
I _{GSSF}	Gate–Body Leakage, Forward	V _{GS} = 8 V, V _{DS} = 0 V			100	nA
I _{GSSR}	Gate–Body Leakage, Reverse	V _{GS} = –8 V, V _{DS} = 0 V			–100	nA

ON CHARACTERISTICS (Note 2)

V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = –250 μA	–0.4	–0.8	–1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I _D = –250 μA, Referenced to 25°C		3		mV/°C
R _{DS(on)}	Static Drain–Source On–Resistance	V _{GS} = –4.5 V, I _D = –2.4 A		36	52	mΩ
		V _{GS} = –2.5 V, I _D = –2 A		47	70	
		V _{GS} = –1.8 V, I _D = –1.8 A		65	100	
I _{D(on)}	On–State Drain Current	V _{GS} = –4.5 V, V _{DS} = –5 V	–10			A
g _{FS}	Forward Transconductance	V _{DS} = –5 V, I _D = –1.25 A		12		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = –10 V, V _{GS} = 0 V, f = 1.0 MHz		1312		pF
C _{oss}	Output Capacitance			240		pF
C _{rss}	Reverse Transfer Capacitance			106		pF

SWITCHING CHARACTERISTICS (Note 2)

t _{d(on)}	Turn–On Delay Time	V _{DD} = –10 V, I _D = –1 A, V _{GS} = –4.5 V, R _{GEN} = 6 Ω		15	27	ns
t _r	Turn–On Rise Time			15	27	ns
t _{d(off)}	Turn–Off Delay Time			40	64	ns
t _f	Turn–Off Fall Time			25	40	ns

FDN304P

ELECTRICAL CHARACTERISTICS (continued)

$T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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SWITCHING CHARACTERISTICS (Note 2)

Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}$, $I_D = -2.4\text{ A}$, $V_{GS} = -4.5\text{ V}$		12	20	nC
Q_{gs}	Gate–Source Charge			2		nC
Q_{gd}	Gate–Drain Charge			2		nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain–Source Diode Forward Current				–0.42	A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = -0.42\text{ A}$ (Note 2)		–0.6	–1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in^2 pad of 2 oz copper.



b) 270°C/W when mounted on a minimum pad.

- Pulse Test: Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping [†]
FDN304P	304P	SOT–23 (Pb–Free)	3000 units / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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TYPICAL CHARACTERISTICS

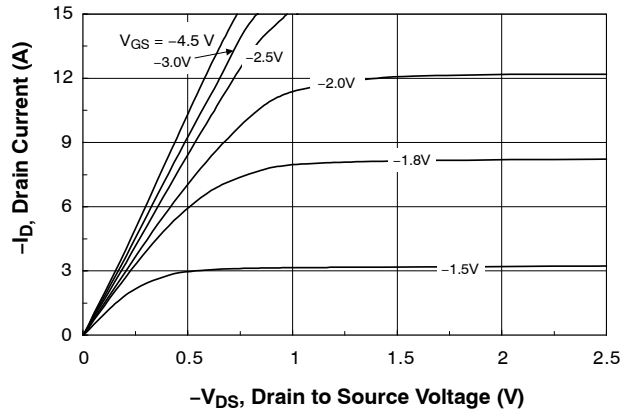


Figure 1. On-Region Characteristics

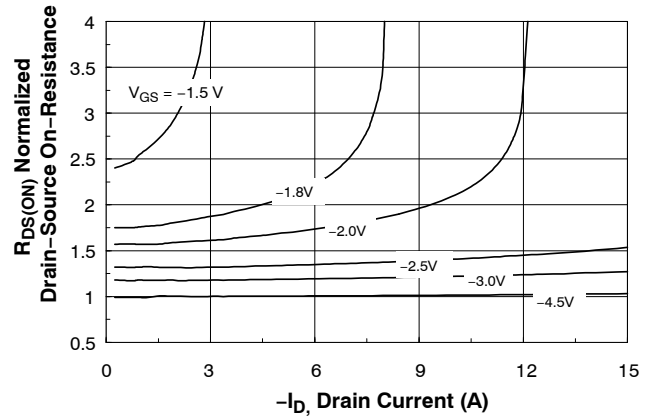


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

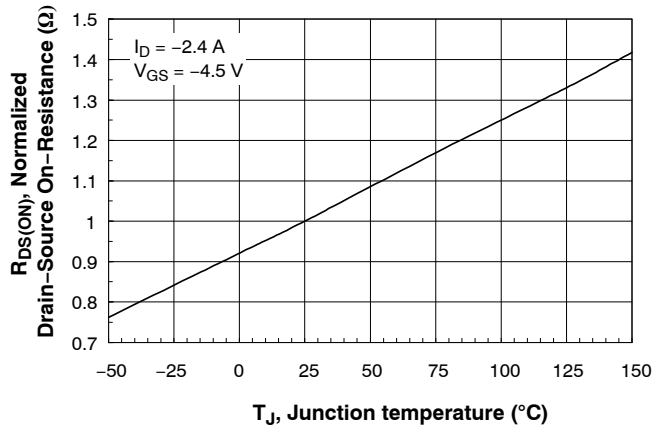


Figure 3. On-Resistance Variation with Temperature

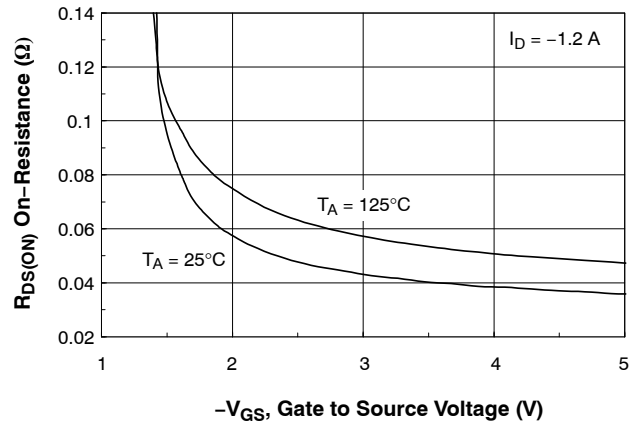


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

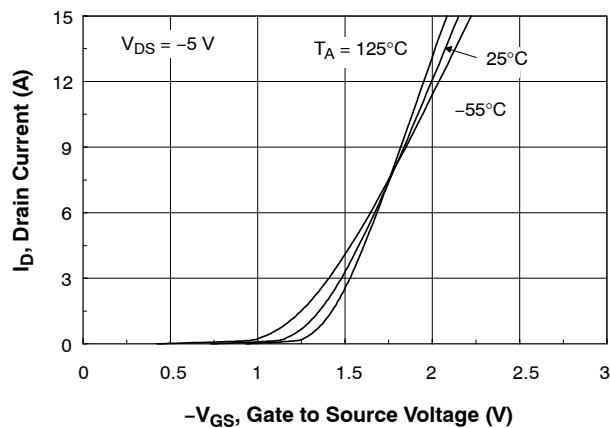


Figure 5. Transfer Characteristics

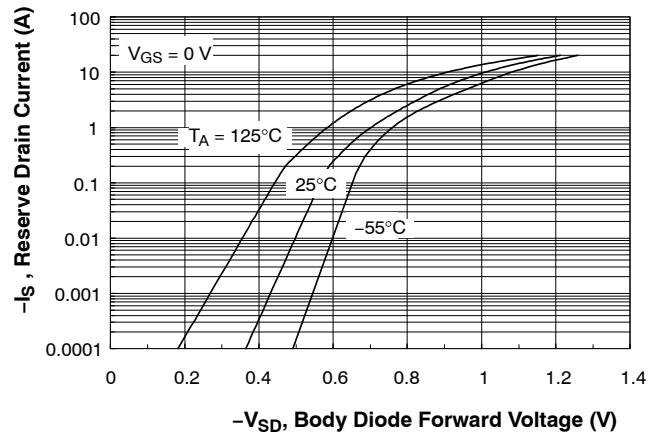


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Continued)

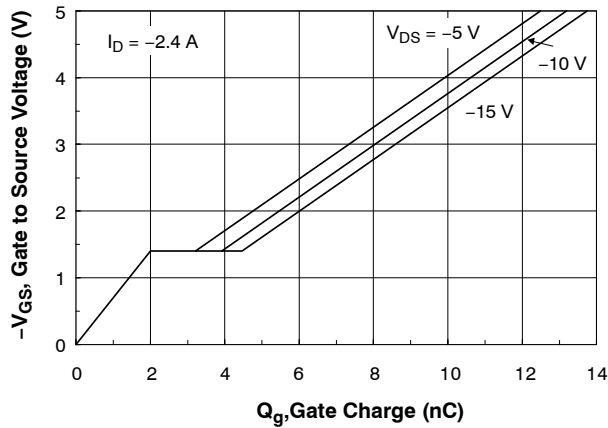


Figure 7. Gate Charge Characteristics

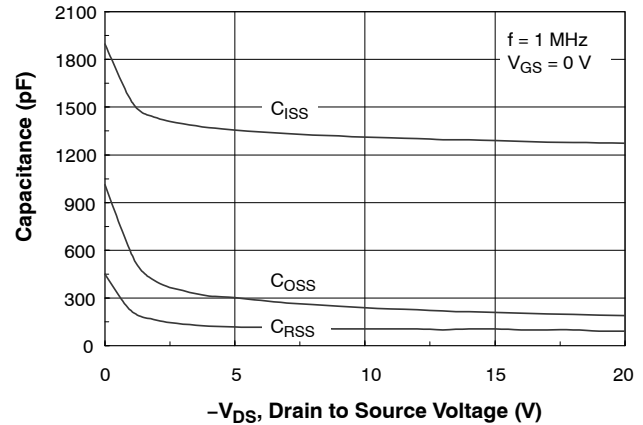


Figure 8. Capacitance Characteristics

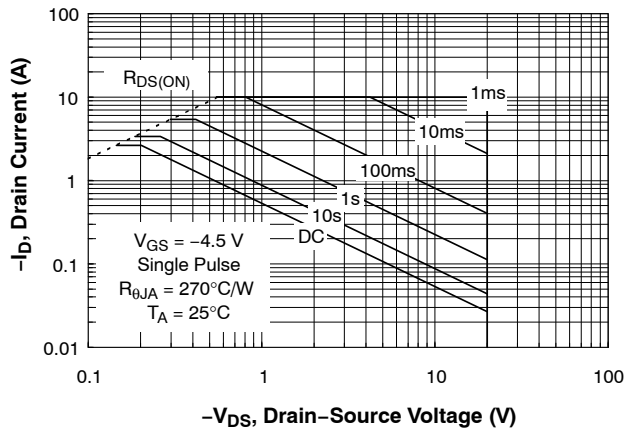


Figure 9. Maximum Safe Operating Area

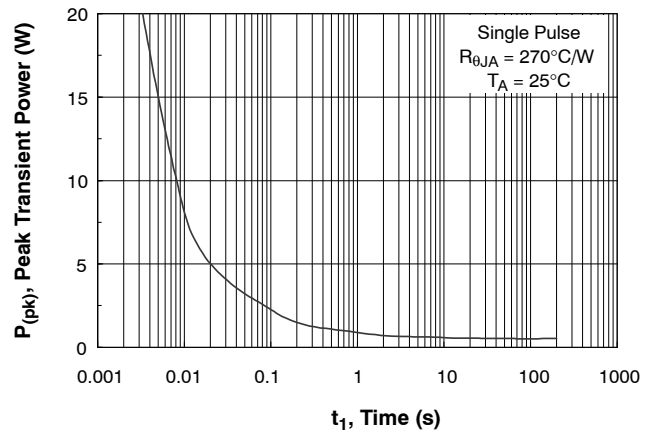


Figure 10. Single Pulse Maximum Power Dissipation

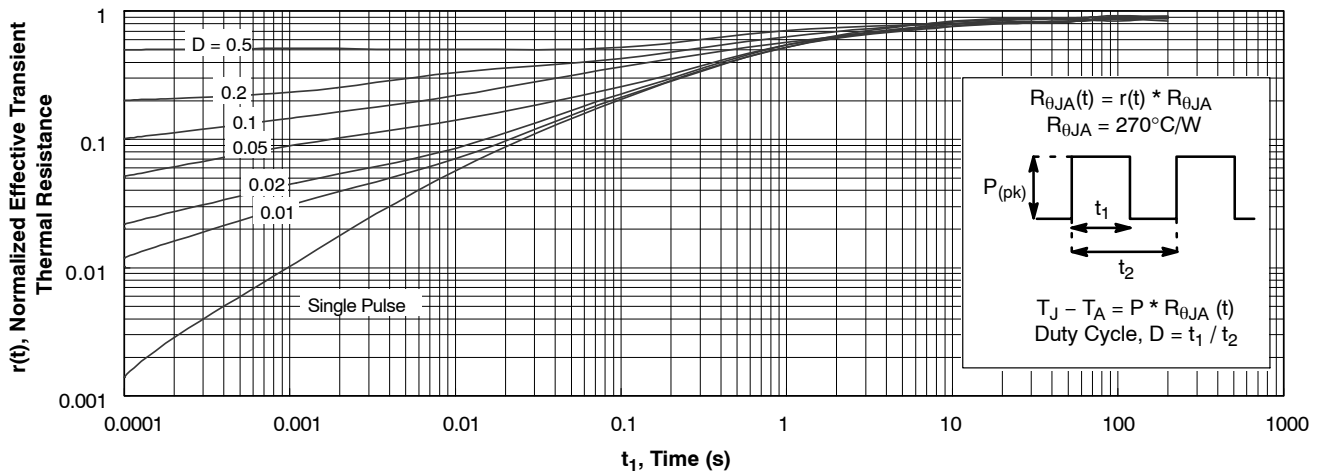
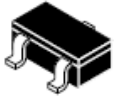
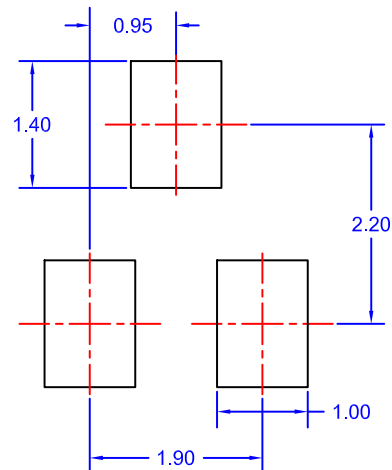
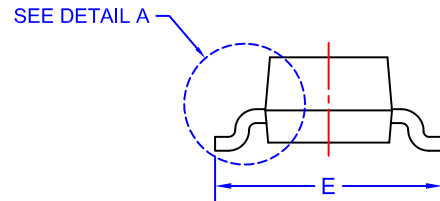
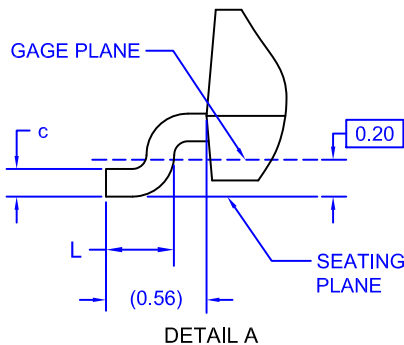
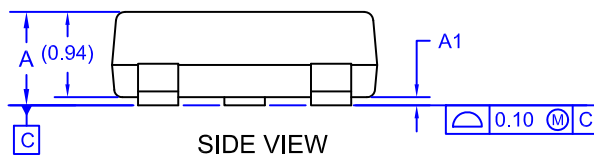
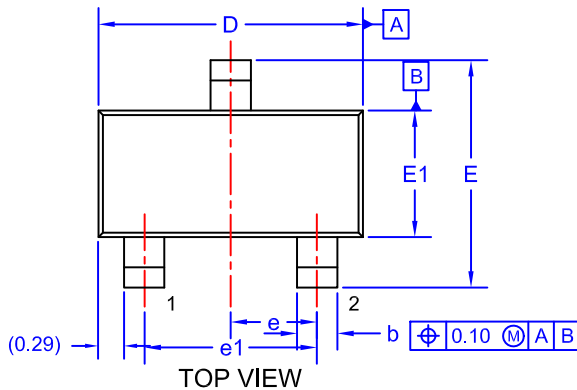


Figure 11. Transient Thermal Response Curve

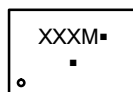
Thermal characterization performed using the conditions described in Note 1b.
Transient thermal response will change depending on the circuit board design.


SOT-23/SUPERSOT™ –23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019


LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*


XXX = Specific Device Code
M = Month Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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