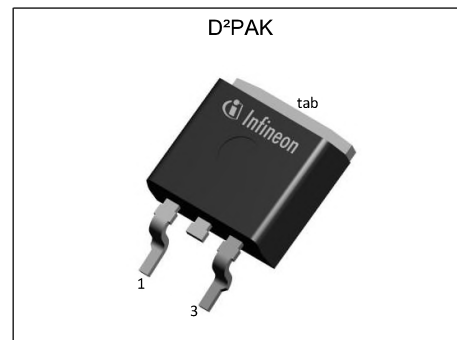


MOSFET

OptiMOS™ Power-Transistor, -100 V

Features

- P-channel
- Very low on-resistance $R_{DS(on)}$ @ $V_{GS}=4.5\text{ V}$
- 100% avalanche tested
- Logic level
- Enhancement mode
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

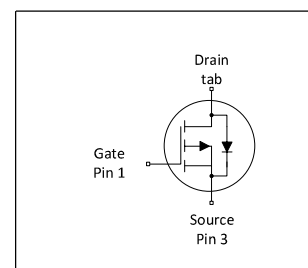


Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	-100	V
$R_{DS(on),max}$	32	mΩ
I_D	-63	A
Q_{oss}	-67	nC
Q_G	-219	nC



RoHS

Type / Ordering Code	Package	Marking	Related Links
IPB320P10LM	PG-TO263-3	320P10LM	-

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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	-63 -44 -41 -6.5	A	$V_{GS}=-10\text{ V}$, $T_C=25\text{ °C}$ $V_{GS}=-10\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_C=100\text{ °C}$ $V_{GS}=-4.5\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^{2)}$
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	-252	A	$T_A=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	1710	mJ	$I_D=-54\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	300 3.8	W	$T_C=25\text{ °C}$ $T_A=25\text{ °C}$, $R_{thJA}=40\text{ °C/W}^{2)}$
Operating and storage temperature	T_j , T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.5	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area	R_{thJA}	-	-	40	°C/W	-
Thermal resistance, junction - ambient, minimal footprint ²⁾	R_{thJA}	-	-	62	°C/W	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-100	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	-1	-1.5	-2	V	$V_{DS}=V_{GS}$, $I_D=-5550\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1 -10	-1 -100	μA	$V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=-100\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	25.4 26.1	32 37	m Ω	$V_{GS}=-10\text{ V}$, $I_D=-54\text{ A}$ $V_{GS}=-4.5\text{ V}$, $I_D=-37\text{ A}$
Gate resistance	R_G	-	5.4	-	Ω	-
Transconductance	g_{fs}	-	110	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=-54\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance ¹⁾	C_{iss}	-	8600	11000	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Output capacitance ¹⁾	C_{oss}	-	530	690	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Reverse transfer capacitance ¹⁾	C_{rss}	-	110	190	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-50\text{ V}$, $f=1\text{ MHz}$
Turn-on delay time	$t_{d(on)}$	-	26.47	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-54\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Rise time	t_r	-	150.85	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-54\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Turn-off delay time	$t_{d(off)}$	-	170.93	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-54\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$
Fall time	t_f	-	110	-	ns	$V_{DD}=-50\text{ V}$, $V_{GS}=-4.5\text{ V}$, $I_D=-54\text{ A}$, $R_{G,ext}=1.6\text{ }\Omega$

Table 6 Gate charge characteristics²⁾

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-26	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-54\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$	-	-12.9	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-54\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate to drain charge ¹⁾	Q_{gd}	-	-55	-83	nC	$V_{DD}=-50\text{ V}$, $I_D=-54\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Switching charge	Q_{sw}	-	-68	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-54\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total ¹⁾	Q_g	-	-110	-138	nC	$V_{DD}=-50\text{ V}$, $I_D=-54\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate plateau voltage	$V_{plateau}$	-	-3.1	-	V	$V_{DD}=-50\text{ V}$, $I_D=-54\text{ A}$, $V_{GS}=0\text{ to }-4.5\text{ V}$
Gate charge total	Q_g	-	-219	-	nC	$V_{DD}=-50\text{ V}$, $I_D=-54\text{ A}$, $V_{GS}=0\text{ to }-10\text{ V}$
Output charge ¹⁾	Q_{oss}	-	-67	-89	nC	$V_{DS}=-50\text{ V}$, $V_{GS}=0\text{ V}$

¹⁾ Defined by design. Not subject to production test.

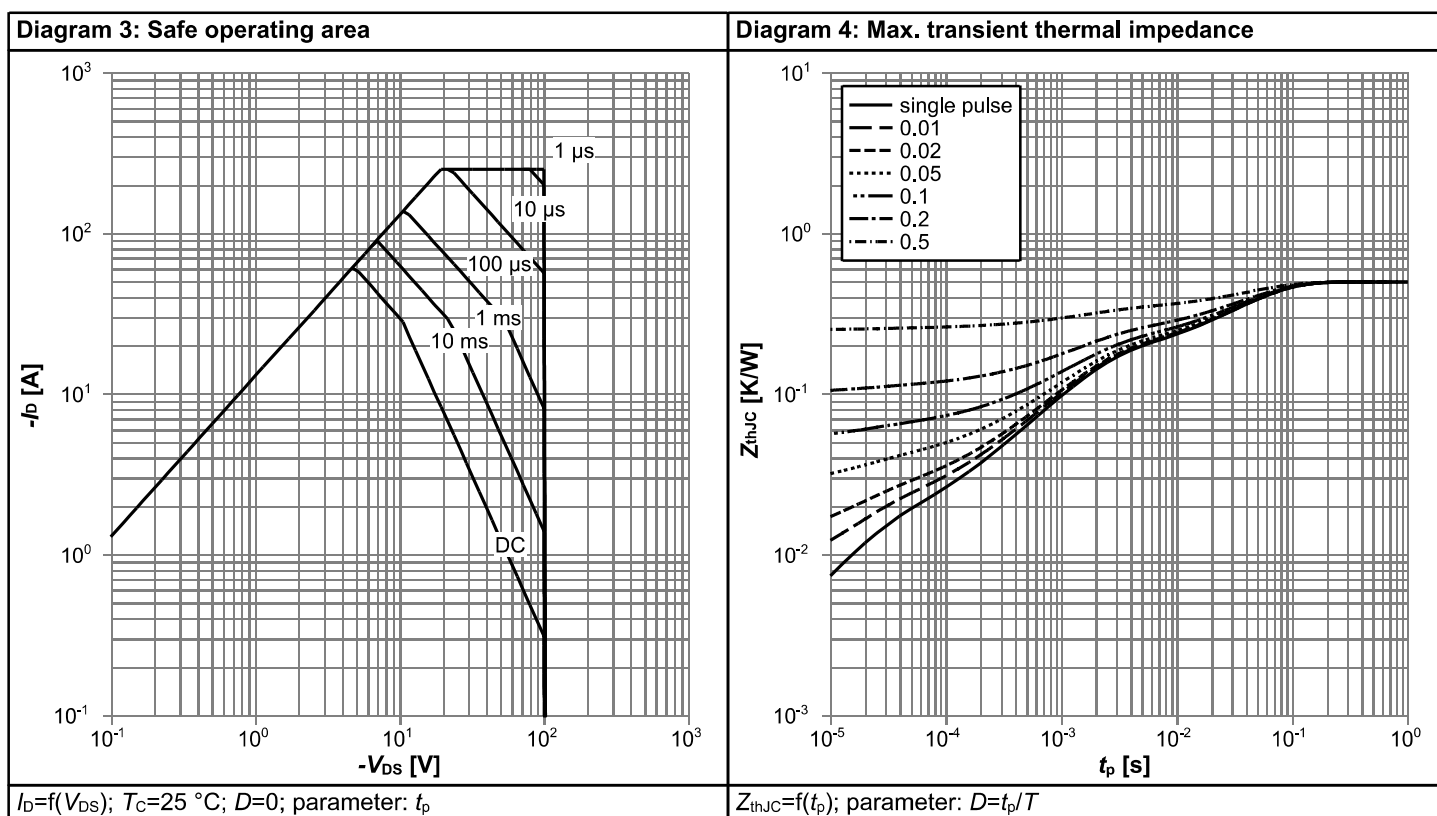
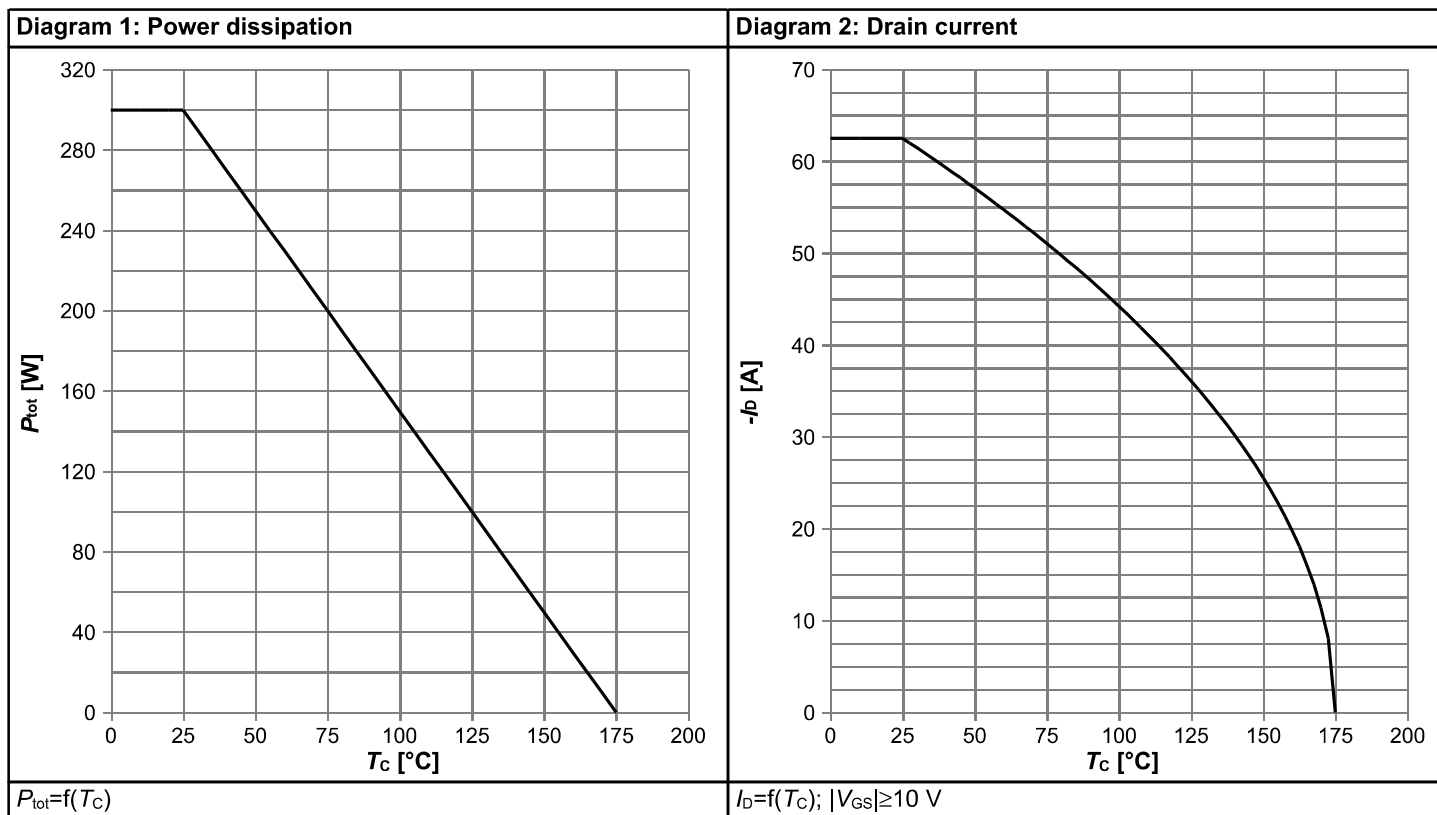
²⁾ See "Gate charge waveforms" for parameter definition

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-63	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$	-	-	-252	A	$T_C=25\text{ °C}$
Diode forward voltage	V_{SD}	-	-0.87	-1.2	V	$V_{GS}=0\text{ V}$, $I_F=-54\text{ A}$, $T_j=25\text{ °C}$
Reverse recovery time ¹⁾	t_{rr}	-	102.2	204.4	ns	$V_R=-50\text{ V}$, $I_F=-54\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$
Reverse recovery charge ¹⁾	Q_{rr}	-	457.01	914.02	nC	$V_R=-50\text{ V}$, $I_F=-54\text{ A}$, $di_F/dt=-100\text{ A}/\mu\text{s}$

¹⁾ Defined by design. Not subject to production test.

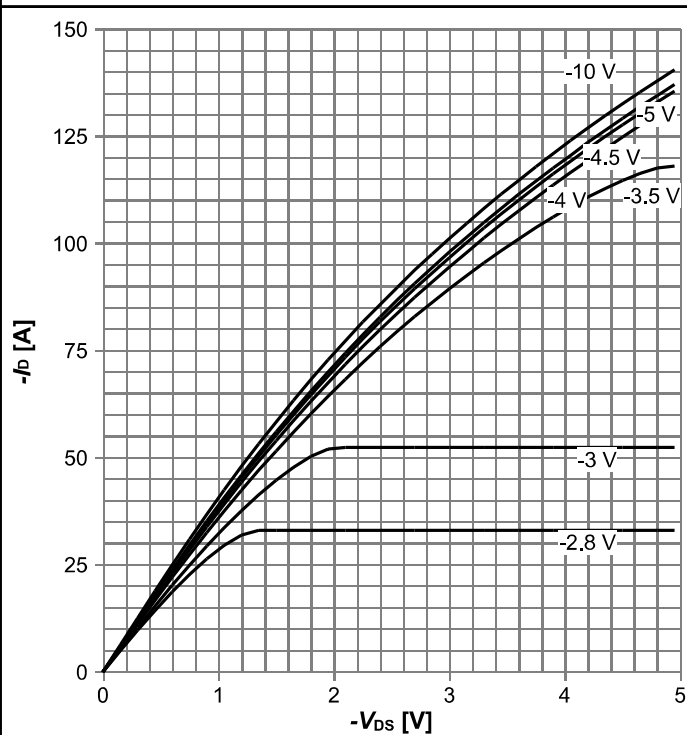
4 Electrical characteristics diagrams



OptiMOS™ Power-Transistor, -100 V

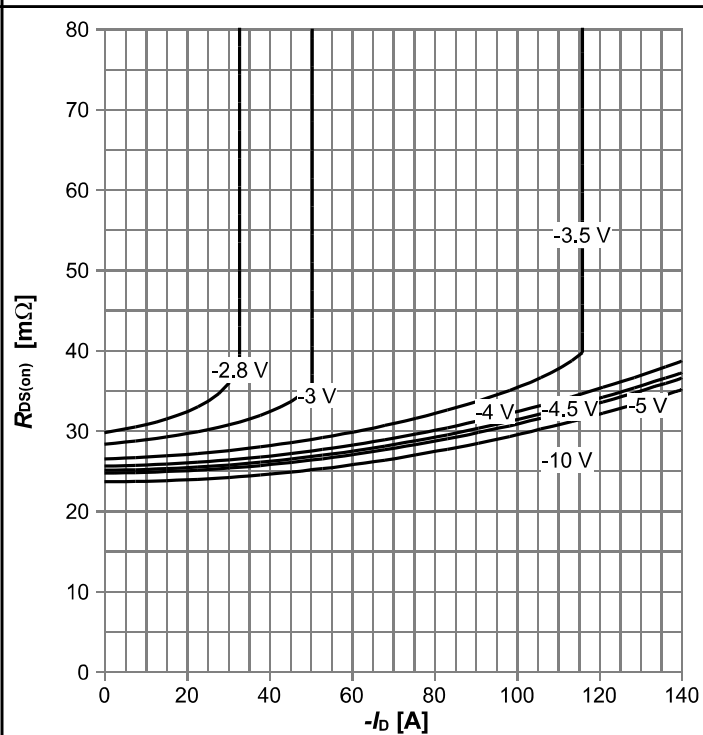
IPB320P10LM

Diagram 5: Typ. output characteristics



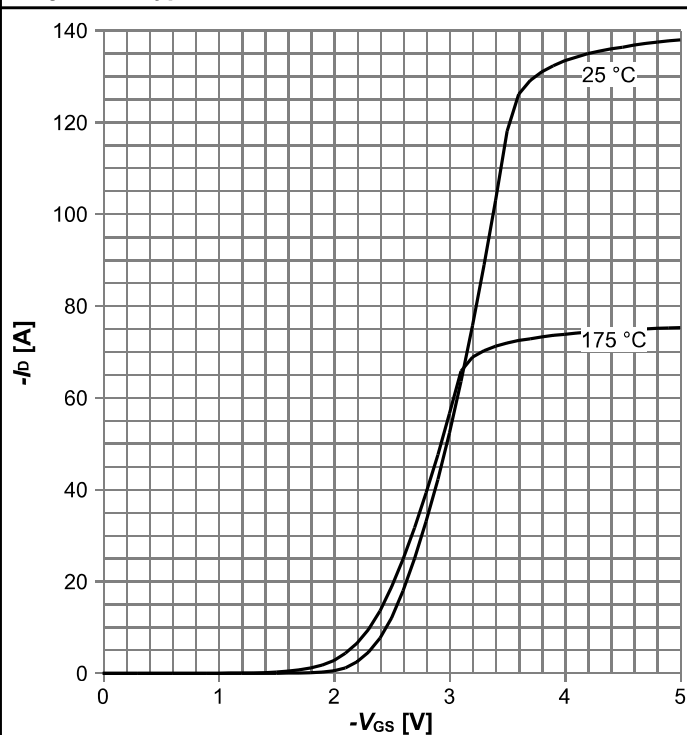
$I_D = f(V_{DS})$, $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



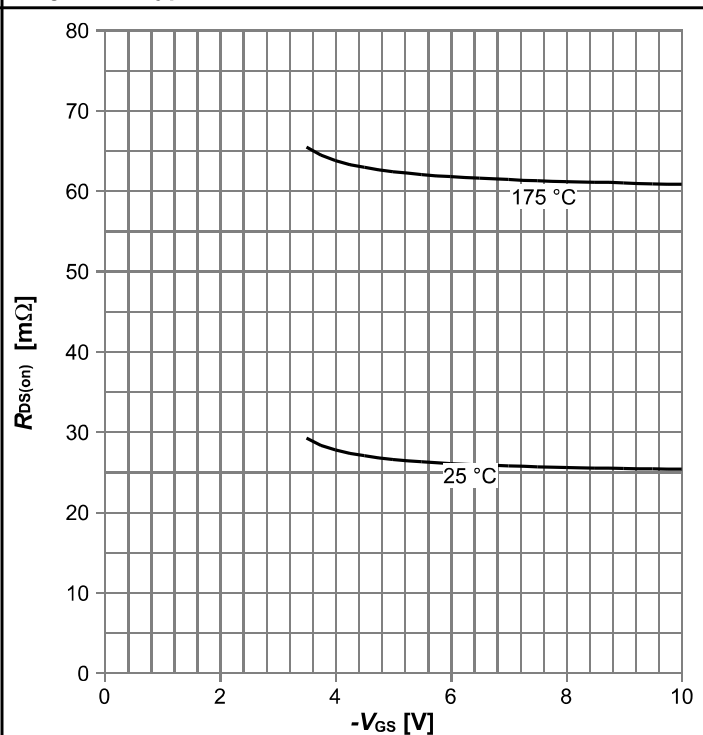
$R_{DS(on)} = f(I_D)$, $T_J = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



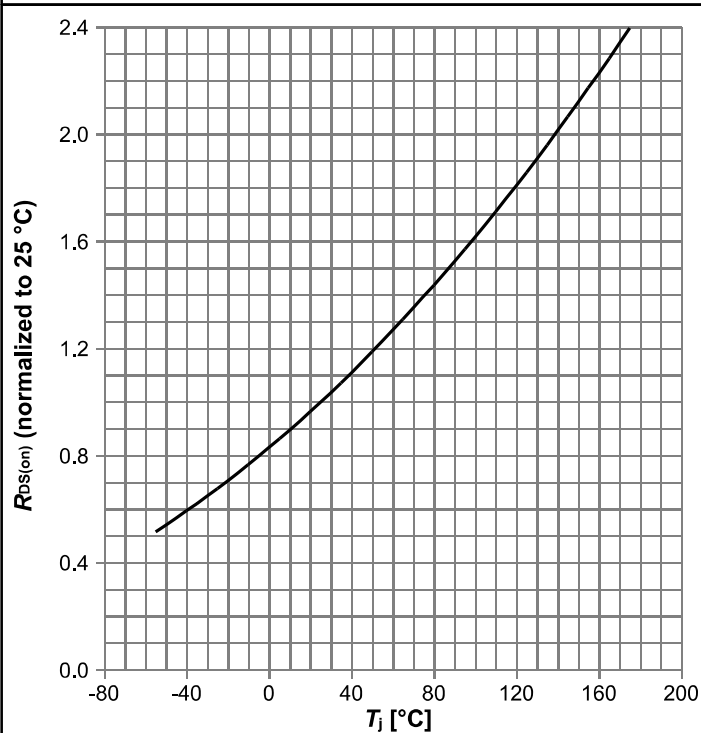
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)\text{max}}$; parameter: T_J

Diagram 8: Typ. drain-source on resistance



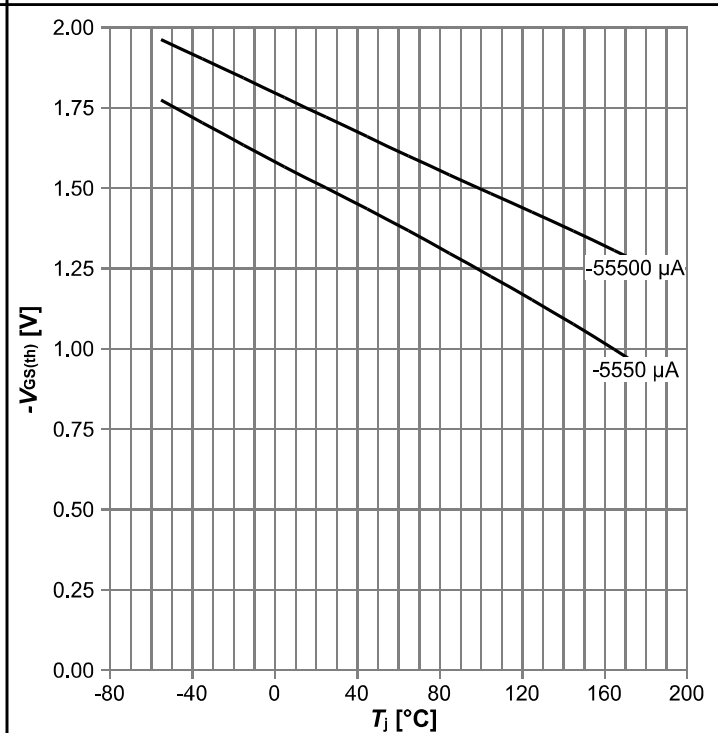
$R_{DS(on)} = f(V_{GS})$, $I_D = -54\text{ A}$; parameter: T_J

Diagram 9: Normalized drain-source on resistance



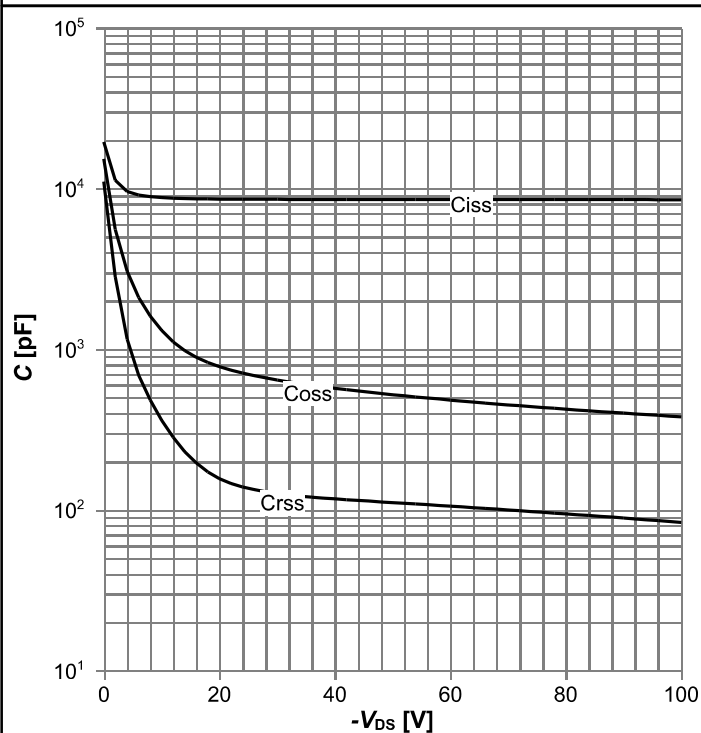
$R_{DS(on)} = f(T_j)$, $I_D = -54$ A, $V_{GS} = -10$ V

Diagram 10: Typ. gate threshold voltage



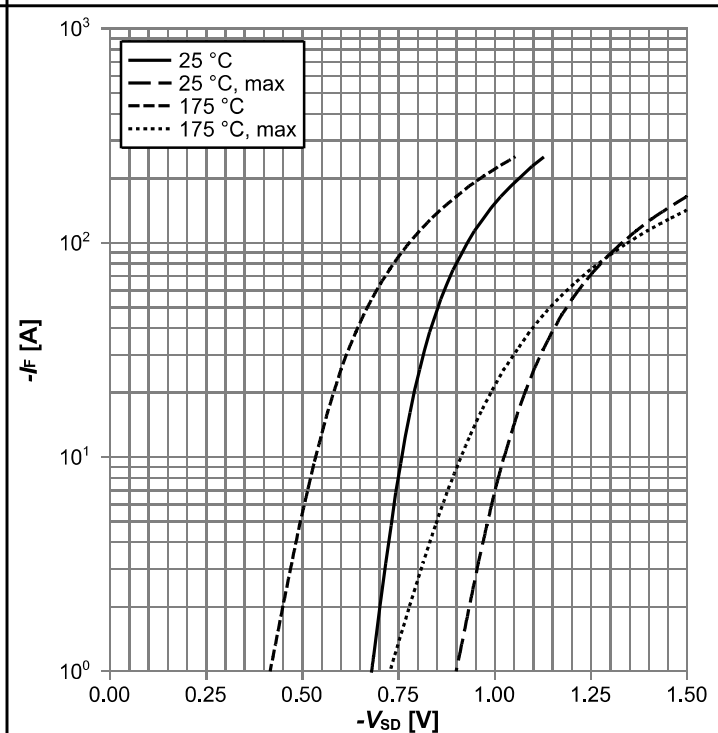
$V_{GS(th)} = f(T_j)$, $V_{GS} = V_{DS}$; parameter: I_D

Diagram 11: Typ. capacitances



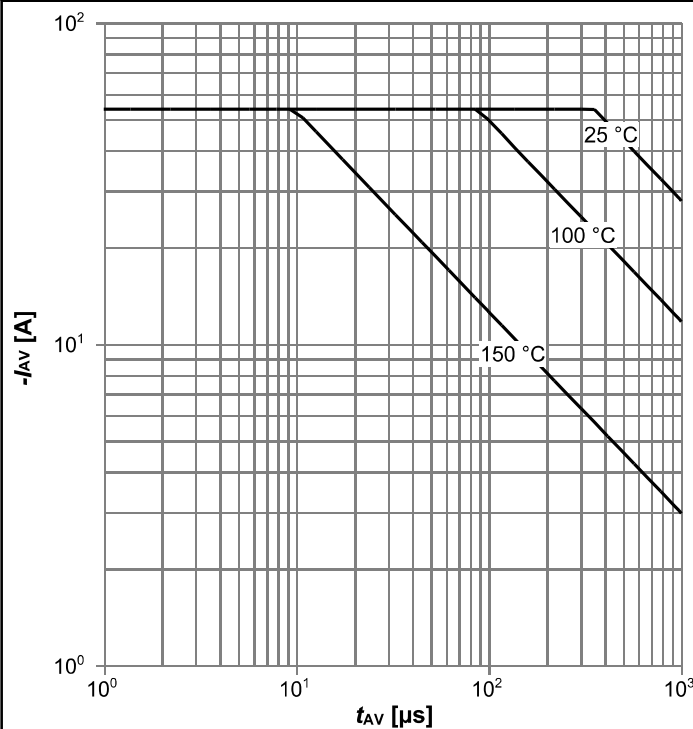
$C = f(V_{DS})$; $V_{GS} = 0$ V; $f = 1$ MHz

Diagram 12: Forward characteristics of reverse diode



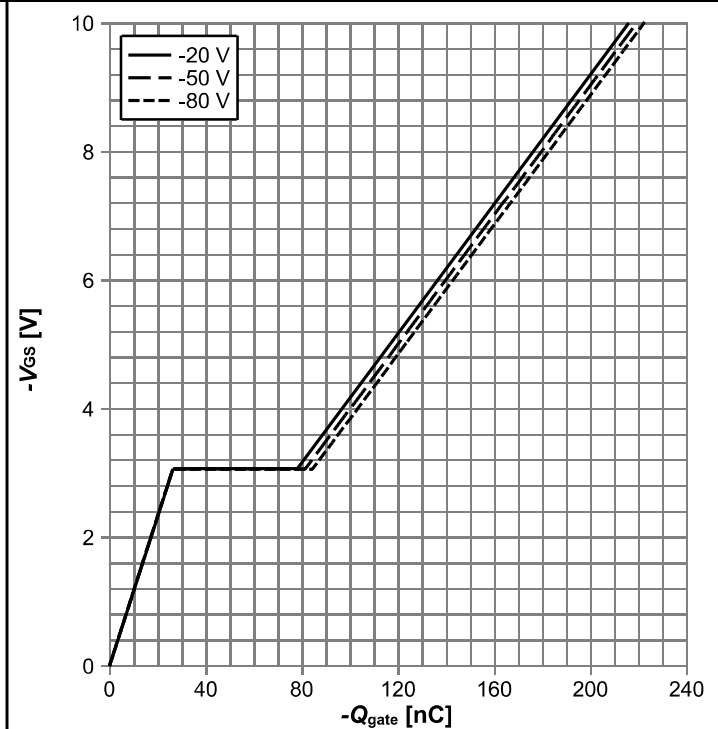
$I_F = f(V_{SD})$; parameter: T_j

Diagram 13: Avalanche characteristics



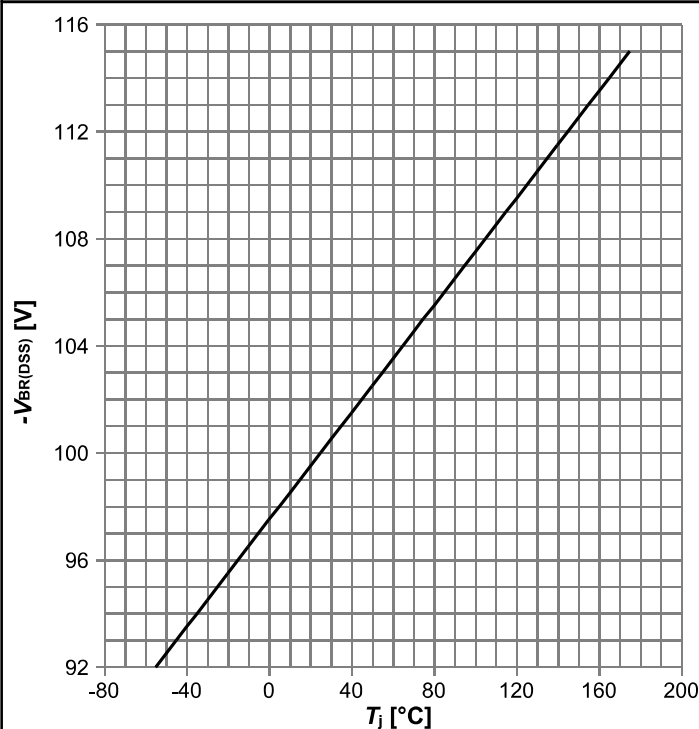
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



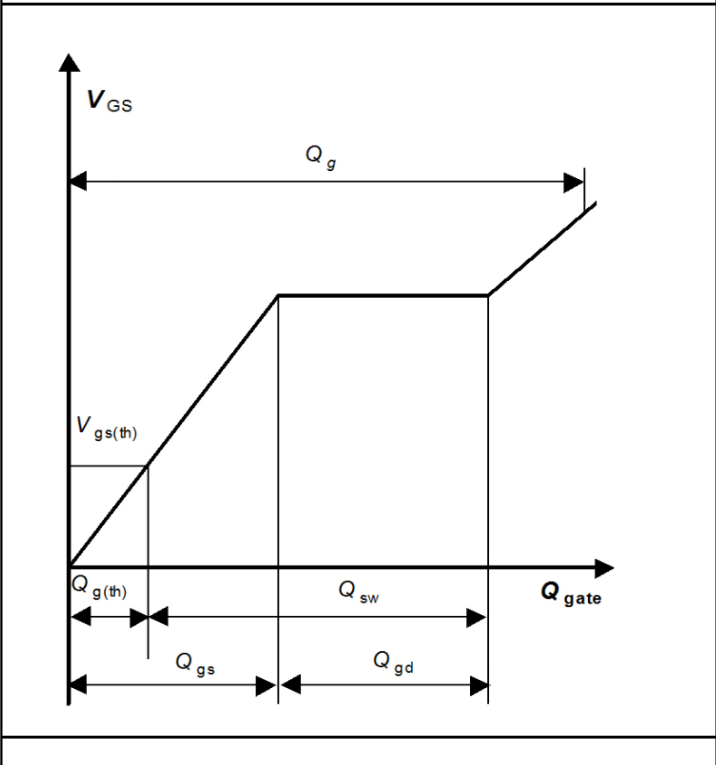
$V_{GS}=f(Q_{gate})$, $I_D=-54\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=-1\text{ mA}$

Diagram Gate charge waveforms



5 Package Outlines

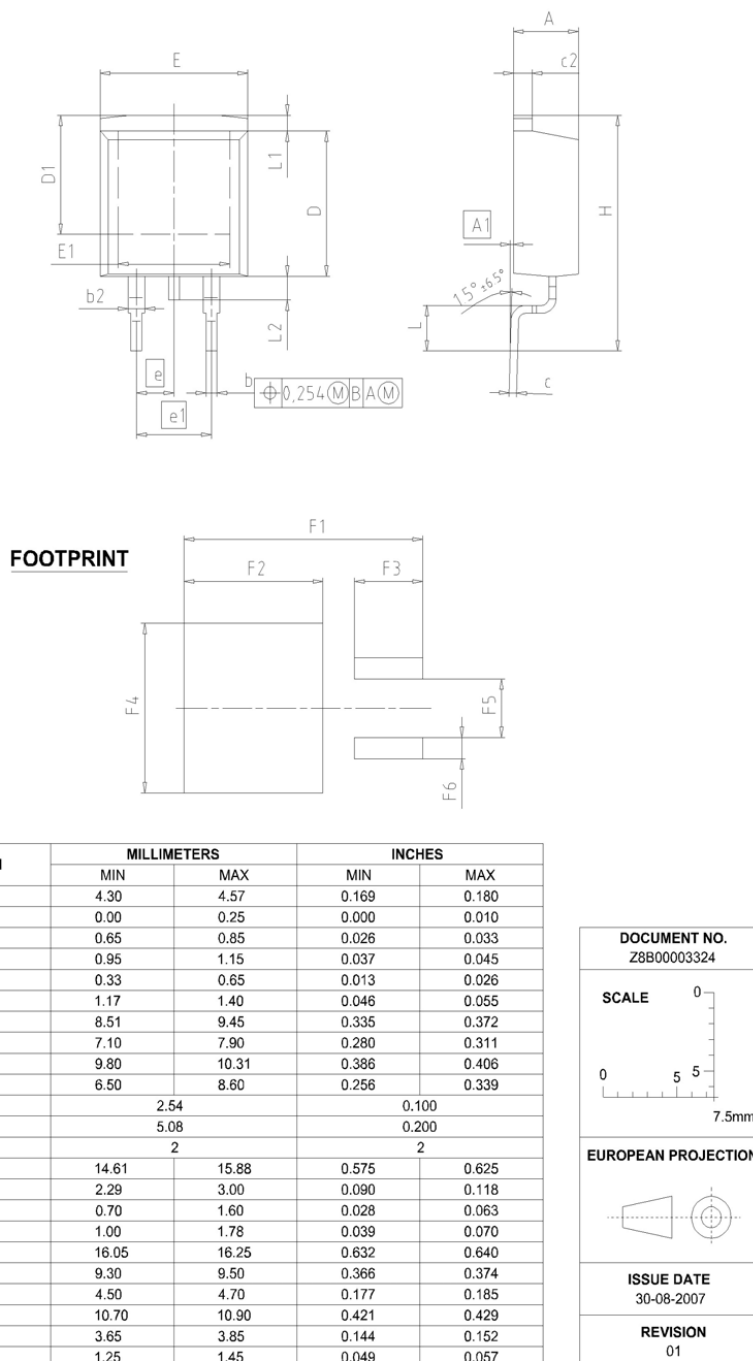


Figure 1 Outline PG-TO263-3, dimensions in mm/inches

Revision History

IPB320P10LM

Revision: 2021-05-10, Rev. 2.0

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2021-05-10	Release of final version

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