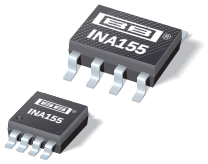
BURR - BROWN®



INA155

For most current data sheet and other product information, visit www.burr-brown.com

Single-Supply, Rail-to-Rail Output, CMOS INSTRUMENTATION AMPLIFIER

FEATURES

- RAIL-TO-RAIL OUTPUT SWING: Within 10mV
- LOW OFFSET VOLTAGE: ±200µV
- LOW OFFSET DRIFT: ±5µV/°C
- INTERNAL FIXED GAIN = 10V/V OR 50V/V
- SPECIFIED TEMPERATURE RANGE: –55°C to +125°C
- LOW INPUT BIAS CURRENT: 0.2pA
- WIDE BANDWIDTH: 550kHz in G = 10
- HIGH SLEW RATE: 6.5V/µs
- LOW COST
- SO-8 AND TINY MSOP-8 PACKAGES

APPLICATIONS

- INDUSTRIAL SENSOR AMPLIFIERS
  Bridge, RTD, Thermocouple, Flow, Position
- MEDICAL EQUIPMENT
  ECG, EEG, EMG Amplifiers
- DRIVING A/D CONVERTERS
- PCMCIA CARDS
- AUDIO PROCESSING
- COMMUNICATIONS
- TEST EQUIPMENT
- LOW COST AUTOMOTIVE INSTRUMENTATION

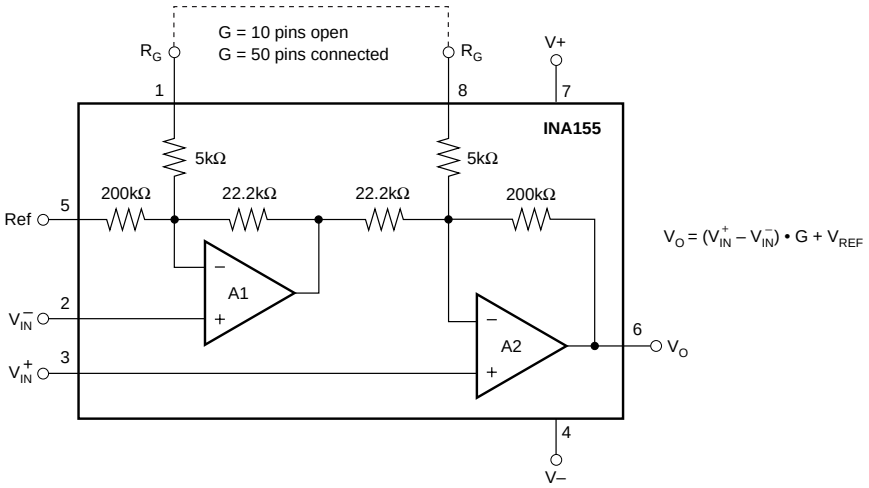
DESCRIPTION

The INA155 is a low-cost CMOS instrumentation amplifier with rail-to-rail output swing optimized for low voltage, single-supply operation.

Wide bandwidth (550kHz in G = 10) and high slew rate (6.5V/µs) make the INA155 suitable for driving sampling A/D converters as well as general purpose and audio applications. Fast settling time allows use with higher speed sensors and transducers and rapid scanning data acquisition systems.

Gain can be set to 10V/V or 50V/V by pin strapping. Gains between these two values can be obtained with the addition of a single resistor. The INA155 is fully specified over the supply range of +2.7 to +5.5V.

The INA155 is available in MSOP-8 and SO-8 surface-mount packages. Both are specified for operation over the temperature range –55°C to 125°C.



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Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1529B
Printed in U.S.A. February, 2000
SBOS114

SPECIFICATIONS: V_S = +2.7V to +5.5V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C**

At T_A = +25°C, R_L = 10kΩ connected to V_S/2. R_G pins open (G = 10), and Ref = V_S/2, unless otherwise noted.

PARAMETER		CONDITION	INA155E, U MIN	INA155E, U TYP	INA155E, U MAX	INA155EA, UA MIN	INA155EA, UA TYP	INA155EA, UA MAX	UNITS
INPUT									
Offset Voltage, RTI	V_{OS}	V_S = +5.0V, V_{CM} = V_S/2		±0.2	±1		✻	✻	mV
Over Temperature					**±1.5**			✻	mV
Drift	dV_{OS}/d_T			**±5**			✻		µV/°C
vs Power Supply	PSRR	V_S = +2.7V to +6V, V_{CM} = 0.2 • V_S		±50	±200		✻	✻	µV/V
Over Temperature					**±250**			✻	µV/V
vs Time				±0.4			✻		µV/mo
INPUT VOLTAGE RANGE									
Safe Input Voltage			(V–) – 0.5		(V+) + 0.5	✻		✻	V
Common-Mode Range[1]	V_{CM}	V_S = 5.5V	0.3		5.2[2]	✻		✻	V
		V_S = 2.7V	0.2		2.5[2]	✻		✻	V
Common-Mode Rejection Ratio	CMRR	V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 10	92	100		80	✻		dB
Over Temperature			**85**			**79**			dB
		V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 50	86	90		77	✻		dB
Over Temperature			**85**			**76**			dB
INPUT IMPEDANCE									
Differential				10^{13} || 3			✻		Ω || pF
Common-Mode				10^{13} || 3			✻		Ω || pF
INPUT BIAS CURRENT									
Input Bias Current	I_B			±1	±10		✻	✻	pA
Offset Current	I_{OS}			±1	±10		✻	✻	pA
NOISE, RTI		R_S = 0Ω, G = 10 or 50							
Voltage Noise: f = 0.1Hz to 10Hz				4.5			✻		µV/Vp-p
Voltage Noise Density: f = 10Hz				260			✻		nV/√Hz
f = 100Hz				99			✻		nV/√Hz
f = 1kHz				40			✻		nV/√Hz
Current Noise: f = 1kHz				2			✻		fA/√Hz
GAIN			10		50	✻		✻	V/V
Gain Equation				G = 10 + 400kΩ/(10kΩ + R_G)			✻		V/V
Gain Error[3]		V_S = 5.5V, V_O = 0.01V to 5.49V, G = 10		±0.02	±0.1		✻	✻	%
vs Temperature				**±2**	**±10**		✻	✻	ppm/°C
		V_S = 5.5V, V_O = 0.05V to 5.45V, G = 50		±0.05	±0.25		✻	✻	%
vs Temperature				**±15**	**±30**		✻	✻	ppm/°C
Nonlinearity		V_S = 5.5V, G = 10 or 50		±0.005	±0.015		✻	✻	% of FSR
Over Temperature					**±0.015**			✻	% of FSR
OUTPUT									
Voltage Output Swing from Rail		R_L = 10kΩ, G_{ERR} < 0.1%		5	10		✻	✻	mV
Over Temperature					**10**			✻	mV
Short-Circuit Current		Short Circuit to Ground		±50			✻		mA
Capacitance Load (stable operation)				See Typical Curve			✻		
FREQUENCY RESPONSE									
Bandwidth, –3dB	BW	G = 10		550			✻		kHz
		G = 50		110			✻		kHz
Slew Rate	SR	V_S = 5.5V, C_L = 100pF		6.5			✻		V/µs
Settling Time: 0.1%	t_S	V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 10		5			✻		µs
		V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 50		11			✻		µs
0.01%		V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 10		8			✻		µs
		V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 50		15			✻		µs
Overload Recovery		50% Input Overload		0.2			✻		µs
Total Harmonic Distortion + Noise	THD+N			See Typical Curve			✻		
POWER SUPPLY									
Specified Voltage Range			+2.7		+5.5	✻		✻	V
Operating Voltage Range				+2.5 to +6			✻		V
Quiescent Current		V_{IN} = 0, I_O = 0		1.7	2.1		✻	✻	mA
Over Temperature		**V_{IN} = 0, I_O = 0**			**2.6**			✻	mA
TEMPERATURE RANGE									
Specified Range			–40		+85	✻		✻	°C
Operating Range			–65		+150	✻		✻	°C
Storage Range			–65		+150	✻		✻	°C
Thermal Resistance	θ_{JA}								
MSOP-8 Surface Mount				150			✻		°C/W
SO-8 Surface Mount				150			✻		°C/W

✻ Same as INA155E, U.

NOTES: (1) For further information, refer to typical performance curves on common-mode input range. (2) Operation above (V+) – 1.8V (max) results in reduced common-mode rejection. See discussion and Figure 6 in the text of this data sheet. (3) Does not include error and TCR of additional optional gain-setting resistor in series with R_G, if used.

SPECIFICATIONS: V_S = +2.7V to +5.5V

Boldface limits apply over the specified temperature range, T_A = –55°C to +125°C

At T_A = +25°C, R_L = 10kΩ connected to V_S/2. R_G pins open (G = 10), and Ref = V_S/2, unless otherwise noted.

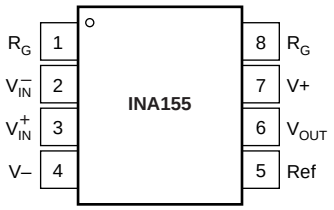
PARAMETER		CONDITION	INA155E, U MIN	INA155E, U TYP	INA155E, U MAX	INA155EA, UA MIN	INA155EA, UA TYP	INA155EA, UA MAX	UNITS
INPUT									
Offset Voltage, RTI	V_{OS}	V_S = +5.0V, V_{CM} = V_S/2		±0.2	±1		✻	✻	mV
Over Temperature					**±2**			✻	mV
Drift	dV_{OS}/d_T			**±5**			✻		µV/°C
vs Power Supply	PSRR	V_S = +2.7V to +6V, V_{CM} = 0.2 • V_S		±50	±200		✻	✻	µV/V
Over Temperature					**±250**			✻	µV/V
vs Time				±0.4			✻		µV/mo
INPUT VOLTAGE RANGE									
Safe Input Voltage			(V–) – 0.5		(V+) + 0.5	✻		✻	V
Common-Mode Range[1]	V_{CM}	V_S = 5.5V	0.3		5.2[2]	✻		✻	V
		V_S = 2.7V	0.2		2.5[2]	✻		✻	V
Common-Mode Rejection Ratio	CMRR	V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 10	92	100		80	✻		dB
Over Temperature			**82**			**78**			dB
		V_S = 5.5V, 0.6V < V_{CM} < 3.7V, G = 50	86	90		77	✻		dB
Over Temperature			**84**			**76**			dB
INPUT IMPEDANCE									
Differential				10^{13} || 3			✻		Ω || pF
Common-Mode				10^{13} || 3			✻		Ω || pF
INPUT BIAS CURRENT									
Input Bias Current	I_B			±1	±10		✻	✻	pA
Offset Current	I_{OS}			±1	±10		✻	✻	pA
NOISE, RTI		R_S = 0Ω, G = 10 or 50							
Voltage Noise: f = 0.1Hz to 10Hz				4.5			✻		µV/Vp-p
Voltage Noise Density: f = 10Hz				260			✻		nV/√Hz
f = 100Hz				99			✻		nV/√Hz
f = 1kHz				40			✻		nV/√Hz
Current Noise: f = 1kHz				2			✻		fA/√Hz
GAIN			10		50	✻		✻	V/V
Gain Equation				G = 10 + 400kΩ/(10kΩ + R_G)			✻		V/V
Gain Error[3]		V_S = 5.5V, V_O = 0.01V to 5.49V, G = 10		±0.02	±0.1		✻	✻	%
vs Temperature				**±2**	**±10**		✻	✻	ppm/°C
		V_S = 5.5V, V_O = 0.05V to 5.45V, G = 50		±0.05	±0.25		✻	✻	%
vs Temperature				**±15**	**±30**		✻	✻	ppm/°C
Nonlinearity		V_S = 5.5V, G = 10 or 50		±0.005	±0.015		✻	✻	% of FSR
Over Temperature					**±0.015**			✻	% of FSR
OUTPUT									
Voltage Output Swing from Rail		R_L = 10kΩ, G_{ERR} < 0.1%		5	10		✻	✻	mV
Over Temperature					**10**			✻	mV
Short-Circuit Current		Short Circuit to Ground		±50			✻		mA
Capacitance Load (stable operation)				See Typical Curve			✻		
FREQUENCY RESPONSE									
Bandwidth, –3dB	BW	G = 10		550			✻		kHz
		G = 50		110			✻		kHz
Slew Rate	SR	V_S = 5.5V, C_L = 100pF		6.5			✻		V/µs
Settling Time: 0.1%	t_S	V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 10		5			✻		µs
		V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 50		11			✻		µs
0.01%		V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 10		8			✻		µs
		V_S = 5.5V, V_O = 2V Step, C_L = 100pF, G = 50		15			✻		µs
Overload Recovery		50% Input Overload		0.2			✻		µs
Total Harmonic Distortion + Noise	THD+N			See Typical Curve			✻		
POWER SUPPLY									
Specified Voltage Range			+2.7		+5.5	✻		✻	V
Operating Voltage Range				+2.5 to +6			✻		V
Quiescent Current		V_{IN} = 0, I_O = 0		1.7	2.1		✻	✻	mA
Over Temperature		**V_{IN} = 0, I_O = 0**			**2.8**			✻	mA
TEMPERATURE RANGE									
Specified Range			–55		+125	✻		✻	°C
Operating Range			–65		+150	✻		✻	°C
Storage Range			–65		+150	✻		✻	°C
Thermal Resistance	θ_{JA}								
MSOP-8 Surface Mount				150			✻		°C/W
SO-8 Surface Mount				150			✻		°C/W

✻ Same as INA155E, U.

NOTES: (1) For further information, refer to typical performance curves on common-mode input range. (2) Operation above (V+) – 1.8V (max) results in reduced common-mode rejection. See discussion and Figure 6 in the text of this data sheet. (3) Does not include error and TCR of additional optional gain-setting resistor in series with R_G, if used.

PIN CONFIGURATION

Top View **SO-8 (U), MSOP-8 (E)**



ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	7.5V
Signal Input Terminals, Voltage[2]	(V–) – 0.5V to (V+) + 0.5V
Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–65°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power supply rails. Input signals that can swing more that 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short circuit to ground.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

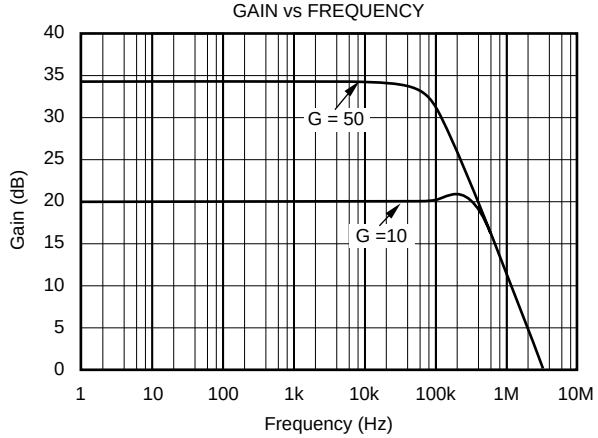
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
INA155U	SO-8	182	–55°C to +125°C	INA155U	INA155U	Rails
"	"	"	"	"	INA155U/2K5	Tape and Reel
INA155UA	SO-8	182	–55°C to +125°C	INA155UA	INA155UA	Rails
"	"	"	"	"	INA155UA/2K5	Tape and Reel
INA155E	MSOP-8	337	–55°C to +125°C	A55	INA155E/250	Tape and Reel
"	"	"	"	"	INA155E/2K5	Tape and Reel
INA155EA	MSOP-8	337	–55°C to +125°C	A55	INA155EA/250	Tape and Reel
"	"	"	"	"	INA155EA/2K5	Tape and Reel

NOTES: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /2K5 indicates 2500 devices per reel). Ordering 2500 pieces of “INA155UA/2K5” will get a single 2500-piece Tape and Reel.

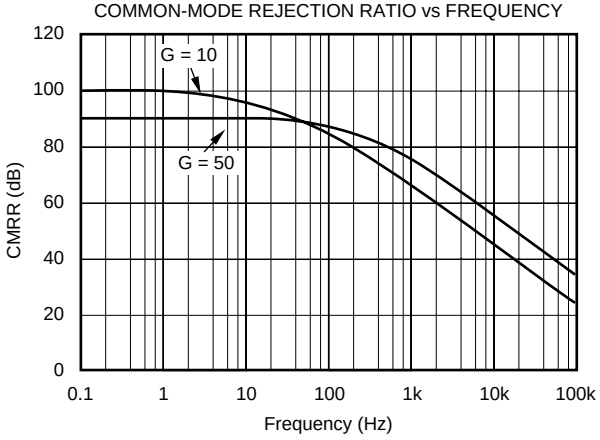
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S/2. R_G pins open (G = 10), and Ref = V_S/2, unless otherwise noted.

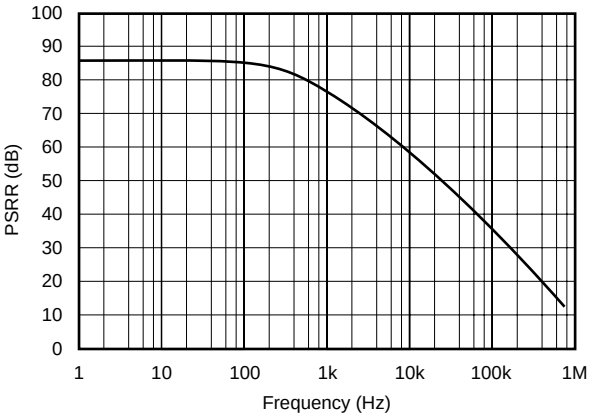
GAIN vs FREQUENCY



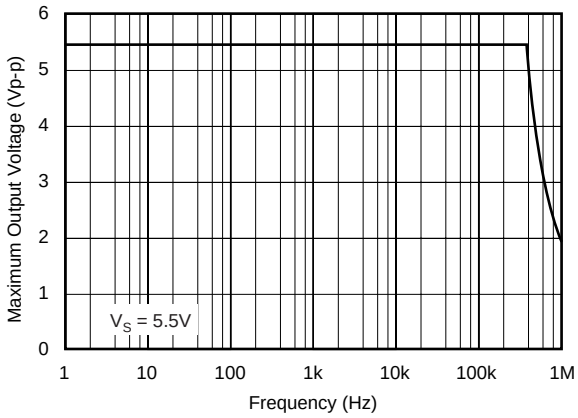
COMMON-MODE REJECTION RATIO vs FREQUENCY



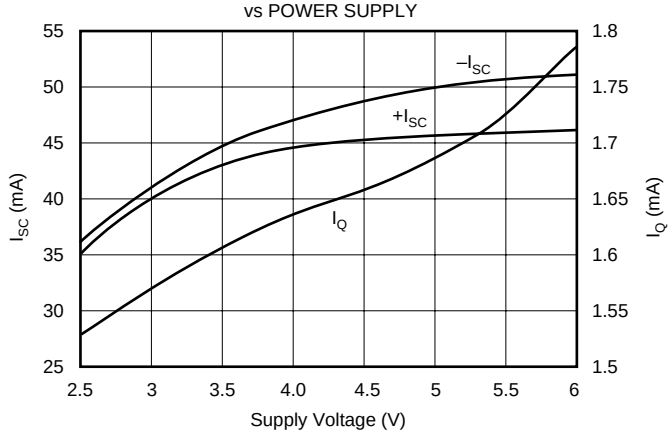
POWER SUPPLY REJECTION RATIO vs FREQUENCY



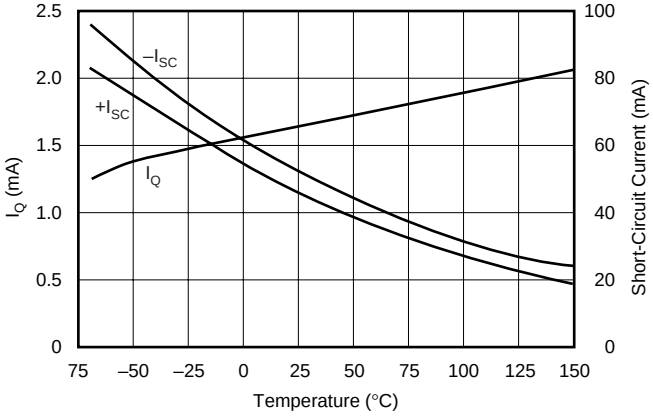
MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



SHORT-CIRCUIT CURRENT AND QUIESCENT CURRENT vs POWER SUPPLY



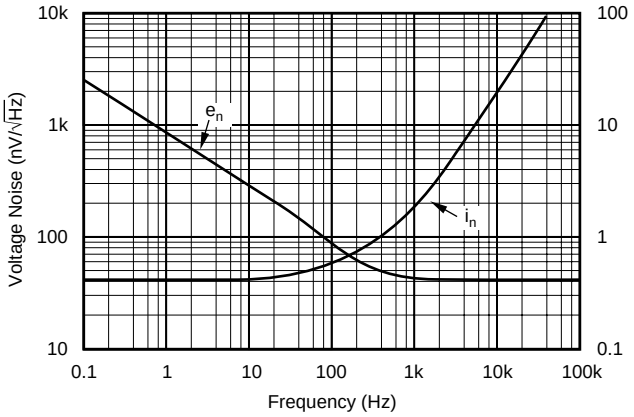
QUIESCENT CURRENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE



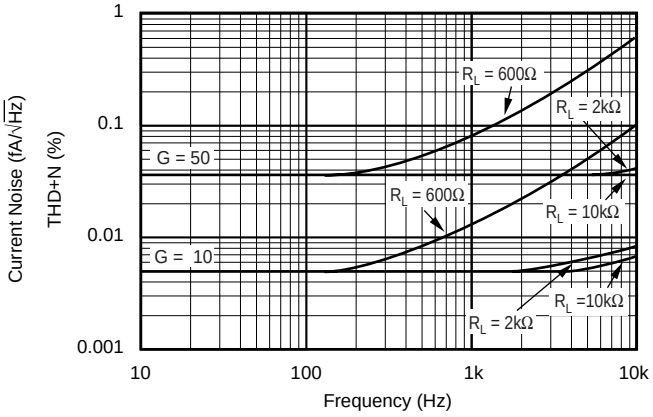
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S/2. R_G pins open (G = 10), and Ref = V_S/2, unless otherwise noted.

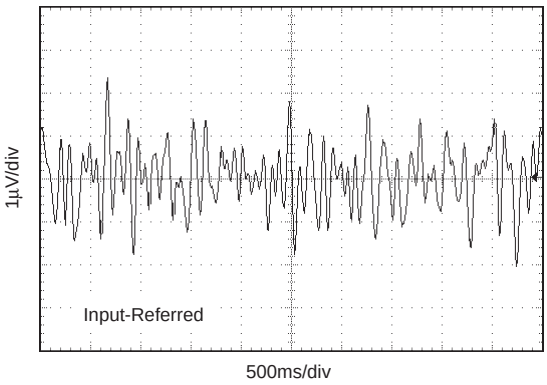
INPUT VOLTAGE AND CURRENT NOISE DENSITY vs FREQUENCY



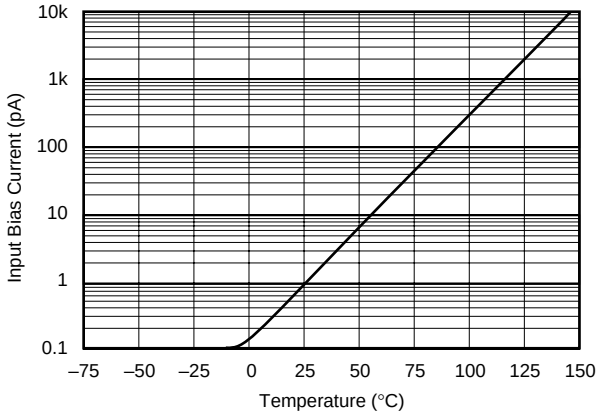
TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY



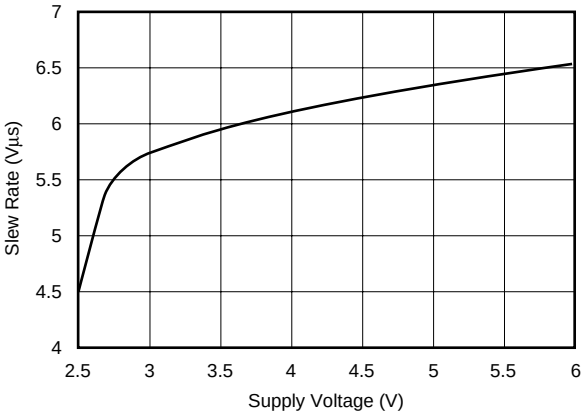
0.1Hz TO 10Hz VOLTAGE NOISE



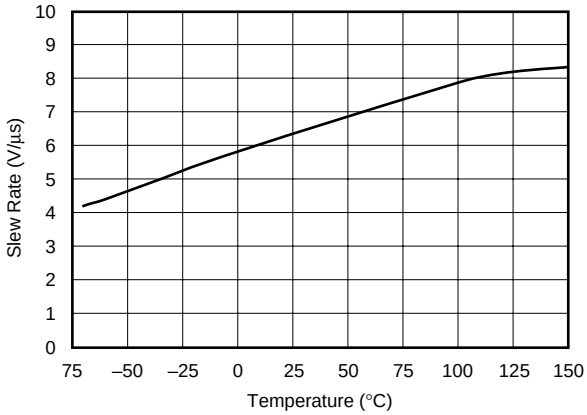
INPUT BIAS CURRENT vs TEMPERATURE



SLEW RATE vs POWER SUPPLY



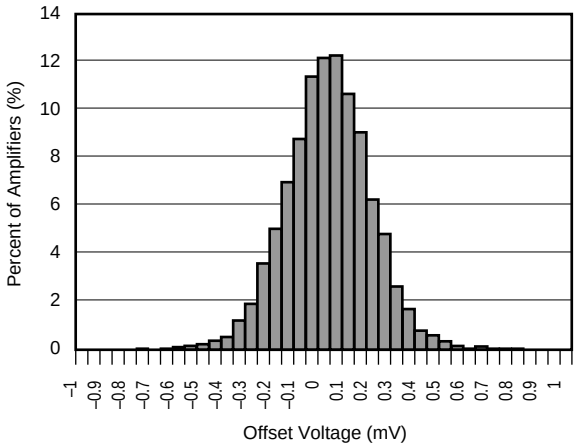
SLEW RATE vs TEMPERATURE



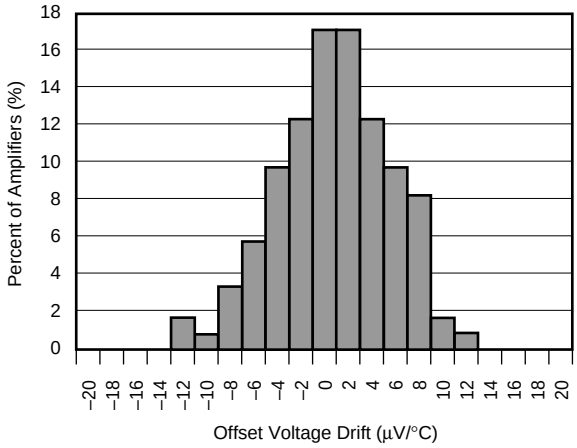
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S/2. R_G pins open (G = 10), and Ref = V_S/2, unless otherwise noted.

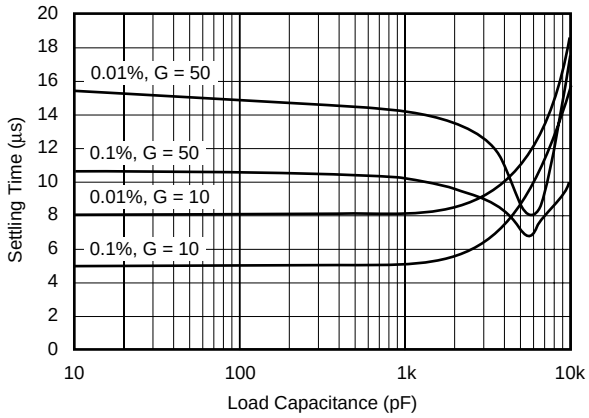
OFFSET VOLTAGE
PRODUCTION DISTRIBUTION



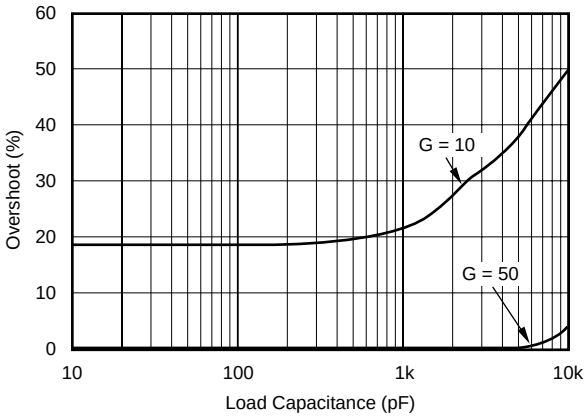
OFFSET VOLTAGE DRIFT
PRODUCTION DISTRIBUTION



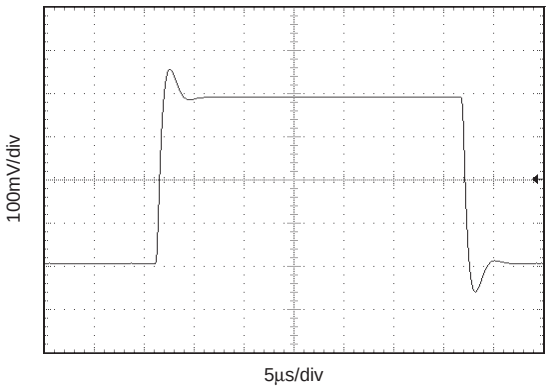
SETTLING TIME vs LOAD CAPACITANCE



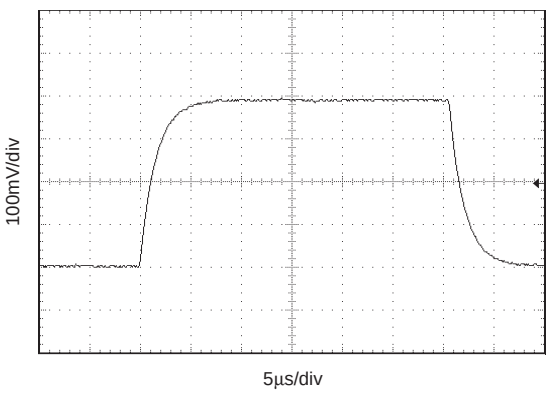
OVERSHOOT vs LOAD CAPACITANCE



SMALL-SIGNAL STEP RESPONSE
G = 10, C_L = 100pF, R_L = 10kΩ



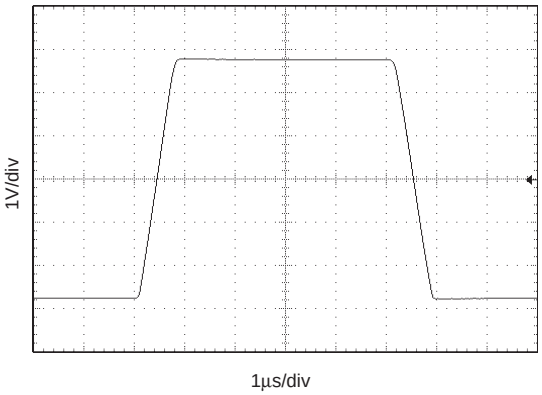
SMALL-SIGNAL STEP RESPONSE
G = 50, C_L = 100pF, R_L = 10kΩ



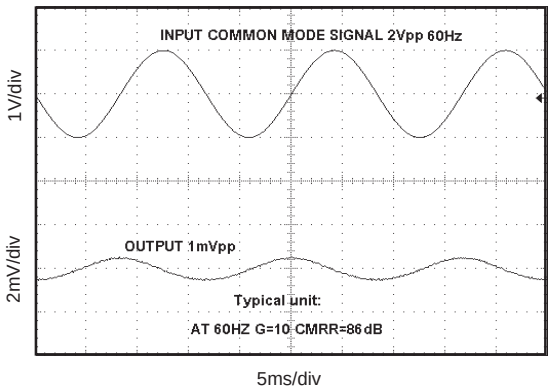
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, V_S = 5.5V, R_L = 10kΩ connected to V_S/2. R_G pins open (G = 10), and Ref = V_S/2, unless otherwise noted.

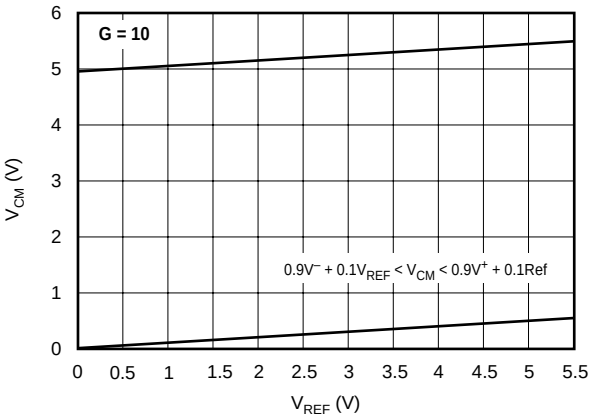
LARGE-SIGNAL STEP RESPONSE
G = 10, G = 50, C_L = 100pF, R_L = 10kΩ



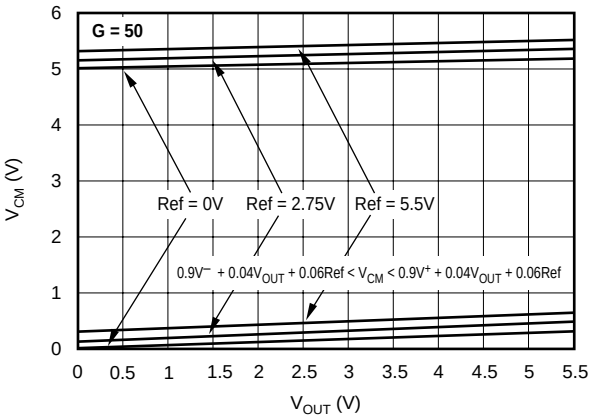
COMMON-MODE REJECTION AT 60Hz



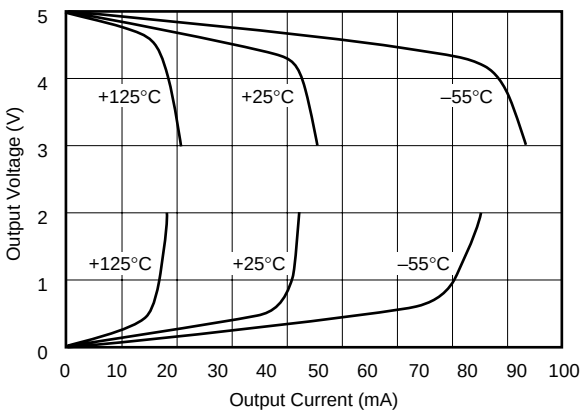
INPUT COMMON-MODE RANGE
vs REFERENCE VOLTAGE, G = 10



INPUT COMMON-MODE RANGE
vs OUTPUT VOLTAGE, G = 50



OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



APPLICATIONS INFORMATION

Figure 1 shows the basic connections required for operation of the INA155. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

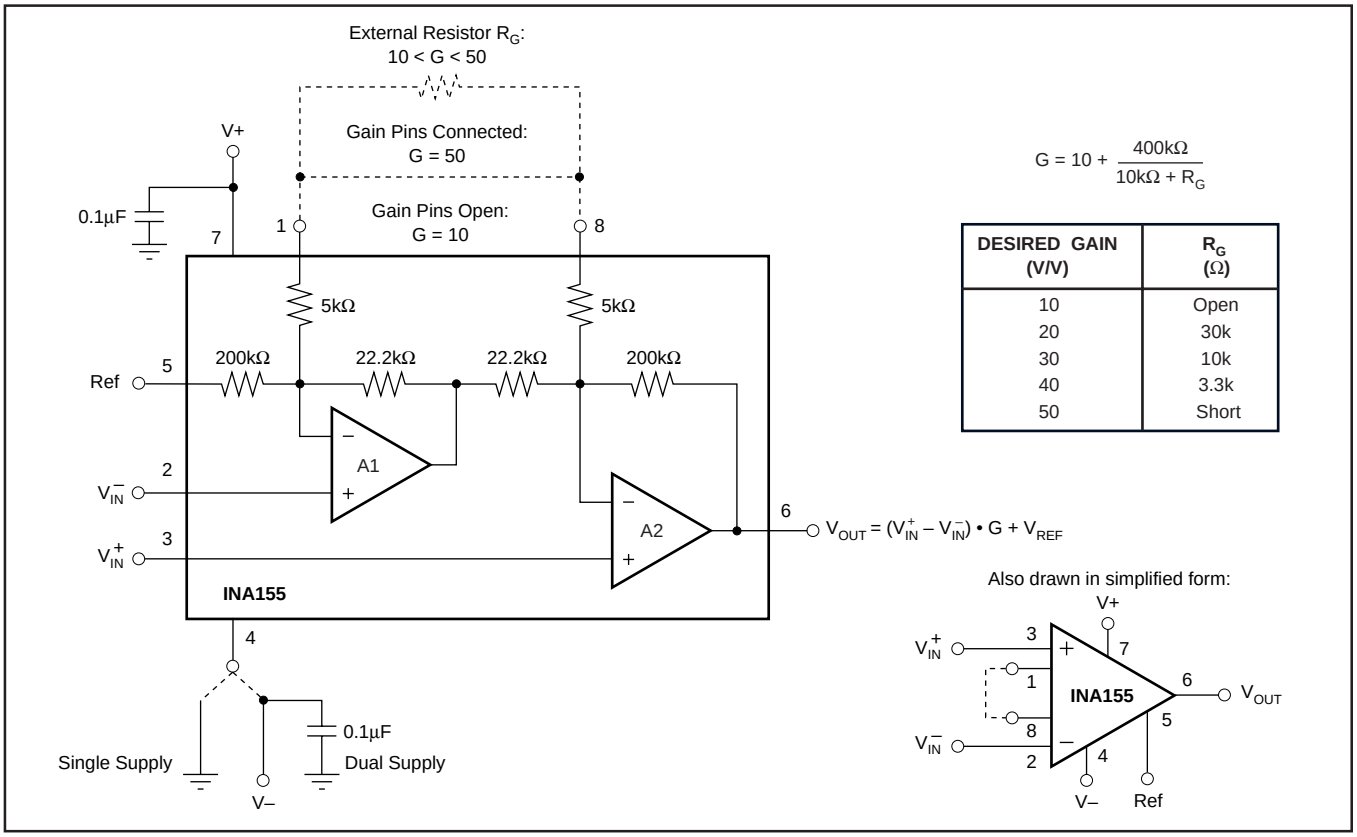
The output is referred to the output reference terminal, Ref, which is normally set to $V_S/2$. This must be a low-impedance connection to ensure good common-mode rejection. A resistance of 200Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMRR.

In addition, for the G = 50 configuration, the connection between pins 1 and 8 must be low-impedance. A connection impedance of 20Ω can cause a 0.2% shift in gain error.

OPERATING VOLTAGE

The INA155 is fully specified and guaranteed over the supply range +2.7V to +5.5V, with key parameters guaranteed over the temperature range of –55°C to +125°C. Parameters that vary significantly with operating voltages, load conditions or temperature are shown in the Typical Performance Curves.

The INA155 can be operated from either single or dual power supplies. By adjusting the voltage applied to the reference terminal, the input common-mode voltage range and the output range can be adjusted within the bounds shown in the Typical Performance Curves. Figure 2 shows a bridge amplifier circuit operated from a single +5V power supply. The bridge provides a relatively small differential voltage on top of an input common-mode voltage near 2.5V.



DESIRED GAIN (V/V)	R_G (Ω)
10	Open
20	30k
30	10k
40	3.3k
50	Short

FIGURE 1. Basic Connections.

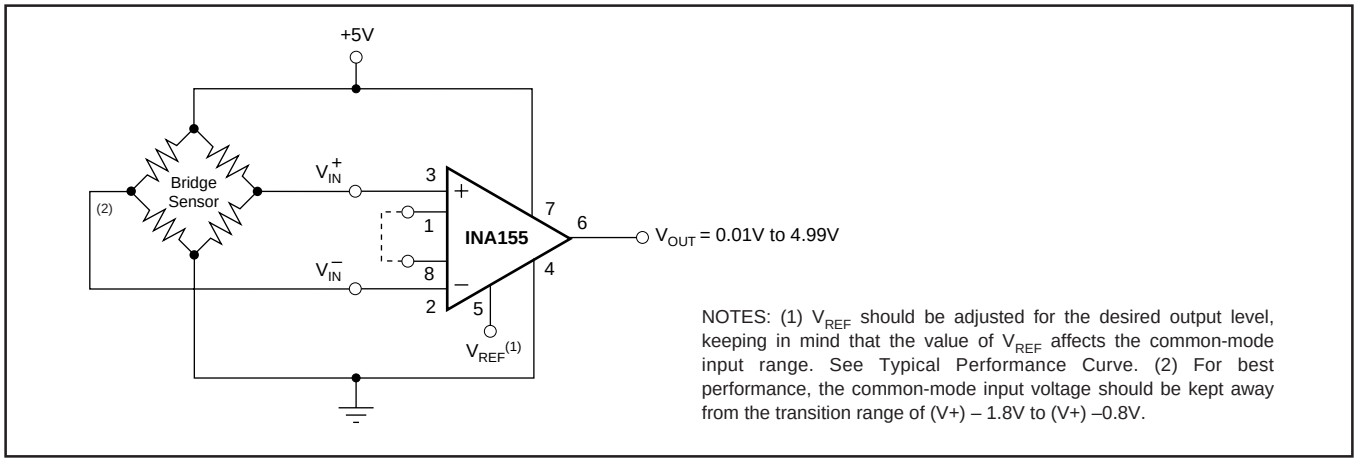


FIGURE 2. Single-Supply Bridge Amplifier.

SETTING THE GAIN

Gain of 10 is achieved simply by leaving the two gain pins (1 and 8) open. Gain of 50 is achieved by connecting the gain pins together directly. In the G = 10 configuration, the gain error is less than 0.1%. In the G = 50 configuration, the gain error is less than 0.25%.

Gain can be set to any value between 10 and 50 by connecting a resistor R_G between the gain pins according to the following equation:

$$10 + 400k\Omega/(10k\Omega + R_G) \quad (1)$$

This is demonstrated in Figure 1 and is shown with the commonly used gains and resistor R_G values. However, because the absolute value of internal resistors is not guaranteed, using the INA155 in this configuration will increase the gain error and gain error drift with temperature, as shown in Figure 3.

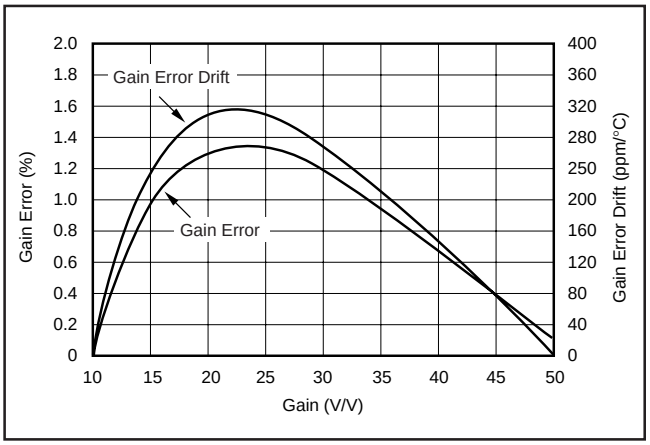
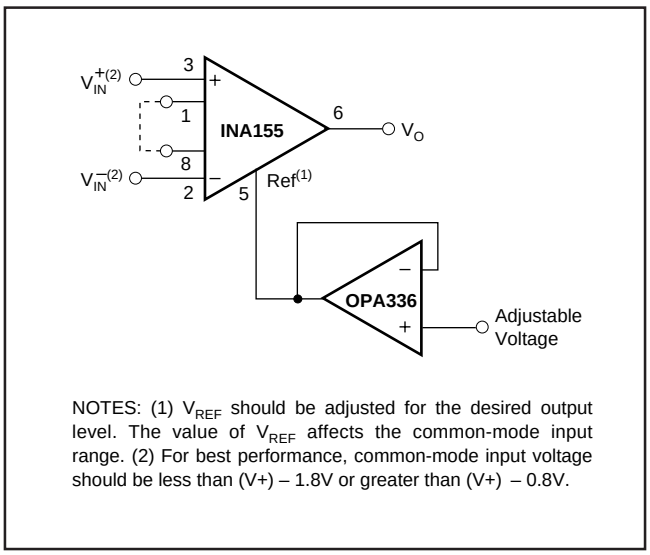


FIGURE 3. Typical Gain Error and Gain Error Drift with External Resistor.

OFFSET TRIMMING

The INA155 is laser trimmed for low offset voltage. In most applications, no external offset adjustment is required. However, if necessary, the offset can be adjusted by applying a correction voltage to the reference terminal. Figure 4 shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is added to the output signal. An op amp buffer is used to provide low impedance at the Ref terminal to preserve good common-mode rejection.



NOTES: (1) V_{REF} should be adjusted for the desired output level. The value of V_{REF} affects the common-mode input range. (2) For best performance, common-mode input voltage should be less than (V+) – 1.8V or greater than (V+) – 0.8V.

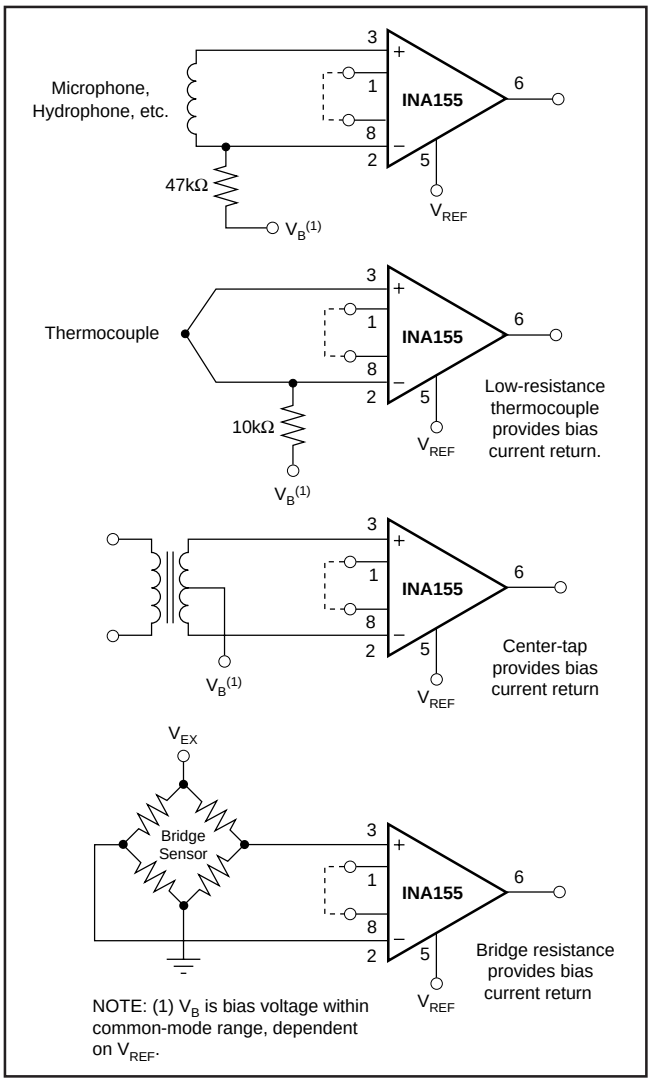
FIGURE 4. Optional Trimming of Output Offset Voltage.

INPUT BIAS CURRENT RETURN

The input impedance of the INA155 is extremely high—approximately $10^{13}\Omega$, making it ideal for use with high-impedance sources. However, a path must be provided for the input bias current of both inputs. This input bias current is less than 10pA and is virtually independent of the input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 5 shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential that exceeds the common-mode range and the input amplifier will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple in Figure 5). With higher source impedance, using two equal resistors provides a balanced input with advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.



NOTE: (1) V_B is bias voltage within common-mode range, dependent on V_{REF}.

FIGURE 5. Providing an Input Common-Mode Current Path.

INPUT COMMON-MODE RANGE

The input common-mode range of the INA155 for various operating conditions is shown the in Typical Performance Curves. The common-mode input range is limited by the output voltage swing of A1, an internal circuit node. For the G = 10 configuration, output voltage of A1 can be expressed as:

$$V_{OUTA1} = -\,{}^{1}/_{9}V_{REF} + (1 + {}^{1}/_{9})\,V_{IN} \quad (2)$$

Using this equation given that the output of A1 can swing to within 10mV of either rail, the input common-mode voltage range can be calculated. When the input common-mode range is exceeded (A1's output is saturated), A2 can still be in linear operation and respond to changes in the non-inverting input voltage. However, the output voltage will be invalid.

The common-mode range for the G = 50 configuration is included in the Typical Performance Curve, "Input Common-Mode Range vs Output Voltage."

INPUT RANGE FOR BEST ACCURACY

The internal amplifiers have rail-to-rail input stages, achieved by using complementary n- and p-channel input pairs. The common-mode input voltage determines whether the p-channel or the n-channel input stage is operating. The transition between the input stages is gradual and occurs between (V+) – 1.8V to (V+) – 0.8V. Due to these characteristics operating the INA155 with input voltages within the transition region of (V+) – 1.8V to (V+) – 0.8V results in a shift in input offset voltage and reduced common-mode and power supply rejection performance. Typical patterns of the offset voltage change throughout the input common-mode range are illustrated in Figure 6. The INA155 can be operated below or above the transition region with excellent results. Figure 7 demonstrates the use of the INA155 in a single-supply, high-side current monitor. In this application, the INA155 is operated above the transition region.

RAIL-TO-RAIL OUTPUT

A class AB output stage with common-source transistors is used to achieve rail-to-rail output. For resistive loads greater than 10kΩ, the output voltage can swing to within a few millivolts of the supply rail while maintaining low gain error. For heavier loads and over temperature, see the typical performance curve "Output Voltage Swing vs Output Current." The INA155's low output impedance at high frequencies makes it suitable for directly driving Capacitive Digital-to-Analog (CDAC) input A/D converters, as shown in Figure 9.

INPUT PROTECTION

Device inputs are protected by ESD diodes that will conduct if the input voltages exceed the power supplies by more than 500mV. Momentary voltages greater than 500mV beyond the power supply can be tolerated if the current on the input pins is limited to 10mA. This is easily accomplished with input resistors R_{LIM} as shown in Figure 8. Many input signals are inherently current-limited to less than 10mA, therefore, a limiting resistor is not required.

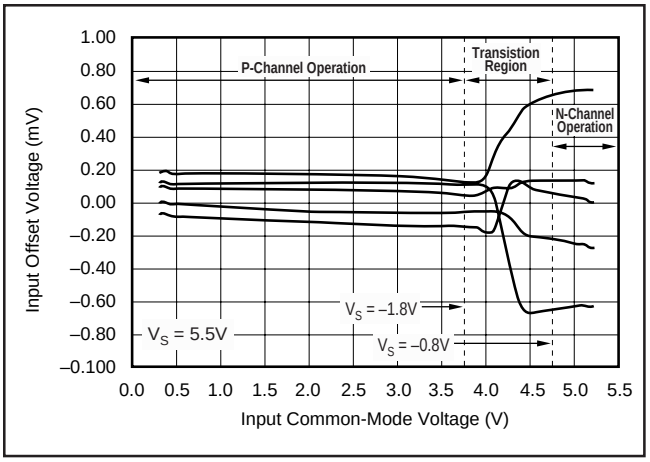


FIGURE 6. Input Offset Voltage Changes with Common-Mode Voltage.

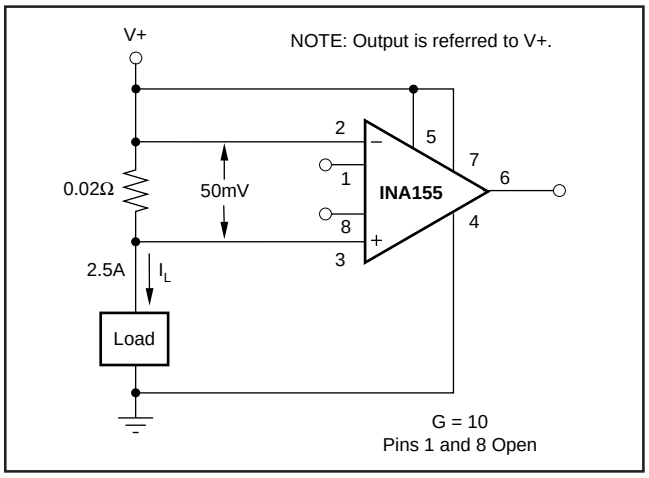


FIGURE 7. Single-Supply, High-Side Current Monitor.

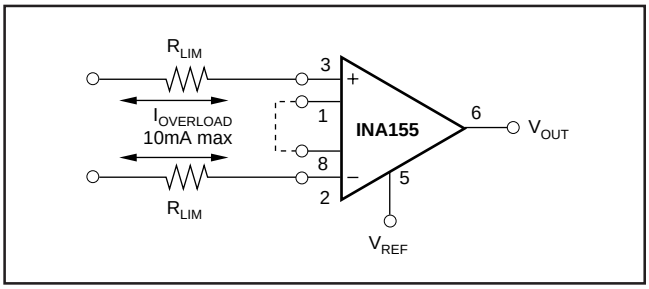


FIGURE 8. Input Current Protection for Voltages Exceeding the Supply Voltage.

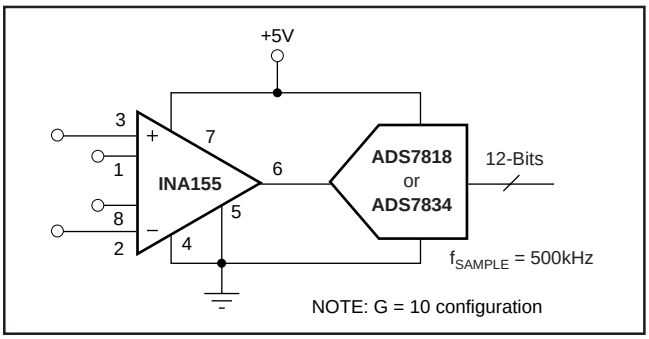


FIGURE 9. INA155 Directly Drives Capacitive-Input, High-Speed A/D Converter.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA155E/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A55	Samples
INA155E/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A55	Samples
INA155EA/250	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A55	Samples
INA155EA/250G4	ACTIVE	VSSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A55	Samples
INA155EA/2K5	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A55	Samples
INA155EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR		A55	Samples
INA155U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		INA 155U	Samples
INA155U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		INA 155U	Samples
INA155U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		INA 155U	Samples
INA155UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		INA 155U A	Samples
INA155UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		INA 155U A	Samples
INA155UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		INA 155U A	Samples
INA155UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		INA 155U	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

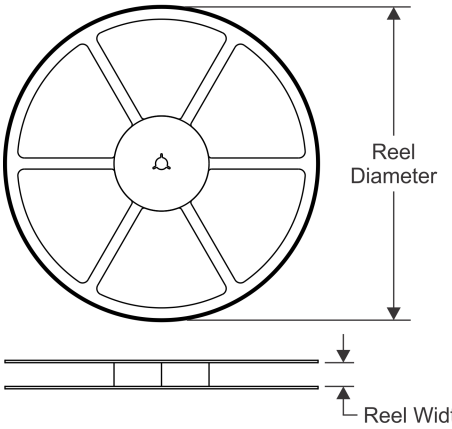
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

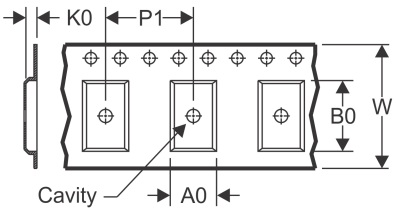
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

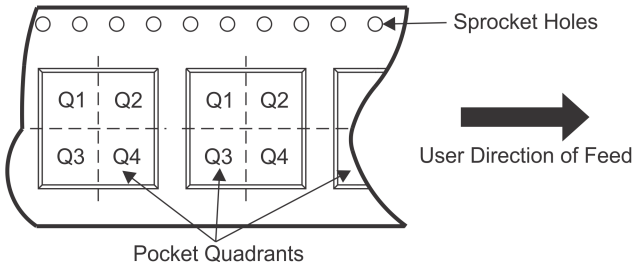


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

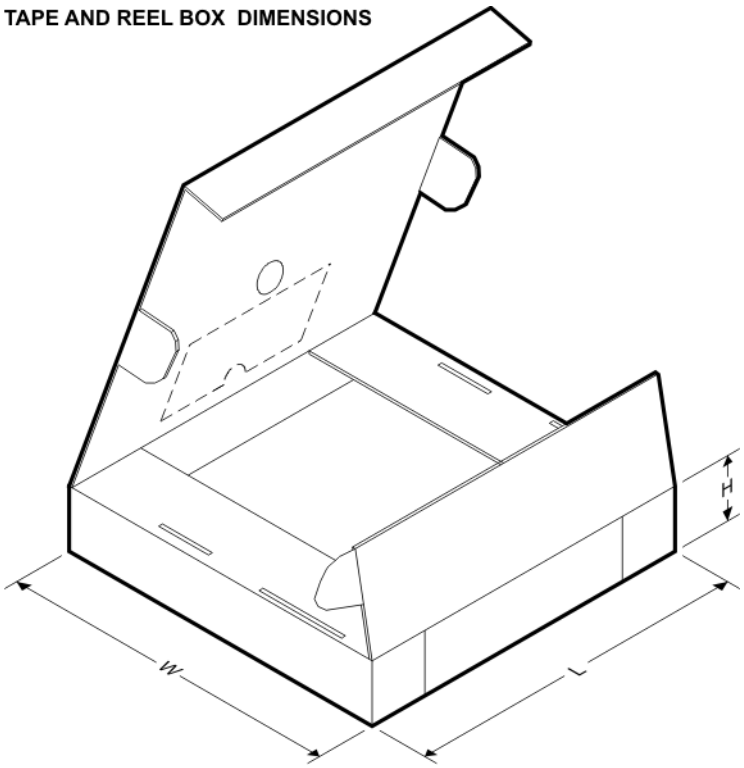
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA155E/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA155EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA155EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
INA155U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA155UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA155E/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA155EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
INA155EA/2K5	VSSOP	DGK	8	2500	367.0	367.0	35.0
INA155U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA155UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

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