

CoolGaN™ G5

CoolGaN™ Transistor 650 V G5 (IGT65R035D2)

Infineon’s CoolGaN™ is a highly efficient gallium nitride (GaN) transistor designed for power conversion at 650 V. It enables higher power density, supports reduced system BOM cost, and facilitates miniaturized form factors. Produced using 200 mm (8 inch) wafer technology and fully automated production lines, it features narrow production tolerances and the highest product quality. This makes it suitable for a wide range of applications, from consumer electronics to industrial applications.

Features

- Enhancement mode transistor
- Ultra-fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate and output charge
- Superior commutation ruggedness
- 2 kV HBM ESD standards

Benefits

- Normally OFF transistor technology ensures safe operation
- Enables rapid and precise power delivery control
- Improves system efficiency and reliability
- Ensures robust performance under challenging conditions

These features collectively make CoolGaN™ a game-changer in the realm of power conversion, offering a compelling combination of efficiency, compactness, and reliability.

Potential applications

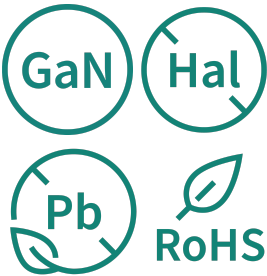
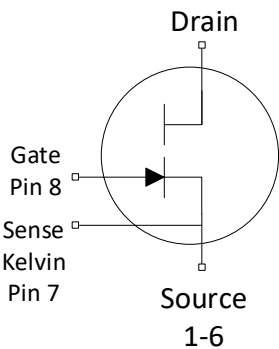
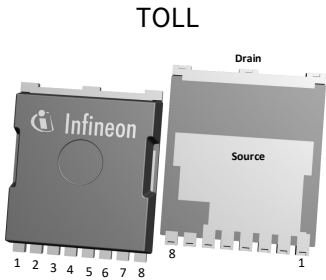
Industrial, telecom, datacenter SMPS based on half-bridge hard and soft switching topologies such as totem pole PFC and high frequency LLC, as well as charger and adapter.

Product validation

Qualified according to relevant JEDEC tests.

Table 1 Key performance parameters

Parameter	Value	Unit
$V_{DS,max}$	650	V
$V_{DS,trans-max}$	900	V
$R_{DS(on),max}$	42	mΩ
$Q_{g,typ}$	7.7	nC
$I_{D,pulse}$	97	A
$Q_{oss} @ 400 V$	57	nC
Q_{rr}	0	nC



Part number	Package	Marking	Related links
IGT65R035D2	PG-HSOF-8	65R035D2	see Appendix A



Table of contents

Description 1

Maximum ratings 3

Thermal characteristics 5

Electrical characteristics 6

Electrical characteristics diagrams 8

Test circuits 13

Package outlines 14

Appendix A 17

Revision history 18

Trademarks 19

Disclaimer 19

1 Maximum ratings

at $T_j = 25^\circ\text{C}$, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80% of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain source voltage, continuous	$V_{DS,max}$	-	-	650	V	$V_{GS} = 0\text{ V}$; derating recommendation according JEDEC JEP198
Leakage current at drain source transient voltage	$I_{DS,trans}$	-	-	20	mA	$V_{GS} = 0\text{ V}$; $V_{DS,trans} = 900\text{ V}$
Drain source voltage transient	$V_{DS,trans}$	-	-	900	V	<1% duty cycle; <1 μs ; 1 million pulses
Drain source voltage, pulsed	$V_{DS,pulsed}$	-	-	750	V	$T_j = 25^\circ\text{C}$; $V_{GS} \leq 0\text{ V}$; cumulated stress time $\leq 10\text{ h}$
						$T_j = 125^\circ\text{C}$; $V_{GS} \leq 0\text{ V}$; cumulated stress time $\leq 1\text{ h}$
Switching surge voltage, pulsed	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse} = 750\text{ V}$; turn on $I_{D,pulse} = 44\text{ A}$; $f \leq 100\text{ kHz}$; $T_j = 105^\circ\text{C}$; $t \leq 100\text{ s}$ (10 million pulses)
Continuous current, drain source ¹⁾	I_D	-	-	49	A	$T_C = 25^\circ\text{C}$; $T_j = T_{j,max}$
Pulsed current, drain source ²⁾	$I_{D,pulse}$	-97	-	97	A	$T_j = 25^\circ\text{C}$; $I_G = 42\text{ mA}$; See Diagram 3, 5
		-58		58		$T_j = 125^\circ\text{C}$; $I_G = 42\text{ mA}$; See Diagram 4, 6
Gate current, continuous ³⁾	$I_{G,avg}$	-	19	32	mA	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$; See Table 9
Gate current, pulsed ³⁾	$I_{G,pulsed}$	-3.2	-	3.2	A	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$; $t_{pulse} = 50\text{ ns}$; $f = 100\text{ kHz}$; See Table 9
Gate source voltage, continuous ³⁾	V_{GS}	-10	-	-	V	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$; See Diagram 12
Gate source voltage, pulsed ³⁾	$V_{GS,pulse}$	-25	-	-	V	$T_j = -55^\circ\text{C}$ to $T_j = 150^\circ\text{C}$; $t_{pulse} = 50\text{ ns}$; $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	-	-	167	W	$T_C = 25^\circ\text{C}$
Operating junction temperature	T_j	-55	-	150	$^\circ\text{C}$	-
Storage temperature	T_{stg}	-55	-	150	$^\circ\text{C}$	Max shelf life depends on storage conditions
Drain-source voltage slew-rate	dv/dt	-	-	200	V/ns	-

- 1) Limited by $T_{j,max}$. Maximum duty cycle $D = 0.75$
- 2) Defined by design. Not subject to production test.
- 3) Consider the influence of the gate current (I_G) on the drain current (I_D). For further details, refer to the [gate drive whitepaper](#) and the [reliability whitepaper](#), or contact your local Infineon sales office.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.76	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	86	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	62	°C/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm ² (one layer, 70 µm thickness) copper area for tab (source) connection and cooling. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL1

3 Electrical characteristics

at $T_j=25^\circ\text{C}$, unless specified otherwise

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9	1.2	1.6	V	$I_{DS}=4.2\text{ mA}; V_{DS}=10\text{ V}; T_j=25^\circ\text{C}$
		-	1	-		$I_{DS}=4.2\text{ mA}; V_{DS}=10\text{ V}; T_j=150^\circ\text{C}$
Gate-Source reverse clamping voltage	$V_{GS, clamp}$	-	-	-8	V	$I_{GS}=-1\text{ mA}$
Drain-Source leakage current	I_{DSS}	-	1.6	160	μA	$V_{DS}=650\text{ V}; V_{GS}=0\text{ V}; T_j=25^\circ\text{C}$
			32	-		$V_{DS}=650\text{ V}; V_{GS}=0\text{ V}; T_j=150^\circ\text{C}$
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.035	0.042	Ω	$I_G=42\text{ mA}; I_D=13\text{ A}; T_j=25^\circ\text{C}$
			0.075	-		$I_G=42\text{ mA}; I_D=13\text{ A}; T_j=150^\circ\text{C}$
Gate resistance ⁴⁾	$R_{G,int}$	-	1.4	-	Ω	LCR impedance measurement; $f=f_{res}$, open drain

⁴⁾ Defined by design. Not subject to production test.

Table 5 Dynamic characteristics

Defined by design. Not subject to production test.

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	540	-	pF	$V_{GS}=0\text{ V}; V_{DS}=400\text{ V}; f=1\text{ MHz}$
Output capacitance	C_{oss}		91			
Reverse transfer capacitance	C_{rss}		1.3			
Effective output capacitance, time related ⁵⁾	$C_{o(tr)}$	-	142	-	pF	$V_{GS}=0\text{ V}; V_{DS}=0\text{ to }400\text{ V}; I_D=\text{const}$
Effective output capacitance, energy related ⁶⁾	$C_{o(er)}$	-	105	-	pF	$V_{DS}=0\text{ to }400\text{ V}$
Output charge	Q_{oss}		57	-	nC	
Coss stored energy	E_{oss}		8.4	-	μJ	
Turn-on delay time	$t_{d(on)}$	-	11	-	ns	$I_D=13\text{ A}; R_{ON}=3.3\text{ }\Omega; R_{OFF}=3.3\text{ }\Omega;$ $R_{SS}=220\text{ }\Omega; C_C=5.3\text{ nF};$ $V_{DRV}=12\text{ V}; \text{ see Table 8}$
Turn-off delay time	$t_{d(off)}$		15			
Rise time	t_r		10			
Fall time	t_f		11			

⁵⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

⁶⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate charge ⁷⁾	Q_G	-	7.7	-	nC	$V_{GS}=0$ to 3 V; $V_{DS}=400$ V; $I_D=13$ A

⁷⁾ Defined by design. Not subject to production test.

Table 7 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.0	2.4	V	$V_{GS}=0$ V; $I_{SD}=13$ A
Pulsed current, reverse	$I_{SD,pulse}$	-	-	97	A	$I_G=42$ mA
Reverse recovery charge ⁸⁾	Q_{rr}	-	0	-	nC	$I_{SD}=13$ A; $V_{DS}=400$ V

⁸⁾ Defined by design. Not subject to production test. Excluding Q_{oss} .

4 Electrical characteristics diagrams

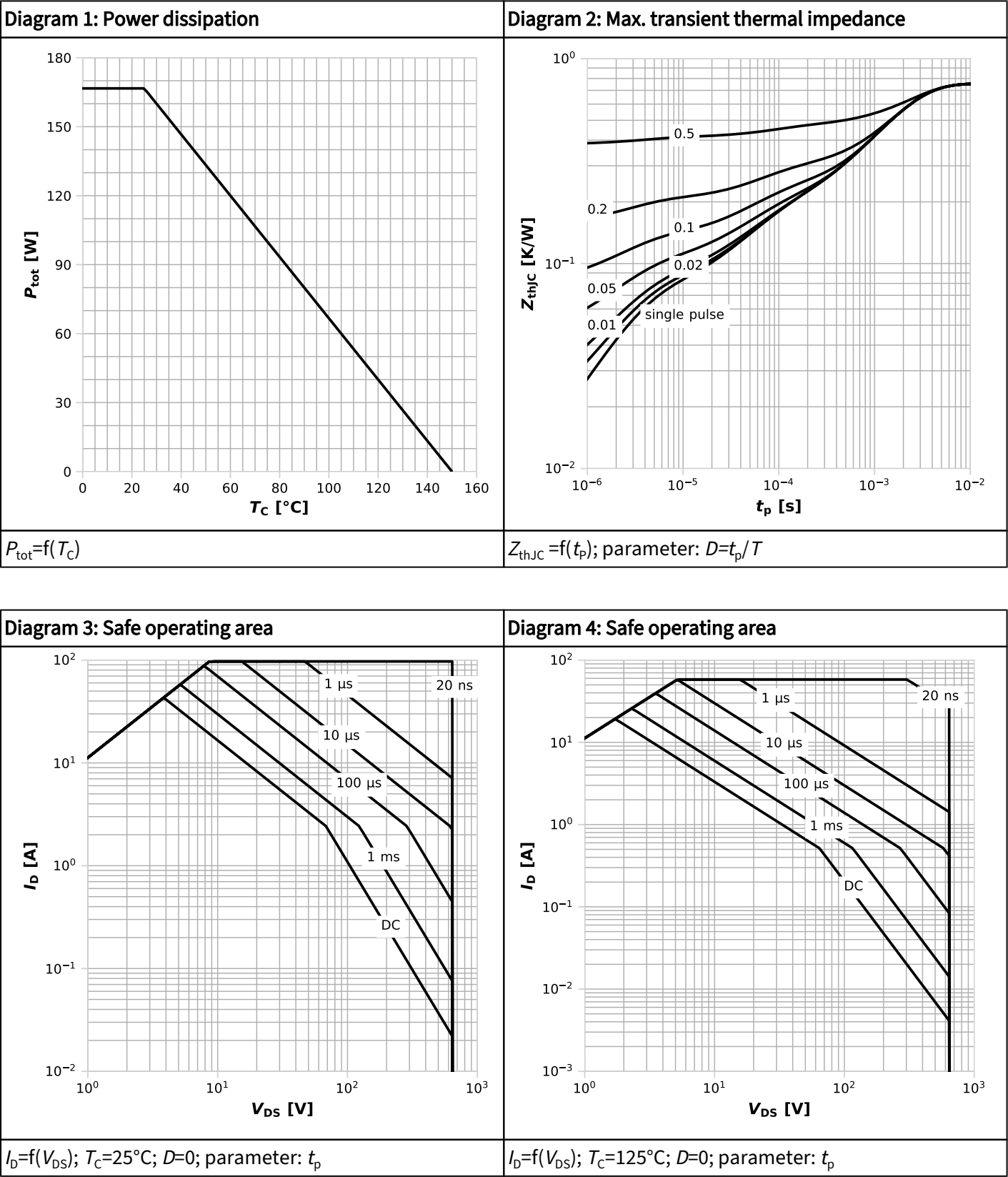
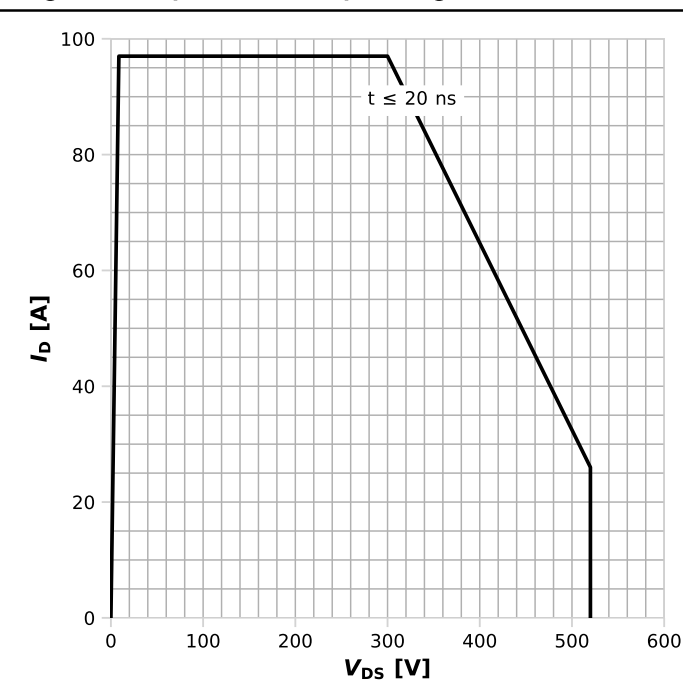
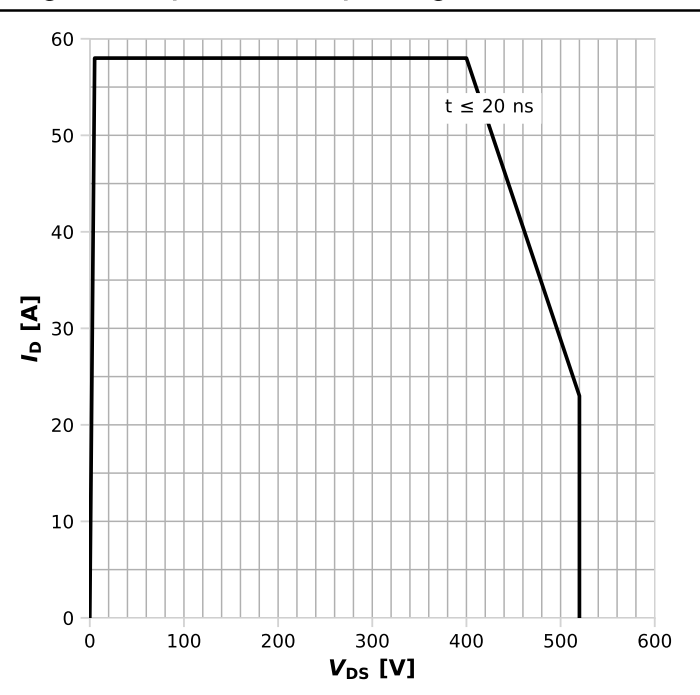


Diagram 5: Repetitive safe operating area



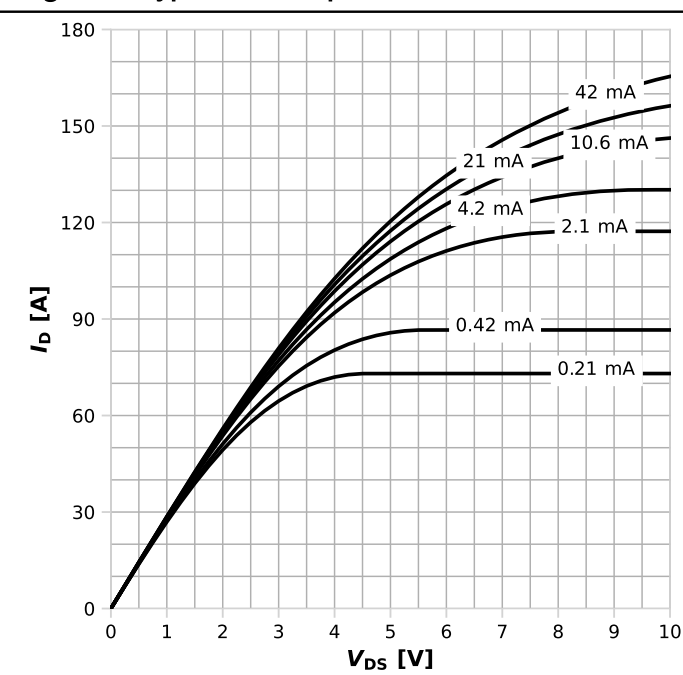
$I_D = f(V_{DS})$; $T_C = 25^\circ\text{C}$; $T_J \leq 150^\circ\text{C}$; parameter: t_p

Diagram 6: Repetitive safe operating area



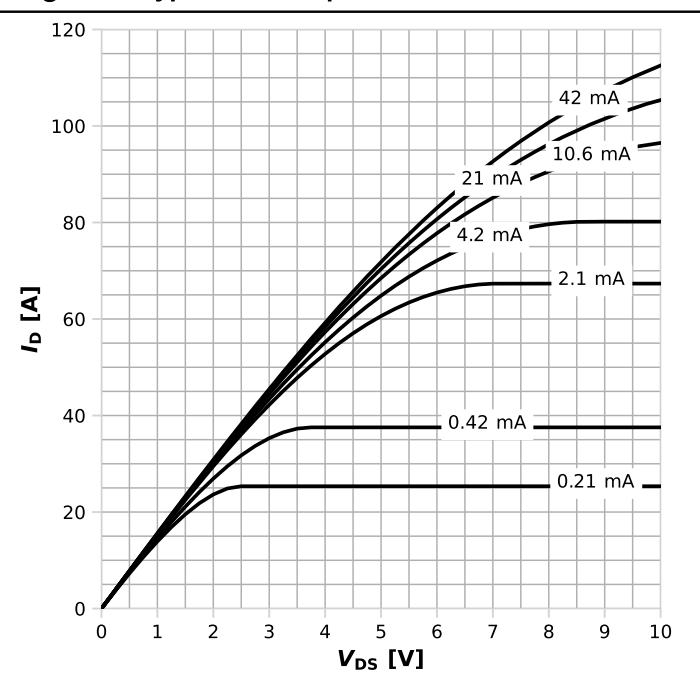
$I_D = f(V_{DS})$; $T_C = 125^\circ\text{C}$; $T_J \leq 150^\circ\text{C}$; parameter: t_p

Diagram 7: Typ. static* output characteristics



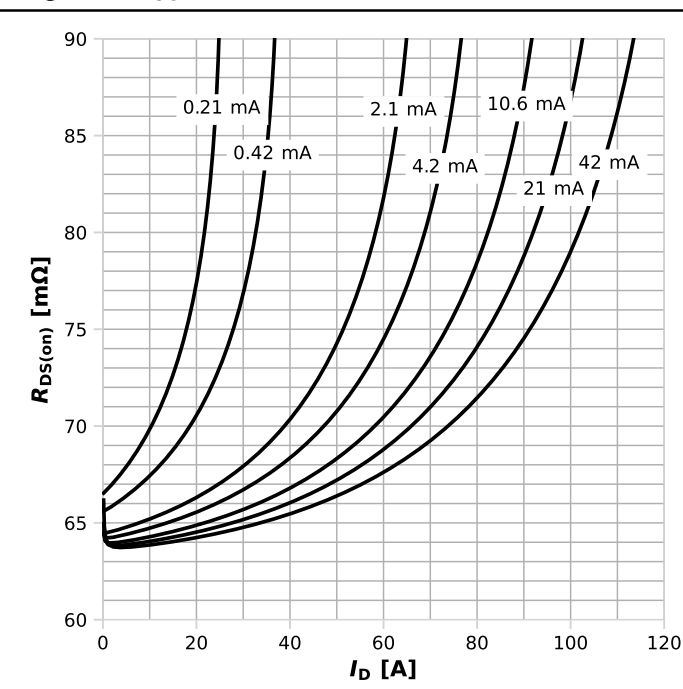
$I_D = f(V_{DS})$; $T_J = 25^\circ\text{C}$; parameter: I_{GS} ;
* Refer to gate drive application note (see table 10)

Diagram 8: Typ. static* output characteristics



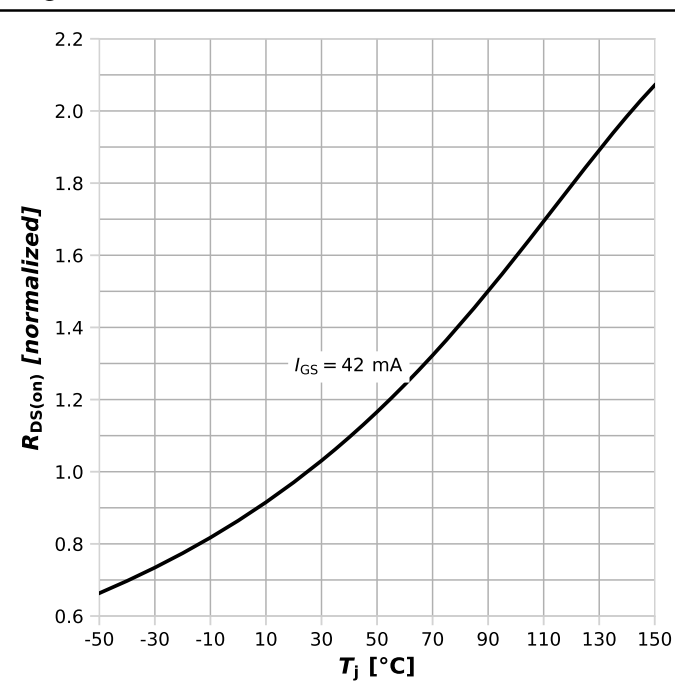
$I_D = f(V_{DS})$; $T_J = 125^\circ\text{C}$; parameter: I_{GS} ;
* Refer to gate drive application note (see table 10)

Diagram 9: Typ. Drain-source on-state resistance



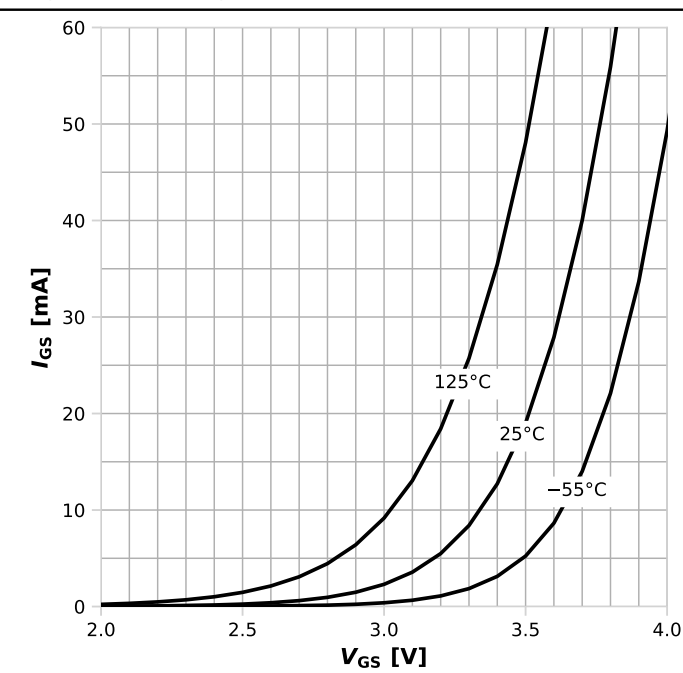
$R_{DS(on)} = f(I_D); T_j = 125^\circ\text{C}; \text{parameter: } I_{GS}$

Diagram 10: Drain-source on-state resistance



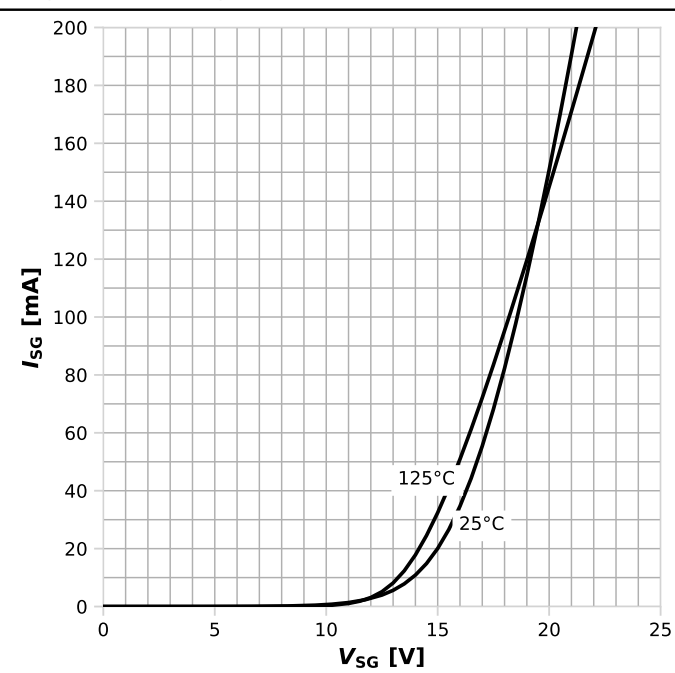
$R_{DS(on)} = f(T_j); I_D = 13 \text{ A}$

Diagram 11: Typ. gate characteristics forward



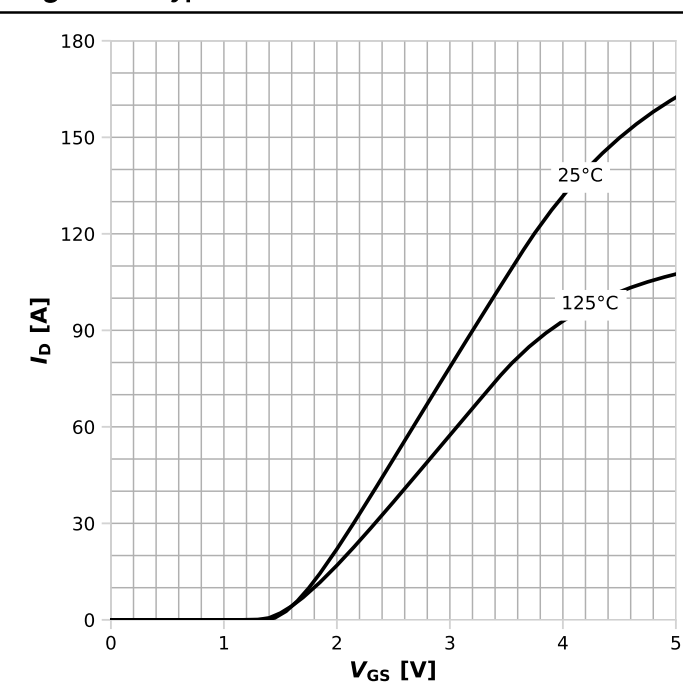
$I_{GS} = f(V_{GS}); \text{open drain}; \text{parameter: } T_j$

Diagram 12: Typ. gate characteristics reverse



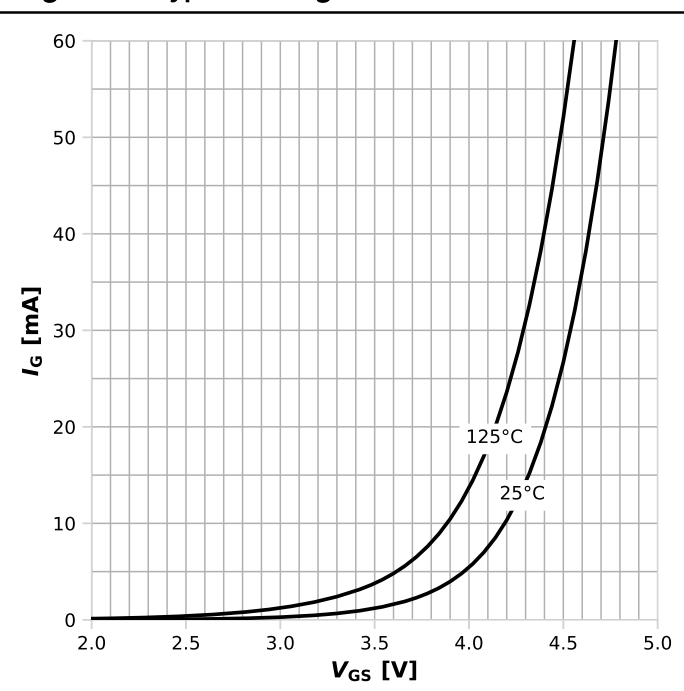
$I_{SG} = f(V_{SG}); \text{parameter: } T_j$

Diagram 13: Typ. transfer characteristics



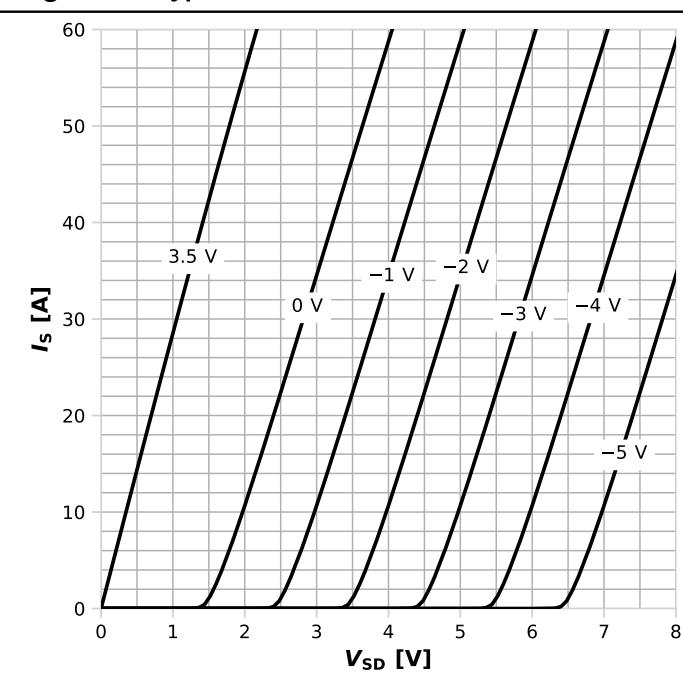
$I_D = f(V_{GS})$; $V_{DS} = 8V$; parameter: T_j

Diagram 14: Typ. transfer gate current characteristic



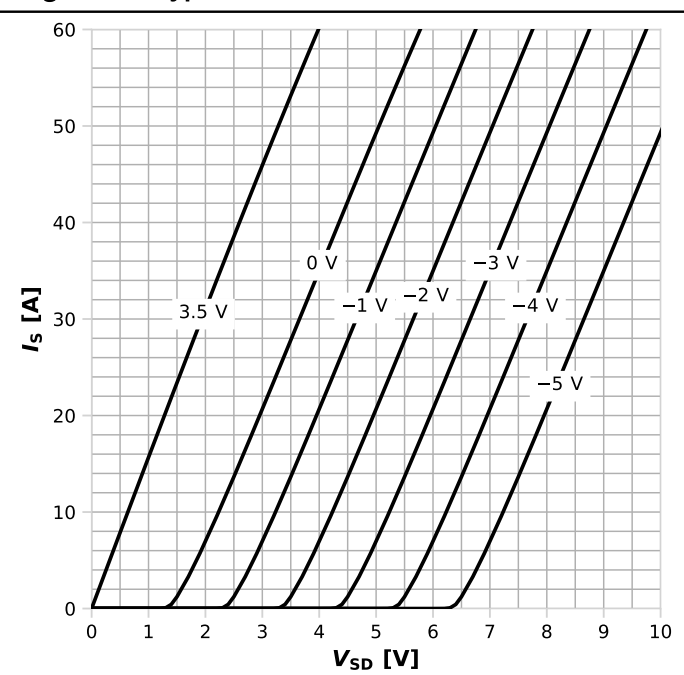
$I_G = f(V_{GS})$; $V_{DS} = 8V$; parameter: T_j

Diagram 15: Typ. channel reverse characteristics



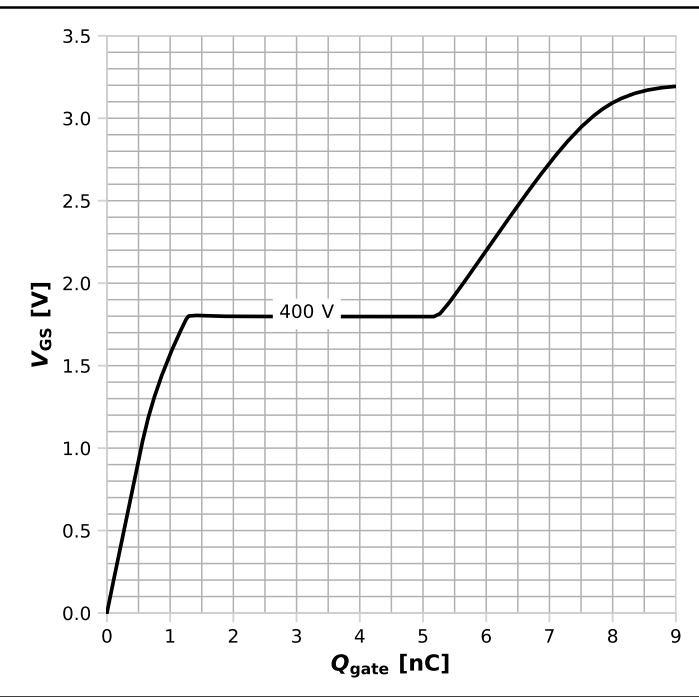
$I_S = f(V_{SD})$; $T_j = 25^\circ C$; parameter: V_{GS}

Diagram 16: Typ. channel reverse characteristics



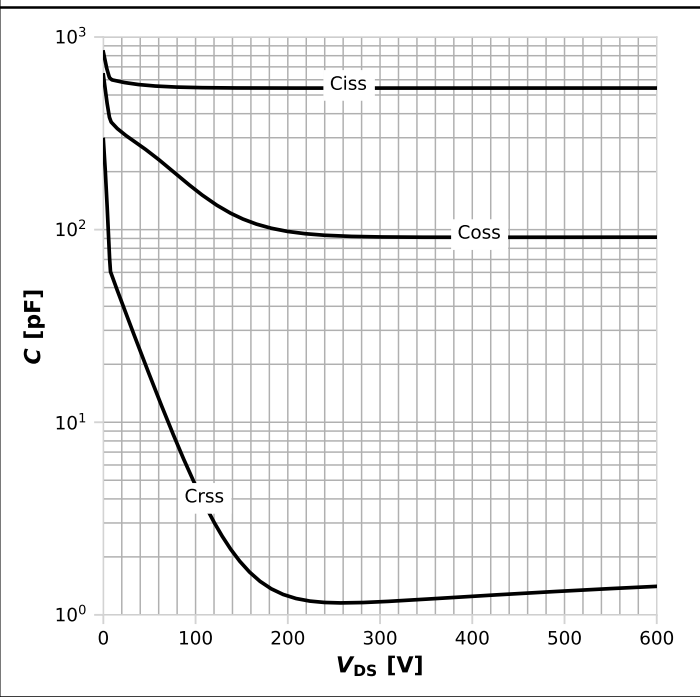
$I_S = f(V_{SD})$; $T_j = 125^\circ C$; parameter: V_{GS}

Diagram 17 Typ. gate charge



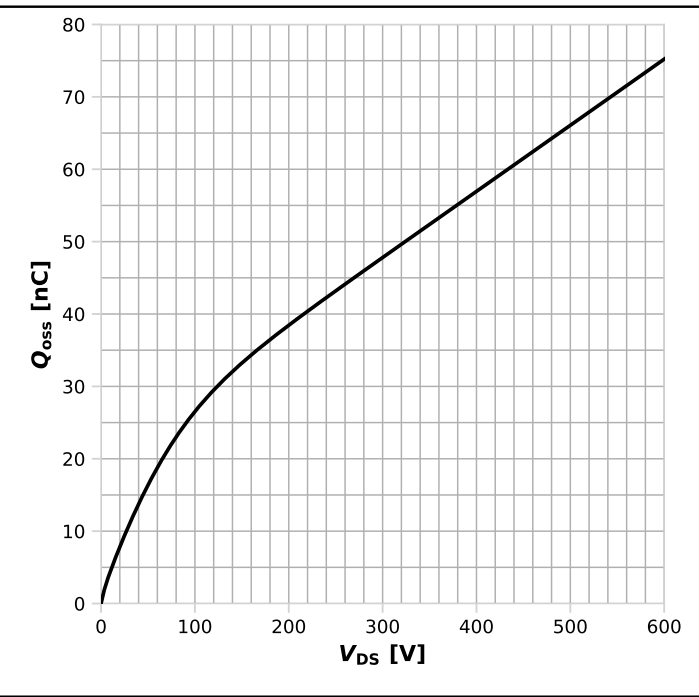
$V_{GS}=f(Q_{gate})$; $I_D=13$ A pulsed; $I_G=4.5$ mA; parameter: V_{DD}

Diagram 18: Typ. capacitances



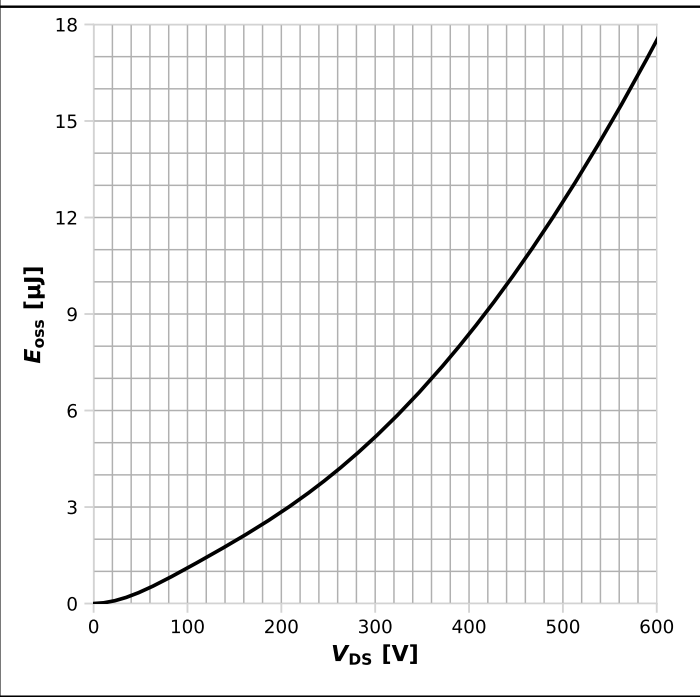
$C=f(V_{DS})$; $V_{GS}=0$ V

Diagram 19: Typ. output charge



$Q_{oss}=f(V_{DS})$

Diagram 20: Typ. Coss stored energy



$E_{oss}=f(V_{DS})$

5 Test circuits

Table 8 Reverse channel characteristics test

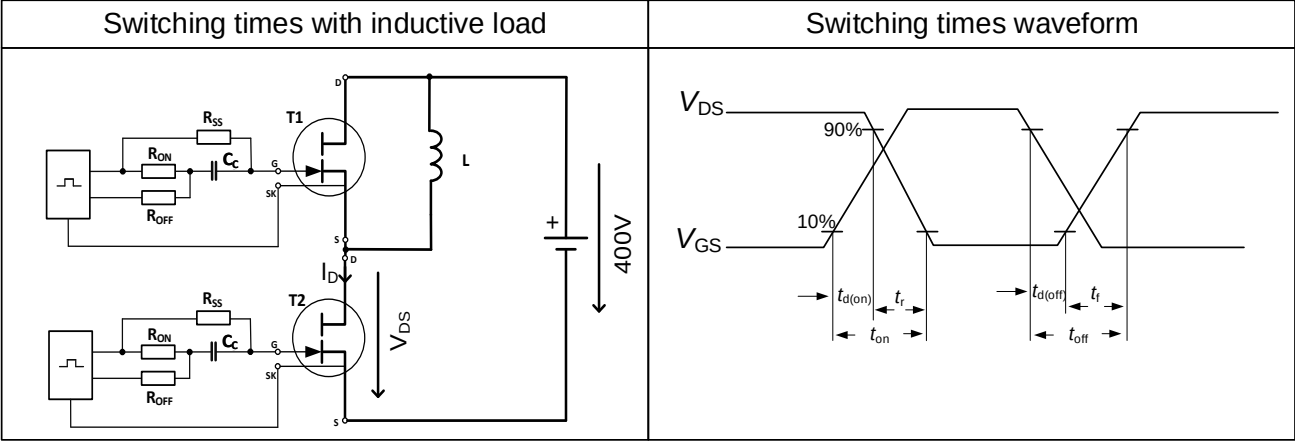
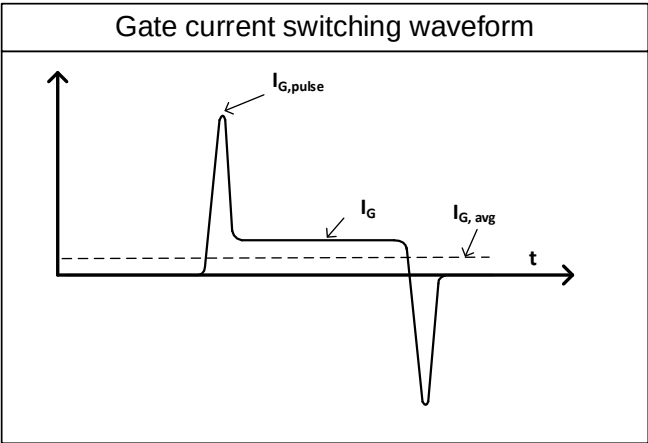
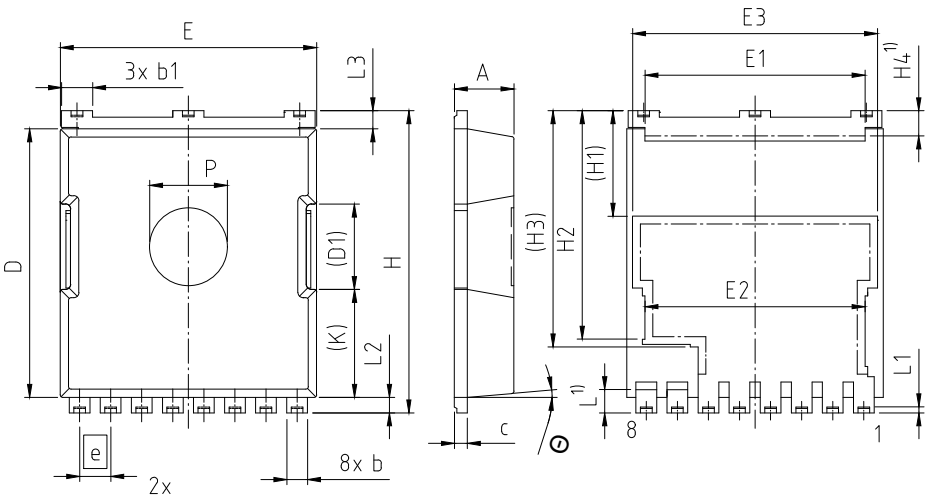


Table 9 Gate current switching waveform



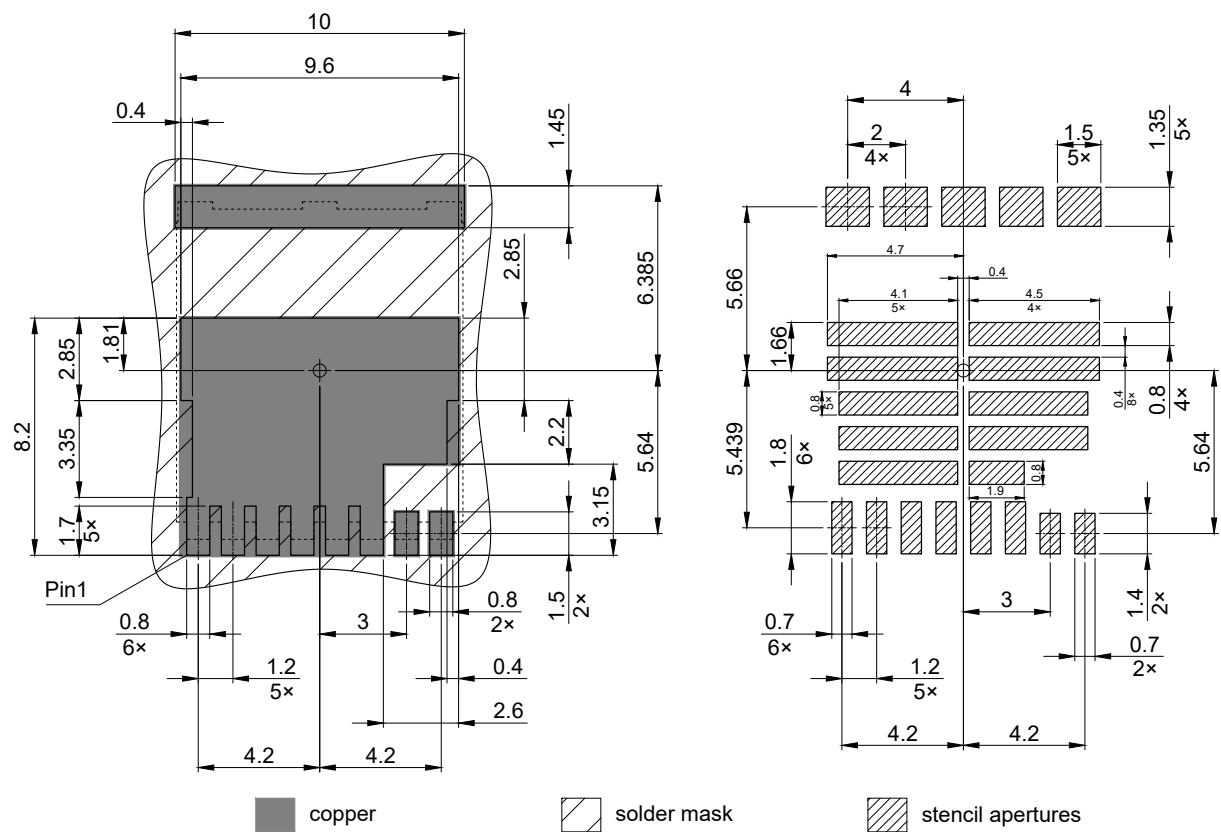
6 Package outlines



PACKAGE - GROUP NUMBER: PG-HSOF-8-U04		
DIMENSIONS	MILLIMETERS	
	MIN.	MAX.
A	2.20	2.40
b	0.70	0.90
b1	1.10	1.30
c	0.40	0.60
D	10.275	10.575
D1	(3.20)	(3.40)
E	9.70	10.10
E1	8.40	8.60
E2	8.40	8.60
E3	9.36	9.56
e	1.20	
H	11.475	11.875
H1	(3.98)	(4.18)
H2	8.73	8.93
H3	(9.03)	(9.23)
H4	0.88	1.08
N	8	
K	(4.07)	(4.27)
L	0.80	1.00
L1	0.13	0.33
L2	0.50	0.70
L3	0.60	0.80
P	2.90	3.10
Θ	3.5°	6.5°

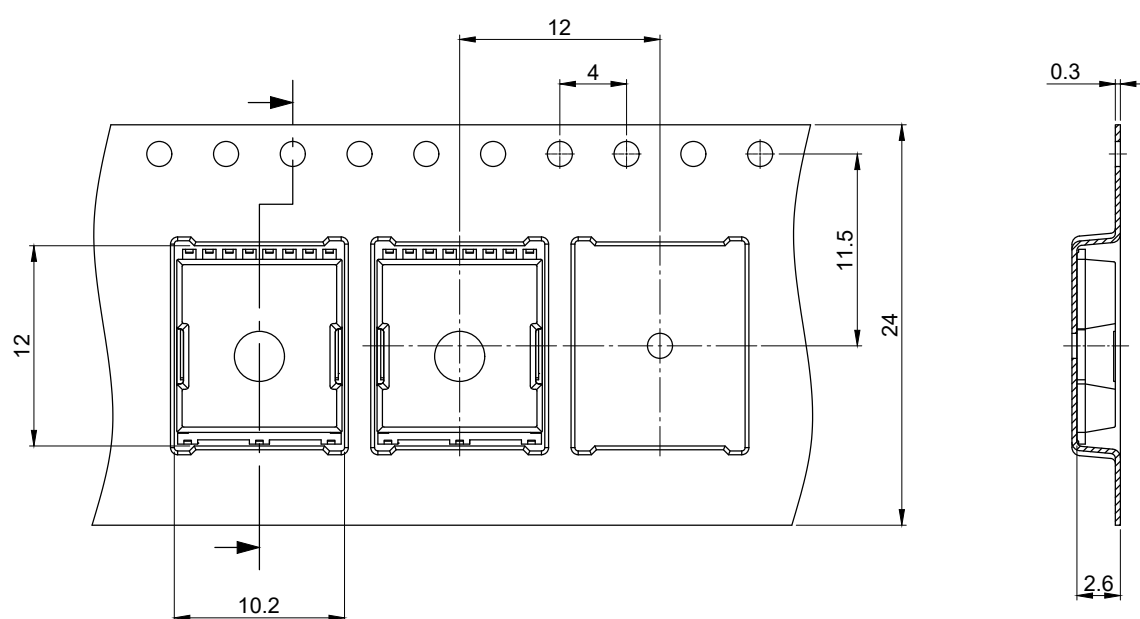
NOTES:
1) LEAD LENGTH UP TO ANTI FLASH PROFILE, MOLD FLASHES EXCLUDED

Figure 1 Outline PG-HSOF-8, dimensions in mm



Based on stencil thickness 0.130 mm
All dimensions are in units mm

Figure 2 Footprint drawing PG-HSOF-8, dimensions in mm



All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [—]

Figure 3 Packaging variant PG-HSOF-8, dimensions in mm

7 Appendix A

Table 10 **Related links**

- **CoolGaN™ Transistor 650 V G5: IGT65R035D2**
- **CoolGaN™ Transistor 650 V G5 family**
- **Package information**
- **Where & why GaN: applications and value propositions**
- **How to GaN: design tips and tricks**



Revision history

IGT65R035D2

Revision 2026-03-05, Rev. 1.1

Previous revisions

Revision	Date	Subjects (major changes since last revision)
1.0	2024-11-28	Release of final
1.1	2026-03-05	Update of format and footnotes. Typical gate current added.

Trademarks

All referenced product or service names and trademarks are the property of their respective owners.

Published by Infineon Technologies AG, Am Campeon 1-15, 85579 Neubiberg, Germany
Copyright (c) 2026 Infineon Technologies AG and its affiliates. All Rights Reserved.

Important notice

Products which may also include samples and may be comprised of hardware or software or both ("Product(s)") are sold or provided and delivered by Infineon Technologies AG and its affiliates ("Infineon") subject to the terms and conditions of the frame supply contract or other written agreement(s) executed by a customer and Infineon or, in the absence of the foregoing, the applicable Sales Conditions of Infineon. General terms and conditions of a customer or deviations from applicable Sales Conditions of Infineon shall only be binding for Infineon if and to the extent Infineon has given its express written consent.

For the avoidance of doubt, Infineon disclaims all warranties of non-infringement of third-party rights and implied warranties such as warranties of fitness for a specific use/purpose or merchantability.

Infineon shall not be responsible for any information with respect to samples, the application or customer's specific use of any Product or for any examples or typical values given in this document.

The data contained in this document is exclusively intended for technically qualified and skilled customer representatives. It is the responsibility of the customer to evaluate the suitability of the Product for the intended application and the customer's specific use and to verify all relevant technical data contained in this document in the intended application and the customer's specific use. The customer is responsible for properly designing, programming, and testing the functionality and safety of the intended application, as well as complying with any legal requirements related to its use.

Unless otherwise explicitly approved by Infineon, Products may not be used in any application where a failure of the Products or any consequences of the use thereof can reasonably be expected to result in personal injury. However, the foregoing shall not prevent the customer from using any Product in such fields of use that Infineon has explicitly designed and sold it for, provided that the overall responsibility for the application lies with the customer.

Infineon expressly reserves the right to use its content for commercial text and data mining (TDM) according to applicable laws, e.g. Section 44b of the German Copyright Act (UrhG).

If the Product includes security features: Because no computing device can be absolutely secure, and despite security measures implemented in the Product, Infineon does not guarantee that the Product will be free from intrusion, data theft or loss, or other breaches ("Security Breaches"), and Infineon shall have no liability arising out of any Security Breaches.

If this document includes or references software:

The software is owned by Infineon under the intellectual property laws and treaties of the United States, Germany, and other countries worldwide. All rights reserved. Therefore, you may use the software only as provided in the software license agreement accompanying the software. If no software license agreement applies, Infineon hereby grants you a personal, non-exclusive, non-transferable license (without the right to sublicense) under its intellectual property rights in the software (a) for software provided in source code form, to modify and reproduce the software solely for use with Infineon hardware products, only internally within your organization, and (b) to distribute the software in binary code form externally to end users, solely for use on Infineon hardware products. Any other use, reproduction, modification, translation, or compilation of the software is prohibited.

For further information on the Product, technology, delivery terms and conditions, and prices, please contact your nearest Infineon office or visit <https://www.infineon.com>.