THCV333-Q

Audio Visual Serializer with bi-directional transceiver

1. General Description

THCV333-Q video serializer is designed to support 1080p60 24bit uncompressed video data by V-by-One® HS II Forward Channel (FC) on 100ohm differential STP or 50ohm Coaxial cable between Open-LDI (LVDS) (oLDI) output graphic processor and panel display.

THCV333-Q supports audio.

THCV333-Q supports bi-directional command communication including 2-wire interface and GPIO, which can control and monitor touch panel at remote side.

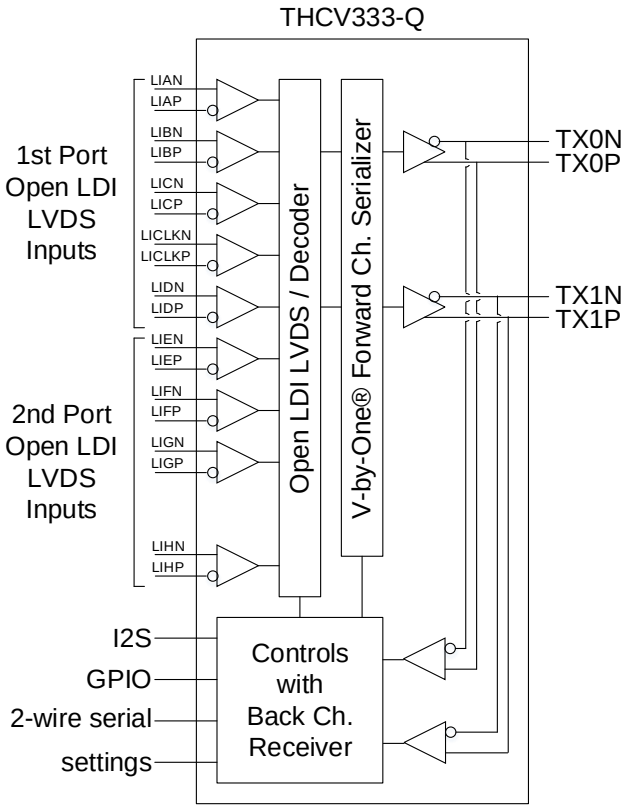
2. Applications

Automotive Infotainment Display
Instrument Cluster Display
Touch Screen Monitor and Panel Display
Security and Surveillance Camera

3. Features

- AEC-Q100 Grade2 (-40 to 105˚C)
- Forward Channel V-by-One® HS II 3.75Gbps 2lane
- Open-LDI(LVDS) Single to FC 10 to 109MHz
- Open-LDI(LVDS) Single to 2xFC 50 to 150MHz
- Open-LDI(LVDS) Dual to FC 50 to 109MHz
- Open-LDI(LVDS) Dual to 2xFC 50 to 218MHz
- Color depth per pixel:18bit or 24bit
- Back Channel GPIO support up to 120kbps
- 2-wire 1Mbps serial interface bridge function
- Remote side GPIO control and monitoring
- 15 meters of cable transmission
- Wide range IO voltage from 1.71V to 3.465V
- Additional spread spectrum on data stream
- Error Detect and Notification
- 0.5mm pitch QFN64 9x9mm package
- Compliant with RoHS and REACH

4. Block Diagram



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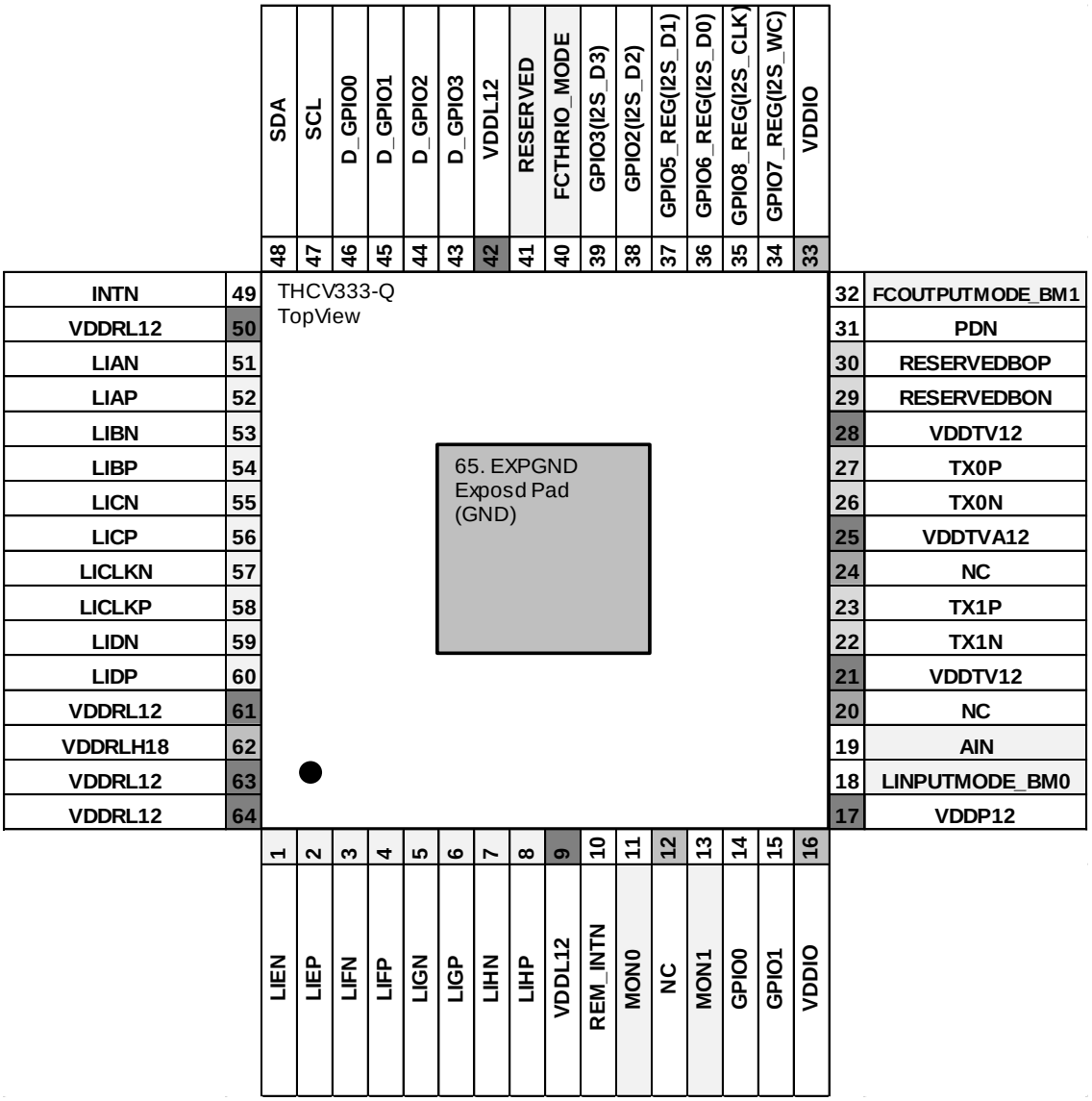
5. Pin Configuration and Functions



Pin Functions

Settings				
Pin Name	Pin#	I/O	PU/PD	Description
RESERVED	41	IL2	-	**Must be tied to GND** 0: GND MUST 1: Not Allowed.
FCTHRIO_MODE	40	IL	PD	**SELECT Forward Chanel Through IO MODE** 0 : 8cycle mode (default / audio-video balanced) 1 : 4cycle mode (enhanced audio bandwidth)
LINPUTMODE_BM0	18	IL	PD	**oLDI LVDS Input Mode Select (Base Mode 0)** 0: 1Port Single-Link Open-LDI LVDS input 1: 2Port Dual-Link Open-LDI LVDS input
FCOUTPUTMODE_BM1	32	IL	PD	**Forward Ch. Output Mode Select (Base Mode 1)** 0: 1Lane V-by-One® HS II output 1: 2Lane V-by-One® HS II output
PDN	31	IL2	-	**Chip Power Down Negative** 0: Power-Down State 1: Normal Operation
2-Wire Serial Interface				
Pin Name	Pin#	I/O	PU/PD	Description
AIN	19	IL	PD	**Device Address Setting for 2-Wire Serial Interface** 0 : Device Address = 7'h0B (=7'b000_1011) 1 : Device Address = 7'h34 (=7'b011_0100)
SCL	47	B2	-	**2-wire serial I/F Clock Line**
SDA	48	B2	-	**2-wire serial I/F Data Line**
I2S Interface				
Pin Name	Pin#	I/O	PU/PD	Description
I2S_WC	34	I	-	I2S WC(Word Clock) input *Shared with GPIO7_REG
I2S_CLK	35	I	-	I2S Bit Clock input *Shared with GPIO8_REG
I2S_D0	36	I	-	I2S Data input 0 *Shared with GPIO6_REG
I2S_D1	37	I	-	I2S Data input 1 *Shared with GPIO5_REG
I2S_D2	38	I	-	I2S Data input 2 *Shared with GPIO2
I2S_D3	39	I	-	I2S Data input 3 *Shared with GPIO3

I:VDDIO CMOS Input, IL/IL2:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B/B2:VDDIO CMOS Input and Output,

PU/PD:Pull-Up/Down

LI:Open-LDI (LVDS) Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply

Pin Functions (continued)

General Purpose I/O				
Pin Name	Pin#	I/O	PU/PD	Description
GPIO0, GPIO1, GPIO2, GPIO3, GPIO5_REG, GPIO6_REG, GPIO7_REG, GPIO8_REG, D_GPIO0, D_GPIO1, D_GPIO2, D_GPIO3	14, 15, 38, 39, 37, 36, 34, 35, 46, 45, 44, 43	B	-	**General Purpose Input Output**
Interrupt/Error/External Sync				
Pin Name	Pin#	I/O	PU/PD	Description
INTN	49	O	-	**Interrupt Signal Output** 0: Interrupt State 1: No Interrupt State
REM_INTN	10	O	-	**Remote Interrupt Signal Output** 0: Interrupt State 1: No Interrupt State
Signal Monitor				
Pin Name	Pin#	I/O	PU/PD	Description
MON0,MON1	11,13	O	PD	**Internal Status Monitor**

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

LI:Open-LDI (LVDS) Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply

Pin Functions (continued)

V-by-One® HS II Tx / Back Channel Rx				
Pin Name	Pin#	I/O	P-Domain	Description
TX0P, TX0N	27, 26	VO	VDDTV	**V-by-One® HS II Tx Output** (0lane) **Back Channel Rx Input** (0lane)
TX1P, TX1N	23, 22	VO	VDDTV	**V-by-One® HS II Output** (1lane) **Back Channel Rx Input** (1lane)
LVDS Rx				
Pin Name	Pin#	I/O	P-Domain	Description
LIAP, LIAN	52, 51	LI	VDDRL	**LVDS Input** (Data0 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LIBP, LIBN	54, 53	LI	VDDRL	**LVDS Input** (Data1 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LICP, LICN	56, 55	LI	VDDRL	**LVDS Input** (Data2 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LICLKP, LICLKN	58, 57	LI	VDDRL	**LVDS Input** (Clock channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LIDP, LIDN	60, 59	LI	VDDRL	**LVDS Input** (Data3 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LIEP, LIEN	2, 1	LI	VDDRL	**LVDS Input** (Data4 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LIFP, LIFN	4, 3	LI	VDDRL	**LVDS Input** (Data5 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LIGP, LIGN	6, 5	LI	VDDRL	**LVDS Input** (Data6 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels
LIHP, LIHN	8, 7	LI	VDDRL	**LVDS Input** (Data7 channel) Each pair requires internal 100-Ω±25% differential termination for standard LVDS levels

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

LI:Open-LDI (LVDS) Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply

Pin Functions (continued)

BC receive monitor				
Pin Name	Pin#	I/O	P-Domain	Description
RESERVEDBON	29	O	VDDTV	**Open or tie to GND**
RESERVEDBOP	30	O	VDDTV	**Open or connect with 50ohm to GND**
Power Line				
Pin Name	Pin#	I/O	P-Domain	Description
VDDIO	16,33	PS	VDDIO	**Power Supply for LVCMOS I/O (1.8V/3.3V)**
VDDL12	9,42	PS	VDDL	**Power Supply for Digital (1.2V)**
VDDP12	17	PS	VDDP	**Power Supply for PLL (1.2V)**
VDDTV12	21,28	PS	VDDTV	**Power Supply for V-by-One Tx and Back Channel Analog (1.2V)**
VDDTVA12	25	PS	VDDTVA	**Power Supply for V-by-One PLL (1.2V)**
VDDRL12	50,61,63, 64	PS	VDDRL	**Power Supply for LVDS Rx PLL and Selialiser Logic (1.2V)**
VDDRLH18	62	PS	VDDRLH	**Power Supply for LVDS Rx (1.8V)**
EXPGND	65	PS	VSSEXP	**Exposed Pad Ground**
Others				
Pin Name	Pin#	I/O	P-Domain	Description
NC	12,20,24	-	-	**Not Connected**

I:VDDIO CMOS Input, IL:VDDIO CMOS Input (Low speed), O:VDDIO CMOS Output, B:VDDIO CMOS Input and Output, PU/PD:Pull-Up/Down

LI:Open-LDI (LVDS) Input, VO:V-by-One® Forward Ch. Output and Back Ch. Input, BM:Back Ch. monitor Output, PS:Power Supply

6. Specifications

6.1. Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings*

Parameter	min.	typ.	max.	Unit
Supply Voltage (VDDIO,VDDRLH)	-0.3	-	+4.0	V
Supply Voltage (VDDL,VDDP,VDDTV,VDDTVA,VDDRL)	-	-	1.6	V
LVCMOS Input Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Output Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Bi-directional buffer Input Voltage	-0.3	-	VDDIO+0.3	V
LVCMOS Bi-directional buffer Output Voltage	-0.3	-	VDDIO+0.3	V
LVDS Receiver Voltage	-0.3	-	VDDRLH+0.3	V
CML Transmitter Voltage Back Channel Receiver Voltage	-0.3	-	VDDTV+0.3	V
Storage Temperature	-55	-	+125	˚C
Junction Temperature	-	-	+125	˚C
Reflow Peak Temperature/time	-	-	+260/10	˚C/sec

* “Absolute Maximum Ratings” are values of safety limit for a device beyond which a device safety cannot be guaranteed.

They do not imply that a device should be operated at these limits. The tables of “Recommended Operating Condition” specify conditions for device operation.

6.2. Electrostatic discharge Ratings

Table 2. Electrostatic discharge (ESD) Ratings

Symbol	Parameter	Condition		Value	Unit
VESD	Electrostatic Discharge	Human Body Model (HBM) on AEC-Q100-002		+/-2000	V
		Charged Device Model (CDM) on AEC-Q100-011		+/-750	
		IEC61000-4-2	Air Discharge	+/-15000	
			Contact Discharge	+/-8000	
		ISO10605	Air Discharge	+/-15000	
			Contact Discharge	+/-8000	

6.3. Recommended Operating Conditions

Table 3. Recommended Operating Conditions

Parameter	min.	typ.	max.	Unit
Supply Voltage (VDDIO)	3.135	3.300	3.465	V
	1.89	2.5 / 2.8	3.135	V
	1.71	1.8	1.89	V
Supply Voltage (VDDRLH)	1.71	1.8	1.89	V
Supply Voltage (VDDL,VDDP,VDDTV,VDDTVA,VDDRL)	1.14	1.2	1.26	V
Operating Temperature (Ta)	-40	-	105	˚C

6.4. Thermal Information

Table 4. Thermal Information

Symbol	Parameter	Value	Unit
θja	Junction-to-ambient thermal resistance	28.34	˚C/W
θjc(top)	Junction-to-case (top) thermal resistance	12.07	˚C/W
θjb	Junction-to-board thermal resistance	4.02	˚C/W
Ψjt	Junction-to-top characterization parameter	2.78	˚C/W
Ψjb	Junction-to-board characterization parameter	2.89	˚C/W
θjc(bot)	Junction-to-case (bottom) thermal resistance	1.54	˚C/W

6.5. DC Specifications

6.5.1. LVCMOS DC Specifications

Table 5. LVCMOS DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
IIH	Input Leak Current High	-	-10	-	+10	uA
IIL	Input Leak Current Low	-	-10	-	+10	uA
VIH1	High Level Input Voltage (I, IL and B)	VDDIO=3~3.465V	2.00	-	VDDIO	V
		VDDIO=2~3V	0.70*VDDIO	-	VDDIO	V
		VDDIO=1.71~2V	0.65*VDDIO	-	VDDIO	V
VIL1	Low Level Input Voltage (I, IL and B)	VDDIO=3~3.465V	0	-	0.80	V
		VDDIO=2~3V	0	-	0.30*VDDIO	V
		VDDIO=1.71~2V	0	-	0.35*VDDIO	V
VIH2	High Level Input Voltage (IL2 and B2)	-	0.70*VDDIO	-	VDDIO	V
VIL2	Low Level Input Voltage (IL2 and B2)	-	0	-	0.30*VDDIO	V
VOH	High Level Output Voltage	IOH=1mA	VDDIO-0.45		VDDIO	V
VOL	Low Level Output Voltage	IOL=1mA	0	-	0.45	V

6.5.2. CML Forward Channel Transmitter DC Specifications

Table 6. CML Forward Channel (FC) Transmitter DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
VTOD	CML Differential Mode Output Voltage	DRV[1:0]=00	133	200	267	mV
		DRV[1:0]=01	200	300	400	mV
		DRV[1:0]=10	300	400	500	mV
		DRV[1:0]=11	350	450	550	mV
VTOC	CML Common Mode Output Voltage	-	-	VDDTV-VTOD	-	mV
ITOZH	CML Output Leak Current High	PDN=L	-	-	10	uA
ITOZL	CML Output Leak Current Low	PDN=L	-	-	10	uA
ITOS	CML Output Short Current	VDDTV=1.2V	-60	-	-33	mA

6.5.3. Open-LDI LVDS Receiver DC Specifications

Table 7. Open-LDI (oLDI) LVDS Receiver DC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
VTTH	LVDS Differential Input High Threshold	-	-	-	100	mV
VTTL	LVDS Differential Input Low Threshold	-	-100	-	-	mV
ITIH	LVDS Input Leak Current High	TLxn+/-=VDH,PDN=L	-	-	±10	uA
ITIL	LVDS Input Leak Current Low	TLxn+/-=0,PDN=L	-	-	±10	uA
RTIN	LVDS Differential Input Resistance	-	80	100	120	ohm
VIN_RX	LVDS Input Voltage Range	VDDRLH=1.71V~1.8V	0.3	-	VDDRLH	V
		VDDRLH=1.8V~1.89V	0.3	-	1.8	
VIC_RX	LVDS Input Voltage Common	-	0.6	-	1.5	V
|VID_RX|	LVDS Input Voltage Differential Amplitude	-	100	-	600	mV

6.6. AC Specifications

6.6.1. General AC Specifications

Table 8. General AC Specifications (1/3)

Symbol	Parameter	Condition	min.	typ.	max.	Unit
tDL_V2V_1	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 4cycle mode 1/TRCIP=85MHz	331*TRCIP	341*TRCIP	351*TRCIP +10	ns
tDL_V2V_2	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode 1/TRCIP=85MHz	367*TRCIP	377*TRCIP	387*TRCIP +10	ns
tDL_V2V_3	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Single CML FC output Des: Single CML FC input / Dual-Link oLDI output FC_THRIO: 4cycle mode 1/TRCIP=85MHz	171*TRCIP	181*TRCIP	191*TRCIP +10	ns
tDL_V2V_4	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Single CML FC output Des: Single CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode 1/TRCIP=85MHz	180*TRCIP	190*TRCIP	200*TRCIP +10	ns
tDL_V2V_5	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Single CML FC output Des: Single CML FC input / Single-Link oLDI output FC_THRIO: 4cycle mode 1/TRCIP=85MHz	227*TRCIP	237*TRCIP	247*TRCIP +10	ns
tDL_V2V_6	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Single CML FC output Des: Single CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode 1/TRCIP=85MHz	244*TRCIP	254*TRCIP	264*TRCIP +10	ns
tDL_V2V_7	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: Off 1/TRCIP=85MHz	260*TRCIP	270*TRCIP	280*TRCIP +10	ns

*Serializer above table is THCV333-Q. Deserializer above table is THCV334-Q.

Table 9. General AC Specifications (2/3)

Symbol	Parameter	Condition	min.	typ.	max.	Unit
tDL_V2V_8	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	245*TRCIP	255*TRCIP	265*TRCIP +10	ns
tDL_V2V_9	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Single CML FC output Des: Single CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	149*TRCIP	159*TRCIP	169*TRCIP +10	ns
tDL_V2V_10	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: 4cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	175*TRCIP	185*TRCIP	195*TRCIP +10	ns
tDL_V2V_11	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x2mode 1/TRCIP=85MHz	180*TRCIP	190*TRCIP	200*TRCIP +10	ns
tDL_V2V_12	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 4cycle mode Low Freq mode: x4mode 1/TRCIP=85MHz	172*TRCIP	182*TRCIP	192*TRCIP +10	ns
tDL_V2V_13	Data Latency Video from Serializer input to Deserializer output	Ser: Single-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Single-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x4mode 1/TRCIP=85MHz	180*TRCIP	190*TRCIP	200*TRCIP +10	ns
tDL_V2V_14	Data Latency Video from Serializer input to Deserializer output	Ser: Dual-Link oLDI input/ Dual CML FC output Des: Dual CML FC input / Dual-Link oLDI output FC_THRIO: 8cycle mode Low Freq mode: x4mode 1/TRCIP=85MHz	150*TRCIP	160*TRCIP	170*TRCIP +10	ns

*Serializer above table is THCV333-Q. Deserializer above table is THCV334-Q.

Table 10. General AC Specifications (3/3)

Symbol	Parameter	Condition	min.	typ.	max.	Unit
tDL_A2A	Data Latency Audio from Serializer input to Deserializer output	Ser. I2S_WC input to Des. I2S_WC output 1/TRCIP=91.5MHz	106*TTFC BIT*30	116*TTFC BIT*30	126*TTFC BIT*30+10	ns
tDL_GPI2FC 2GPO	Data Latency Through GPIO from Serializer GPI to Deserializer GPO	FC THRIO_MODE=8cycle, FC Through GPIO=8bit 1/TRCIP=91.5MHz	75*TTFCBI T*30	85*TTFCBI T*30	95*TTFCBI T*30+10	ns
tDL_GPI2BC 2GPO	Data Latency Through GPIO from Deserializer GPI to Serializer GPO	BC Through GPIO=8bit 1/TRCIP=91.5MHz	367*TTFC BIT*30	527*TTFC BIT*30	687*TTFC BIT*30+10	ns
tDL_2WIRE WRITE2FC2 REM2WIRE	Data Latency 2-wire remote write from Serializer input to Deserializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	262*TTFC BIT*30	282*TTFC BIT*30	302*TTFC BIT*30+10	ns
tDL_2WIRE WRITEACK2 BC2LOCAL2 WIRE	Data Latency 2-wire remote ACK from Deserializer input to Serializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	736*TTFC BIT*30	1136*TTFC BIT*30	1536*TTF CBIT*30 +10	ns
tDL_2WIRE READ2FC2 REM2WIRE	Data Latency 2-wire remote read from Serializer input to Deserializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	240*TTFC BIT*30	260*TTFC BIT*30	280*TTFC BIT*30+10	ns
tDL_2WIRE READBACK 2BC2LOCAL 2WIRE	Data Latency 2-wire remote read from Deserializer input to Serializer output	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	1302*TTFC BIT*30	1502*TTF CBIT*30	1702*TTF CBIT*30 +10	ns
tDL_INTIN2I NTN	Data Latency Interrupt from Deserializer INTN_IN to Serializer INTN	FC THRIO_MODE=8cycle, 1/TRCIP=91.5MHz	1470*TTFC BIT*30	2170*TTF CBIT*30	2870*TTF CBIT*30 +10	ns

*Serializer above table is THCV333-Q. Deserializer above table is THCV334-Q.

6.6.2. Open-LDI LVDS Receiver AC Specifications

Table 11. Open-LDI (oLDI) LVDS Receiver AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TRCIP	LICLKP/N Period	LFEN=0 LFEN=1	6.66 25.0	-	34.0 100.0	ns
FOLDIIN	LICLKP/N Frequency Per port	-	10	-	150	MHz
TRCIWH	LICLKP High pulse width	-	-	4/7 TRCIP	-	-
TRCIWL	LICLKP Low pulse width	-	-	3/7 TRCIP	-	-
|TRMG|	Receiver data input margin FCLKIN = 65 MHz FCLKIN = 75 MHz FCLKIN = 85 MHz FCLKIN = 100 MHz FCLKIN = 116 MHz	R_BPDEN =0x1 LVDS Rx BB Enable	 - - - - -	 - - - - -	 550 470 400 330 250	ps
	Receiver data input margin for Single Link F_{CLKIN} = 135 MHz F_{CLKIN} = 150 MHz	R_BPDEN =0x1 LVDS Rx BB Enable	-	-	 200 170	ps
TRIP1	Receiver input data position for Bit1	-	TRCIP - |TRMG|	0	TRCIP + |TRMG|	-
TRIP0	Receiver input data position for Bit0	-	1/7 TRCIP - |TRMG|	1/7 TRCIP	1/7 TRCIP + |TRMG|	-
TRIP6	Receiver input data position for Bit6	-	2/7 TRCIP - |TRMG|	2/7 TRCIP	2/7 TRCIP + |TRMG|	-
TRIP5	Receiver input data position for Bit5	-	3/7 TRCIP - |TRMG|	3/7 TRCIP	3/7 TRCIP + |TRMG|	-
TRIP4	Receiver input data position for Bit4	-	4/7 TRCIP - |TRMG|	4/7 TRCIP	4/7 TRCIP + |TRMG|	-
TRIP3	Receiver input data position for Bit3	-	5/7 TRCIP - |TRMG|	5/7 TRCIP	5/7 TRCIP + |TRMG|	-
TRIP2	Receiver input data position for Bit2	-	6/7 TRCIP - |TRMG|	6/7 TRCIP	6/7 TRCIP + |TRMG|	-
TRPLL	Phase Lock loop set	-	-	-	1	ms
TPWUP	Power On Time	-	0.1	-	-	ms

6.6.3. CML Forward Channel Transmitter AC Specifications

Table 12. CML Forward Channel (FC) Transmitter AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TTFCBIT	TXxP/N out each bit Period Forward Ch. (Unit Interval)	-	266.7 (3.75Gbps)	-	666.7 (1.5Gbps)	ps
FTFC	Forward Channel Data-Rate	-	1.5	-	3.75	Gbps
TTRF	CML Output Rise and Fall Time (20-80%)	-	50	-	150	ps
|TTOSK_INTRA|	Intra-pair Skew	-	-	-	40	ps
|TTOSK_INTER|	Inter-pair Skew between TX0P/N and TX1P/N	-	-	-	2	UI
Δmod	Spread Spectrum Clock Amplitude Tolerance	30KHz modulation	-0.5	-	0.5	%

6.6.4. CML Back Channel Receiver AC Specifications

Table 13. CML Back Channel Receiver AC Specifications

Symbol	Parameter	Condition	min.	typ.	max.	Unit
TTBCBIT	TXxP/N input each bit Period Back Channel (Unit Interval)	-	40 (25Mbps)	TTFCBIT *150	100 (10Mbps)	ns

6.6.5. 2-wire serial Interface AC Specifications

Table 14. 2-wire serial Interface AC Specifications

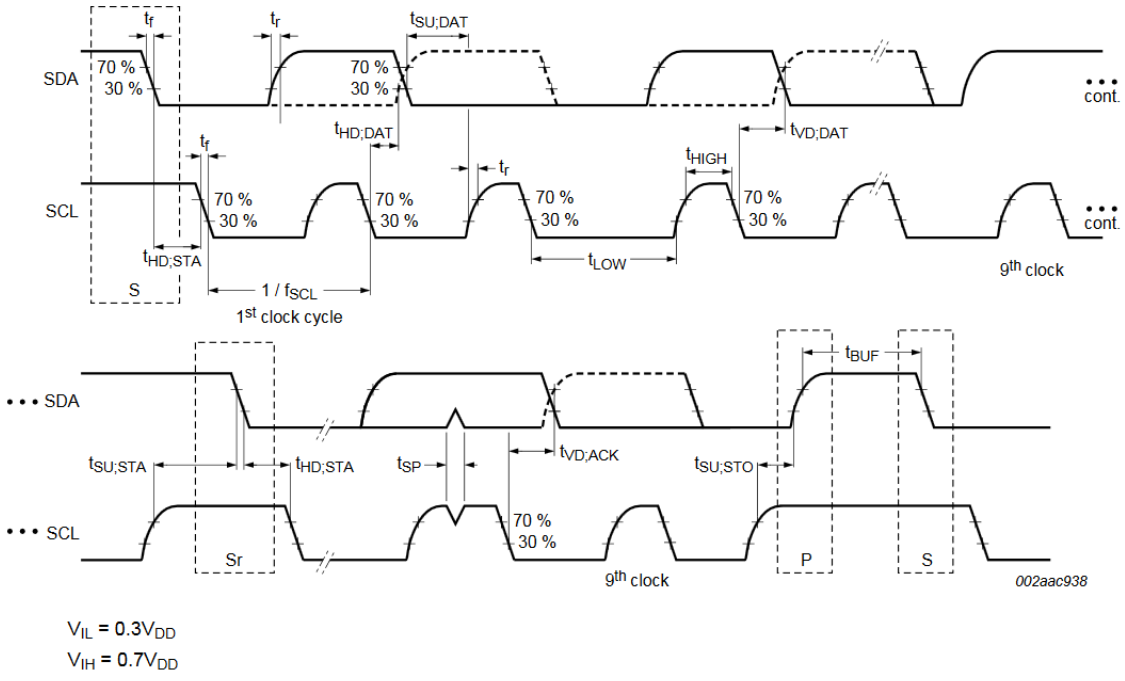
Symbol	Parameter	Condition	min.	typ.	max.	Unit
t_{OSC}	Cycle of internal oscillator clock	-	10.4	12.5	15.7	ns
F_{scl}	SCL clock frequency	-	-	-	1000	kHz
t_{LOW}	LOW period of the SCL clock	-	0.5	-	-	us
t_{HIGH}	HIGH period of the SCL clock	-	0.26	-	-	us
$t_{HD;STA}$	hold time START condition	-	0.26	-	-	us
$t_{SH;STA}$	set-up time for a repeated START condition	-	0.26	-	-	us
$t_{HD;DAT}$	Data hold time (input)	-	0	-	-	ns
$t_{SU;DAT}$	Data setup time (input)	-	50	-	-	ns
t_r	rise time of both SDA and SCL signals	-	-	-	120	ns
t_f	fall time of both SDA and SCL signals	pull-up:2.5kohm bus cap:400pF	-	-	120	ns
$t_{SU;STO}$	set-up time for STOP condition	-	0.26	-	-	us
t_{BUF}	Bus free time between a STOP and START condition	-	0.5	-	-	us
$t_{VD;DAT}$	Data valid time	-	-	-	0.45	us
$t_{VD;ACK}$	Data valid acknowledge time	-	-	-	0.45	us
t_{SP}	Pulse width of spikes which must be suppressed by the input filter	-	-	-	50	ns
t_{PDS}	Required wait time from PDN high to START condition	-	500	-	-	us

6.6.6. Power On and Re-Lock Sequence AC Specifications

Table 15. Power On Sequence AC Specifications

symbol	discription	min	typ	max	unit
t050	VDDIO to 1.8V	0	0	-	us
t1	1.8V to 1.2V	0	0	-	us
t2	Internal Power On Reset	1	-	-	us
t3	PDN Pin ReleaseTime	-	any	-	us
t5	OSC EN to CLKOUT output delay	4.99	-	8.75	us
t6	Register Access Enable from tOSC start after Reset Release	80	100	120	us
t690	1.8V to Open-LDI LVDS clock input	0	0	-	us
t710	Open-LDI LVDS received clock processing	-	-	1.016	ms
t8	FNPLL Lock Time	-	500	1000	1/F(PFD) Cycle
t9	FC PLL Lock Time	-	0.5	1	ms
t10	FCBC CX Link Up Time	-	-	10	ms

6.6.7. AC Specifications Timing Diagrams



$V_{IL} = 0.3V_{DD}$
$V_{IH} = 0.7V_{DD}$

Figure 1. 2-wire serial Interface AC timing

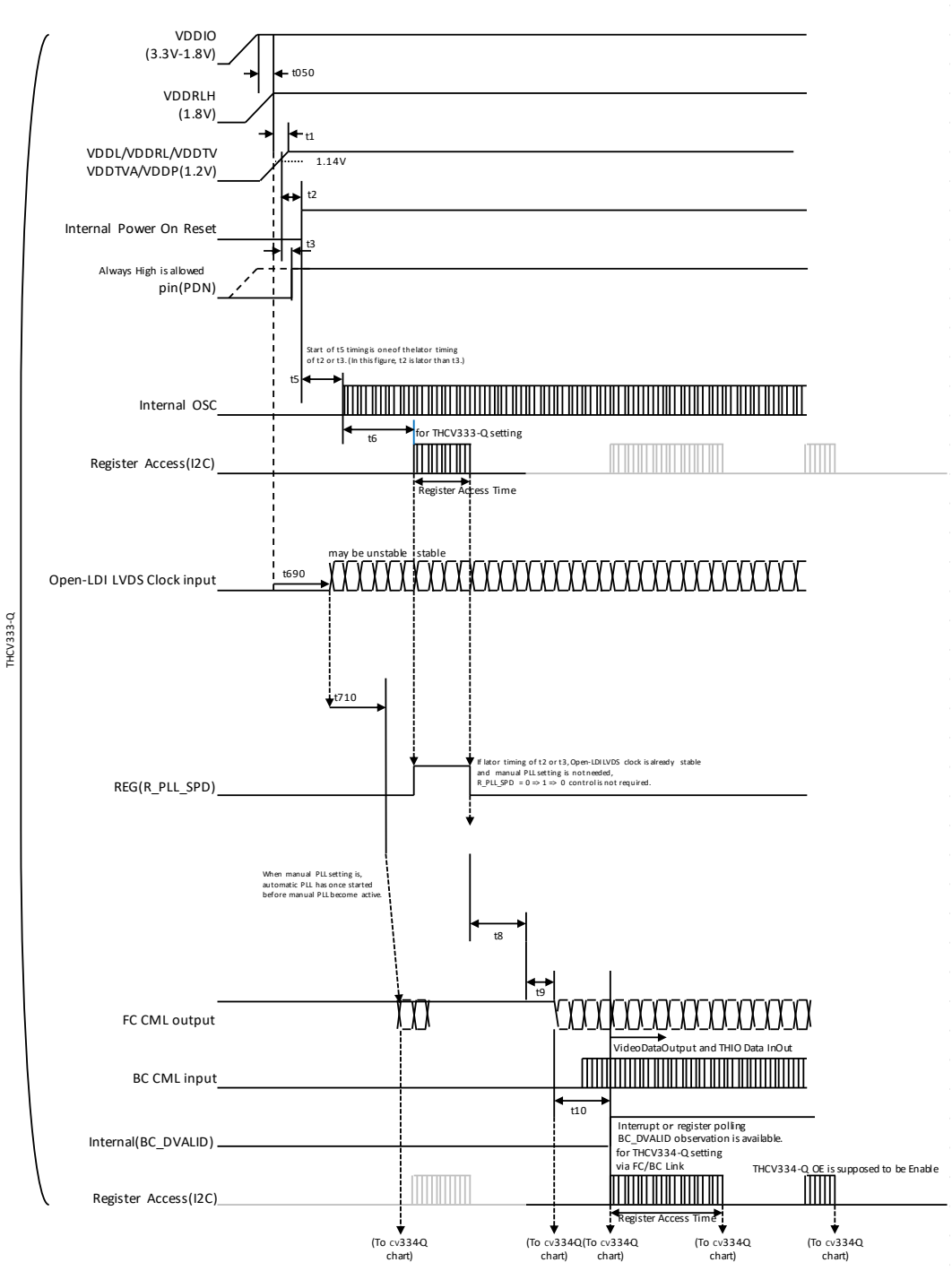


Figure 2. THCV333-Q Power On Sequence Register Entry

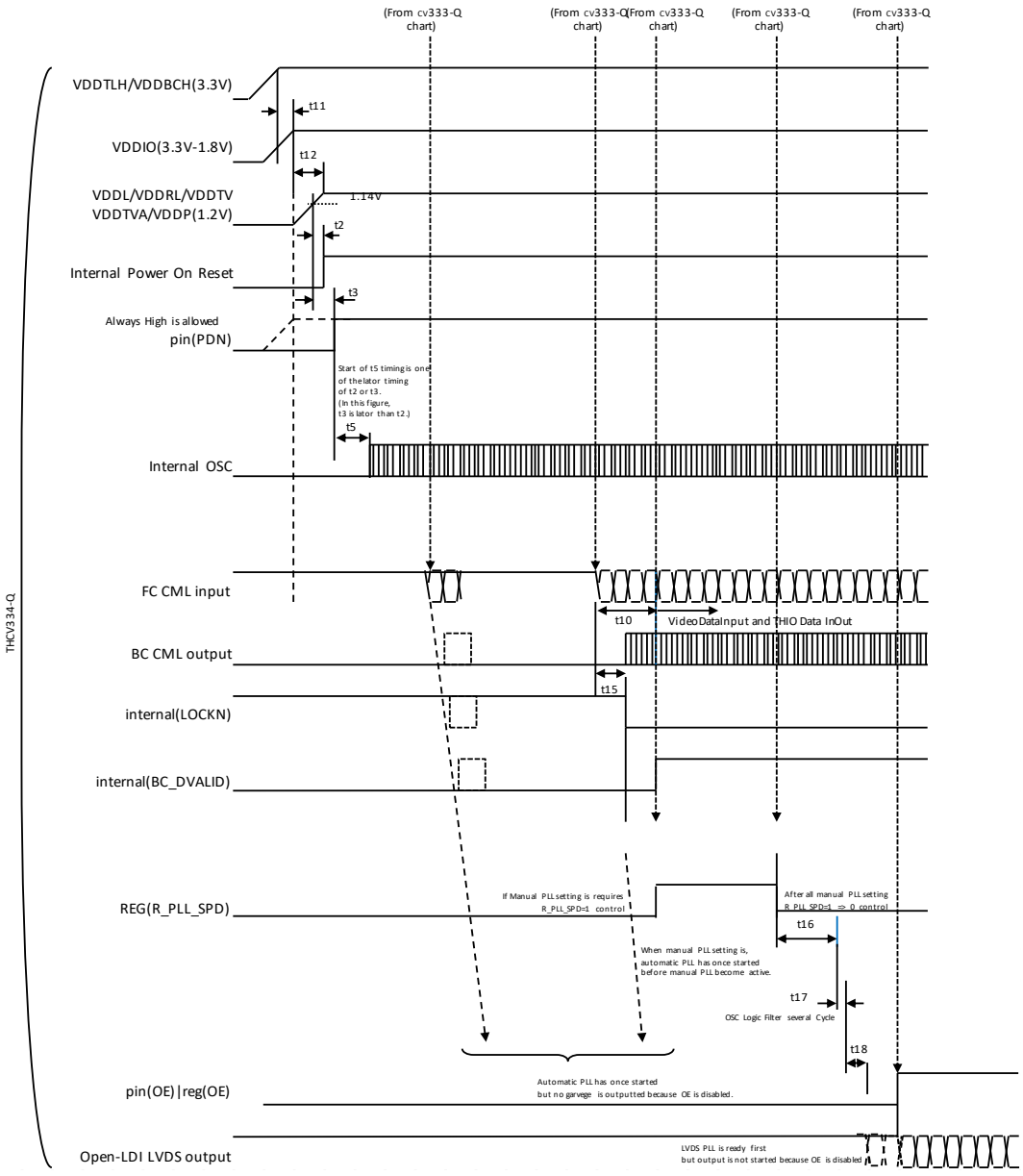


Figure 3. THCV334-Q Power On Sequence Register Entry

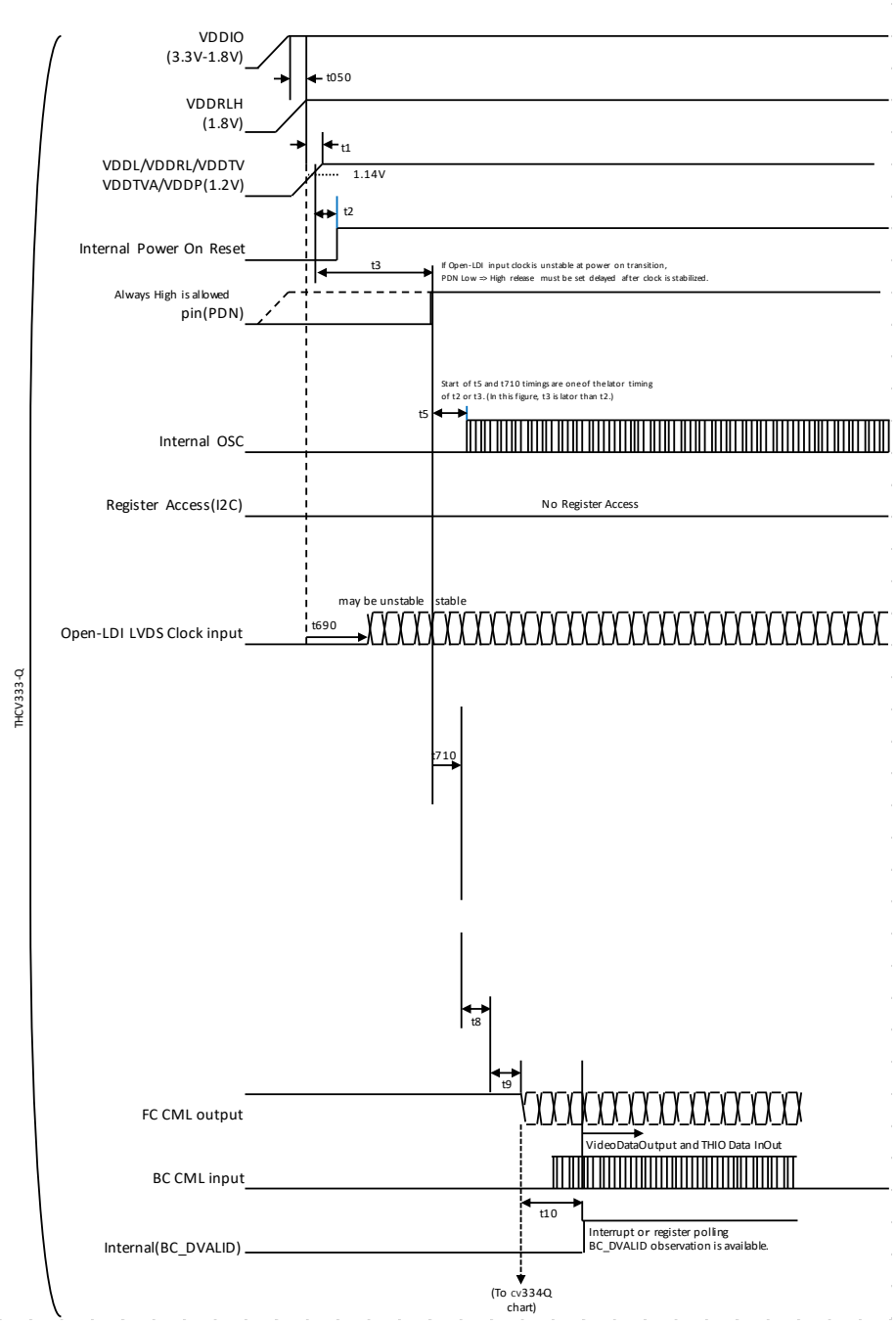


Figure 4. THCV333-Q Power On Sequence Pin Entry

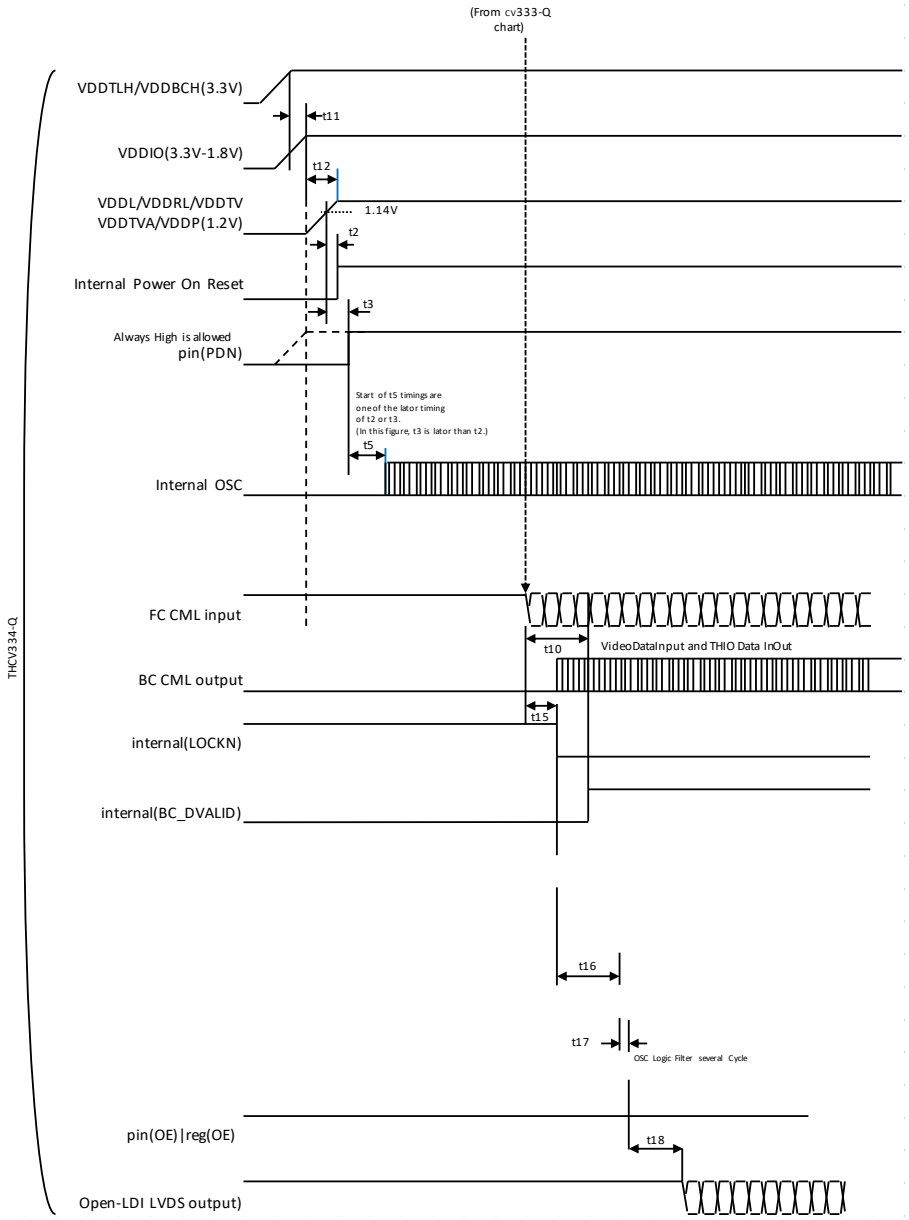


Figure 5. THCV334-Q Power On Sequence Pin Entry

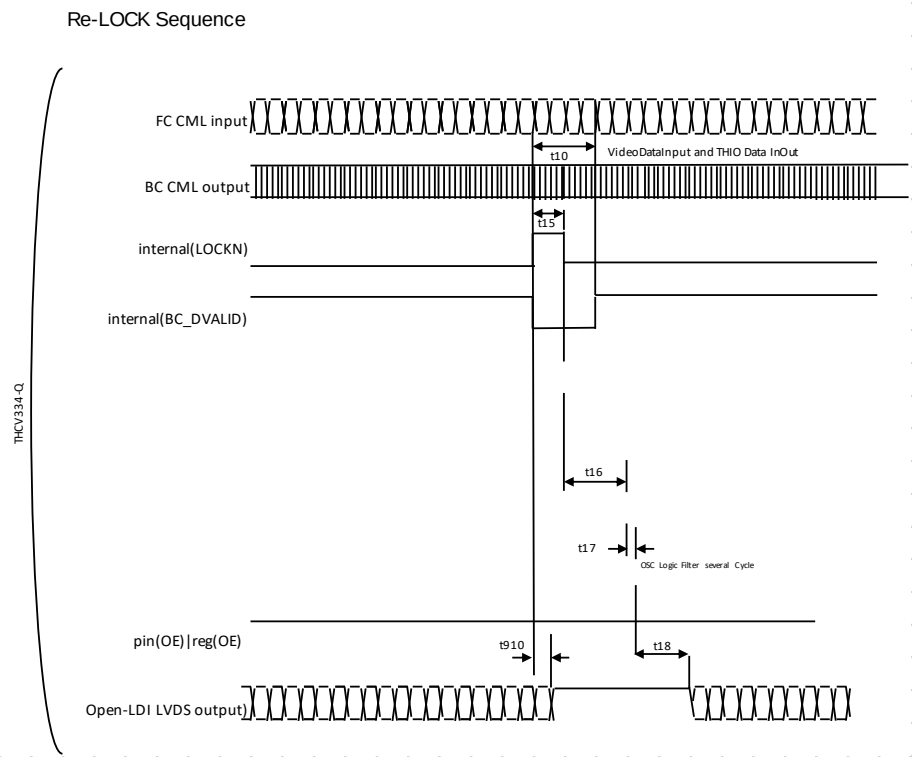


Figure 6. THCV334-Q Re-LOCK Sequence

6.7. Consumption Current

Table 16. Consumption Current at Power Down

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ICCS33	Power Down Supply Current	PDN=0, VDDIO=3.465V	-	0.01	0.1	mA
ICCS18		PDN=0, VDDRLH=1.89V	-	0.01	0.1	mA
ICCS12		PDN=0, VDDL,VDDP,VDDTV,VDDTVA,VDDRL=1.26V	-	6	20	mA

Table 17. Consumption Current of VDDIO, VDDRLH

Symbol	Parameter	Condition	Min	Typ	Max	Unit
ITCCWIO_33_1	VDDIO=3.3V	No Audio, No GPIO	-	0.1	0.4	mA
ITCCWIO_33_2		I2S Audio 48kHz 16bit stereo, No GPIO	-	0.1	0.4	mA
ITCCWIO_33_3		No Audio, GPIO UART 115200bps Tx/Rx and PWM 20kHz 99% to FC	-	0.3	0.7	mA
ITCCWIO_33_4		I2S Audio 48kHz 16bit stereo, GPIO UART 115200bps Tx/Rx and PWM 20kHz 99% to FC	-	0.3	0.7	mA
ITCCWIO_18_1	VDDIO=1.8V	No Audio, No GPIO	-	0.05	0.2	mA
ITCCWRLH_18_2	VDDRLH=1.8V	85MHz x oLDI Single-Link	-	5.6	6.8	mA
ITCCWRLH_18_4		150MHz x oLDI Single-Link	-	5.8	7	mA
ITCCWRLH_18_9		109MHzxoLDI Dual-Link (218MHz)	-	9.4	11.5	mA

Table 18. Consumption Current of VDD12

Symbol	port.in#	port.out#	video format	input	output	min.	typ.	max.	Unit
ITCCW12_1	1	1	640x480p60 RGB888	25MHz x oLDI Single-Link	1.72Gbps x1lane	-	73.5	99.5	mA
ITCCW12_2	1	1	1920x720p60(1) RGB888	85MHz x oLDI Single-Link	3Gbps x1lane	-	96.4	123.3	mA
ITCCW12_3	1	1	1920x720p60(2) RGB888	109MHz x oLDI Single-Link	3.75Gbps x1lane	-	110.2	137.9	mA
ITCCW12_4	1	2	1920x1080p60(1) RGB888	150MHz x oLDI Single-Link	2.6Gbps x2lane	-	130.4	162.1	mA
ITCCW12_5	1	2	1920x720p60(3) RGB888	85MHz x oLDI Single-Link	3Gbps x2lane (Replicate)	-	125.8	156.3	mA
ITCCW12_6	2	1	1920x720p60(4) RGB888	54.5MHz x oLDI Dual-Link	3.75Gbps x1lane	-	98.7	126.5	mA
ITCCW12_7	2	2	1920x1080p60(2) RGB888	75MHz x oLDI Dual-Link(150MHz)	2.6Gbps x2lane	-	115.1	145.0	mA
ITCCW12_8	2	2	2880x720p60 RGB888	85MHz x oLDI Dual-Link(170MHz)	3Gbps x2lane	-	122.2	152.2	mA
ITCCW12_9	2	2	3840x720p60 RGB888	109MHzxoLDI Dual-Link(232MHz)	3.75Gbps x2lane	-	138.3	169.5	mA

Condition: Checkerboard Pattern

7. Detailed Description

7.1. Overview

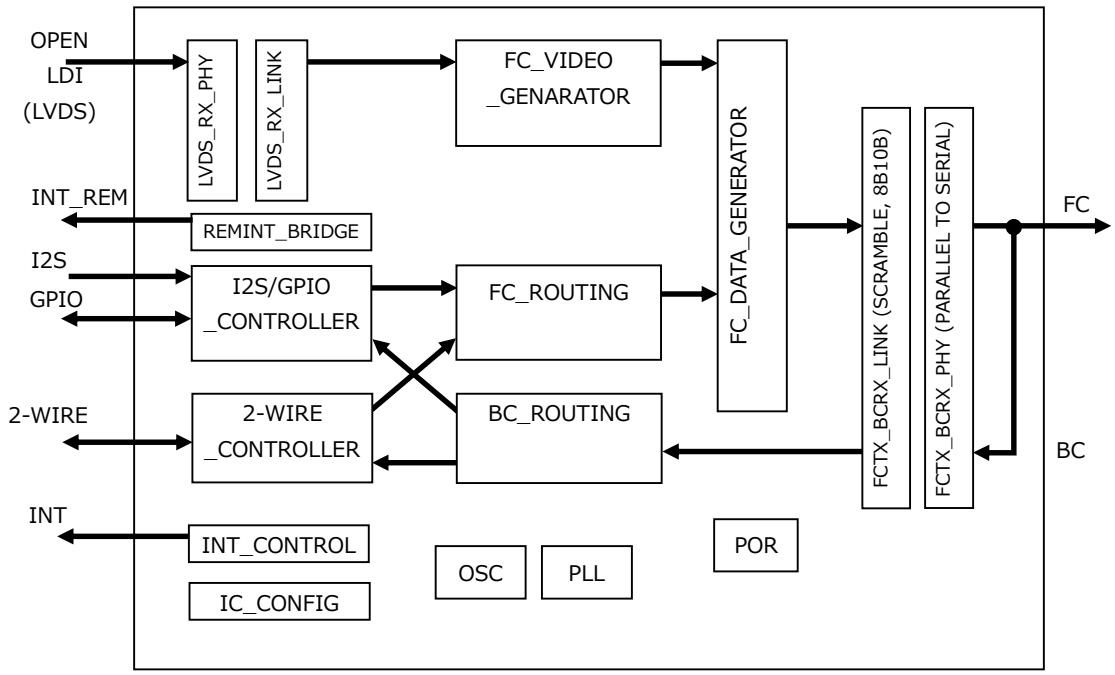
The THCV333-Q converts a single or dual Open LDI (LVDS) interface (up to 8 LVDS lanes + 1 clock) to an V-by-One® HS II interface. This device transmits a 24-bit video and several control symbol over a single serial pair operating up to 4Gbps line rate, or two serial pairs operating up to 4Gbps line rate. The serial stream contains an embedded clock, video control signals, RGB video data, and audio data. The payload is DC-balanced to enhance signal quality and support AC coupling.

The THCV333-Q serializer is intended for use with a THCV334-Q deserializer.

The THCV333-Q serializer and companion deserializer incorporate a 2-wire serial interface. The 2-wire serial interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote 2-wire serial slave devices.

The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse back channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge 2-wire serial transactions across the serial link from one 2-wire serial bus to another.

7.2. Functional Block Diagram



7.3. Feature Description

7.3.1. High-Speed Forward Channel Data Transfer

The High-Speed Forward Channel (FC) is composed of 30 bits of data containing RGB data, sync signals, 2-wire interface, GPIOs, and I2S audio transmitted from serializer to deserializer. The serial stream mostly contains RGB data, sync signals and internally calculated CRC information, while once in determined cycle time by FCTHRIO_MODE it contains 2-wire interface, GPIOs and I2S audio. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

The device supports Open LDI (LVDS) clocks in the range of 10 MHz to 150 MHz over one lane, or 50 MHz to 218 MHz over two lanes. The V-by-One® HS II serial stream rate is 3.75 Gbps maximum (1.5 Gbps minimum).

[PCLK.input] = Pixel clock input on Open-LDI per port = [F(oLDIin)]
[oLDIportNum] = Open-LDI input port number selected by pin setting
[PCLK.input.total] = Total Pixel clock input on Open-LDI = [F(oLDIin.total)] = [F(oLDIin)] x [oLDIportNum]
[FClaneNum] = V-by-One® HS II Forward Channel output Lane number selected by pin setting
[THRIOrate] = 8/7 (when FCTHRIO_MODE=0 selected by pin setting as 8cycle mode)
4/3 (when FCTHRIO_MODE=1 selected by pin setting as 4cycle mode)
[LowFreqMode] = x1 or x2 or x4 selected by register setting
[PCLK.FCout)] = Pixel clock output on Forward Channel (FC) per lane
[Data-rate.FCout)] = Output Data-rate on Forward Channel (FC) per lane
[PCLK.FCout)] = [PCLK.input] x {[oLDIportNum] / [FClaneNum]} x [THRIOrate] x [LowFreqMode]
[Data-rate.FCout)] = [PCLK.FCout] x (3 x 8 x 10/8)

The THCV333-Q requires internal settings to be adjusted according to the PCLK (FOLDIIN) from Open-LDI per port. See the table below for details.

PCLK (FOLDIN)		
Item	10MHz to 25MHz	25MHz to 150MHz
PLL (0x0271 to 0x0278)	See 7.3.20 section	Auto (Default)

PCLK (FOLDIN)		
Item	10MHz to 85MHz	85MHz to 150MHz
ULDT_EN (0x0019 bit[2:0])	0x7 (Default)	0x3

PCLK (FOLDIN)		
Item	10MHz to 60MHz	60MHz to 150MHz
R_BPDEN (0x0506 bit[0])	0x0 (Default)	0x1

PCLK (FOLDIN)		
Item	10MHz to 30MHz	30MHz to 150MHz
R_LFEN (0x0503 bit[0])	0x1	0x0 (Default)

The THCV333-Q also requires internal settings to be adjusted according to the V-by-One® HS II serial stream rate. See the table below for details.

V-by-One® HS II serial stream rate (TFCBIT)		
Item	1.5Gbps to 1.6Gbps	1.6Gbps to 3.75Gbps
FILTSEL (0x091A bit[3:0])	0x8	0x0 (Default)

7.3.2. Back Channel Data Transfer

The Backward Channel (BC) provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data with DC balance coding. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the 2-wire interface, CRC and GPIO information with 10 ~ 25 Mbps line rate (configured by the compatible deserializer).

[Data-rate.BCin)] = Input Data-rate on Backward Channel (BC)

[Data-rate.BCin)] = [Data-rate.FCout)] / 150

7.3.3. BCC Port Register Access

The THCV333-Q contains two downstream ports. Two ports are independent each other which requires independent setting transaction.

The THCV333-Q and counterpart compatible deserializer have independent 2-wire slave address respectively. They require independent setting transaction.

7.3.4. OpenLDI Input Frame and Color Bit Mapping Select

The THCV333-Q can be configured to accept 24-bit color (8-bit RGB) with several mapping schemes. Each unit corresponds to a single pixel clock (PCLK) cycle. The Open-LDI LVDS clock input to CLK± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by Register.

Open-LDI LVDS JEIDA 8bit Format

CLK

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A/E ch	G2	R7	R6	R5	R4	R3	R2
B/F ch	B3	B2	G7	G6	G5	G4	G3
C/G ch	DE	VS	HS	B7	B6	B5	B4
D/H ch	-	B1	B0	G1	G0	R1	R0

Open-LDI LVDS VESA 8bit Format

CLK

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A/E ch	G0	R5	R4	R3	R2	R1	R0
B/F ch	B1	B0	G5	G4	G3	G2	G1
C/G ch	DE	VS	HS	B5	B4	B3	B2
D/H ch	-	B7	B6	G7	G6	R7	R6

MIPI DPI THC63LVD827-Q Conversion Format

CLK

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A ch	R2	R1	R0	G7	G6	G5	G4
B ch	-	-	R7	R6	R5	R4	R3
C ch	DE	VS	HS	-	-	-	-
D ch	-	-	-	-	-	-	-

	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
E ch	B6	B5	B4	B3	B2	B1	B0
F ch	-	-	G3	G2	G1	G0	B7
G ch	DE	VS	HS	-	-	-	-
H ch	-	-	-	-	-	-	-

FCB-EV Single Pixel Link External Sync Format

SONY.S	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B ch	-	-	-	DE	VS	HS	Y7
C ch	-	C5	C4	C3	C2	C1	C0
D ch	-	-	-	-	-	C6	C7

FCB-EV Single Pixel Link Internal Sync Format

SONY.S	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B ch	-	-	-	-	-	-	Y7
C ch	-	C5	C4	C3	C2	C1	C0
D ch	-	-	-	-	-	C6	C7

FCB-EV Dual Pixel Link External Sync Format

SONY.D	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A/E ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B/F ch	-	-	-	-	VS	HS	Y7
C/G ch	DE	C5	C4	C3	C2	C1	C0
D/H ch	-	-	-	-	-	C6	C7

FCB-EV Dual Pixel Link Internal Sync Format

SONY.D	D<6>	D<5>	D<4>	D<3>	D<2>	D<1>	D<0>
A/E ch	Y6	Y5	Y4	Y3	Y2	Y1	Y0
B/F ch	-	-	-	-	-	-	Y7
C/G ch	-	C5	C4	C3	C2	C1	C0
D/H ch	-	-	-	-	-	C6	C7

7.3.5. Video Control Signals

The video control signal bits embedded in the high-speed Open LDI LVDS are subject to certain limitations relative to the video pixel clock period (PCLK).

First, Data Enable(DE) must have transition from High to Low to High,,, repeated cycle. DE high period is dedicated to send mainly RGB data, while DE low period is dedicated to send mainly Sync Control Information on FC.

In addition by default, the THCV333-Q applies a minimum pulse width filter on these signals to help eliminate spurious transitions.

Normal Mode Control Signals (VS, HS, DE) have the following restrictions:

· Horizontal Sync (HS): The video control signal pulse width must be 4 PCLKs or longer when the Control Signal Filter (register) is enabled. Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). As an additional function, HS could be activated to have at most two transitions per 130 PCLKs by register. Dual Open-LDI input or 2Lane V-by-One® HS output mode must have adequate even number of HS High and Low periods.

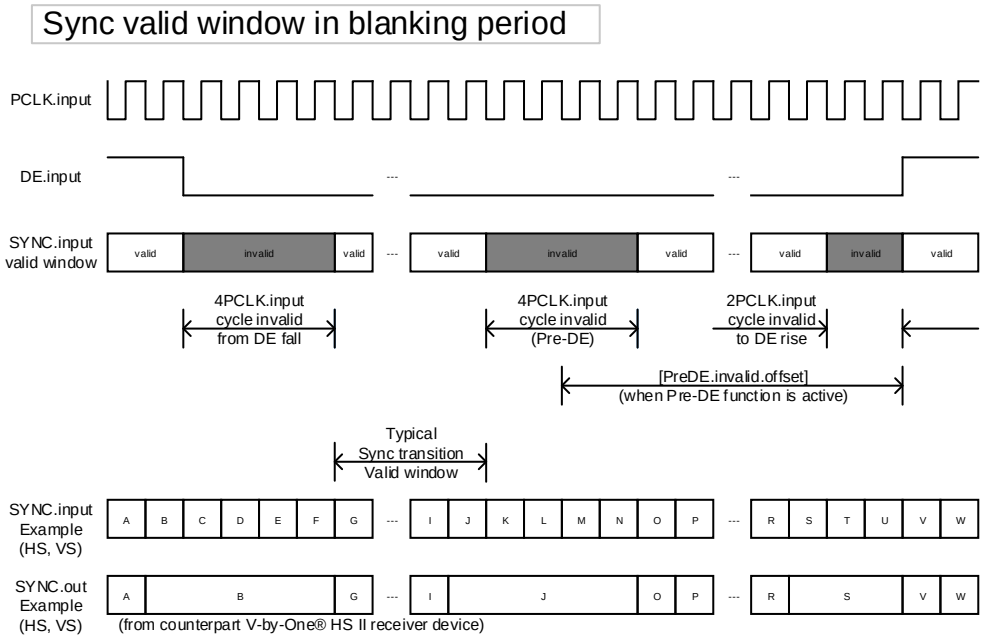
· Vertical Sync (VS): The video control signal pulse width must be 4 PCLKs or longer when the Control Signal Filter (register) is enabled. As an additional function, VS could be activated to be limited to 1 transition per 130 PCLKs by register, whose minimum pulse width could be 130 PCLKs. Period from DE High=>Low fall timing to VS activating timing and period from VS inactivating timing to DE Low=>High rise timing must be both at least 1 Line time period of the video frame. Dual Open-LDI input or 2Lane V-by-One® HS output mode must have adequate even number of VS High and Low periods.

· Data Enable Input (DE): The video control signal pulse width must be 4 PCLKs or longer when the Control Signal Filter (register) is enabled. Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). DE could be activated to have at most two transitions per 130 PCLKs by register. DE High maximum time period is 5000PCLKs. Dual Open-LDI input or 2Lane V-by-One® HS output mode must have adequate even number of DE High and Low periods.

In addition, Sync Control Signals (VS, HS) have the following restrictions related with DE.

In DE=Low blanking period, at the beginning and around at the end of DE=Low, there are several invalid window.

DE Low period also must have more than PreDE length.



[PreDE.invalid.offset] = Pre-DE invalid period offset from DE rise (when Pre-DE function is active)

[PreDE.Set] = Pre-DE position set by register PRE_DE_POSITION

[oLDIportNum] = Open-LDI input port number selected by pin setting

[FClaneNum] = V-by-One® HS II Forward Channel output Lane number selected by pin setting

[THRIOrate] = 8/7 (when FCTHRIO_MODE=0 selected by pin setting as 8cycle mode)

4/3 (when FCTHRIO_MODE=1 selected by pin setting as 4cycle mode)

[LowFreqMode] = x1 or x2 or x4 selected by register setting

[PreDE.invalid.offset] = [PreDE.set] x {[FClaneNum] / [oLDIportNum]} x {1 / [THRIOrate]} x [LowFreqMode]

7.3.5.1. Dummy DE operation

When only clock signal is supplied from source and DE input have not yet been supplied, THCV333-Q is able to start BCC communication not with DE input but with utilizing Dummy DE function prepared as register trigger. Dummy DE internally generates DE signal for BCC communication for mainly GPIO, 2-wire and other control signal bridge.

Video RGB image is usually not be appropriate to display panel; therefore, counterpart receiver OE Output Enable is supposed to be disabled to block further video output transfer.

After proper DE is input from Open-LDI source, Dummy DE function is supposed to be turned off to transfer input RGB data.

Just after turning off Dummy DE function, the very first DE High input from Open-LDI is discarded and is not able to be sent properly. From the next DE High, proper DE started to process properly.

Note : During Dummy DE=High to Low transition, any 2-wire, GPIO and I2S control bridge communication are all unstable and not able to be used. Users must take care of this behavior.

7.3.6. Power Down (PDN)

The Serializer has a PDN input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through VDDIO, where VDDIO = 1.71 V to 1.89 V. To save power, disable the link when the display is not needed (PDN = LOW). Ensure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, ensure that the pin is driven to 0V for at least 3ms before releasing or driving high. In the case where PDN is pulled up to VDDIO directly, register clock domain reset control after stable frequency (not transitioning) Open LDI LVDS clock input may be required (See Power-On-Sequence).

Toggling PDN low will POWER DOWN the device and RESET all control registers to default. During this time, PDN must be held low for a minimum of 3ms before going high again.

7.3.7. Serial Link Fault Detect

The THCV333-Q can detect fault conditions in the FC, BC and BCC interconnect. If a fault condition occurs, the Link Status is detected. The THCV333-Q will detect any of the following conditions:

1. Cable open
2. “+” to “-” short
3. ”+” to GND short
4. ”-” to GND short
5. ”+” to battery short
6. ”-” to battery short
7. Cable is linked incorrectly (DOUT+/DOUT- connections reversed)

Note: The device will detect any of the above conditions, but does not report specifically which one has occurred.

7.3.8. Interrupt Pin (INTN)

The INTN pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions. For the remote interrupt condition, the INTN pin works in conjunction with the INTN_IN pin on the deserializer. This interrupt signal, when configured, will propagate from the deserializer to the serializer.

1. On the Serializer, set remote INTN_IN interrupt Enable
2. Deserializer INTN_IN pin is set LOW by some downstream device.
3. Serializer pulls INTN pin LOW. The signal is active LOW, so a LOW indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read Interrupt source indicator register.
5. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTN_IN. This would be when the downstream device releases the INTN_IN pin on the Deserializer. The system is now ready to return to step (2) at next falling edge of INTN_IN.
6. A wrote to Interrupt clear will clear the interrupt at the Serializer, releasing INTN.

7.3.9. Remote Interrupt Pin (REM_INTN)

REM_INTN will mirror the status of INTN_IN pin on the deserializer and does not need to be cleared. If the serializer is not linked to the deserializer, REM_INTN will be high.

7.3.10. General-Purpose I/O

7.3.10.1. GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers.

7.3.10.2. D_GPIO[3:0] Configuration

In normal operation, D_GPIO[3:0] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers.

7.3.10.3. GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode.

NOTE: Local GPIO value may be configured and read through local register access.

7.3.11. General Protocol Communication

7.3.11.1. SPI Communication

SPI Communication can be configured by utilizing GPIO function.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel. The SPI Control Channel can operate in a high-speed when writing data only by FC, but must operate at lower frequencies when reading data by FC, BC, and BCC.

NOTE: SPI cannot be used to access Serializer / Deserializer registers.

7.3.11.2. UART Communication

UART Communication can be configured by utilizing GPIO function.

7.3.11.3. PWM Bridge

PWM Bridge can be configured by utilizing GPIO function. Data over the forward channel can be sent much faster than data over the reverse channel.

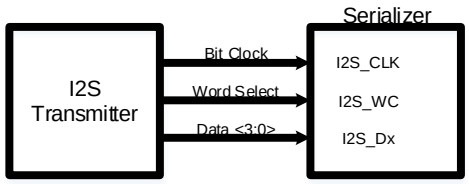
7.3.12. Family Compatibility

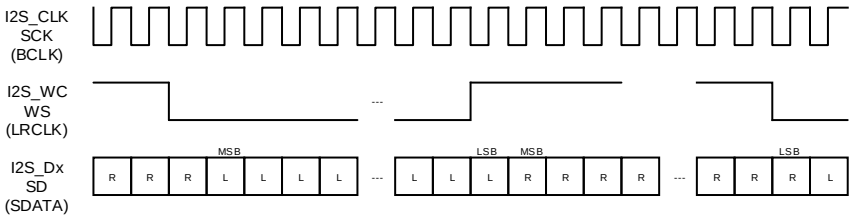
This V-by-One® HS II serializer is not backward compatible to the THCV23x nor THCV24x series.

7.3.13. Audio Modes

7.3.13.1. I2S Audio Interface

The THCV333-Q serializer features six I2S input pins that, when paired with a compatible deserializer, supports 7.1 High-Definition (HD) Surround Sound audio applications. The bit clock (I2S_CLK) supports frequencies restricted by FC PCLK. Four I2S data inputs transport two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input.





SAMPLE RATE (kHz)	I2S DATA WORD SIZE (bits)	I2S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
32	24	1.536
44.1	24	2.117
48	24	2.304
32	32	2.048
44.1	32	2.822
48	32	3.072

7.3.14. Data Transfer Speed

Symbol	Parameter	Condition	formula	unit
fSMPL_A2FC	Digitize Sampling Rate Audio from I2S_CLK, I2S_WC and I2S_D[3:0] to FC	x=FCTHRIO_MODE =4or8 (cycle)	fSMPL_A2FC =1/[{x/8}*8*(30*TTFCBIT)]	(sample /second)
fSMPL _GPI2FC	Digitize Sampling Rate Through GPIO from GPI to FC	x=FCTHRIO_MODE =4or8 (cycle) y=GPIO_CNT_REGS.SMPNUM=4or8 (active GPIOs)	fSMPL_GPI2FC =1/[{(x*y)/8}*(30*TTFCBIT)]	(sample /second)

7.3.15. Link Status Monitor

The THCV333-Q serializer have several Link Status Monitor functions like below.

2-wire interface unique ID

Open-LDI LVDS Rx monitor (including CRC, which is only available with specially prepared counterpart Tx)

Bi-directional Control Channel remote status monitor

Backward Channel status monitor (including CRC)

7.3.16. Internal Pattern Generation

The THCV333-Q serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode but with clock input, the test pattern will be displayed even if no data input is applied.

7.3.17. Internal Status Monitoring output

Internal status signal can be monitored as external MON0/MON1 pin output by register setting.

7.3.18. Output Spread Spectrum

Spread Spectrum Clock Generation (SSCG) modulation is available to apply on FC output.

SSCG modulated input and internal additional SSCG modulation are not available at the same time.

$$[PCLK.FCout]|_{no\ SSCG} \times \frac{(100 - |[R\_SPREAD]|)}{100} < [PCLK.FCout]|_{SSCG.CenterSpread} < [PCLK.FCout]|_{no\ SSCG} \times \frac{(100 + |[R\_SPREAD]|)}{100}$$

$$[PCLK.FCout]|_{no\ SSCG} \times \frac{(100 - |[R\_SPREAD]|)}{100} < [PCLK.FCout]|_{SSCG.DownSpread} < [PCLK.FCout]|_{no\ SSCG}$$

7.3.19. IO digital filter

Digital filters are prepared for IOs. GPIO digital filter can be arranged by register setting. SCL, SDA, and PDN, several VDDIO CMOS Input (Low speed) pins have also prepared digital filters with fixed tOSC x8 cycle filter setting behavior.

7.3.20. PLL manual operation for Low Frequency PCLK (OLDIIN) input between 10MHz to 25MHz

For typical operation, PLL manual setting is not required for normal operation. When PCLK (OLDIIN) is between 10MHz to 25MHz, PLL manual setting is required.

PLL Setting	PCLK (FOLDIN)	
	10MHz to 20MHz	20MHz to 25MHz
0x0271	0x01	0x01
0x0272	0x00	0x00
0x0273	0x40	0x40
0x0274	0x00	0x00
0x0276	0x00	0x00
0x0277	0x23	0x26
0x0278	0x01	0x01
-	Register set1	Register set2

For PLL manual setting, PLL_SPD is supposed to be set 1 (PLL Power down) from default value 0 before PLL manual parameters setting and re-activation (PLL power on) and start of normal operation.

cmd: write devaddr: 0x0B regaddr: 0x0019 val: 0x03 //ULDT_EN

cmd: write devaddr: 0x0B regaddr: 0x0506 val: 0x00 //R_BPDEN

cmd: write devaddr: 0x0B regaddr: 0x0503 val: 0x01 //R_LFEN

cmd: write devaddr: 0x0B regaddr: 0x0000 val: 0x01 /PLL Power down

Set Register set1 or 2

cmd: write devaddr: 0x0B regaddr: 0x0000 val: 0x00 /PLL Power on

cmd: read devaddr: 0x0B regaddr: 0x0125

//val: 0x00 Link not ready.

//val: 0x01 Link ready for VbyOneHSII port0.

Set Register for deserializer part as necessary

7.3.21. Internal Oscillator Clock operation mode

To link up with the Deserializer to enable the control signal when Open LDI (LVDS) Clock is not input, the THCV333-Q Internal Oscillator can be used to link up. The PATGEN function is used because DE is needed to synchronize the control signals. Since the PATGEN signal is output from the Deserializer, it is recommended that the Deserilizer output be set to disable. After the Open LDI signal is input, this function should be set to disable.

// Internal Oscillator Clock operation enable

cmd: write devaddr: 0x0B regaddr: 0x0680 val: 0x01 // PTGEN enable

cmd: write devaddr: 0x0B regaddr: 0x001A val: 0x02 // RXLOCKEN disable

cmd: write devaddr: 0x0B regaddr: 0x1C16 val: 0x22 // Tuning Registers access enable

cmd: write devaddr: 0x0B regaddr: 0x1C11 val: 0x30 // Internal Oscillator Clock enable

// Internal Oscillator Clock operation disable

cmd: write devaddr: 0x0B regaddr: 0x0680 val: 0x00 // PTGEN Disable

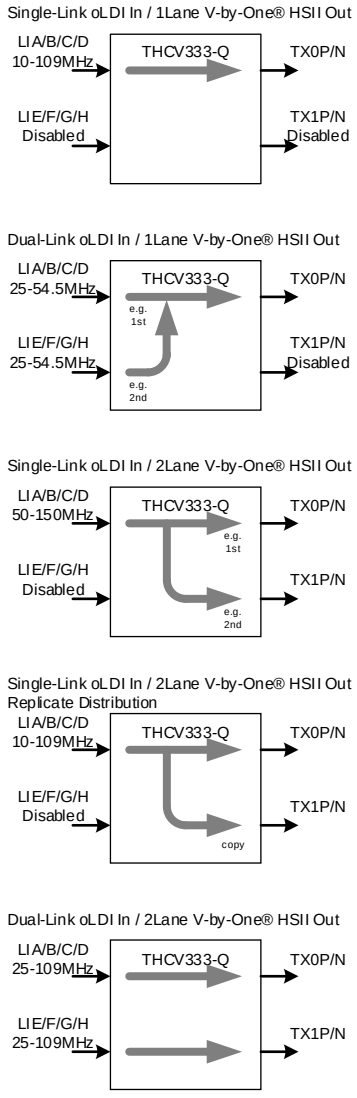
cmd: write devaddr: 0x0B regaddr: 0x001A val: 0x03 // RXLOCKEN enable

cmd: write devaddr: 0x0B regaddr: 0x1C11 val: 0x00 // Normal operation

7.4. Device Functional Modes

7.4.1. Mode Select Configuration Settings (BASEMODE[1:0])

Configuration of the device may be done via the LINPUTMODE_BM 0 / FCOUTPUTMODE_BM1 ,BASEMODE [1:0] input pins, or via the configuration registers.



7.4.2. V-by-One® HS II Modes of Operation

The V-by-One® HS II transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered.

7.4.2.1. Single Link Open-LDI LVDS Input / 1Lane V-by-One® HS II Output Operation

Single Link Open-LDI LVDS Input / 1Lane V-by-One® HS II Output mode supports frequency up to 109MHz for 24-bit video when paired with the compatible deserializer.

7.4.2.2. Dual Link Open-LDI LVDS Input / 1Lane V-by-One® HS II Output Operation

Dual Link Open-LDI LVDS Input / 1Lane V-by-One® HS II Output mode supports frequency up to 109MHz for 24-bit video when paired with the compatible deserializer.

7.4.2.3. Single Link Open-LDI LVDS Input / 2Lane V-by-One® HS II Output Operation

Single Link Open-LDI LVDS Input / 2Lane V-by-One® HS II Output mode supports frequency up to 150MHz for 24-bit video when paired with the compatible deserializer. This allows support for full 1080p video.

7.4.2.4. Single Link Open-LDI LVDS Input / 2Lane V-by-One® HS II Output Replicate Distribution

In this mode, the same video (up to 109MHz, 24-bit color) is delivered to each receiver.

7.4.2.5. Dual Link Open-LDI LVDS Input / 2Lane V-by-One® HS II Output Operation

In Dual Link Open-LDI LVDS Input / 2Lane V-by-One® HS II Output mode, the serializer splits a single video stream and sends alternating pixels on two downstream links. The receiver must be capable of receiving the dual stream video. This mode is capable of supporting an Open LDI clock frequency of up to 218MHz, with each V-by-One® HS II Tx port running at one-half the frequency. This allows support for full 1080p video.

7.4.2.6. Manual Setting of V-by-One® HS II Modes

The V-by-One® HS II modes of operation is supposed to be manually set.

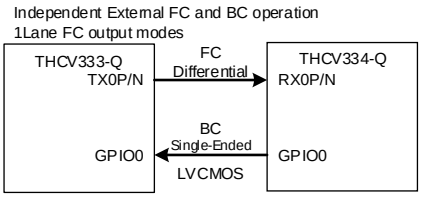
7.4.3. Low Frequency mode

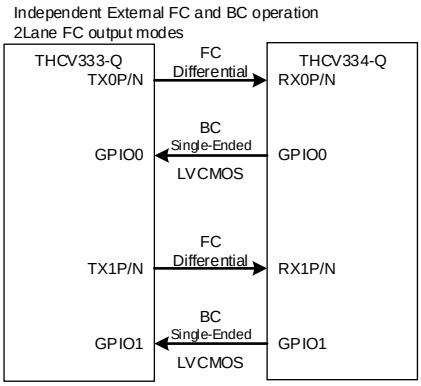
Low Frequency mode speed up the Forward Channel data-rate x2 or x4 in order to support the situation in which Open-LDI input frequency is too low to excess minimum data-rate of Forward Channel by the use of normal speed. For usage of Low Frequency mode, counterpart V-by-One® HS II receiver must have installed Low Frequency mode format decoder.

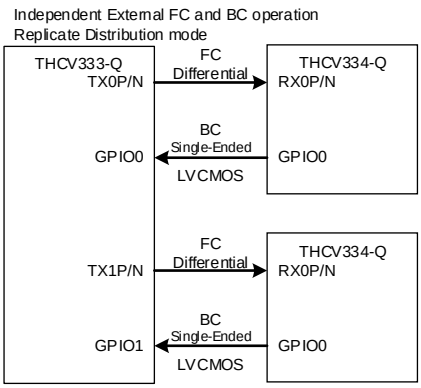
7.4.4. Independent External FC and BC operation mode

BCC operation can be separated in Independent External FC and BC mode. Register EXTBC (0x010A) control can enable separated BC. GPIO0/1 pins operate as external inputs.

cmd: write devaddr: 0x0B regaddr: 0x010A val: 0x01 // VbyOneHSII BCC external input select



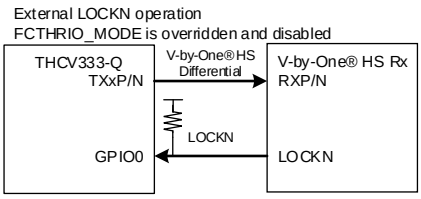




7.4.5. V-by-One® HS external LOCKN mode

V-by-One® HS behavior, in which FCTHRIO is disabled, is connectable to standard V-by-One® HS product with external LOCKN connection.

V-by-One® HS LOCKN inputs for respective lanes, Lane0 and Lane1, are supposed to be input separately, which may require external care on PCB.



cmd: write devaddr: 0x0B regaddr: 0x0101 val: 0x12 //Through IO Disable

cmd: write devaddr: 0x0B regaddr: 0x010A val: 0x01 //without BC

cmd: write devaddr: 0x0B regaddr: 0x1002 val: 0x00 //FSBP data through Disable

cmd: write devaddr: 0x0B regaddr: 0x1C16 val: 0x22 //Tuning Registers access enable

cmd: write devaddr: 0x0B regaddr: 0x1C13 val: 0x01 //VbyOneHSII lane0 LOCKN input mode

cmd: write devaddr: 0x0B regaddr: 0x1C02 val: 0x03 //GPIO0 LOCKN lane0 input

7.5. Programming

7.5.1. Serial Control Bus

This serializer may also be configured by the use of a 2-wire interface serial control bus. Multiple devices may share the serial control bus (multiple device addresses supported). The device address (2-wire slave address) is set by AIN pin or register setting.

THCV333-Q has 2-wire serial slave function. BCC function of THCV333-Q realize 2-wire serial interface remote bridge from local 2-wire serial master to BCC compatible counterpart deserializer or remote 2-wire slave device.

7.5.2. Serial slave device ID

AIN pin determines 2-wire slave Device ID setting.

2-wire slave Device ID of BCC Slave device which is used for BCC communication is defined in register in THCV333-Q as BCC Master. 2-wire slave Device ID of BCC Slave device which is used for BCC communication may be different from 2-wire slave Device ID of BCC Slave device which is defined by AIN pin of BCC Slave device and is used for local access (NOT from BCC Master side) on BCC Slave device PCB board.

7.5.3. Serial Read/Write access to local Register

HOST MPU can directly access THCV333-Q local register by 2-wire serial I/F.

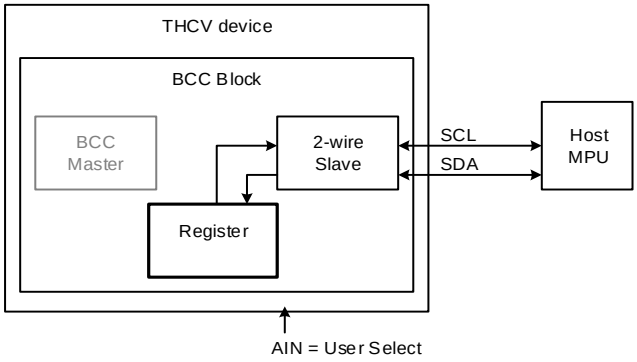


Figure 7. Host to local register access configuration

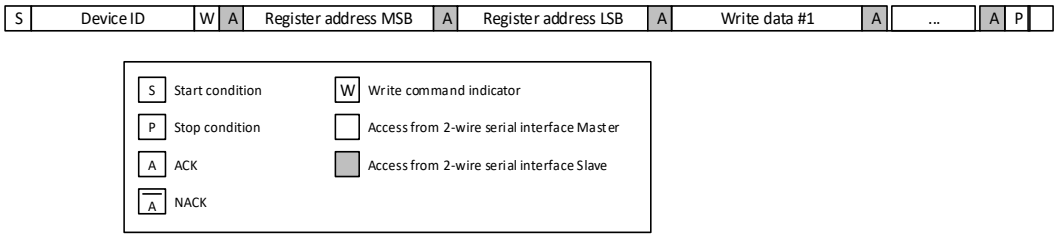


Figure 8. Serial I/F write to local register protocol

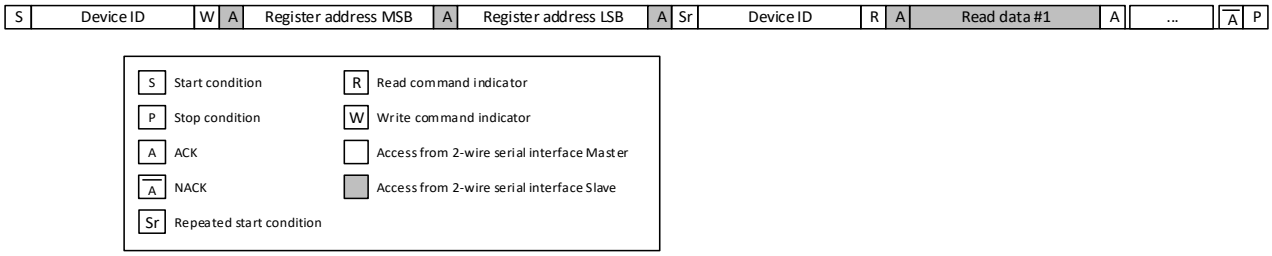


Figure 9. Serial I/F read to local register protocol

7.5.4. Bi-directional Control Channel bus

THCV333-Q has Bi-directional Control Channel (BCC) which enables bi-directional transmission of 2-wire serial interface signals, GPIO signals and also HTPDN/LOCKN signals for FC. THCV333-Q is BCC Master and connectable to BCC Slave device such as THCV334-Q.

To use GPIO (General Purpose Input/Output) pin, fault/error detection and interrupt function, “2-wire Set & Trigger mode”, “2-wire Pass Through mode” enables remote register access. THCV333-Q, BCC Master device has 2-wire serial slave block and can connect to HOST MPU. On the other hand, the counterpart BCC Slave device has 2-wire serial master block and can connect to remote side 2-wire serial slave devices.

HOST MPU can access register of BCC Master device, BCC Slave device and remote side 2-wire serial slave devices.

7.5.4.1. Serial Read/Write access to remote Register

The same serial access protocol as ones to local register are also available even in the case to remote register of BCC Slave device or remote-side 2-wire serial slave devices.

In addition, another read access protocol is available for remote read.

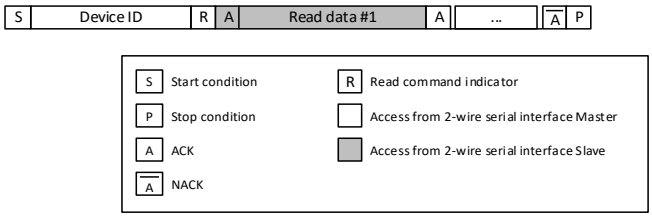


Figure 10. Serial I/F read to remote register protocol 2

7.5.4.2. BCC 2-wire Set and Trigger mode

HOST MPU can access to BCC Slave device register via THCV333-Q as BCC Master only by THCV333-Q internal local register control and monitoring on 2-wire Set&Trigger mode.

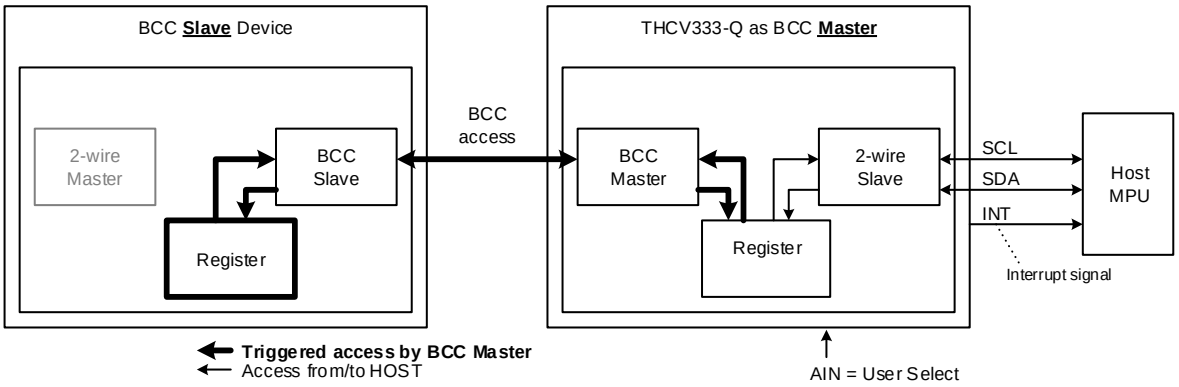


Figure 11. Host MPU to BCC Slave Register via BCC access configuration

HOST MPU can access to remote side 2-wire serial slave register via THCV333-Q as BCC Master only by THCV333-Q internal local register control and monitoring on 2-wire Set&Trigger mode.

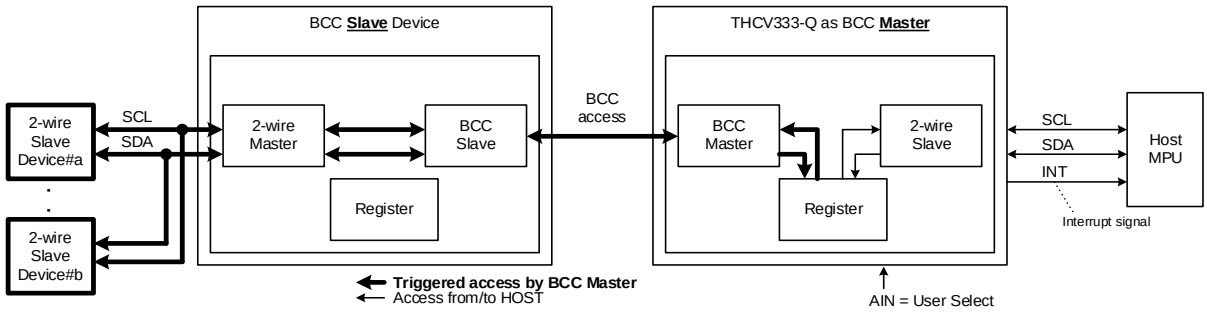


Figure 12. Host MPU to remote 2-wire slave devices via BCC access configuration

In principle, when BCC bridges 2-wire serial interface communication from BCC Master to BCC Slave or remote side 2-wire serial slave devices, time lag occurs between HOST MPU side 2-wire serial access and BCC Slave internal bus access or remote side 2-wire serial access.

When Set&Trigger mode is selected, 2-wire serial slave of BCC Master does not perform clock stretching. THCV333-Q, BCC Master device, informs HOST MPU that BCC Slave register access or remote side 2-wire serial register access has completed by interruption (detectable on INTN pin) without clock stretching.

7.5.4.3. BCC 2-wire Pass Through mode

BCC Master 2-wire Pass Through mode can bridge original local 2-wire commands to remote side.

2-wire Pass Through mode uses 2-wire slave clock stretching scheme at local BCC Master side. Host MCU 2-wire master must be no problem with clock stretching wait from 2-wire slave.

On address processing protocol “Assigned address & rename”, THCV333-Q 2-wire slave respond only to pre-defined-by-register particular 2-wire device address for remote Pass Through operation. Otherwise, 2-wire commands are ignored except THCV333-Q itself address. The device address can be renamed before remote send. The counterpart BCC Slave internal register access is available with separately defined another register setting.

On address processing protocol “All Through”, THCV333-Q 2-wire slave respond basically all 2-wire device address for remote Pass Through operation except THCV333-Q itself address. Additionally, Particular defined-by-register addresses can be ignored by THCV333-Q.

7.5.4.3.1. Divided write/read mode

BCC Slave side processing protocol “Divided write/read” scheme divides 2-wire commands into determined data Byte groups. Each data Byte groups are sent separately on remote side. Burst write/read access target Sub-Address (Word-Address) is interpreted so that subsequent Sub-Address (Word-Address) from 2nd group is automatically and properly incremented. As shown below, remote side 2-wire accesses are independent each other by determined Byte, which are defined in R_2WIRE_PASS_ADR_BYTE_NUM and R_2WIRE_PASS_DATA_BYTE_NUM at R_2WIRE_PASS_MODE=0x00 or 0x01.

Must be set the same mode with the BCC Slave (Deserializer) side.

cmd: write devaddr: 0x0B regaddr: 0x0B6A val: 0x00 //Default

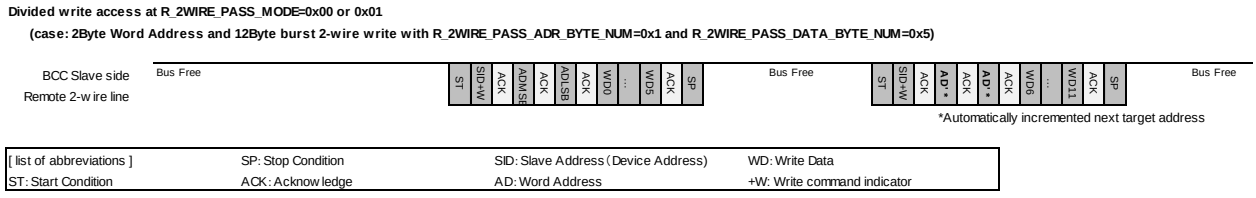


Figure 13. 2-wire Pass Through Divided mode BCC Slave command write scheme

7.5.4.3.2. Non-divided write/read mode

BCC Slave side processing protocol "Non-divided write/read" scheme divides 2-wire commands into determined data Byte groups. Each data Byte groups are also sent separately on remote side. However burst write/read access target Sub-Address (Word-Address) is NOT incremented, the access complete including SCL Low period.

cmd: write devaddr: 0x0B regaddr: 0x0B6A val: 0x01 //Non-divided write/read mode enable

Figure 14. 2-wire Pass Through Non-divided mode BCC Slave command write/read scheme

7.5.5. Restrictions on Multi-Master Coexistence Operation

Only one 2-wire interface transaction should be active at any time across the Bidirectional Control Channel. If Multi-Master coexistence are required, some method of transferring control initiative and avoidance of control collision between 2-wire interface masters at local and remote should be implemented.

7.6. Register Maps

Register regions are sectioned as below.

Register address		
Start	End	Description
0x0000	0x00FF	RST_control
0x0100	0x01FF	MODE_of_operation_control
0x0200	0x02FF	CLK_and_PLL_control
0x0500	0x05FF	LVDS_RX_control
0x0600	0x067F	FC_V-by-OneHSII_control
0x0680	0x06FF	PATTERN_GENarator
0x0900	0x09FF	FCTX_BCRX_LINK_control
0x0B00	0x0BFF	I2C_control
0x0C00	0x0CFF	I2SGPIO_control
0x1000	0x10FF	FC_MODE_control
0x1200	0x12FF	CHECKSUM
0x1300	0x13FF	INTN_interrupt_control
0x1400	0x14FF	REM_INTN_bridge_control
0x1C00	0x1CFF	Extra_control

NOTE

Any registers, which are not explained in this Register Maps, must be left untouched (No write nor read are allowed.) as default.

Any reserved registers, which are explained in this Register Maps and its all bits of the register address is reserved, must be left untouched (No write nor read are allowed.) as default.

Any reserved bits, which are explained in this Register Maps and remained bits other than the reserved bits in the same address is available function bits, according to the instruction of function bits, reserved bits can be write or read as 1 Byte unit access of 2-wire communication.

Any Read Only registers, whose “R/W” classification column is “R” in this Register Maps, are prohibited to be written by Write access.

Address	bit	Register Name	width	R/W	Init	Description
0x0000	[7:2]	reserved	6	-	-	-
	[1]	I2SPLL_SPD	1	R/W	1'h0	I2S PLL Power down 0x0: Power on 0x1: Power down
	[0]	PLL_SPD	1	R/W	1'h0	PLL Power down 0x0: Power on 0x1: Power down When changing PLL settings in Manual mode, need to power down once.
0x0001	[7:0]	reserved	8	-	-	-
0x0002	[7:0]	reserved	8	-	-	-
0x0003	[7:0]	reserved	8	-	-	-
0x0004	[7:0]	reserved	8	-	-	-
0x0005	[7:0]	reserved	8	-	-	-
0x0006	[7:0]	reserved	8	-	-	-
0x0007	[7:0]	reserved	8	-	-	-
0x0008	[7:0]	reserved	8	-	-	-
0x000B	[7:0]	reserved	8	-	-	-
0x000C	[7:0]	reserved	8	-	-	-
0x000D	[7:0]	reserved	8	-	-	-
0x000E	[7:0]	reserved	8	-	-	-
0x000F	[7:0]	KEY	8	R/W	1'h0	Power down registers access Enable 0x77: Enable (0x0000 - 0x000E registers are able to set) Other: Disable
0x0010	[7:0]	reserved	8	-	-	-
0x0011	[7:0]	reserved	8	-	-	-
0x0012	[7:0]	reserved	8	-	-	-
0x0013	[7:0]	reserved	8	-	-	-
0x0014	[7:0]	reserved	8	-	-	-
0x0015	[7:0]	reserved	8	-	-	-
0x0016	[7:0]	reserved	8	-	-	-
0x0017	[7:0]	reserved	8	-	-	-
0x0018	[7:0]	reserved	8	-	-	-
0x0019	[7:3]	reserved	6	-	-	-
	[2:0]	ULDT_EN	2	R/W	3'h7	LVDS RX unlock detecter enable register 0x7: Set when LVDS clock frequency 10MHz to 85MHz 0x3: Set when LVDS clock frequency 85MHz to 150MHz Other: Reserved
0x001A	[7:2]	reserved	6	-	-	-
	[1]	PLZLOCK_EN	1	R/W	1'h1	PLL Lock signal select 0x0: Disable PLL Lock signal 0x1: Enable PLL Lock signal
	[0]	RXLOCKN_EN	1	R/W	1'h1	LVDS RX Lock signal select 0x0: Disable LVDS RX Lock signal 0x1: Enable LVDS RX Lock signal When using internal OSC clock for PATGEN enable, should be set 0x0.
0x001B	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0020	[7:1]	reserved	7	-	-	-
	[0]	CMN_SRST	1	WC	1'h0	All Register clear 0x1: Reset and automatic clear
0x0021	[7:5]	reserved	3	-	-	-
	[4]	FCTXPDX_MON	1	R	1'h0	VbyOneHSII FC TX Power down Status Monitor 0x1: Power on, 0x0: Power down
	[3:2]	FCRXPDX_MON	2	R	2'h0	VbyOneHSII FC RX Power down Status Monitor [3]: Lane1 0x1: Power on, 0x0: Power down [2]: Lane0 0x1: Power on, 0x0: Power down
	[1]	reserved	1	-	-	-
	[0]	FPLLPDX_MON	1	R	1'h0	PLL Power down Status Monitor 0x1: Power on, 0x0: Power down
0x0022	[7:6]	reserved	2	-	-	-
	[5:4]	reserved	2	-	-	-
	[3:2]	BCBIASPDX_MON	2	R	2'h0	VbyOneHSII BC Bias Power down Status Monitor [3]: Lane1 0x1: Power on, 0x0: Power down [2]: Lane0 0x1: Power on, 0x0: Power down
	[1:0]	BCLDOPDX_MON	2	R	2'h0	VbyOneHSII BC LDO Power down Status Monitor [1]: Lane1 0x1: Power on, 0x0: Power down [0]: Lane0 0x1: Power on, 0x0: Power down
0x0023	[7:6]	FIFO_FCTXRSTX_MON	2	R	2'h0	VbyOneHSII FC TX FIFO Reset Status Monitor [7]: Lane1 0x1: Reset release , 0x0: Reset [6]: Lane0 0x1: Reset release , 0x0: Reset
	[5:4]	FCTXRSTX_MON	2	R	2'h0	VbyOneHSII FC TX Reset Status Monitor [5]: Lane1 0x1: Reset release , 0x0: Reset [4]: Lane0 0x1: Reset release , 0x0: Reset
	[3:2]	FIFO_FCRXRSTX_MON	2	R	2'h0	VbyOneHSII FC RX FIFO Reset Status Monitor [7]: Lane1 0x1: Reset release , 0x0: Reset [6]: Lane0 0x1: Reset release , 0x0: Reset
	[1:0]	FCRXRSTX_MON	2	R	2'h0	VbyOneHSII FC RX Reset Status Monitor [5]: Lane1 0x1: Reset release , 0x0: Reset [4]: Lane0 0x1: Reset release , 0x0: Reset
0x0024	[7:6]	reserved	2	-	-	-
	[5]	I2CBRSTX_MON	1	R	1'h0	BCC 2-wire Reset Status Monitor 0x1: Reset release , 0x0: Reset
	[4]	reserved	1	-	-	-
	[3]	APBRSTX_MON	1	R	1'h0	APB Reset Status Monitor 0x1: Reset release , 0x0: Reset
	[2]	OSCRSTX_MON	1	R	1'h0	Internal OSC Reset Status Monitor 0x1: Reset release , 0x0: Reset
	[1:0]	BCRSTX_MON	2	R	2'h0	VbyOneHSII BC Reset Status Monitor [1]: Lane1 0x1: Reset release , 0x0: Reset [0]: Lane0 0x1: Reset release , 0x0: Reset
0x0025	[7]	reserved	1	-	-	-
	[6]	reserved	1	-	-	-
	[5]	reserved	1	-	-	-
	[4]	LRZ_ULDTBP_MON	1	R	1'h0	LVDS RX Unlock detector status monitor for BP 0x1: Unlock, 0x0: Lock
	[3]	LRZ_ULDTLP_MON	1	R	1'h0	LVDS RX Unlock detector status monitor for LP 0x1: Unlock, 0x0: Lock
	[2]	LRZ_ULDTLF_MON	1	R	1'h0	LVDS RX Unlock detector status monitor for LF 0x1: Unlock, 0x0: Lock
	[1]	PLL_PD_MON	1	R	1'h0	PLL Power down status monitor 0x1: Power down, 0x0: Power on
	[0]	UNSTABLE_DET_MON	1	R	1'h0	Unstable detector status monitor 0x1: Detect unstable, 0x0: Not detect unstable
0x0026	[7:0]	reserved	8	-	-	-
0x0027	[7:0]	reserved	8	-	-	-
0x0028	[7:0]	reserved	8	-	-	-
0x0029	[7:0]	reserved	8	-	-	-
0x002A	[7:0]	reserved	8	-	-	-
0x002B	[7:0]	reserved	8	-	-	-
0x002C	[7:0]	reserved	8	-	-	-
0x002D	[7:0]	reserved	8	-	-	-
0x002E	[7:0]	reserved	8	-	-	-
0x002F	[7:0]	reserved	8	-	-	-
0x0030	[7:0]	GBL_SRST	8	R/W	8'h0	Global Reset 0x00: Normal operation 0xAA: Logic Reset. All registers return to the initial values. This register also returns to 0x00. Others: reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0100	[7:5]	reserved	3	-	-	-
	[4]	BASEMODE_OVERRIDE	1	R/W	1'h0	BASEMODE override enable. Can overridee the BM0/1 pin settings. 0x0: disable 0x1: enable
	[3:2]	reserved	2	-	-	-
	[1:0]	BASEMODE_REG	2	R/W	2'h0	<this regiseter is valid only when 0x0100[4]=1> BASEMODE setting 0x0: Single LVDS input, Single VbyOneHSII output mode 0x1: Dual LVDS input, Single VbyOneHSII output mode 0x2: Single LVDS input, Dual VbyOneHSII output mode 0x3: Dual LVDS input, Dual VbyOneHSII output mode
0x0101	[7:5]	reserved	3	-	-	-
	[4]	FCTHRIO_MODE_OVERRIDE	1	R/W	1'h0	FCTHRIO MODE override enable. Can overridee the FCTHRIO_MODE pin setting. 0x0: disable 0x1: enable
	[3:2]	reserved	2	-	-	-
	[1]	FCTHRIO_MODE_DISABLE	1	R/W	1'h0	<this regiseter is valid only when 0x0101[4]=1> FCTHRIO disable setting. To connect with VbyOneHS Deserializer may set disable. 0x0: enable 0x1: disable
	[0]	FCTHRIO_MODE_REG	1	R/W	1'h0	<this regiseter is valid only when 0x0101[4]=1> FCTHRIO MODE setting 0x0: 8cycle mode 0x1: 4cycle mode Need to set the same mode with Deserializer.
0x0102	[7:2]	reserved	7	-	-	-
	[1:0]	DUPLICATE_REG	2	R/W	2'h0	Low frequency mode select. This register is used when the VbyOneHSII FC rate is too slow to meet the specification or to increase the sampling rate of the control signal. 0x0: FC data rate x1 mode 0x1: FC data rate x2 mode 0x2: FC data rate x4 mode 0x3: Reserved
0x0103	[7:1]	reserved	7	-	-	-
	[0]	HIGHFREQIN_REG	1	R/W	1'h1	LVDS clock frequency select 0x0: Set when LVDS clock frequency 10MHz to 60MHz 0x1: Set when LVDS clock frequency 60MHz to 150MHz
0x0104	[7:1]	reserved	7	-	-	-
	[0]	LVDSBITMODE_REG	1	R/W	1'h0	LVDS bit mode select 0x0: 8bit mode 0x1: 6bit mode
0x0105	[7:1]	reserved	7	-	-	-
	[0]	DISTMODE_REG	1	R/W	1'h0	VbyOneHSII Distribution output mode select 0x0: Distribution output mode disable 0x1: Distribute VbyOneHSII output mode enable
0x0106	[7:0]	reserved	8	-	-	-
0x0107	[7:1]	reserved	7	-	-	-
	[0]	RXLSWAP_REG	1	R/W	1'h0	LVDS input port swap enable setting 0x0: Disable 0x1: Swaps LVDS input port.
0x0108	[7:1]	reserved	7	-	-	-
	[0]	TXLSWAP_REG	1	R/W	1'h0	VbyOneHSII output lane swap enable setting 0x0: Disable 0x1: Swaps VbyOneHSII output lane
0x0109	[7:0]	reserved	8	-	-	-
0x010A	[7:1]	reserved	7	-	-	-
	[0]	EXTBC_EN_REG	1	R/W	1'h0	VbyOneHSII BCC external input select. It also should be set enable when connect to VbyOneHS protocol Deserializer. 0x0: Disable, Normal operation. 0x1: Enable
0x010B	[7:0]	reserved	8	-	-	-
0x010C	[7:0]	reserved	8	-	-	-
0x010D	[7:0]	reserved	8	-	-	-
0x010E	[7:0]	reserved	8	-	-	-
0x010F	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0110	[7:0]	reserved	8	-	-	-
0x0111	[7:2]	reserved	6	-	-	-
	[1:0]	SER_TXPRE0	2	R/W	2'h0	VbyOneHSII Pre Emphasis Select for lane0 0x0: 0% 0x1: 50% 0x2: 100% 0x3: Reserved
0x0112	[7:2]	reserved	6	-	-	-
	[1:0]	SER_TXPRE1	2	R/W	2'h0	VbyOneHSII Pre Emphasis Select for lane1 0x0: 0% 0x1: 50% 0x2: 100% 0x3: Reserved
0x0113	[7:2]	reserved	6	-	-	-
	[1:0]	SER_TXDRV0	2	R/W	2'h2	VbyOneHSII Drive Strangth Select for lane0 0x0: 200mV 0x1: 300mV 0x2: 400mV 0x3: 600mV (Only valid when SER_TXPRE0 = 0x0)
0x0114	[7:2]	reserved	6	-	-	-
	[1:0]	SER_TXDRV1	2	R/W	2'h2	VbyOneHSII Drive Strangth Select for lane1 0x0: 200mV 0x1: 300mV 0x2: 400mV 0x3: 600mV (Only valid when SER_TXPRE1 = 0x0)
0x0115	[7:1]	reserved	7	-	-	-
	[0]	SER_TXFLIP	1	R/W	1'h0	VbyOneHSII P/N swap enable setting 0x0: Disable 0x1: Swaps VbyOneHSII output P/N
0x0116	[7:0]	reserved	8	-	-	-
0x0117	[7:1]	reserved	7	-	-	-
	[0]	SER_TXBET	1	R/W	1'h0	Field BET Mode enable setting 0x0: Disable 0x1: Enable
0x0121	[7:0]	reserved	8	-	-	-
0x0122	[7:0]	reserved	8	-	-	-
0x0123	[7:0]	reserved	8	-	-	-
0x0124	[7:0]	reserved	8	-	-	-
0x0125	[7:0]	reserved	8	-	-	-
0x0126	[7:0]	reserved	8	-	-	-
0x0127	[7:0]	reserved	8	-	-	-
0x0128	[7:0]	reserved	8	-	-	-
0x0129	[7:0]	reserved	8	-	-	-
0x012A	[7:0]	reserved	8	-	-	-
0x012B	[7:0]	reserved	8	-	-	-
0x012C	[7:0]	reserved	8	-	-	-
0x012D	[7:0]	reserved	8	-	-	-
0x012E	[7:0]	reserved	8	-	-	-
0x012F	[7:0]	reserved	8	-	-	-
0x0130	[7:0]	reserved	8	-	-	-
0x0131	[7:0]	reserved	8	-	-	-
0x0132	[7:5]	reserved	3	-	-	-
	[4]	BC_DVALID_1	1	R	1'h0	VbyOneHSII FC/BC Link status for lane1 0x0: Not ready, Unlock 0x1: Ready, Lock When VbyOneHSII lane swap enable, this value should be "1". When VbyOneHSII Distribution output mode enable, this value should be "1". When Dual VbyOneHSII mode, this value should be "0" because Link checks lane0 only.
	[3:1]	reserved	3	-	-	-
	[0]	BC_DVALID_0	1	R	1'h0	VbyOneHSII FC/BC Link status for lane0 0x0: Not ready, Unlock 0x1: Ready, Lock When VbyOneHSII lane swap enable, this value should be "0".

Address	bit	Register Name	width	R/W	Init	Description
0x0140	[7:2]	reserved	6	-	-	-
	[1]	L12UP_EN	1	R/W	1'h0	VDDL 1.2V power supply monitor enable setting. High voltage fault can be detected. The detection result can be output as an Interrupt. 0x0: Disable, 0x1: Enable
	[0]	IO33UN_EN	1	R/W	1'h0	VDDIO 3.3V power supply monitor enable setting. Under voltage fault can be detected. The detection result can be output as an Interrupt. 0x0: Disable, 0x1: Enable
0x0141	[7]	AIN_PE	1	R/W	1'h1	AIN pin pull-down select setting 0x0: disable 0x1: enable
	[6]	FCTHRIO_MODE_PE	1	R/W	1'h1	FCTHRIO_MODE pin pull-down select setting 0x0: disable 0x1: enable
	[5]	BASEMODE1_PE	1	R/W	1'h1	FCOUTPUTMODE_BM1 pin pull-down select setting 0x0: disable 0x1: enable
	[4]	BASEMODE0_PE	1	R/W	1'h1	LINPUTMODE_BM0 pin pull-down select setting 0x0: disable 0x1: enable
	[3]	MON1_PE	1	R/W	1'h1	MON1 pin pull-down select setting 0x0: disable 0x1: enable
	[2]	MON0_PE	1	R/W	1'h1	MON0 pin pull-down select setting 0x0: disable 0x1: enable
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x0142	[7:0]	reserved	8	-	-	-
0x0143	[7:2]	reserved	6	-	-	-
	[1]	reserved	1	-	-	-
	[0]	REM_INTN_PE	1	R/W	1'h0	REM_INTN pin pull-down select setting 0x0: disable 0x1: enable
0x0144	[7:0]	reserved	8	-	-	-
0x01F0	[7:0]	ID0	8	R	8'h74	ID code "t"
0x01F1	[7:0]	ID1	8	R	8'h68	ID code "h"
0x01F2	[7:0]	ID2	8	R	8'h63	ID code "c"
0x01F3	[7:0]	ID3	8	R	8'h76	ID code "v"
0x01F4	[7:0]	ID4	8	R	8'h33	ID code "3"
0x01F5	[7:0]	ID5	8	R	8'h33	ID code "3"
0x01F6	[7:0]	ID6	8	R	8'h33	ID code "3"
0x01F7	[7:0]	ID7	8	R	8'h00	ID code " "

Address	bit	Register Name	width	R/W	Init	Description
0x0250	[7:5]	reserved	3	-	-	-
	[4:0]	CDET_EN	5	R/W	5'h0	Clock Frequency Detector enable. This register can detect the internal clock frequency using the internal oscillator or the VbyOneHSII clock. It can also detect when the clock frequency crosses above or below a set value. 0x0: Disable, 0x1: Enable [0]: LVDS RX clock [1]: Reserved [2]: VbyOneHSII clock [3]: Internal oscillator clock by LVDS RX clock [4]: Reserved [0][2] are detected by internal oscillator [3] is detected by LVDS RX clock. It's necessary the stable lock.
0x0260	[7:0]	TGETCNT0_1	8	R	7'h0	<this regiseter is valid only when 0x0250[0]=1> LVDS RX clock frequency counter [15:8] TRCIP ~ MEASURE_VALUE0 * tosc / TGETCNT0[15:0] MEASURE_VALUE0 = 480 as default when it is unchanged.
0x0261	[7:0]	TGETCNT0_0	8	R	7'h0	<this regiseter is valid only when 0x0250[0]=1> LVDS RX clock frequency counter [7:0]
0x0262	[7:0]	reserved	8	-	-	-
0x0263	[7:0]	reserved	8	-	-	-
0x0264	[7:0]	TGETCNT2_1	8	R	7'h0	<this regiseter is valid only when 0x0250[2]=1> VbyOneHSII clock frequency counter [15:8] TTFCBIT * 30 = PCLK.FCout ~ MEASURE_VALUE2 * tosc / TGETCNT2[15:0] MEASURE_VALUE2 = 480 as default when it is unchanged.
0x0265	[7:0]	TGETCNT2_0	8	R	7'h0	<this regiseter is valid only when 0x0250[2]=1> VbyOneHSII clock frequency counter [7:0]
0x0266	[7:0]	TGETCNT3_1	8	R	7'h0	<this regiseter is valid only when 0x0250[3]=1> Internal oscillator clock frequency counter [15:8] tOSC ~ MEASURE_VALUE3 * TRCIP / TGETCNT3[15:0] MEASURE_VALUE3 = 480 as default when it is unchanged.
0x0267	[7:0]	TGETCNT3_0	8	R	7'h0	<this regiseter is valid only when 0x0250[3]=1> Internal oscillator clock frequency counter [7:0]
0x0268	[7:0]	reserved	8	-	-	-
0x0269	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0270	[7:0]	reserved	8	-	-	-
0x0271	[7:6]	reserved	2	-	-	-
	[5:0]	REFDIV	6	R/W	6'h3	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0272	[7:4]	reserved	4	-	-	-
	[3:0]	INTIN_1	4	R/W	4'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0273	[7:0]	INTIN_0	8	R/W	8'h18	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0274	[7:0]	FRACIN_2	8	R/W	8'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0275	[7:0]	FRACIN_1	8	R/W	8'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0276	[7:0]	FRACIN_0	8	R/W	8'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0277	[7]	reserved	1	-	-	-
	[6:4]	POSTDIV2	3	R/W	3'h1	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
	[3]	reserved	1	-	-	-
	[2:0]	POSTDIV1	3	R/W	3'h7	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0278	[7:1]	reserved	7	-	-	-
	[0]	DIRECTMODE	1	R/W	1'h0	PLL Manual Setting for Low Frequency LVDS Clock Input See 7.3.20 section.
0x0280	[7:4]	reserved	4	-	-	-
	[3:0]	DIVVAL	4	R/W	4'hC	<this regiseter is valid only when 0x0283[0]=0> SSCG modulation frequency setting. Must be not set 0x0. FMOD = PCLK / (DIVVAL*128) ≦ 30kHz
0x0281	[7:5]	reserved	3	-	-	-
	[4:0]	SPREAD	5	R/W	5'h3	<this regiseter is valid only when 0x0283[0]=0> SSCG modulation depth select setting 0x0: 0% 0x1: 0.1% 0x2: 0.2% 0x3: 0.3% 0x4: 0.4% 0x5: 0.5% others: Reserved
0x0282	[7:1]	reserved	7	-	-	-
	[0]	DOWNSPREAD	1	R/W	1'h0	<this regiseter is valid only when 0x0283[0]=0> Spread mode select setting 0x0: Center Spread 0x1: Down Spread
0x0283	[7:1]	reserved	7	-	-	-
	[0]	DISABLE_SSCG	1	R/W	1'h1	SSCG enable setting 0x0: Enable 0x1: Disable

Address	bit	Register Name	width	R/W	Init	Description
0x0500	[7:0]	reserved	8	-	-	-
0x0501	[7:1]	reserved	7	-	-	-
	[0]	R_TERMEN	1	R/W	1'h1	LVDS RX Internal termination enable setting for port0 0x0: Disable, 0x1: Enable
0x0502	[7:1]	reserved	7	-	-	-
	[0]	R_TERMBEN	1	R/W	1'h1	LVDS RX Internal termination enable setting for port1 0x0: Disable, 0x1: Enable
0x0503	[7:1]	reserved	7	-	-	-
	[0]	R_LFEN	1	R/W	1'h0	LVDS RX Low Frequency mode setting 0x0: 30MHz to 150MHz 0x1: 10MHz to 30MHz
0x0504	[7:0]	reserved	8	-	-	-
0x0505	[7:0]	reserved	8	-	-	-
0x0506	[7:1]	reserved	7	-	-	-
	[0]	R_BPDEN	1	R/W	1'h0	LVDS RX BB enable register 0x0: Disabled; Set when LVDS clock frequency 10MHz to 60MHz 0x1: Enabled; Set when LVDS clock frequency 60MHz to 150MHz
0x0507	[7:0]	reserved	8	-	-	-
0x0508	[7:0]	reserved	8	-	-	-
0x0509	[7:0]	reserved	8	-	-	-
0x050A	[7:0]	reserved	8	-	-	-
0x0580	[7:0]	reserved	8	-	-	-
0x0581	[7:0]	reserved	8	-	-	-
0x0582	[7:0]	reserved	8	-	-	-
0x0583	[7:0]	reserved	8	-	-	-
0x0584	[7:0]	reserved	8	-	-	-
0x0585	[7:0]	reserved	8	-	-	-
0x0586	[7:0]	reserved	8	-	-	-
0x0587	[7:0]	reserved	8	-	-	-
0x0588	[7:0]	reserved	8	-	-	-
0x0589	[7:0]	reserved	8	-	-	-
0x058A	[7:0]	reserved	8	-	-	-
0x058B	[7:0]	reserved	8	-	-	-
0x058C	[7:0]	reserved	8	-	-	-
0x058D	[7:0]	reserved	8	-	-	-
0x058E	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0600	[7:4]	reserved	4	-	-	-
	[3:0]	R_TERMEN	4	R/W	4'h0	LVDS color format setting 0x0 : JEIDA format 0x1 : VESA format 0x2 : MIPI DPI LVD827-Q Conversion format 0x3 : FCB-EV Single External Sync0 0x4 : FCB-EV Single Internal Sync0 0x5 : FCB-EV Dual External Sync 0x6 : FCB-EV Dual Internal Sync Others : Reserved
0x0601	[7:3]	reserved	5	-	-	-
	[2]	SYNC_POL_HS	1	R/W	1'h0	LVDS input HSYNC Polarity 0x0: Low active, 0x1: High active
	[1]	SYNC_POL_VS	1	R/W	1'h0	LVDS input VSYNC Polarity 0x0: Low active, 0x1: High active
	[0]	SYNC_POL_DE	1	R/W	1'h1	LVDS input DE Polarity 0x0: Low active, 0x1: High active
0x0602	[7:6]	reserved	2	-	-	-
	[5:4]	SYNC_FILTER_HS	2	R/W	2'h2	Hsync filter 0 : No Filter 1 : 1cyc Filter 2 : 2cyc Filter(default) 3 : 3cyc Filter
	[3:2]	SYNC_FILTER_VS	2	R/W	2'h2	Vsync filter 0 : No Filter 1 : 1cyc Filter 2 : 2cyc Filter(default) 3 : 3cyc Filter
	[1:0]	SYNC_FILTER_DE	2	R/W	2'h2	DE filter 0 : No Filter 1 : 1cyc Filter 2 : 2cyc Filter(default) 3 : 3cyc Filter
0x0603	[7:3]	reserved	5	-	-	-
	[2]	VPULSE_SUPPRESSION	1	R/W	1'h1	VSYNC pulse suppression 0 : disable / 1: enable
	[1]	HPULSE_SUPPRESSION	1	R/W	1'h1	HSYNC pulse suppression 0 : disable / 1: enable
	[0]	DEPULSE_SUPPRESSION	1	R/W	1'h1	DE pulse suppression 0 : disable / 1 : enable
0x0604	[7:0]	reserved	8	-	-	-
0x0605	[7:0]	reserved	8	-	-	-
0x0606	[7:0]	reserved	8	-	-	-
0x0607	[7:0]	reserved	8	-	-	-
0x0608	[7:0]	reserved	8	-	-	-
0x0609	[7:0]	reserved	8	-	-	-
0x060A	[7:0]	reserved	8	-	-	-
0x060B	[7:0]	reserved	8	-	-	-
0x060C	[7:0]	reserved	8	-	-	-
0x060D	[7:0]	reserved	8	-	-	-
0x060E	[7:0]	reserved	8	-	-	-
0x060F	[7]	reserved	1	-	-	-
	[6:0]	PRE_DE_POSITION	7	R/W	1'd40	1'd0 : Disable 1'd8 : 8 cycle before DE 1'd16 : 16 cycle before DE PRE_DE_POSITION must be a multiple of 8. PRE_DE_POSITION must be < 127.
0x0610	[7:0]	reserved	8	-	-	-
0x0611	[7:1]	reserved	7	-	-	-
	[0]	DUMMY_DE	1	R/W	1'h0	Dummy DE Enable 0 : disable / 1: enable
0x0612	[7:1]	reserved	7	-	-	-
	[0]	PRE_DE	1	R/W	1'h1	PreDE Enable 0 : disable / 1: enable
0x0613	[7:0]	reserved	8	-	-	-
0x0614	[7:0]	reserved	8	-	-	-
0x0615	[7:0]	reserved	8	-	-	-
0x0616	[7:0]	reserved	8	-	-	-
0x0617	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0680	[7:1]	reserved	7	-	-	-
	[0]	PATGENEN	1	R/W	1'h0	Pattern Generator Enable setting. 0x0: Disable, 0x1: Enable If use internal OSC clock, need to check 0x001A and 0x1C11 registers.
0x0681	[7:1]	reserved	7	-	-	-
	[0]	LANESEL	1	R/W	1'h0	Pattern Generator lane setting. 0x0: Set when LVDS RX is Single link. 0x1: Set when LVDS RX is Dual link.
0x0682	[7:4]	reserved	4	-	-	-
	[3:0]	HACTIVE_UPPER	4	R/W	4'h7	H active period [11:8]. ([pixel])
0x0683	[7:0]	HACTIVE_LOWER	8	R/W	8'h80	H active period [7:0]. ([pixel]) Default value is 1920 pixels.
0x0684	[7:3]	reserved	5	-	-	-
	[2:0]	VACTIVE_UPPER	3	R/W	3'h4	V active period [10:8]. ([line])
0x0685	[7:0]	VACTIVE_LOWER	8	R/W	8'h38	V active period [7:0]. ([line]) Default value is 1080 lines. If this setting is odd value, will automatically add 1 lines.
0x0686	[7:4]	reserved	4	-	-	-
	[3:0]	HBLANK_UPPER	4	R/W	4'h1	H blank period [11:8]. ([pixel])
0x0687	[7:0]	HBLANK_LOWER	8	R/W	8'h18	H blank period [7:0]. ([pixel]) Default value is 280 pixels.
0x0688	[7:2]	reserved	6	-	-	-
	[1:0]	VBLANK_UPPER	2	R/W	2'h0	V blank period [9:8]. ([line])
0x0689	[7:0]	VBLANK_LOWER	8	R/W	8'h2D	V blank period [7:0]. ([line]) Default value is 45 lines.
0x068A	[7:1]	reserved	7	-	-	-
	[0]	HSYNCWIDTH_UPPER	1	R/W	1'h0	H active pluse width [8]. ([pixel])
0x068B	[7:0]	HSYNCWIDTH_LOWER	8	R/W	8'h2C	H active pluse width [7:0]. ([pixel]) Default value is 44 pixels.
0x068C	[7:0]	VSYNCWIDTH	8	R/W	8'h5	V active pluse width [7:0]. ([line]) Default value is 5 lines.
0x068D	[7:1]	reserved	7	-	-	-
	[0]	HBACKPORCH_UPPER	1	R/W	1'h0	H back portch period [8]. ([pixel])
0x068E	[7:0]	HBACKPORCH_LOWER	8	R/W	8'h94	H back portch period [7:0]. ([pixel]) Default value is 148 pixels.
0x068F	[7]	reserved	1	-	-	-
	[6:0]	VBACKPORCH	7	R/W	7'h24	V back porch period [6:0]. ([line]) Default value is 36 lines.
0x0690	[7:0]	reserved	8	-	-	-
0x0691	[7:0]	reserved	8	-	-	-
0x0692	[7:0]	reserved	8	-	-	-
0x0693	[7:0]	reserved	8	-	-	-
0x0694	[7:0]	reserved	8	-	-	-
0x0695	[7:0]	reserved	8	-	-	-
0x0696	[7:1]	reserved	7	-	-	-
	[0]	HSYNCDIS	1	R/W	1'h0	Generate HSYNC setting 0x0: Generate Hsync 0x1: Not generate Hsync
0x0697	[7:5]	reserved	3	-	-	-
	[4]	VSYNCPOL	1	R/W	1'h1	VSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.
	[3:1]	reserved	3	-	-	-
	[0]	HSYNCPOL	1	R/W	1'h1	HSYNC polality setting 0x0: Active low, idle high. 0x1: Active high, idle low.

Address	bit	Register Name	width	R/W	Init	Description
0x0698	[7:6]	reserved	2	-	-	-
	[5:0]	PATGEN_PTN	6	R/W	6'hB	Pattern select setting. 0x0: Automatic pattern switching repetition from 0x1 to 0xE. 0x1: White Raster 0x2: Black Raster 0x3: Red Raster 0x4: Green Raster 0x5: Blue Raster 0x6: Horizontal Clolor Bars 0x7: Vertical Clolor Bars 0x8: Horizontal Gray Ramp 0x9: Vertical Gray Ramp 0xA: Horizontal RGBW Ramp 0xB: Vertical RGBW Ramp 0xC: 16x16 Pixel Cheker 0xD: Frame 0xE: Sub Pixel Checker 0xF: Black Raster 0x10: Frame2 0x11: 4x1 Checker1 0x12: 4x1 Checker2 0x13: 2x1 Checker1 0x14: 2x1 Checker2 0x15: 1x1 Checker1 0x16: 1x1 Checker2 0x17: Cursor 0x18: CheckerA 0x19: CheckerB 0x1A: CheckerC 0x1B: Green Horizontal Stripe 0x1C: Green Vertical Stripe 0x1E: Frame3 0x1F: WindowA 0x20: WindowB 0x21: PRBS7 Others: Reserved
0x0699	[7:0]	GS_SEL_R	8	R/W	8'hFF	Gradient Setting for Red. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Red
0x069A	[7:0]	GS_SEL_G	8	R/W	8'hFF	Gradient Setting for Green. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Green
0x069B	[7:0]	GS_SEL_B	8	R/W	8'hFF	Gradient Setting for Blue. This register effects to the Raster, Color Bars and Dot Pattern. 00:Black <=> FF:Blue
0x069C	[7:4]	reserved	4	-	-	-
	[3:0]	CURSOR_H_UPPER	4	R/W	4'h3	Cursor position on horizontal direction [11:8]. This register effects to the cursor Pattern.
0x069D	[7:0]	CURSOR_H_LOWER	8	R/W	8'hC0	Cursor position on horizontal direction [7:0]. This register effects to the cursor Pattern. Default value is 960 pixels.
0x069E	[7:4]	reserved	4	-	-	-
	[3:0]	CURSOR_V_UPPER	4	R/W	4'h2	Cursor position on vertical direction [11:8]. This register effects to the cursor Pattern.
0x069F	[7:0]	CURSOR_V_LOWER	8	R/W	8'h1C	Cursor position on vertical direction [7:0]. This register effects to the cursor Pattern. Default value is 540 lines.
0x06A0	[7:4]	reserved	4	-	-	-
	[3:0]	DOT_H_UPPER	4	R/W	4'h3	Dot position on horizontal direction [11:8]. This register effects to the cursor Pattern.
0x06A1	[7:0]	DOT_H_LOWER	8	R/W	8'hC0	Dot position on horizontal direction [7:0]. This register effects to the cursor Pattern. Default value is 960 pixels.
0x06A2	[7:4]	reserved	4	-	-	-
	[3:0]	DOT_V_UPPER	4	R/W	4'h2	Dot position on vertical direction [11:8]. This register effects to the cursor Pattern.
0x06A3	[7:0]	DOT_V_LOWER	8	R/W	8'h1C	Dot position on vertical direction [7:0]. This register effects to the cursor Pattern. Default value is 540 lines.
0x06A4	[7:0]	DOT_COL_R	8	R/W	8'hFF	Dot Gradient Setting for Red. This register effects to the Dot Pattern. 00:Black <=> FF:Red
0x06A5	[7:0]	DOT_COL_G	8	R/W	8'hFF	Dot Gradient Setting for Green. This register effects to the Dot Pattern. 00:Black <=> FF:Green
0x06A6	[7:0]	DOT_COL_B	8	R/W	8'hFF	Dot Gradient Setting for Blue. This register effects to the Dot Pattern. 00:Black <=> FF:Blue
0x06A7	[7:1]	reserved	7	-	-	-
	[0]	DOT_INV	1	R/W	1'h0	Invert Dot color setting. 0x0: Not invert, 0x1: Invert

Address	bit	Register Name	width	R/W	Init	Description
0x0900	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_LSEL	1	R/W	1'h0	BC Eye Jitter Monitor lane select. 0x0: Lane0. 0x1: Lane1.
0x0901	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_EN	1	W	1'h0	BC Eye Jitter Monitor Enable (1shot). 0x1: Enable (1shot).
0x0902	[7:1]	reserved	7	-	-	-
	[0]	BC_XEYE_CLR	1	W	1'h0	BC Eye Jitter Monitor Clear. 0x1: Clear.
0x0903	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE0	6	R	-	BC Eye Jitter Monitor Result
0x0904	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE1	6	R	-	BC Eye Jitter Monitor Result
0x0905	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE2	6	R	-	BC Eye Jitter Monitor Result
0x0906	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE3	6	R	-	BC Eye Jitter Monitor Result
0x0907	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE4	6	R	-	BC Eye Jitter Monitor Result
0x0908	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE5	6	R	-	BC Eye Jitter Monitor Result
0x0909	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE6	6	R	-	BC Eye Jitter Monitor Result
0x090A	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE7	6	R	-	BC Eye Jitter Monitor Result
0x090B	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE8	6	R	-	BC Eye Jitter Monitor Result
0x090C	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE9	6	R	-	BC Eye Jitter Monitor Result
0x090D	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE10	6	R	-	BC Eye Jitter Monitor Result
0x090E	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE11	6	R	-	BC Eye Jitter Monitor Result
0x090F	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE12	6	R	-	BC Eye Jitter Monitor Result
0x0910	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE13	6	R	-	BC Eye Jitter Monitor Result
0x0911	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE14	6	R	-	BC Eye Jitter Monitor Result
0x0912	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE15	6	R	-	BC Eye Jitter Monitor Result
0x0913	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE16	6	R	-	BC Eye Jitter Monitor Result
0x0914	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE17	6	R	-	BC Eye Jitter Monitor Result
0x0915	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE18	6	R	-	BC Eye Jitter Monitor Result
0x0916	[7:6]	reserved	2	-	-	-
	[5:0]	X_EYE19	6	R	-	BC Eye Jitter Monitor Result
0x0917	[7:0]	reserved	8	-	-	-
0x0918	[7:0]	reserved	8	-	-	-
0x0919	[7:0]	reserved	8	-	-	-
0x091A	[7:4]	reserved	4	-	-	-
	[3:0]	FILTSEL	4	R/W	4'h0	VbyOneHSII BC RX Filter setting. 0x0: Set when VbyOneHSII FC rate 1.6Gbps to 4.0Gbps 0x8: Set when VbyOneHSII FC rate 1.5Gbps to 1.6Gbps Other: Reserved
0x091B	[7:0]	reserved	8	-	-	-
0x091C	[7:0]	reserved	8	-	-	-
0x091D	[7:0]	reserved	8	-	-	-
0x091E	[7:0]	reserved	8	-	-	-
0x091F	[7:0]	reserved	8	-	-	-
0x0920	[7:4]	reserved	4	-	-	-
	[3:0]	BC_WDT	4	R/W	4'h2	VbyOneHSII BC WDT time out setting. Time out occurs after 2560×BC_WDT×TTFCBIT×30×2 period
0x0921	[7:0]	reserved	8	-	-	-
0x0922	[7:0]	reserved	8	-	-	-
0x0923	[7:0]	reserved	8	-	-	-
0x0924	[7:0]	reserved	8	-	-	-
0x0925	[7:0]	reserved	8	-	-	-
0x0926	[7:0]	reserved	8	-	-	-
0x0927	[7:0]	reserved	8	-	-	-

0x0B00	[7:2]	reserved	6	-	-	-
	[1:0]	R_2WIRE_PASS_MODE	2	R/W	2'h0	BCC 2-wire basic protocol setting as BCC Master. In BCC 2-wire Pass Through mode1, the specified device IDs are passed through. In BCC 2-wire Pass Through mode2, all device IDs are passed through by default. It can set IDs that are not pass through. In BCC 2-wire Set & Trigger mode, only 2-wire access to the local side is performed to provide remote side register access. It does not require clock stretching, so may be used when the Host 2-write controller does not support clock stretching. 0x0: BCC 2-wire Pass Through mode1 (Address rename) 0x1: BCC 2-wire Pass Through mode2 (All pass through) 0x2: BCC 2-wire Set & Trigger mode 0x3: Reserved
0x0B04	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_PASS_RESEND_EN	1	R/W	1'h0	BCC 2-wire retransmission Enable 0x0:Disable 0x1:Enable
0x0B08	[7:0]	R_2WIRE_PASS_L0_DES_ID	8	R/W	8'hEE	<this regiseters is valid only when 0x0B00=0x0, 0x2> Deserializer 2-wire Device ID for VbyOneHSII Lane0. Default ID is 7'h77 [7:1]: 7bit ID [0] Reserved *It is not allowed the same ID with VbyOneHSII lane1 (R_2WIRE_PASS_L1_DES_ID).
0x0B09	[7:0]	R_2WIRE_PASS_L1_DES_ID	8	R/W	8'hCA	<this regiseters is valid only when 0x0B00=0x0, 0x2> Deserializer 2-wire Device ID for VbyOneHSII Lane1. Default ID is 7'h65 [7:1]: 7bit ID [0] Reserved *It is not allowed the same ID with VbyOneHSII lane0 (R_2WIRE_PASS_L0_DES_ID).
0x0B0A	[7:0]	R_2WIRE_PASS_ADR_BYTE_NUM	8	R/W	8'h1	BCC 2-wire Pass Through / Set & Trigger Sub Address (Word Address) unit Byte number setting. 0x0: 1Byte Sub Address 0x1: 2Byte Sub Address ,,, 0x6: 7Byte Sub Address Others : Reserved [Setting Restriction for remote write is that Unit Address + Unit Data Byte must be at most 8Byte] (R_2WIRE_PASS_ADR_BYTE_NUM +1) + (R_2WIRE_PASS_DATA_BYTE_NUM +1) < 'd(8+1) [Setting Restriction for remote read is that Unit Address or Unit Data Byte must be at most 8Byte respectively] (R_2WIRE_PASS_ADR_BYTE_NUM +1)< 'd(8+1) (R_2WIRE_PASS_DATA_BYTE_NUM +1)< 'd(8+1)
0x0B0B	[7:0]	R_2WIRE_PASS_DATA_BYTE_NUM	8	R/W	8'h0	BCC 2-wire Pass Through / Set & Trigger Divided Write/Read Data unit Byte number setting. Larger unit Byte reduces transaction time of burst read/w rite operation. Unit Byte Number = R_2WIRE_PASS_DATA_BYTE_NUM +1 0x0: 1Byte Data 0x1: 2Byte Data ,,, 0x6: 7Byte Data 0x7: 8Byte Data Others : Reserved [Setting Restriction for remote w rite is that Unit Address + Unit Data Byte must be at most 8Byte] (This rule is more strict on Set and Trigger operation.) (R_2WIRE_PASS_ADR_BYTE_NUM +1) + (R_2WIRE_PASS_DATA_BYTE_NUM +1) < 'd(8+1) [Setting Restriction for remote read is that Unit Address or Unit Data Byte must be at most 8Byte respectively] (R_2WIRE_PASS_ADR_BYTE_NUM +1)< 'd(8+1) (R_2WIRE_PASS_DATA_BYTE_NUM +1)< 'd(8+1)

Address	bit	Register Name	width	R/W	Init	Description
0x0B10	[7:0]	R_2WIRE_PASS1_L0_IN_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID0" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID0" before passing the Deserializer. If "before rename ID0" and "after renamed ID0" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B11	[7:0]	R_2WIRE_PASS1_L0_OUT_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID0" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved
0x0B12	[7:0]	R_2WIRE_PASS1_L0_IN_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID1" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID1" before passing the Deserializer. If "before rename ID1" and "after renamed ID1" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B13	[7:0]	R_2WIRE_PASS1_L0_OUT_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID1" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved
0x0B14	[7:0]	R_2WIRE_PASS1_L0_IN_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID2" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID2" before passing the Deserializer. If "before rename ID2" and "after renamed ID2" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B15	[7:0]	R_2WIRE_PASS1_L0_OUT_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID2" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved
0x0B16	[7:0]	R_2WIRE_PASS1_L0_IN_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID3" of the attached to the remote Deselializer for BCC lane0. This ID will be renamed to "after renamed ID3" before passing the Deserializer. If "before rename ID3" and "after renamed ID3" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved
0x0B17	[7:0]	R_2WIRE_PASS1_L0_OUT_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID3" of the attached to the remote Deselializer for BCC lane0. [7:1] 7bit ID [0] Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0B18	[7:0]	R_2WIRE_PASS1_L1_IN_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID0" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID0" before passing the Deserializer. If "before rename ID0" and "after renamed ID0" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved * This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B19	[7:0]	R_2WIRE_PASS1_L1_OUT_ID0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID0" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved
0x0B1A	[7:0]	R_2WIRE_PASS1_L1_IN_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID1" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID1" before passing the Deserializer. If "before rename ID1" and "after renamed ID1" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved *This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B1B	[7:0]	R_2WIRE_PASS1_L1_OUT_ID1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID1" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved
0x0B1C	[7:0]	R_2WIRE_PASS1_L1_IN_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID2" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID2" before passing the Deserializer. If "before rename ID2" and "after renamed ID2" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved *This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B1D	[7:0]	R_2WIRE_PASS1_L1_OUT_ID2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID2" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved
0x0B1E	[7:0]	R_2WIRE_PASS1_L1_IN_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "before rename ID3" of the attached to the remote Deselializer for BCC lane1. This ID will be renamed to "after renamed ID3" before passing the Deserializer. If "before rename ID3" and "after renamed ID3" are the same, the ID will not be renamed. [7:1] 7bit ID [0] Reserved *This ID is not allowed the same ID with the before rename IDX for lane0. If these are the same ID, will work only lane0.
0x0B1F	[7:0]	R_2WIRE_PASS1_L1_OUT_ID3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x0> 2-wire device address "after renamed ID3" of the attached to the remote Deselializer for BCC lane1. [7:1] 7bit ID [0] Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0B24	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID 0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID0" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane0. [7:1] 7bit ID [0]Reserved
0x0B25	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID 1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID1" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane0. [7:1] 7bit ID [0]Reserved
0x0B26	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID 2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID2" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane0. [7:1] 7bit ID [0]Reserved
0x0B27	[7:0]	R_2WIRE_PASS2_L0_BLOCK_ID 3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID3" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane0. [7:1] 7bit ID [0]Reserved
0x0B28	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID 0	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID0" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane1. [7:1] 7bit ID [0]Reserved
0x0B29	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID 1	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID1" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane1. [7:1] 7bit ID [0]Reserved
0x0B2A	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID 2	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID2" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane1. [7:1] 7bit ID [0]Reserved
0x0B2B	[7:0]	R_2WIRE_PASS2_L1_BLOCK_ID 3	8	R/W	8'h0	<this regiseters is valid only when 0x0B00=0x1> This "Ignore ID3" will be not pass though in BCC 2-wire Pass Through mode2 (All Through) mode for VbyOneHSII lane1. [7:1] 7bit ID [0]Reserved
0x0B2C	[7:0]	R_2WIRE_PASS2_LANE_SEL	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x1> BCC 2-wire Pass Through mode2 (All Through) mode Target VbyOneHSII lane select 0x0: lane0 0x1: lane1 Others: Reserved
0x0B30	[7:0]	R_2WIRE_SETTRIG_DATA0	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA0 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B31	[7:0]	R_2WIRE_SETTRIG_DATA1	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA1 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B32	[7:0]	R_2WIRE_SETTRIG_DATA2	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA2 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B33	[7:0]	R_2WIRE_SETTRIG_DATA3	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA3 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B34	[7:0]	R_2WIRE_SETTRIG_DATA4	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA4 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B35	[7:0]	R_2WIRE_SETTRIG_DATA5	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA5 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B36	[7:0]	R_2WIRE_SETTRIG_DATA6	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA6 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B37	[7:0]	R_2WIRE_SETTRIG_DATA7	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote WRITE DATA7 in BCC 2-wire Set & Trigger mode [7:0] 8bit data

Address	bit	Register Name	width	R/W	Init	Description
0x0B38	[7:0]	R_2WIRE_SETTRIG_DEVID_WR	8	R/W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> Target remote device address in BCC 2-wire Set & Trigger mode. [7:1] 7bit ID [0] read/write select 0x0: Write 0x1: Read
0x0B39	[7:0]	R_2WIRE_SETTRIG_START	8	W	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> "Trigger" option in BCC 2-wire Set & Trigger mode. 0x01 : 2-wire remote access start for "Write" and "Read with Sub-Address" for VbyOneHSII lane0 0x02 : 2-wire remote access start for "Read without Sub-Address" for VbyOneHSII lane0 0x03 : 2-wire remote access start for "Write" and "Read with Sub-Address" for VbyOneHSII lane1 0x04 : 2-wire remote access start for "Read without Sub-Address" for VbyOneHSII lane1 Others : Reserved *It is not allowed to set 0x02 or 0x04 even when 0xB38[0]=0x0.
0x0B40	[7:0]	R_2WIRE_SETTRIG_RDATA0	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA0 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B41	[7:0]	R_2WIRE_SETTRIG_RDATA1	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA1 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B42	[7:0]	R_2WIRE_SETTRIG_RDATA2	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA2 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B43	[7:0]	R_2WIRE_SETTRIG_RDATA3	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA3 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B44	[7:0]	R_2WIRE_SETTRIG_RDATA4	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA4 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B45	[7:0]	R_2WIRE_SETTRIG_RDATA5	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA5 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B46	[7:0]	R_2WIRE_SETTRIG_RDATA6	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA6 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B47	[7:0]	R_2WIRE_SETTRIG_RDATA7	8	R	8'h0	<this regiseters is valid only w hen 0x0B00=0x2> 2-wire remote READ DATA7 in BCC 2-wire Set & Trigger mode [7:0] 8bit data
0x0B50	[7:0]	reserved	8	-	-	-
0x0B51	[7:0]	reserved	8	-	-	-
0x0B60	[7:0]	reserved	8	-	-	-
0x0B61	[7:0]	reserved	8	-	-	-
0x0B68	[7:0]	reserved	8	-	-	-
0x0B69	[7:0]	reserved	8	-	-	-
0x0B6A	[7:1]	reserved	7	-	-	-
	[0]	R_2WIRE_INTERMITTENT_MODE	1	R/W	1'h0	BCC 2-wire Non-divided write/read mode enable. Must be set the same mode with the BCC Slave (Deserializer) side. 0x0: Disable 0x1: Enable

Address	bit	Register Name	width	R/W	Init	Description
0x0C00	[7:6]	reserved	2	-	-	-
	[5]	GPIO0_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C00[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO0_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C00[2:0]=0x1, 0x7> GPIO0 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO0_MODE	3	R/W	3'h0	GPIO0 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programmable GPO (To output GPIO0_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C01	[7:6]	reserved	2	-	-	-
	[5]	GPIO1_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C01[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO1_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C01[2:0]=0x1, 0x7> GPIO1 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO1_MODE	3	R/W	3'h0	GPIO1 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programmable GPO (To output GPIO1_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C02	[7:6]	reserved	2	-	-	-
	[5]	GPIO2_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C02[2:0]=0x0, 0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO2_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C02[2:0]=0x1, 0x7> GPIO2 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO2_MODE	3	R/W	3'h2	GPIO2 I/O Mode setting. 0x0: I2S_D2 input mode 0x1: Programmable GPO (To output GPIO2_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO2_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C03	[7:6]	reserved	2	-	-	-
	[5]	GPIO3_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C03[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	GPIO3_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C03[2:0]=0x1, 0x7> GPIO3 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO3_MODE	3	R/W	3'h2	GPIO3 I/O Mode setting. 0x0: I2S_D3 input mode 0x1: Programmable GPO (To output GPIO3_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to GPIO3_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C04	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO5_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C04[2:0]=0x1> GPIO5_REG output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO5_REG_MODE	3	R/W	3'h2	GPIO5_REG I/O Mode setting. 0x0: I2S_D1 input mode 0x1: Programmable GPO (To output GPIO5_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C05	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO6_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C05[2:0]=0x1> GPIO6_REG output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO6_REG_MODE	3	R/W	3'h2	GPIO6_REG I/O Mode setting. 0x0: I2S_D0 input mode 0x1: Programmable GPO (To output GPIO6_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C06	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO7_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C06[2:0]=0x1> GPIO7_REG output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO7_REG_MODE	3	R/W	3'h2	GPIO7_REG I/O Mode setting. 0x0: I2S_WC input mode 0x1: Programmable GPO (To output GPIO7_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved
0x0C07	[7:6]	reserved	2	-	-	-
	[5]	reserved	1	-	-	
	[4]	reserved	1	-	-	
	[3]	GPIO8_REG_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C07[2:0]=0x1> GPIO8_REG output data slect. 0x0: Low output, 0x1: High output
	[2:0]	GPIO8_REG_MODE	3	R/W	3'h2	GPIO8_REG I/O Mode setting. 0x0: I2S_CLK input mode 0x1: Programmable GPO (To output GPIO8_REG_OUTPUT_VALUE) 0x2: Disable (Hi-Z) 0x3: Monitorable GPI Others: Reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C08	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO0_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C08[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO0_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C08[2:0]=0x1, 0x7> D_GPIO0 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO0_MODE	3	R/W	3'h0	D_GPIO0 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programmable GPO (To output D_GPIO0_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO0_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C09	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO1_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C09[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO1_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C09[2:0]=0x1, 0x7> D_GPIO1 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO1_MODE	3	R/W	3'h0	D_GPIO1 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programmable GPO (To output D_GPIO1_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO1_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C0A	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO2_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C0A[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO2_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C0A[2:0]=0x1, 0x7> D_GPIO2 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO2_MODE	3	R/W	3'h0	D_GPIO2 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programmable GPO (To output D_GPIO2_OUTPUT_VALUE) 0x3: Monitorable GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO2_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C0B	[7:6]	reserved	2	-	-	-
	[5]	D_GPIO3_LANESEL	1	R/W	1'h0	<this regiseters is valid only when 0x0C0B[2:0]=0x5> Through GPO output VbyOneHSII lane select. 0x0: lane0, 0x1: lane1
	[4]	reserved	1	-	-	
	[3]	D_GPIO3_OUTPUT_VALUE	1	R/W	1'h0	<this regiseters is valid only when 0x0C0B[2:0]=0x1, 0x7> D_GPIO3 output data slect. 0x0: Low output, 0x1: High output
	[2:0]	D_GPIO3_MODE	3	R/W	3'h0	D_GPIO3 I/O Mode setting. 0x0: Disable (Hi-Z) 0x1: Programable GPO (To output D_GPIO3_OUTPUT_VALUE) 0x3: Monitoramble GPI and Through GPI Mode (When GPI Mode is activated, buffer type of correspondent GPIOx_OD_MODE register must be set to Push-Pull type) 0x5: Through GPO Mode. Output value is hold when BC CRC error or BCC connection lost occurs. 0x7: Through GPO Mode. Output value is changed to D_GPIO3_OUTPUT_VALUE when BC CRC error or BCC connection lost occurs. Others: Reserved
0x0C0C	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C0D	[7:1]	reserved	7	-	-	-
	[0]	GPIO0_IMON	1	R	1'h0	GPIO0 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C0E	[7:1]	reserved	7	-	-	-
	[0]	GPIO1_IMON	1	R	1'h0	GPIO1 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C0F	[7:1]	reserved	7	-	-	-
	[0]	GPIO2_IMON	1	R	1'h0	GPIO2 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C10	[7:1]	reserved	7	-	-	-
	[0]	GPIO3_IMON	1	R	1'h0	GPIO3 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C11	[7:1]	reserved	7	-	-	-
	[0]	GPIO5_REG_IMON	1	R	1'h0	GPIO5_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C12	[7:1]	reserved	7	-	-	-
	[0]	GPIO6_REG_IMON	1	R	1'h0	GPIO6_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C13	[7:1]	reserved	7	-	-	-
	[0]	GPIO7_REG_IMON	1	R	1'h0	GPIO7_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C14	[7:1]	reserved	7	-	-	-
	[0]	GPIO8_REG_IMON	1	R	1'h0	GPIO8_REG Input Monitor Register 0x0: Low input, 0x01: High input
0x0C15	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO0_IMON	1	R	1'h0	D_GPIO0 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C16	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO1_IMON	1	R	1'h0	D_GPIO1 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C17	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO2_IMON	1	R	1'h0	D_GPIO2 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C18	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO3_IMON	1	R	1'h0	D_GPIO3 Input Monitor Register 0x0: Low input, 0x01: High input
0x0C19	[7:0]	reserved	8	-	-	-
0x0C1A	[7:0]	reserved	8	-	-	-
0x0C1B	[7:0]	reserved	8	-	-	-
0x0C1C	[7:0]	reserved	8	-	-	-
0x0C1D	[7:0]	reserved	8	-	-	-
0x0C1E	[7:0]	reserved	8	-	-	-
0x0C1F	[7:0]	reserved	8	-	-	-
0x0C20	[7:0]	reserved	8	-	-	-
0x0C21	[7:0]	reserved	8	-	-	-
0x0C22	[7:0]	reserved	8	-	-	-
0x0C23	[7:0]	reserved	8	-	-	-
0x0C24	[7:0]	reserved	8	-	-	-
0x0C25	[7:0]	reserved	8	-	-	-
0x0C26	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x0C27	[7:1]	reserved	7	-	-	-
	[0]	GPIO0_OD_MODE	1	R/W	1'h0	GPIO0 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C28	[7:1]	reserved	7	-	-	-
	[0]	GPIO1_OD_MODE	1	R/W	1'h0	GPIO1 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C29	[7:1]	reserved	7	-	-	-
	[0]	GPIO2_OD_MODE	1	R/W	1'h0	GPIO2 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2A	[7:1]	reserved	7	-	-	-
	[0]	GPIO3_OD_MODE	1	R/W	1'h0	GPIO3 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2B	[7:1]	reserved	7	-	-	-
	[0]	GPIO5_REG_OD_MODE	1	R/W	1'h0	GPIO5_REG buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2C	[7:1]	reserved	7	-	-	-
	[0]	GPIO6_REG_OD_MODE	1	R/W	1'h0	GPIO6_REG buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2D	[7:1]	reserved	7	-	-	-
	[0]	GPIO7_REG_OD_MODE	1	R/W	1'h0	GPIO7_REG buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2E	[7:1]	reserved	7	-	-	-
	[0]	GPIO8_REG_OD_MODE	1	R/W	1'h0	GPIO8_REG buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C2F	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO0_OD_MODE	1	R/W	1'h0	D_GPIO0 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C30	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO1_OD_MODE	1	R/W	1'h0	D_GPIO1 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C31	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO2_OD_MODE	1	R/W	1'h0	D_GPIO2 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C32	[7:1]	reserved	7	-	-	-
	[0]	D_GPIO3_OD_MODE	1	R/W	1'h0	D_GPIO3 buffer type select (When GPIOx_MODE is set to GPI, buffer must be Push-pull) 0x0: Push pull, 0x1: Open drain
0x0C33	[7:0]	reserved	8	-	-	-
0x0C34	[7:0]	reserved	8	-	-	-
0x0C35	[7:0]	reserved	8	-	-	-
0x0C36	[7:0]	reserved	8	-	-	-
0x0C37	[7:0]	reserved	8	-	-	-
0x0C38	[7:0]	reserved	8	-	-	-
0x0C39	[7:0]	reserved	8	-	-	-
0x0C3A	[7:0]	reserved	8	-	-	-
0x0C3B	[7:0]	reserved	8	-	-	-
0x0C3C	[7:0]	reserved	8	-	-	-
0x0C3D	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM_FIXMODE	1	R/W	1'h1	BCC Through GPIO select 0x0: Flexible, depending on SMP_GPIOx. 0x1: Fixed, depending on SMP_NUM.

Address	bit	Register Name	width	R/W	Init	Description
0x0C3E	[7:1]	reserved	7	-	-	-
	[0]	SMP_NUM	1	R/W	1'h1	BCC Through GPIO select (When SMP_NUM_FIXMODE=0x1 Fixed.) 0x0: Enable GPIO0-3 only. Sampling rate will be double but disable D_GPIO0-3. 0x1: Enable GPIO0-3 and D_GPIO0-3.
0x0C3F	[7:4]	SMP_GPIO7	4	R/W	4'h0	GPIO_ENCOUT[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[7] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[7] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[7] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[7] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[7] output others:reserved
	[3:0]	SMP_GPIO6	4	R/W	4'h0	GPIO_ENCOUT[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[6] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[6] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[6] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[6] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[6] output others:reserved
0x0C40	[7:4]	SMP_GPIO5	4	R/W	4'h0	GPIO_ENCOUT[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[5] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[5] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[5] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[5] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[5] output others:reserved
	[3:0]	SMP_GPIO4	4	R/W	4'h0	GPIO_ENCOUT[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[4] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[4] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[4] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[4] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[4] output others:reserved
0x0C41	[7:4]	SMP_GPIO3	4	R/W	4'h0	GPIO_ENCOUT[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[3] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[3] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[3] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[3] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[3] output others:reserved
	[3:0]	SMP_GPIO2	4	R/W	4'h0	GPIO_ENCOUT[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[2] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[2] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[2] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[2] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[2] output others:reserved
0x0C42	[7:4]	SMP_GPIO1	4	R/W	4'h0	GPIO_ENCOUT[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[1] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[1] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[1] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[1] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[1] output others:reserved
	[3:0]	SMP_GPIO0	4	R/W	4'h0	GPIO_ENCOUT[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd1:GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd2:GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd3:GPIO3 is Encoded to GPIO_ENCOUT[0] output 4'd4:D_GPIO0 is Encoded to GPIO_ENCOUT[0] output 4'd5:D_GPIO1 is Encoded to GPIO_ENCOUT[0] output 4'd6:D_GPIO2 is Encoded to GPIO_ENCOUT[0] output 4'd7:D_GPIO3 is Encoded to GPIO_ENCOUT[0] output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C43	[7:4]	DESMP_GPIO7	4	R/W	4'h0	GPIO_DECIN[7] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[7] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[7] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[7] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[7] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[7] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[7] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[7] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[7] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO6	4	R/W	4'h0	GPIO_DECIN[6] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[6] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[6] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[6] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[6] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[6] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[6] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[6] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[6] is Decodeded to D_GPIO3 output others:reserved
0x0C44	[7:4]	DESMP_GPIO5	4	R/W	4'h0	GPIO_DECIN[5] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[5] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[5] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[5] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[5] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[5] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[5] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[5] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[5] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO4	4	R/W	4'h0	GPIO_DECIN[4] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[4] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[4] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[4] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[4] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[4] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[4] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[4] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[4] is Decodeded to D_GPIO3 output others:reserved
0x0C45	[7:4]	DESMP_GPIO3	4	R/W	4'h0	GPIO_DECIN[3] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[3] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[3] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[3] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[3] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[3] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[3] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[3] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[3] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO2	4	R/W	4'h0	GPIO_DECIN[2] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[2] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[2] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[2] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[2] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[2] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[2] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[2] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[2] is Decodeded to D_GPIO3 output others:reserved
0x0C46	[7:4]	DESMP_GPIO1	4	R/W	4'h0	GPIO_DECIN[1] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[1] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[1] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[1] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[1] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[1] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[1] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[1] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[1] is Decodeded to D_GPIO3 output others:reserved
	[3:0]	DESMP_GPIO0	4	R/W	4'h0	GPIO_DECIN[0] (When SMP_NUM_FIXMODE=0x0 Flexible.) 4'd0:GPIO_DECIN[0] is Decodeded to GPIO0 output 4'd1:GPIO_DECIN[0] is Decodeded to GPIO1 output 4'd2:GPIO_DECIN[0] is Decodeded to GPIO2 output 4'd3:GPIO_DECIN[0] is Decodeded to GPIO3 output 4'd4:GPIO_DECIN[0] is Decodeded to D_GPIO0 output 4'd5:GPIO_DECIN[0] is Decodeded to D_GPIO1 output 4'd6:GPIO_DECIN[0] is Decodeded to D_GPIO2 output 4'd7:GPIO_DECIN[0] is Decodeded to D_GPIO3 output others:reserved

Address	bit	Register Name	width	R/W	Init	Description
0x0C47	[7:5]	reserved	3	-	-	-
	[4]	reserved	1	-	-	-
	[3]	WDTEN_ERRDET_EN	1	R/W	1'h0	BC WDT Error Detection Enable 0x0: Disable, 0x01: Enable
	[2]	MC_ERRDET_EN	1	R/W	1'h1	BC Manchester Code Error Detection Enable 0x0: Disable, 0x01: Enable
	[1]	LOCK_ERRDET_EN	1	R/W	1'h1	FC and BC Lock Error Detection Enable 0x0: Disable, 0x01: Enable
	[0]	CRC_ERRDET_EN	1	R/W	1'h1	FC and BC CRC Error Detection Enable 0x0: Disable, 0x01: Enable
0x0C48	[7:0]	reserved	8	-	-	-
0x0C49	[7:0]	reserved	8	-	-	-
0x0C4A	[7:0]	reserved	8	-	-	-
0x0C4B	[7:0]	reserved	8	-	-	-
0x0C4C	[7:0]	reserved	8	-	-	-
0x0C4D	[7:0]	reserved	8	-	-	-
0x0C4E	[7:0]	reserved	8	-	-	-
0x0C4F	[7:0]	reserved	8	-	-	-
0x0C50	[7:0]	reserved	8	-	-	-
0x0C51	[7:0]	reserved	8	-	-	-
0x0C52	[7:0]	reserved	8	-	-	-
0x0C53	[7:0]	reserved	8	-	-	-
0x0C54	[7:0]	reserved	8	-	-	-
0x0C55	[7:0]	reserved	8	-	-	-
0x0C56	[7:5]	reserved	3	-	-	-
	[4:0]	GPIO_PULLDOWN_UPPER	5	R/W	5'h0	GPIO Pull down setting-1. 0x0: Disable, 0x1: Enable [4]: Reserved [3]: D_GPIO3 [2]: D_GPIO2 [1]: D_GPIO1 [0]: D_GPIO0
0x0C57	[7:0]	GPIO_PULLDOWN_LOWER	8	R/W	8'h0	GPIO Pull down setting-2. 0x0: Disable, 0x1: Enable [7]: GPIO8_REG [6]: GPIO7_REG [5]: GPIO6_REG [4]: GPIO5_REG [3]: GPIO3 [2]: GPIO2 [1]: GPIO1 [0]: GPIO0

Address	bit	Register Name	width	R/W	Init	Description
0x1000	[7:0]	reserved	8	-	-	-
0x1001	[7:0]	reserved	8	-	-	-
0x1002	[7:1]	reserved	7	-	-	-
	[0]	FSBP_DTH_EN	1	R/W	1'h1	VbyOneHSII Controll Data Through Select. It also should be set disable when connect to VbyOneHS protocol Deserializer. 0x0: Disable 0x1: Enable, Normal operation

Address	bit	Register Name	width	R/W	Init	Description
0x1200	[7:1]	reserved	7	-	-	-
	[0]	CLR	1	W	-	Checksum clear 0x1: clear
0x1201	[7:1]	reserved	7	-	-	-
	[0]	EN	1	R/W	1'h0	Checksum Enable 0x0: Disable, 0x1: Enable
0x1202	[7:0]	TIMER	8	R/W	8'h0	Checksum diagnosis interval setting. 1024 x 64 x (N+THIMER[7:0]) x OSC cycle Valid 820us ~ 210ms when OSC is typical value
0x1203	[7:0]	VAL	8	R/W	8'h9F	Checksum calculation pass/fail target setting
0x1204	[7:0]	RES	8	R	8'h0	Checksum calculation result
0x1210	[7:0]	reserved	8	-	-	-
0x1211	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1300	[7:4]	reserved	4	-	-	-
	[3:2]	INTN_REM_BYPASS	2	R/W	2'h0	INTN pin output select. INTN pin will mirror the status of INTN_IN on the Deserializer when set 0x0 and 0x1. It also outputs the enabled Interrupt signal when set to 0x2. 0x0: Mirror VbyOneHSII lane0 0x1: Mirror VbyOneHSII lane1 0x2: Intrrupt output 0x3: Reserved
	[1:0]	INTN_MODE	2	R/W	2'h1	INTN pin output mode select 0x0: Disable 0x1: Open drain 0x2: Push pull, Low Active 0x3: Push pull, High Active
0x1301	[7:0]	reserved	8	-	-	-
0x1302	[7:0]	reserved	8	-	-	-
0x1303	[7:0]	reserved	8	-	-	-
0x1304	[7:2]	reserved	6	-	-	-
	[1]	INTN_M_CLEAR	1	W	-	INTN Mask all clear. Interrupt Mask settings will be disable. 0x1: clear
	[0]	INTN_S_CLEAR	1	W	-	INTN Interrupt all clear. Interrupt statuses will be clear. 0x1: clear

Address	bit	Register Name	width	R/W	Init	Description
0x1310	[7:1]	reserved	7	-	-	-
	[0]	INTN_LOCK	1	R/W1C	1'h0	PLL Lock Detect 0x0: No interrupt, 0x1: Interrupt
0x1311	[7]	INTN_ERR_OSCOUTU	1	R/W1C	1'h0	Internal OSC Clockout Upper Error 0x0: No interrupt, 0x1: Interrupt
	[6]	INTN_ERR_OSCOUTL	1	R/W1C	1'h0	Internal OSC Clockout Low er Error 0x0: No interrupt, 0x1: Interrupt
	[5]	INTN_ERR_PLLOUTU	1	R/W1C	1'h0	PLL Clock Upper Error 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_ERR_PLLOUTL	1	R/W1C	1'h0	PLL Clock Low er Error 0x0: No interrupt, 0x1: Interrupt
	[3]	reserved	1	-	-	-
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_RX0CHU	1	R/W1C	1'h0	LVDS RX Clock Upper Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_RX0CHL	1	R/W1C	1'h0	LVDS RX Clock Lower Error 0x0: No interrupt, 0x1: Interrupt
0x1312	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1313	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_E	1	R/W1C	1'h0	LVDS Channel E PRBS Check Error 0x0: No interrupt, 0x1: Interrupt
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_A	1	R/W1C	1'h0	LVDS Channel A PRBS Check Error 0x0: No interrupt, 0x1: Interrupt
0x1314	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETA	1	R/W1C	1'h0	Hiz detector indicate signal for LVDS input 0x0: No interrupt, 0x1: Interrupt
0x1315	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETCLK	1	R/W1C	1'h0	Hiz detector indicate signal for LVDS input 0x0: No interrupt, 0x1: Interrupt
0x1316	[7:5]	reserved	3	-	-	-
	[4]	INTN_DETE_VDD	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input 0x0: No interrupt, 0x1: Interrupt
	[3:1]	reserved	3	-	-	-
	[0]	INTN_DETA_VDD	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input 0x0: No interrupt, 0x1: Interrupt
0x1317	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETCLK_VDD	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input 0x0: No interrupt, 0x1: Interrupt
0x1318	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETA_GND	1	R/W1C	1'h0	GND Level detector indicate signal for LVDS input 0x0: No interrupt, 0x1: Interrupt
0x1319	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETCLK_GND	1	R/W1C	1'h0	GND Level detector indicate signal for LVDS input 0x0: No interrupt, 0x1: Interrupt
0x131A	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETLAT	1	R/W1C	1'h0	LVDSCLK input level error Latch 0x0: No interrupt, 0x1: Interrupt
0x131B	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR0	1	R/W1C	1'h0	LVDS0 Input CRC Error 0x0: No interrupt, 0x1: Interrupt
0x131C	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR	1	R/W1C	1'h0	Forward Channel FIFO Error 0x0: No interrupt, 0x1: Interrupt
0x131D	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH	1	R/W1C	1'h0	LVDS Domain PATCHK VSYNCWIDTH Error 0x0: No interrupt, 0x1: Interrupt
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_VTOTAL	1	R/W1C	1'h0	LVDS Domain PATCHK VTOTAL Error 0x0: No interrupt, 0x1: Interrupt
0x131E	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_EVENRGB	1	R/W1C	1'h0	LVDS Domain PATCHK EVEN RGB Error 0x0: No interrupt, 0x1: Interrupt
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_HBLANK	1	R/W1C	1'h0	LVDS Domain PATCHK HBLANK Error 0x0: No interrupt, 0x1: Interrupt
0x131F	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH_FC	1	R/W1C	1'h0	FC Domain PATCHK VSYNCWIDTH Error 0x0: No interrupt, 0x1: Interrupt
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_VTOTAL_FC	1	R/W1C	1'h0	FC Domain PATCHK VTOTAL Error 0x0: No interrupt, 0x1: Interrupt

Address	bit	Register Name	width	R/W	Init	Description
0x1320	[7:0]	reserved	8	-	-	-
0x1321	[7]	INTN_FC_CRC	1	R/W1C	1'h0	VbyOneHSII FC CRC Error 0x0: No interrupt, 0x1: Interrupt
	[6]	INTN_REMDEVICE_NACK	1	R/W1C	1'h0	Remote device attached to Deselializer NACK Error 0x0: No interrupt, 0x1: Interrupt
	[5]	INTN_REMDEVICE_TIMEOUT	1	R/W1C	1'h0	Remote device attached to Deselializer Time Out Error 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_DONE_TRANS	1	R/W1C	1'h0	2-wire bridge Access Complete Flag 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_FAIL_TRANS	1	R/W1C	1'h0	2-wire bridge Access Fail Flag 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_ERR_CRC	1	R/W1C	1'h0	VbyOneHSII BCC CRC Error 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_TIMEOUT_BRIDGE_TRANS	1	R/W1C	1'h0	2-write bridge Time Out Error 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_TIMEOUT_SLAVE	1	R/W1C	1'h0	Local 2-wire Time Out Error 0x0: No interrupt, 0x1: Interrupt
0x1322	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR	1	R/W1C	1'h0	Register CheckSum Error 0x0: No interrupt, 0x1: Interrupt
0x1323	[7:0]	reserved	8	-	-	-
0x1324	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L0	1	R	1'h0	VbyOneHSII FC/BC Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_CTRL_THRIO_FCDATA_L0	1	R	1'h0	Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_GPIO_VALID0_L0	1	R	1'h0	VbyOneHSII FC Through I/O data valid Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_REM_L0	1	R	1'h0	Remote Deserializer Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
0x1325	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1326	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L0	1	R/W1C	1'h0	VbyOneHSII BC Buffer Write Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_CRC_OCLK_L0	1	R/W1C	1'h0	VbyOneHSII BC OCLK domain CRC Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_CRC_VCLK_L0	1	R/W1C	1'h0	VbyOneHSII BC VCLK domain CRC Error for lane0 0x0: No interrupt, 0x1: Interrupt
0x1327	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC/BC Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
	[2]	INTN_CTRL_THRIO_FCDATA_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_GPIO_VALID0_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC Through I/O data valid Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_REM_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> Remote Deserializer Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
0x1328	[7:0]	reserved	8	-	-	-
0x1329	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC Buffer Write Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[1]	INTN_ERR_CRC_OCLK_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC OCLK domain CRC Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	INTN_ERR_CRC_VCLK_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC VCLK domain CRC Error for lane1 0x0: No interrupt, 0x1: Interrupt
0x132A	[7:6]	reserved	2	-	-	-
	[5]	INTN_THRIO_VALID_L0	1	R/W1C	1'h0	VbyOneHSII FC/BC Through I/O Valid Status for lane0 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_UNLOCK_VX1_L0	1	R/W1C	1'h0	VbyOneHSII FC Unlock Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_MC_L0	1	R/W1C	1'h0	VbyOneHSII BC Manchester Code Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x132B	[7:0]	reserved	8	-	-	-
	[5]	INTN_THRIO_VALID_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC/BC Through I/O Valid Status for lane1 0x0: No interrupt, 0x1: Interrupt
	[4]	INTN_UNLOCK_VX1_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC Unlock Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[3]	INTN_ERR_MC_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC Manchester Code Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x132C	[7:0]	reserved	8	-	-	-
0x132D	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1350	[7:1]	reserved	7	-	-	-
	[0]	INTN_LOCK_M	1	R/W	1'h1	PLL Lock Detect Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1351	[7]	INTN_ERR_OSCOUTU_M	1	R/W	1'h1	Internal OSC Clockout Upper Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	INTN_ERR_OSCOUTL_M	1	R/W	1'h1	Internal OSC Clockout Low er Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	INTN_ERR_PLLOUTU_M	1	R/W	1'h1	PLL Clock Upper Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	INTN_ERR_PLLOUTL _M	1	R/W	1'h1	PLL Clock Low er Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	reserved	1	-	-	-
	[2]	reserved	1	-	-	-
	[1]	INTN_ERR_RX0CHU_M	1	R/W	1'h1	LVDS RX Clock Upper Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_RX0CHL_M	1	R/W	1'h1	LVDS RX Clock Lower Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1352	[7:0]	reserved	8	-	-	-
0x1353	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_E_M	1	R/W1C	1'h0	LVDS Channel E PRBS Check Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_A_M	1	R/W1C	1'h0	LVDS Channel A PRBS Check Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1354	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETA_M	1	R/W1C	1'h0	Hiz detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1355	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETCLK_M	1	R/W1C	1'h0	Hiz detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1356	[7:5]	reserved	3	-	-	-
	[4]	INTN_DETE_VDD_M	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	INTN_DETA_VDD_M	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1357	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETCLK_VDD_M	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1358	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETA_GND_M	1	R/W1C	1'h0	GND Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1359	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETCLK_GND_M	1	R/W1C	1'h0	GND Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x135A	[7:1]	reserved	7	-	-	-
	[0]	INTN_DETLAT_M	1	R/W1C	1'h0	LVDSCLK input level error Latch Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor

Address	bit	Register Name	width	R/W	Init	Description
0x135B	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR0_M	1	R/W1C	1'h0	LVDS0 Input CRC Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x135C	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR_M	1	R/W1C	1'h0	Forward Channel FIFO Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x135D	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH_M	1	R/W1C	1'h0	LVDS Domain PATCHK VSYNCWIDTH Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_VTOTAL_M	1	R/W1C	1'h0	LVDS Domain PATCHK VTOTAL Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x135E	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_EVENRGB_M	1	R/W1C	1'h0	LVDS Domain PATCHK EVEN RGB Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_HBLANK_M	1	R/W1C	1'h0	LVDS Domain PATCHK HBLANK Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x135F	[7:5]	reserved	3	-	-	-
	[4]	INTN_ERR_VSYNCWIDTH_FC_M	1	R/W1C	1'h0	FC Domain PATCHK VSYNCWIDTH Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	INTN_ERR_VTOTAL_FC_M	1	R/W1C	1'h0	FC Domain PATCHK VTOTAL Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1360	[7:0]	reserved	8	-	-	-
0x1361	[7]	INTN_FC_CRC_M	1	R/W	1'h1	VbyOneHSII FC CRC Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	INTN_REMDEVICE_NACK_M	1	R/W	1'h1	Remote device attached to Deselializer NACK Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	INTN_REMDEVICE_TIMEOUT_M	1	R/W	1'h1	Remote device attached to Deselializer Time Out Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	INTN_DONE_TRANS_M	1	R/W	1'h1	2-wire bridge Access Complete Flag Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_FAIL_TRANS_M	1	R/W	1'h1	2-wire bridge Access Fail Flag Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_ERR_CRC_M	1	R/W	1'h1	VbyOneHSII BCC CRC Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_TIMEOUT_BRIDGE_TRANS_M	1	R/W	1'h1	2-write bridge Time Out Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_TIMEOUT_SLAVE_M	1	R/W	1'h1	Local 2-wire Time Out Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1362	[7:1]	reserved	7	-	-	-
	[0]	INTN_ERR_M	1	R/W	1'h1	Register CheckSum Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1363	[7:0]	reserved	8	-	-	-
0x1364	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L0_M	1	R/W	1'h1	VbyOneHSII FC/BC Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_CTRL_THRIO_FCDATA_L0_M	1	R/W	1'h1	Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_GPIO_VALID0_L0_M	1	R/W	1'h1	VbyOneHSII FC Through I/O data valid Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_REM_L0_M	1	R/W	1'h1	Remote Deserializer Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1365	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1366	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L0_M	1	R/W	1'h1	VbyOneHSII BC Buffer Write Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_CRC_OCLK_L0_M	1	R/W	1'h1	VbyOneHSII BC OCLK domain CRC Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_CRC_VCLK_L0_M	1	R/W	1'h1	VbyOneHSII BC VCLK domain CRC Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1367	[7:4]	reserved	4	-	-	-
	[3]	INTN_FC_BC_LINK_L1_M	1	R/W	1'h1	VbyOneHSII FC/BC Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	INTN_CTRL_THRIO_FCDATA_L1_M	1	R/W	1'h1	Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_GPIO_VALID0_L1_M	1	R/W	1'h1	VbyOneHSII FC Through I/O data valid Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_REM_L1_M	1	R/W	1'h1	Remote Deserializer Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1368	[7:0]	reserved	8	-	-	-
0x1369	[7:3]	reserved	5	-	-	-
	[2]	INTN_ERR_WRITE_L1_M	1	R/W	1'h1	VbyOneHSII BC Buffer Write Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	INTN_ERR_CRC_OCLK_L1_M	1	R/W	1'h1	VbyOneHSII BC OCLK domain CRC Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	INTN_ERR_CRC_VCLK_L1_M	1	R/W	1'h1	VbyOneHSII BC VCLK domain CRC Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x136A	[7:6]	reserved	2	-	-	-
	[5]	INTN_THRIO_VALID_L0_M	1	R/W	1'h1	VbyOneHSII FC/BC Through I/O Valid Status for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	INTN_UNLOCK_VX1_L0_M	1	R/W	1'h1	VbyOneHSII FC Unlock Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_MC_L0_M	1	R/W	1'h1	VbyOneHSII BC Manchester Code Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x136B	[7:6]	reserved	2	-	-	-
	[5]	INTN_THRIO_VALID_L1_M	1	R/W	1'h1	VbyOneHSII FC/BC Through I/O Valid Status for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	INTN_UNLOCK_VX1_L1_M	1	R/W	1'h1	VbyOneHSII FC Unlock Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	INTN_ERR_MC_L1_M	1	R/W	1'h1	VbyOneHSII BC Manchester Code Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x136C	[7:0]	reserved	8	-	-	-
0x136D	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1400	[7:4]	reserved	4	-	-	-
	[3:2]	REM_INTN_REM_BYPASS	2	R/W	2'h0	REM_INTN pin output select. REM_INTN pin will mirror the status of INTN_IN on the Deserializer when set 0x0 and 0x1. It also outputs the enabled Interrupt signal when set to 0x2. 0x0: Mirror VbyOneHSII lane0 0x1: Mirror VbyOneHSII lane1 0x2: Intrrupt output 0x3: Reserved
	[1:0]	REM_INTN_MODE	2	R/W	2'h1	REM_INTN pin output mode select 0x0: Disable 0x1: Open drain 0x2: Push pull, Low Active 0x3: Push pull, High Active
0x1401	[7:0]	reserved	8	-	-	-
0x1402	[7:0]	reserved	8	-	-	-
0x1403	[7:4]	reserved	4	-	-	-
	[3:0]	REM_INTN_FILT_RANGE	4	R/W	4'h1	Back Channel INT Filter Range 0x0: Disable Others: REM_INTN_FILT_RANGE * 1280 * TTFCBIT *30 is pulse filter threshold.
0x1404	[7:2]	reserved	6	-	-	-
	[1]	REM_INTN_M_CLEAR	1	W	-	REM_INTN Mask all clear. Interrupt Mask settings will be disable. 0x1: clear
	[0]	REM_INTN_S_CLEAR	1	W	-	REM_INTN Interrupt all clear. Interrupt statuses will be clear. 0x1: clear

Address	bit	Register Name	width	R/W	Init	Description
0x1410	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_LOCK	1	R/W1C	1'h0	PLL Lock Detect 0x0: No interrupt, 0x1: Interrupt
0x1411	[7]	REM_INTN_ERR_OSCOUTU	1	R/W1C	1'h0	Internal OSC Clockout Upper Error 0x0: No interrupt, 0x1: Interrupt
	[6]	REM_INTN_ERR_OSCOUTL	1	R/W1C	1'h0	Internal OSC Clockout Low er Error 0x0: No interrupt, 0x1: Interrupt
	[5]	REM_INTN_ERR_PLLOUTU	1	R/W1C	1'h0	PLL Clock Upper Error 0x0: No interrupt, 0x1: Interrupt
	[4]	REM_INTN_ERR_PLLOUTL	1	R/W1C	1'h0	PLL Clock Low er Error 0x0: No interrupt, 0x1: Interrupt
	[3]	reserved	1	-	-	-
	[2]	reserved	1	-	-	-
	[1]	REM_INTN_ERR_RX0CHU	1	R/W1C	1'h0	LVDS RX Clock Upper Error 0x0: No interrupt, 0x1: Interrupt
	[0]	REM_INTN_ERR_RX0CHL	1	R/W1C	1'h0	LVDS RX Clock Lower Error 0x0: No interrupt, 0x1: Interrupt
0x1413	[7:0]	reserved	8	-	-	-
0x1414	[7:0]	reserved	8	-	-	-
0x1415	[7:0]	reserved	8	-	-	-
0x1416	[7:0]	reserved	8	-	-	-
0x1417	[7:0]	reserved	8	-	-	-
0x1418	[7:0]	reserved	8	-	-	-
0x1419	[7:0]	reserved	8	-	-	-
0x141A	[7:0]	reserved	8	-	-	-
0x141B	[7:0]	reserved	8	-	-	-
0x141C	[7:0]	reserved	8	-	-	-
0x141D	[7:0]	reserved	8	-	-	-
0x141E	[7:0]	reserved	8	-	-	-
0x141F	[7:0]	reserved	8	-	-	-
0x1420	[7:0]	reserved	8	-	-	-
0x1421	[7]	REM_INTN_FC_CRC	1	R/W1C	1'h0	VbyOneHSII FC CRC Error 0x0: No interrupt, 0x1: Interrupt
	[6]	REM_INTN_REMDEVICE_NACK	1	R/W1C	1'h0	Remote device attached to Deselializer NACK Error 0x0: No interrupt, 0x1: Interrupt
	[5]	REM_INTN_REMDEVICE_TIMEOUT	1	R/W1C	1'h0	Remote device attached to Deselializer Time Out Error 0x0: No interrupt, 0x1: Interrupt
	[4]	REM_INTN_DONE_TRANS	1	R/W1C	1'h0	2-wire bridge Access Complete Flag 0x0: No interrupt, 0x1: Interrupt
	[3]	REM_INTN_FAIL_TRANS	1	R/W1C	1'h0	2-wire bridge Access Fail Flag 0x0: No interrupt, 0x1: Interrupt
	[2]	REM_INTN_ERR_CRC	1	R/W1C	1'h0	VbyOneHSII BCC CRC Error 0x0: No interrupt, 0x1: Interrupt
	[1]	REM_INTN_TIMEOUT_BRIDGE_TRANS	1	R/W1C	1'h0	2-write bridge Time Out Error 0x0: No interrupt, 0x1: Interrupt
	[0]	REM_INTN_TIMEOUT_SLAVE	1	R/W1C	1'h0	Local 2-wire Time Out Error 0x0: No interrupt, 0x1: Interrupt
0x1422	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_ERR	1	R/W1C	1'h0	Register CheckSum Error 0x0: No interrupt, 0x1: Interrupt
0x1423	[7:0]	reserved	8	-	-	-
0x1424	[7:4]	reserved	4	-	-	-
	[3]	REM_INTN_FC_BC_LINK_L0	1	R	1'h0	VbyOneHSII FC/BC Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
	[2]	REM_INTN_CTRL_THRIO_FCDATA_L0	1	R	1'h0	Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
	[1]	REM_INTN_GPIO_VALID0_L0	1	R	1'h0	VbyOneHSII FC Through I/O data valid Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	REM_INTN_REM_L0	1	R	1'h0	Remote Deserializer Interrupt for lane0 0x0: No interrupt, 0x1: Interrupt
0x1425	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1426	[7:3]	reserved	5	-	-	-
	[2]	REM_INTN_ERR_WRITE_L0	1	R/W1C	1'h0	VbyOneHSII BC Buffer Write Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[1]	REM_INTN_ERR_CRC_OCLK_L0	1	R/W1C	1'h0	VbyOneHSII BC OCLK domain CRC Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[0]	REM_INTN_ERR_CRC_VCLK_L0	1	R/W1C	1'h0	VbyOneHSII BC VCLK domain CRC Error for lane0 0x0: No interrupt, 0x1: Interrupt
0x1427	[7:4]	reserved	4	-	-	-
	[3]	REM_INTN_FC_BC_LINK_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC/BC Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
	[2]	REM_INTN_CTRL_THRIO_FCDATA_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
	[1]	REM_INTN_GPIO_VALID0_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC Through I/O data valid Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	REM_INTN_REM_L1	1	R	1'h0	<Valid only when VbyOneHSII Distribution mode> Remote Deserializer Interrupt for lane1 0x0: No interrupt, 0x1: Interrupt
0x1428	[7:0]	reserved	8	-	-	-
0x1429	[7:3]	reserved	5	-	-	-
	[2]	REM_INTN_ERR_WRITE_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC Buffer Write Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[1]	REM_INTN_ERR_CRC_OCLK_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC OCLK domain CRC Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[0]	REM_INTN_ERR_CRC_VCLK_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC VCLK domain CRC Error for lane1 0x0: No interrupt, 0x1: Interrupt
0x142A	[7:6]	reserved	2	-	-	-
	[5]	REM_INTN_THRIO_VALID_L0	1	R/W1C	1'h0	VbyOneHSII FC/BC Through I/O Valid Status for lane0 0x0: No interrupt, 0x1: Interrupt
	[4]	REM_INTN_UNLOCK_VX1_L0	1	R/W1C	1'h0	VbyOneHSII FC Unlock Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[3]	REM_INTN_ERR_MC_L0	1	R/W1C	1'h0	VbyOneHSII BC Manchester Code Error for lane0 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x142B	[7:0]	reserved	8	-	-	-
	[5]	REM_INTN_THRIO_VALID_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC/BC Through I/O Valid Status for lane1 0x0: No interrupt, 0x1: Interrupt
	[4]	REM_INTN_UNLOCK_VX1_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII FC Unlock Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[3]	REM_INTN_ERR_MC_L1	1	R/W1C	1'h0	<Valid only when VbyOneHSII Distribution mode> VbyOneHSII BC Manchester Code Error for lane1 0x0: No interrupt, 0x1: Interrupt
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x142C	[7:0]	reserved	8	-	-	-
0x142D	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1450	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_LOCK_M	1	R/W	1'h1	PLL Lock Detect Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1451	[7]	REM_INTN_ERR_OSCOUTU_M	1	R/W	1'h1	Internal OSC Clockout Upper Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	REM_INTN_ERR_OSCOUTL_M	1	R/W	1'h1	Internal OSC Clockout Low er Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	REM_INTN_ERR_PLLOUTU_M	1	R/W	1'h1	PLL Clock Upper Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	REM_INTN_ERR_PLLOUTL _M	1	R/W	1'h1	PLL Clock Low er Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	reserved	1	-	-	-
	[2]	reserved	1	-	-	-
	[1]	REM_INTN_ERR_RX0CHU_M	1	R/W	1'h1	LVDS RX Clock Upper Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	REM_INTN_ERR_RX0CHL_M	1	R/W	1'h1	LVDS RX Clock Lower Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1452	[7:0]	reserved	8	-	-	-
0x1453	[7:5]	reserved	3	-	-	-
	[4]	REM_INTN_ERR_E_M	1	R/W1C	1'h0	LVDS Channel E PRBS Check Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	REM_INTN_ERR_A_M	1	R/W1C	1'h0	LVDS Channel A PRBS Check Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1454	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_DETA_M	1	R/W1C	1'h0	Hiz detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1455	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_DETCLK_M	1	R/W1C	1'h0	Hiz detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1456	[7:5]	reserved	3	-	-	-
	[4]	REM_INTN_DETE_VDD_M	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	REM_INTN_DETA_VDD_M	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1457	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_DETCLK_VDD_M	1	R/W1C	1'h0	VDD Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1458	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_DETA_GND_M	1	R/W1C	1'h0	GND Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1459	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_DETCLK_GND_M	1	R/W1C	1'h0	GND Level detector indicate signal for LVDS input Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x145A	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_DETLAT_M	1	R/W1C	1'h0	LVDSCLK input level error Latch Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor

Address	bit	Register Name	width	R/W	Init	Description
0x145B	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_ERR0_M	1	R/W1C	1'h0	LVDS0 Input CRC Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x145C	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_ERR_M	1	R/W1C	1'h0	Forward Channel FIFO Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x145D	[7:5]	reserved	3	-	-	-
	[4]	REM_INTN_ERR_VSYNCWIDTH_M	1	R/W1C	1'h0	LVDS Domain PATCHK VSYNCWIDTH Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	REM_INTN_ERR_VTOTAL_M	1	R/W1C	1'h0	LVDS Domain PATCHK VTOTAL Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x145E	[7:5]	reserved	3	-	-	-
	[4]	REM_INTN_ERR_EVENRGB_M	1	R/W1C	1'h0	LVDS Domain PATCHK EVEN RGB Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	REM_INTN_ERR_HBLANK_M	1	R/W1C	1'h0	LVDS Domain PATCHK HBLANK Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x145F	[7:5]	reserved	3	-	-	-
	[4]	REM_INTN_ERR_VSYNCWIDTH_FC_M	1	R/W1C	1'h0	FC Domain PATCHK VSYNCWIDTH Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3:1]	reserved	3	-	-	-
	[0]	REM_INTN_ERR_VTOTAL_FC_M	1	R/W1C	1'h0	FC Domain PATCHK VTOTAL Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1460	[7:0]	reserved	8	-	-	-
0x1461	[7]	REM_INTN_FC_CRC_M	1	R/W	1'h1	VbyOneHSII FC CRC Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[6]	REM_INTN_REMDEVICE_NACK_M	1	R/W	1'h1	Remote device attached to Deselializer NACK Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[5]	REM_INTN_REMDEVICE_TIMEOUT_M	1	R/W	1'h1	Remote device attached to Deselializer Time Out Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	REM_INTN_DONE_TRANS_M	1	R/W	1'h1	2-wire bridge Access Complete Flag Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	REM_INTN_FAIL_TRANS_M	1	R/W	1'h1	2-wire bridge Access Fail Flag Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	REM_INTN_ERR_CRC_M	1	R/W	1'h1	VbyOneHSII BCC CRC Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	REM_INTN_TIMEOUT_BRIDGE_TRANS_M	1	R/W	1'h1	2-write bridge Time Out Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	REM_INTN_TIMEOUT_SLAVE_M	1	R/W	1'h1	Local 2-wire Time Out Error Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1462	[7:1]	reserved	7	-	-	-
	[0]	REM_INTN_ERR_M	1	R/W	1'h1	Register CheckSum Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1463	[7:0]	reserved	8	-	-	-
0x1464	[7:4]	reserved	4	-	-	-
	[3]	REM_INTN_FC_BC_LINK_L0_M	1	R/W	1'h1	VbyOneHSII FC/BC Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	REM_INTN_CTRL_THRIO_FCDATA_L0_M	1	R/W	1'h1	Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	REM_INTN_GPIO_VALID0_L0_M	1	R/W	1'h1	VbyOneHSII FC Through I/O data valid Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	REM_INTN_REM_L0_M	1	R/W	1'h1	Remote Deserializer Interrupt for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1465	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1466	[7:3]	reserved	5	-	-	-
	[2]	REM_INTN_ERR_WRITE_L0_M	1	R/W	1'h1	VbyOneHSII BC Buffer Write Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	REM_INTN_ERR_CRC_OCLK_L0_M	1	R/W	1'h1	VbyOneHSII BC OCLK domain CRC Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	REM_INTN_ERR_CRC_VCLK_L0_M	1	R/W	1'h1	VbyOneHSII BC VCLK domain CRC Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1467	[7:4]	reserved	4	-	-	-
	[3]	REM_INTN_FC_BC_LINK_L1_M	1	R/W	1'h1	VbyOneHSII FC/BC Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	REM_INTN_CTRL_THRIO_FCDATA_L1_M	1	R/W	1'h1	Remote Deserializer Chip Control, FC/BC Through I/O Interrupt, FC data packer Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	REM_INTN_GPIO_VALID0_L1_M	1	R/W	1'h1	VbyOneHSII FC Through I/O data valid Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	REM_INTN_REM_L1_M	1	R/W	1'h1	Remote Deserializer Interrupt for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x1468	[7:0]	reserved	8	-	-	-
0x1469	[7:3]	reserved	5	-	-	-
	[2]	REM_INTN_ERR_WRITE_L1_M	1	R/W	1'h1	VbyOneHSII BC Buffer Write Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[1]	REM_INTN_ERR_CRC_OCLK_L1_M	1	R/W	1'h1	VbyOneHSII BC OCLK domain CRC Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[0]	REM_INTN_ERR_CRC_VCLK_L1_M	1	R/W	1'h1	VbyOneHSII BC VCLK domain CRC Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
0x146A	[7:6]	reserved	2	-	-	-
	[5]	REM_INTN_THRIO_VALID_L0_M	1	R/W	1'h1	VbyOneHSII FC/BC Through I/O Valid Status for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	REM_INTN_UNLOCK_VX1_L0_M	1	R/W	1'h1	VbyOneHSII FC Unlock Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	REM_INTN_ERR_MC_L0_M	1	R/W	1'h1	VbyOneHSII BC Manchester Code Error for lane0 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x146B	[7:6]	reserved	2	-	-	-
	[5]	REM_INTN_THRIO_VALID_L1_M	1	R/W	1'h1	VbyOneHSII FC/BC Through I/O Valid Status for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[4]	REM_INTN_UNLOCK_VX1_L1_M	1	R/W	1'h1	VbyOneHSII FC Unlock Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[3]	REM_INTN_ERR_MC_L1_M	1	R/W	1'h1	VbyOneHSII BC Manchester Code Error for lane1 Mask 0x0: Apply interrupt factor for INTN pin, 0x1: Mask interrupt factor
	[2]	reserved	1	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x146C	[7:0]	reserved	8	-	-	-
0x146D	[7:0]	reserved	8	-	-	-

Address	bit	Register Name	width	R/W	Init	Description
0x1C00	[7]	reserved	1	-	-	-
	[6:0]	MON0	7	R/W	7'h0	MON0 pin debug output select. See MONitor configuration table.
0x1C01	[7]	reserved	1	-	-	-
	[6:0]	MON1	7	R/W	7'h0	MON1 pin debug output select. See MONitor configuration table.
0x1C02	[7:0]	EXTRA_GPIO0_IOSEL	8	R/W	8'h0	GPIO0 pin extra/external input select. 0x00: Normal operation 0x03: LOCKN input mode for VbyOneHS lane0 Others: reserved
0x1C03	[7:0]	EXTRA_GPIO1_IOSEL	8	R/W	8'h0	GPIO1 pin extra/internal clock output select. 0x00: Normal operation 0x11: Internal OSC clock output 0x12: VbyOneHSII BC Clock output 0x13: VbyOneHSII FC Pixel Clock output 0x14: LVDS Clock output Others: reserved
0x1C04	[7:0]	EXTRA_GPIO2_IOSEL	8	R/W	8'h0	GPIO2 pin extra/internal clock output select. 0x00: Normal operation 0x11: Internal OSC clock output 0x12: VbyOneHSII BC Clock output 0x13: VbyOneHSII FC Pixel Clock output 0x14: LVDS Clock output Others: reserved
0x1C05	[7:0]	EXTRA_GPIO3_IOSEL	8	R/W	8'h0	GPIO3 pin extra/internal clock output select. 0x00: Normal operation 0x11: Internal OSC clock output 0x12: VbyOneHSII BC Clock output 0x13: VbyOneHSII FC Pixel Clock output 0x14: LVDS Clock output Others: reserved
0x1C06	[7:0]	EXTRA_GPIO5_REG_IOSEL	8	R/W	8'h0	GPIO5_REG pin extra/external input select. 0x00: Normal operation 0x04: LOCKN input mode for VbyOneHS lane1 Others: reserved
0x1C07	[7:0]	reserved	8	-	-	-
0x1C08	[7:0]	reserved	8	-	-	-
0x1C09	[7:0]	reserved	8	-	-	-
0x1C0A	[7:0]	reserved	8	-	-	-
0x1C0B	[7:0]	reserved	8	-	-	-
0x1C0C	[7:0]	reserved	8	-	-	-
0x1C0D	[7:0]	reserved	8	-	-	-
0x1C0E	[7:0]	reserved	8	-	-	-
0x1C0F	[7:0]	reserved	8	-	-	-
0x1C10	[7:0]	reserved	8	-	-	-
0x1C11	[7:6]	reserved	2	-	-	-
	[5:4]	TUNING_RXCLK_SEL	2	R/W	2'h0	LVDS RX Clock select 0x0: Normal operation, LICLKP/N input 0x3: Internal OSC Clock Others: reserved
	[3:2]	reserved	2	-	-	-
	[1]	reserved	1	-	-	-
	[0]	reserved	1	-	-	-
0x1C12	[7:0]	reserved	8	-	-	-
0x1C13	[7]	reserved	1	-	-	-
	[6]	reserved	1	-	-	-
	[5:4]	TUNING_LOCKN_CTRL1	2	R/W	2'h0	VbyOneHSII CDR LOCKN select for lane1 0x0: Normal operation, from BCC 0x1: External input from GPIOx 0x2: Low fix, Fix CDR Lock 0x3: High fix, Fix CDR Unlock
	[3]	reserved	1	-	-	-
	[2]	reserved	1	-	-	-
	[1:0]	TUNING_LOCKN_CTRL0	2	R/W	2'h0	VbyOneHSII CDR LOCKN select for lane0 0x0: Normal operation, from BCC 0x1: External input from GPIOx 0x2: Low fix, Fix CDR Lock 0x3: High fix, Fix CDR Unlock
0x1C14	[7:0]	reserved	8	-	-	-
0x1C15	[7:0]	reserved	8	-	-	-
0x1C16	[7:0]	TUNING_EN	8	R/W	8'h0	Tuning Registers access enable 0x22: Enable, 0x1C11 to 0x1C15 are able to set Others: Disable

Table 19. MONitor configuration table

MON0/1[7:0]	Error signal	Description
0x00	Disable	Hi-z, Pull-down
0x01	Low fix	-
0x02	High fix	-
0x03	CLK_TOP.TXCLK	VbyOneHS FC PCLK
0x04	CLK_TOP.RX0CLK	LVDS RX PCLK
0x05	Reserved	-
0x06	FCTX_BCRX_LINK.VSYNC0	VbyOneHSII Ser VSYNC for lane0 *
0x07	FCTX_BCRX_LINK.HSYNC0	VbyOneHSII Ser HSYNC for lane0 *
0x08	FCTX_BCRX_LINK.DE0	VbyOneHSII Ser DE for lane0
0x09	FCTX_BCRX_LINK.VSYNC1	VbyOneHSII Ser VSYNC for lane1 *
0x0A	FCTX_BCRX_LINK.HSYNC1	VbyOneHSII Ser HSYNC for lane1 *
0x0B	FCTX_BCRX_LINK.DE1	VbyOneHSII Ser DE for lane1
0x0C	FC_LVRX_TOP.RCOR	LVDS RX PCLK
0x0D	FC_LVRX_TOP.LVDS_DIN0[0]	LVDS LIA[0]
0x0E	FC_LVRX_TOP.LVDS_DIN0[1]	LVDS LIA[1]
0x0F	FC_LVRX_TOP.LVDS_DIN0[2]	LVDS LIA[2]
0x10	FC_LVRX_TOP.LVDS_DIN0[3]	LVDS LIA[3]
0x11	FC_LVRX_TOP.LVDS_DIN0[4]	LVDS LIA[4]
0x12	FC_LVRX_TOP.LVDS_DIN0[5]	LVDS LIA[5]
0x13	FC_LVRX_TOP.LVDS_DIN0[6]	LVDS LIA[6]
0x14	FC_LVRX_TOP.LVDS_DIN0[7]	LVDS LIB[0]
0x15	FC_LVRX_TOP.LVDS_DIN0[8]	LVDS LIB[1]
0x16	FC_LVRX_TOP.LVDS_DIN0[9]	LVDS LIB[2]
0x17	FC_LVRX_TOP.LVDS_DIN0[10]	LVDS LIB[3]
0x18	FC_LVRX_TOP.LVDS_DIN0[11]	LVDS LIB[4]
0x19	FC_LVRX_TOP.LVDS_DIN0[12]	LVDS LIB[5]
0x1A	FC_LVRX_TOP.LVDS_DIN0[13]	LVDS LIB[6]
0x1B	FC_LVRX_TOP.LVDS_DIN0[14]	LVDS LIC[0]
0x1C	FC_LVRX_TOP.LVDS_DIN0[15]	LVDS LIC[1]
0x1D	FC_LVRX_TOP.LVDS_DIN0[16]	LVDS LIC[2]
0x1E	FC_LVRX_TOP.LVDS_DIN0[17]	LVDS LIC[3]
0x1F	FC_LVRX_TOP.LVDS_DIN0[18]	LVDS LIC[4]
0x20	FC_LVRX_TOP.LVDS_DIN0[19]	LVDS LIC[5]
0x21	FC_LVRX_TOP.LVDS_DIN0[20]	LVDS LIC[6]
0x22	FC_LVRX_TOP.LVDS_DIN0[21]	LVDS LID[0]
0x23	FC_LVRX_TOP.LVDS_DIN0[22]	LVDS LID[1]
0x24	FC_LVRX_TOP.LVDS_DIN0[23]	LVDS LID[2]
0x25	FC_LVRX_TOP.LVDS_DIN0[24]	LVDS LID[3]
0x26	FC_LVRX_TOP.LVDS_DIN0[25]	LVDS LID[4]
0x27	FC_LVRX_TOP.LVDS_DIN0[26]	LVDS LID[5]
0x28	FC_LVRX_TOP.LVDS_DIN0[27]	LVDS LID[6]
0x29	FC_LVRX_TOP.LVDS_DIN1[0]	LVDS LIE[0]
0x2A	FC_LVRX_TOP.LVDS_DIN1[1]	LVDS LIE[1]
0x2B	FC_LVRX_TOP.LVDS_DIN1[2]	LVDS LIE[2]
0x2C	FC_LVRX_TOP.LVDS_DIN1[3]	LVDS LIE[3]
0x2D	FC_LVRX_TOP.LVDS_DIN1[4]	LVDS LIE[4]
0x2E	FC_LVRX_TOP.LVDS_DIN1[5]	LVDS LIE[5]
0x2F	FC_LVRX_TOP.LVDS_DIN1[6]	LVDS LIE[6]
0x30	FC_LVRX_TOP.LVDS_DIN1[7]	LVDS LIF[0]
0x31	FC_LVRX_TOP.LVDS_DIN1[8]	LVDS LIF[1]
0x32	FC_LVRX_TOP.LVDS_DIN1[9]	LVDS LIF[2]
0x33	FC_LVRX_TOP.LVDS_DIN1[10]	LVDS LIF[3]
0x34	FC_LVRX_TOP.LVDS_DIN1[11]	LVDS LIF[4]
0x35	FC_LVRX_TOP.LVDS_DIN1[12]	LVDS LIF[5]
0x36	FC_LVRX_TOP.LVDS_DIN1[13]	LVDS LIF[6]
0x37	FC_LVRX_TOP.LVDS_DIN1[14]	LVDS LIG[0]
0x38	FC_LVRX_TOP.LVDS_DIN1[15]	LVDS LIG[1]
0x39	FC_LVRX_TOP.LVDS_DIN1[16]	LVDS LIG[2]
0x3A	FC_LVRX_TOP.LVDS_DIN1[17]	LVDS LIG[3]
0x3B	FC_LVRX_TOP.LVDS_DIN1[18]	LVDS LIG[4]
0x3C	FC_LVRX_TOP.LVDS_DIN1[19]	LVDS LIG[5]
0x3D	FC_LVRX_TOP.LVDS_DIN1[20]	LVDS LIG[6]
0x3E	FC_LVRX_TOP.LVDS_DIN1[21]	LVDS LIH[0]
0x3F	FC_LVRX_TOP.LVDS_DIN1[22]	LVDS LIH[1]
0x40	FC_LVRX_TOP.LVDS_DIN1[23]	LVDS LIH[2]
0x41	FC_LVRX_TOP.LVDS_DIN1[24]	LVDS LIH[3]
0x42	FC_LVRX_TOP.LVDS_DIN1[25]	LVDS LIH[4]
0x43	FC_LVRX_TOP.LVDS_DIN1[26]	LVDS LIH[5]
0x44	FC_LVRX_TOP.LVDS_DIN1[27]	LVDS LIH[6]

*H/VSYNC signal do not match the input H/VSYNC signals because they are encoded.

8. Application and Implementation

NOTE

Information in the following applications sections is not part of the THine component specification, and THine does not warrant its accuracy or completeness. THine's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1. Applications Information

V-by-One® HSII behavior is connectable to THCV334-Q.

V-by-One® HS behavior, in which FCTHRIO is disabled, is connectable to standard V-by-One® HS product with external LOCKN connection.

8.2. Typical Applications

8.2.1. Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. For applications utilizing single-ended 50Ω coaxial cable, the unused data pins should be terminated with a 50Ω resistor.

8.2.2. Detailed Design Procedure

8.2.2.1. High-Speed Interconnect Guidelines

- ☐ Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer. (Refer to figure below.)
- ☐ PCB traces for high-speed signals must be single-ended micorstirp lines or coupled microstrip lines whose differential characteristic impedance is 100Ω.
- ☐ Minimize the distance between traces of a differential pair (S1) to maximize common mode rejection and coupling effect which works to reduce EMI(Electro-Magnetic Interference).
- ☐ Route differential signal traces symmetrically.
- ☐ Avoid right-angle turns or minimize the number of vias on the high speed traces because they usually cause impedance discontinuity in the transmission lines and degrade the signal integrity.
- ☐ Mismatch among impedances of PCB traces, connectors, or cables also caused reflection, limiting the bandwidth of the high-speed channels.
- ☐ Using common-mode filter on differential traces is desirable to reduce EMI. Pay attention on data-rate driven noise. For example, if data-rate is 1.5Gbps, common mode choke coil of 1.5GHz common mode impedance is desired to be high, while 1.5GHz differential impedance is low.

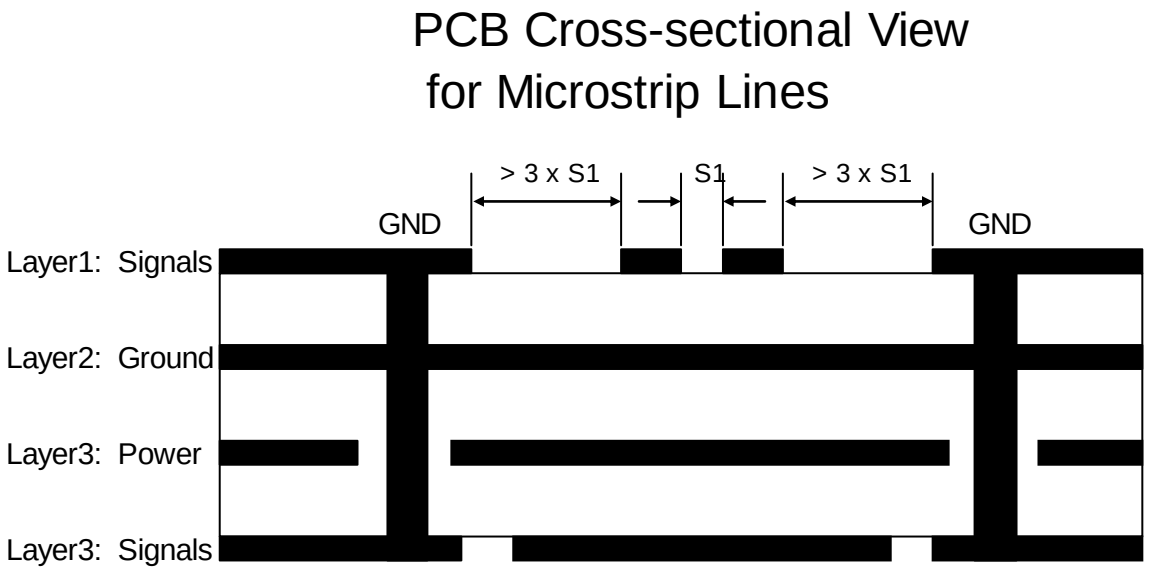


Figure 1 PCB cross-sectional view

9. Power Supply Recommendations

9.1. Power-Up Requirements and PDN Pin

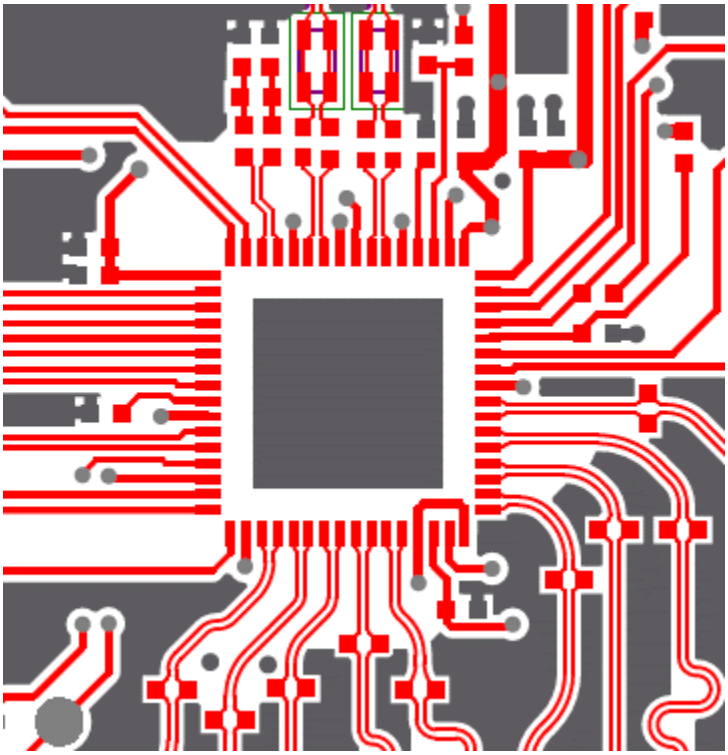
Please refer to 6.6.6. Power On and Re-Lock Sequence AC Specifications.

10. Layout

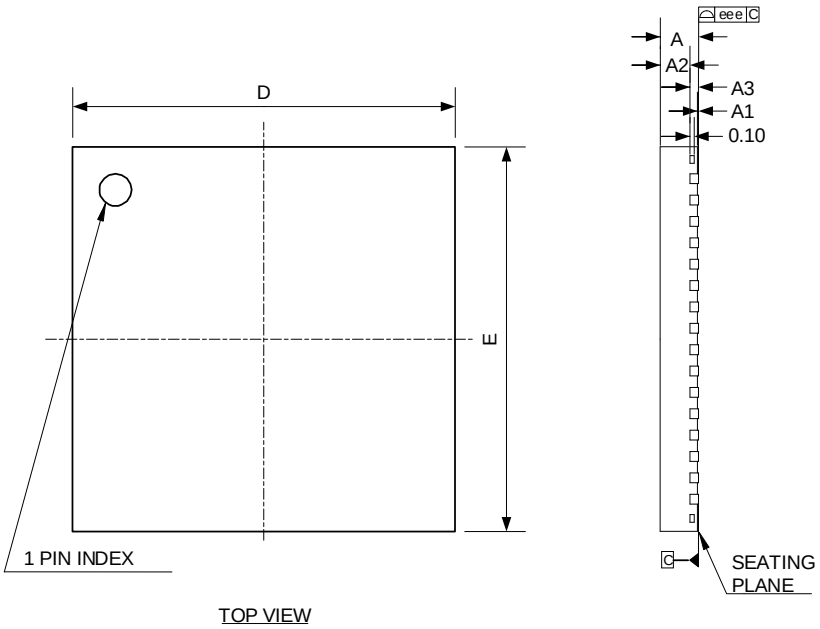
10.1. Layout Guidelines

Use at least four-layer PCBs with signals, ground, power, and signals assigned for each layer.

10.2. Layout Example

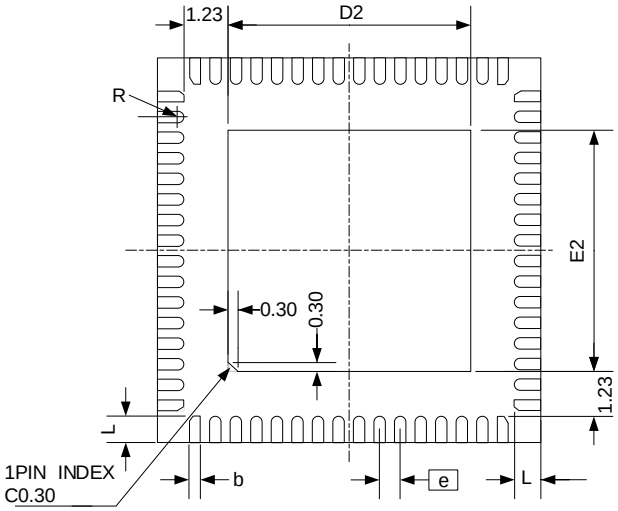


11. Package



TOP VIEW

SIDE VIEW

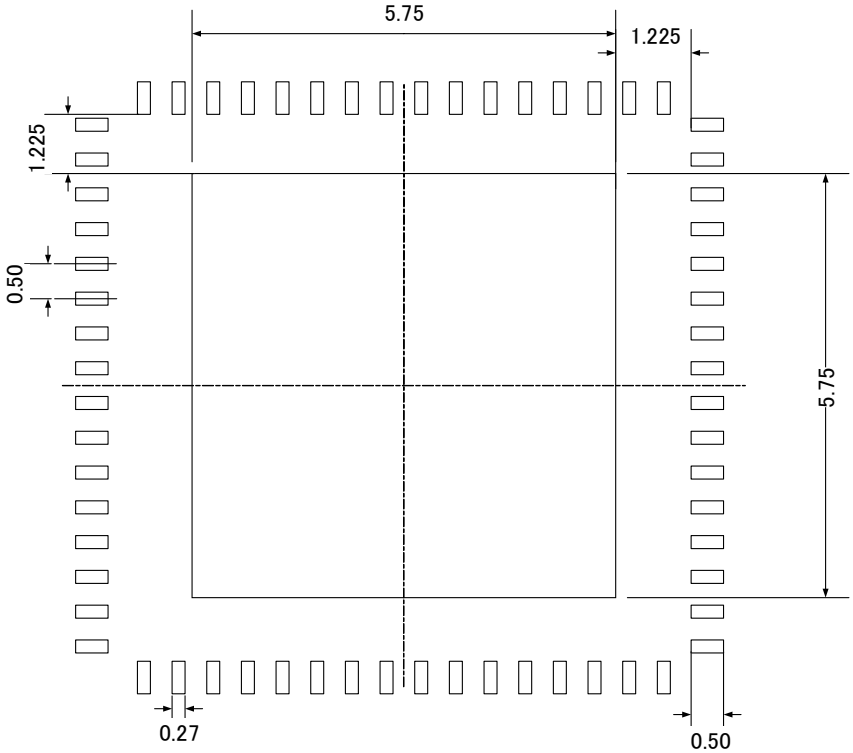


BOTTOM VIEW

Unit: mm

Symbol	Items	Min.	Nom.	Max.
A	Mounting Height	-	-	0.90
A1	Standoff	0.00	-	0.05
A2	-	-	0.65	0.70
A3	-		(0.20)	
b	Terminal Width	0.18	0.25	0.30
D	Body Length		9.00 BSC	
D2	Exposed Length	5.65	5.75	5.85
E	Body Width		9.00 BSC	
E2	Exposed Width	5.65	5.75	5.85
L	-	0.30	0.40	0.50
e	Pitch		0.50 BSC	
R	-	0.09	-	-
eee	Coplanarity		0.08	

12. Land Pattern



TOP VIEW

Unit: mm

LAND PATTERN EXMPLE

(Note)

Please carefully consider your SMT conditions (Material of substrate, Solder Composition, Reflow Condition and so on), and adjusts the Land Pattern at your own risk.

13. Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.

2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. THine Electronics, Inc. ("THine") is not responsible for possible errors and omissions in this material. Please note even if errors or omissions should be found in this material, THine may not be able to correct them immediately.

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7. This product may be permanently damaged and suffer from performance degradation or loss of mechanical functionality if subjected to electrostatic charge exceeding capacity of the ESD (Electrostatic Discharge) protection circuitry. Safety earth ground must be provided to anything in contact with the product, including any operator, floor, tester and soldering iron.

8. Please note that this product is not designed to be radiation-proof.

9. Testing and other quality control techniques are used to this product to the extent THine deems necessary to support warranty for performance of this product. Except where mandated by applicable law or deemed necessary by THine based on the user's request, testing of all functions and performance of the product is not necessarily performed.

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11. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Act in Japan and the Export Administration Regulations in the United States of America on export or transit of this product. This product is prohibited for the purpose of developing military modernization, including the development of weapons of mass destruction (WMD), and the purpose of violating human rights.

12. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses. THine accepts no liability whatsoever for any damage or loss caused to the user due to use under a condition exceeding the limiting values.

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