

Evaluating the **AD5767** 16-Channel, 12-Bit Serial Input, Voltage Output DAC

FEATURES

Full featured evaluation board for the **AD5767** with the **ADP5071** power solution
 PC control in conjunction with the Analog Devices, Inc., **EVAL-SDP-CB1Z** system demonstration platform (SDP)
 Power solution generated from a single 3.3 V supply
 PC software for control using analysis/control/evaluation (ACE) software

GENERAL DESCRIPTION

The **EVAL-AD5767SD2Z** is a fully featured evaluation board that allows the user to easily evaluate all the features of the **AD5767** 16-channel, 12-bit, voltage output digital-to-analog converter (DAC).

This board also integrates a power solution using the **ADP5071** switching regulator to generate a bipolar supply of +8 V and -22 V from a +3.3 V input, allowing a DAC voltage output range of -20 V to +6 V. Alternatively, supplying the DAC with a linear power supply via the on-board connector (J9) achieves all ranges.

The **AD5767** can be controlled using the on-board connector (J10) or the **EVAL-SDP-CB1Z** SDP board (via J1). The SDP allows the evaluation board to be controlled through the USB

port of a Windows®-based PC using the **AD5767** evaluation software.

The **AD5767** is a 16-channel, 12-bit voltage output denseDAC®. The DAC generates output ranges from a 2.5 V reference. The **AD5767** also integrates output buffers allowing the device to source or sink up to 20 mA. The range is software selectable, and any channel can be routed to the monitor pin for external monitoring. The integration of the reference and output buffers allows an easy to use universal solution.

The device requires four power supplies. AV_{DD} and AV_{SS} are the positive and negative high voltage power supplies, AV_{CC} is the analog supply for the low voltage DAC circuitry, and a V_{LOGIC} supply pin sets the logic levels for the digital interface pins.

The ACE software provides an intuitive graphic user interface (GUI), allowing all of the **AD5767** modes of operation to be configured over the synchronous serial port (SPORT) interface. The ACE software also has plugin modules for many other Analog Devices evaluation boards and Circuits from the Lab® (CFTL) demo boards.

Complete specifications for the **AD5767** are available in the **AD5767** data sheet, which must be consulted in conjunction with this user guide when using this evaluation board.

EVALUATION BOARD PHOTOGRAPH

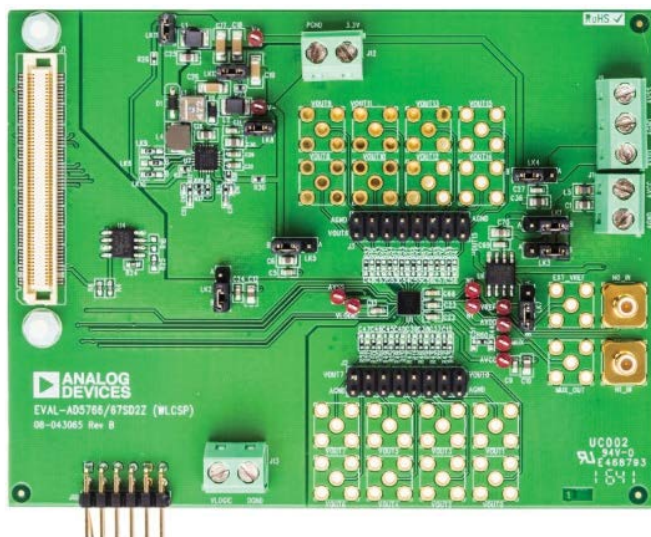


Figure 1.

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REVISION HISTORY

1/2017—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES/DEFAULT LINK OPTIONS

Table 1. Quick Start Jumper Configurations for Both ADP5071 and Bench Supply

Link No.	ADP5071	Bench Supply
LK1	A	A
LK2	A	A
LK3	A	A
LK4	B	A
LK5	B	A
LK7	A	A
LK8	Inserted	Removed
LK11	Removed	Removed
LK12	Removed	Removed

The EVAL-AD5767SD2Z evaluation board can be powered using the on-board ADP5071, which is supplied with a 3.3 V supply via the J12 connector. Alternatively, the J9 connector can provide power to the board instead of the ADP5071 and is intended for use with well regulated bench supplies. See Figure 2 for a functional block diagram.

With either option, first set the link options on the evaluation board for the required operating setup before supplying the board.

Each supply is decoupled to the relevant ground plane with 10 μ F and 0.1 μ F capacitors. Each device supply pin is again decoupled with a 10 μ F and 0.1 μ F capacitor pair to the relevant ground plane.

The analog and digital planes are connected at one location close to the DAC. To avoid ground loop problems, do not connect AGND and DGND elsewhere in the system.

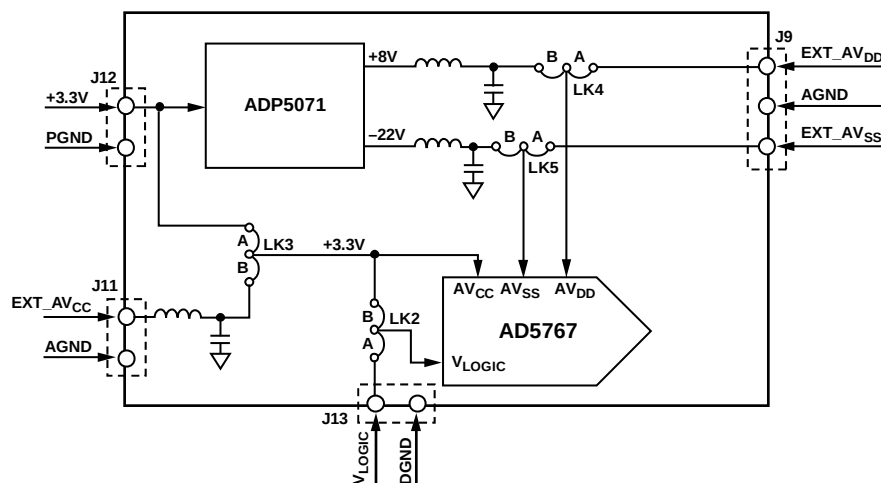


Figure 2. Powering the EVAL-AD5767 SDZ Evaluation Board

Table 2. Quick Start

Board Supply	Compatible Output Voltage Ranges (V)	Power Supplies Required		
		AVSS (J9) Maximum (V)	AVDD (J9) Minimum	J12 Nominal (V)
ADP5071	-20 to 0	Not required	Not required	3.3
	-16 to 0	Not required	Not required	3.3
	-10 to 0	Not required	Not required	3.3
	-10 to +6	Not required	Not required	3.3
	-5 to +5	Not required	Not required	3.3
Bench Supply	-20 to 0	-22	2.97	3.3
	-16 to +0	-18	2.97	3.3
	-10 to +0	-12	2.97	3.3
	-10 to +6	-12	8	3.3
	-12 to +14	-14	16	3.3
	-16 to +10	-18	12	3.3
	-5 to +5	-7	7	3.3
	-10 to +10	-12	12	3.3

Power Solution Option (ADP5071)

The EVAL-AD5767SD2Z board is populated with an ADP5071 switching regulator. This regulator generates +8 V and –22 V supplies from a single +3.3 V supply. The circuit was designed using the Analog Devices ADIsimPower toolset, which selects the components and generates the schematic and bill of materials, and displays the performance specifications. Visit the ADP5071 product page at www.analog.com/ADP5071 to download the design tools.

The ADP5071 requires 3.3 V for correct operation. Following the jumper configuration in Table 1, tie AV_{CC} , V_{LOGIC} , and the ADP5071 supplies together to operate from a single 3.3 V supply.

Alternatively, the AV_{CC} header (J11) and V_{LOGIC} header (J13) can be powered with separate supplies by selecting Position B on LK3 and LK2, respectively. Refer to Table 3 for full link options.

The –12 V to +14 V, –16 V to +10 V, or –10 V to +10 V output voltage ranges are not available with the ADP5071 default configuration because a minimum of 2 V headroom is required. Refer to the Filtered 3.3 V Supply section for further information, or supply the board using a bench supply.

Bench Power Supply Option

The evaluation board can be powered using a bench supply to access all output voltage ranges of the AD5767. A headroom and footroom of at least 2 V is required. Refer to Table 2 for the supply requirements. It is important that the voltage across AV_{DD} to AV_{SS} does not exceed the absolute maximum rating of 34 V. Otherwise, device reliability may be affected.

Following the jumper configuration in Table 2, tie AV_{CC} and V_{LOGIC} together to operate from the same 3.3 V supply, or AV_{CC} (via J11) and V_{LOGIC} (via J13) can be powered with separate supplies by selecting Position B on LK3 and LK2, respectively. Refer to Table 3 for full link options. Refer to Table 3 for full link options.

Table 3. Link Options

Link No.	Description
LK1	Selects the power supply for the ADR4525 reference; requires a minimum of 3 V for correct operation Position A: supplied by the 3.3 V supply (J12) Position B: supplied by the AV_{CC} header (J11)
LK2	Selects the power supply for the DAC V_{LOGIC} pin; requires 1.7 V to 5.5 V for correct operation Position A: supplied by the 3.3 V supply (J12) Position B: supplied by the V_{LOGIC} header (J13)
LK3	Selects the power supply for the DAC AV_{CC} pin; requires 2.97 V to 5.5 V for correct operation Position A: supplied by the 3.3 V supply (J12) Position B: supplied by the AV_{CC} header (J11)
LK4	Selects the power supply for the DAC AV_{DD} pin; ensure that the voltage between AV_{DD} and AV_{SS} does not exceed 34 V Position A: supplied by the AV_{DD} header (J9) Position B: supplied by the ADP5071 power solution
LK5	Selects the power supply for DAC AV_{SS} pin; ensure that the voltage between AV_{DD} and AV_{SS} does not exceed 34 V Position A: supplied by AV_{SS} header (J9) Position B: supplied by the ADP5071 power solution
LK6	Selects the start-up sequence of the ADP5071 outputs Position A: positive and negative output rails are sequenced based on the state of the EN1 and EN2 pins Position B: positive and negative output rails power up simultaneously when EN2 is high No link inserted: manual enable mode
LK7	Selects the voltage reference source Position A: selects the ADR4525 2.5 V reference Position B: selects an external reference source that can applied at the EXT_VREF SMB connector
LK8	Insert link to connect the ADP5071 to the 3.3 V supply header (J12)
LK9	Selects the switching frequency of ADP5071; this link is replaced with a 0 Ω resistor to Position A Position A: 1.2 MHz switching frequency (default) Position B: 2.4 MHz switching frequency
LK10	Selects the slew rate of the ADP5071 output; this link is replaced with a 0 Ω resistor to Position A Position A: slowest slew rate (best noise performance) Position B: normal slew rate
LK11	Insert link to bypass the LC filter on the ADP5071 positive output
LK12	Insert link to bypass the LC filter on the ADP5071 negative output

PMOD Connector (J10) Pin Configuration and Descriptions

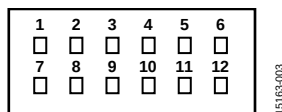


Figure 3. Jumper J10 Pin Configuration

Table 4. Connector J10 Pin Descriptions

Pin No.	Description
1	SYNC
2	SDIN/MOSI
3	SDO/MISO
4	SCLK
5	DGND
6	V _{LOGIC}
7	NC ¹
8	RESET
9	NC ¹
10	NC ¹
11	DGND
12	V _{LOGIC}

¹ NC means no connection.

ON-BOARD CONNECTORS

There are eight connectors on the EVAL-AD5767SD2Z, as shown in Figure 3. For the external supply pins, refer to the Power Supplies/Default Link Options section because AV_{CC} and V_{LOGIC} can be powered using J12, depending on the jumper configuration.

Table 5. On-Board Connectors

Connector	Function
J1	Connection for the EVAL-SDP-CB1Z board
J2	Header pins for V _{OUT0} to V _{OUT7} and AGND
J3	Header pins for V _{OUT8} to V _{OUT15} and AGND
J9	Supplies AV _{DD} and AV _{SS} externally
J10	Peripheral module (PMOD) connection pins
J11	Supplies AV _{CC} pin externally
J12	3.3 V supply for AV _{CC} , V _{LOGIC} , and the ADP5071
J13	Supplies V _{LOGIC} pin externally

ADP5071 SWITCHING REGULATOR

Filtering the ADP5071 Outputs

The EVAL-AD5767SD2Z board has an LC filter fitted on the ADP5071 positive and negative outputs. The filter can be bypassed by inserting LK11 and LK12.

Figure 4 shows the output frequency spectrum of the AD5767 powered by the filtered ADP5071 supply. The dotted red line represents 10% of 1 LSB using the -10 V to +6 V range. For comparison, Figure 5 shows the output frequency spectrum of the AD5767 powered by a bench power supply.

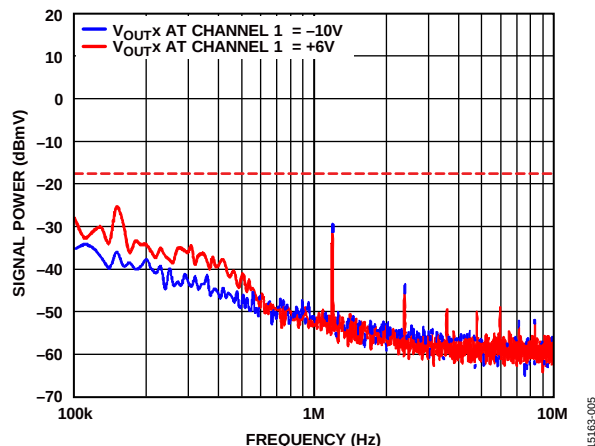


Figure 4. Output of AD5767 with ADP5071 (LC Filtered)

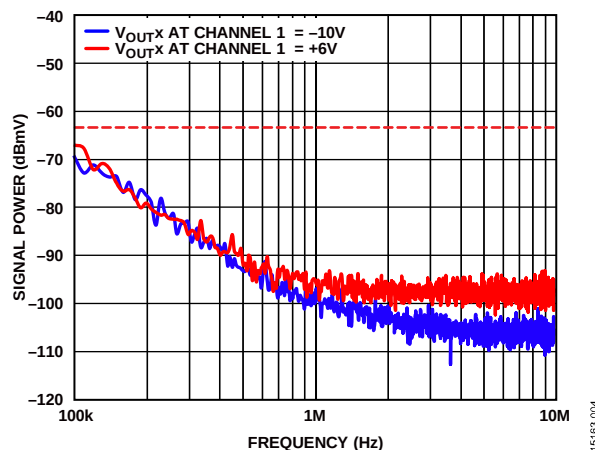


Figure 5. Output of AD5767 with Bench Power Supply

Filtered 3.3 V Supply

The EVAL-AD5767SD2Z board contains a filter on J11 to allow users to filter the AD5767 AV_{CC} rail. Alternatively, users can bypass the filter by using J12. Powering the board via the J12 header allows users to evaluate the board performance with their own supply. See Figure 6 for the functional block diagram.

When enabled with LK8, the ADP5071 can feed noise back onto the 3.3 V rail. Users can attenuate this noise by connecting J12 and J11 externally.

Changing the ADP5071 Output Voltages

By default, the ADP5071 output voltages are +8 V and -22 V. To provide enough headroom to supply the -12 V to +14 V, -16 V to +10 V, and -10 V to +10 V ranges, the feedback resistors must be changed. These are R26 and R31 for the positive output, and R28 and R30 for the negative output. Based on the output supplies required and load current requirements, the Analog Devices ADIsimPower toolset selects the recommended feedback resistors for the application. ADIsimPower is available on the ADP5071 product page at www.analog.com/ADP5071.

It is important that the voltage across AV_{DD} to AV_{SS} does not exceed the absolute maximum rating of 34 V. Otherwise, device reliability may be affected.

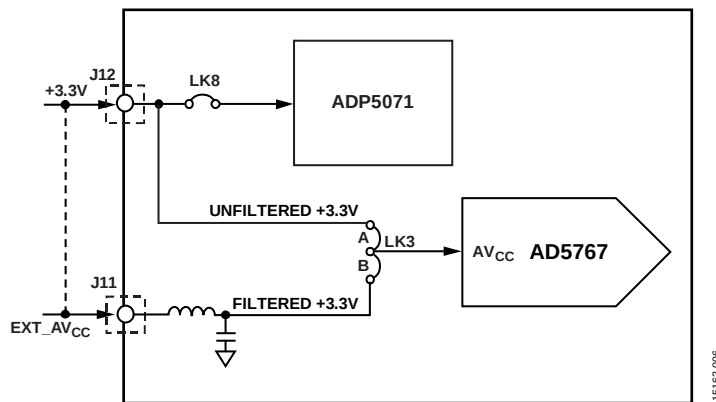


Figure 6. AV_{CC} Selection

EVALUATION BOARD SOFTWARE

ACE SOFTWARE INSTALLATION

The ACE software enables configuration of the [AD5767](#) over a USB port. This section introduces the key features of the program.

To download the ACE software and obtain detailed documentation on the platform, visit www.analog.com/ace. The installer also includes the drivers for the SDP board and plugins for multiple Analog Devices evaluation boards, including the [EVAL-AD5767SD2Z](#).

After the ACE software is installed, connect the evaluation board and SDP controller board together and plug the USB cable from the PC to the SDP controller board. Allow a few moments for the Windows operating system to recognize the SDP board.

ACE SOFTWARE OPERATION

To operate the ACE software, follow these steps:

1. To launch the ACE software, click **Start > All Programs > Analog Devices > ACE**. The software opens in the **Start** view tab and recognizes the [EVAL-AD5767SD2Z](#) (see Figure 7).
2. Double click the **AD5767 Board** icon under **Attached Hardware** to open the **AD5767 Board** tab (see Figure 8).
3. Double click the **AD5767** chip shown in Figure 8 to open the **AD5767** tab (see Figure 9). This tab displays the block diagram and allows the user to configure the DAC input registers and control registers. The hardware registers on the [AD5767](#) are not altered until the **Apply Changes** button is clicked.
4. Click the **Proceed to Memory Map** button (Label 12 in Figure 11) to open the **AD5767 Memory Map** tab and allow access to all registers (see Figure 10). The hardware registers on the [AD5767](#) are not altered until the **Apply Changes** button is clicked.

For a detailed description of all GUI options, see Table 6 and Figure 11.



Figure 7. **Start** Tab

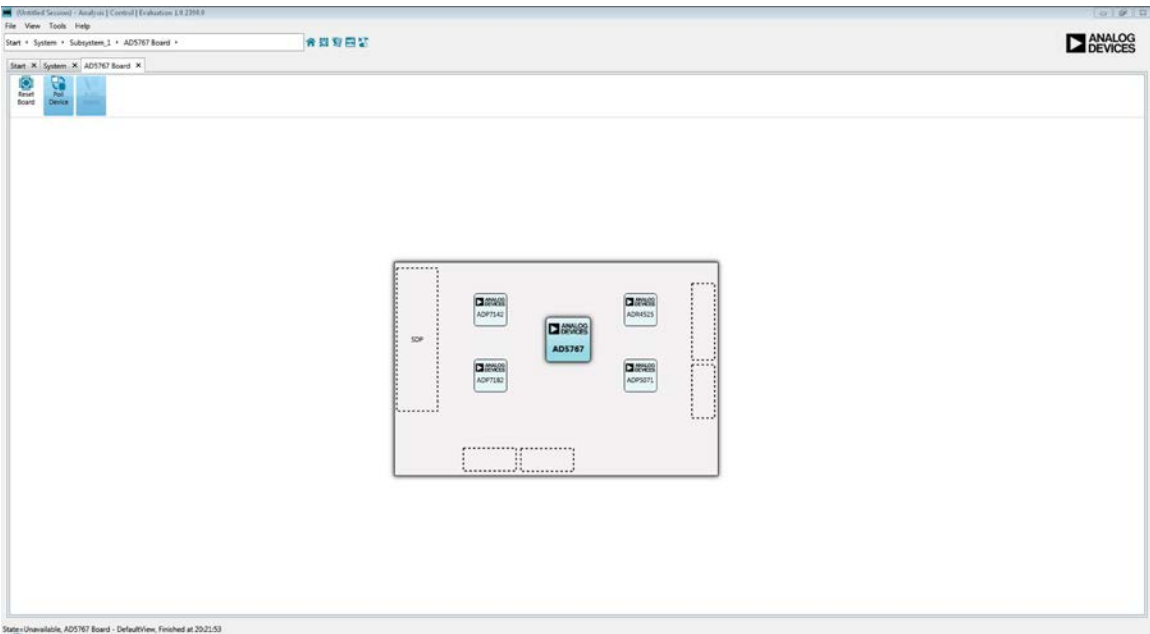


Figure 8. AD5767 Board Tab

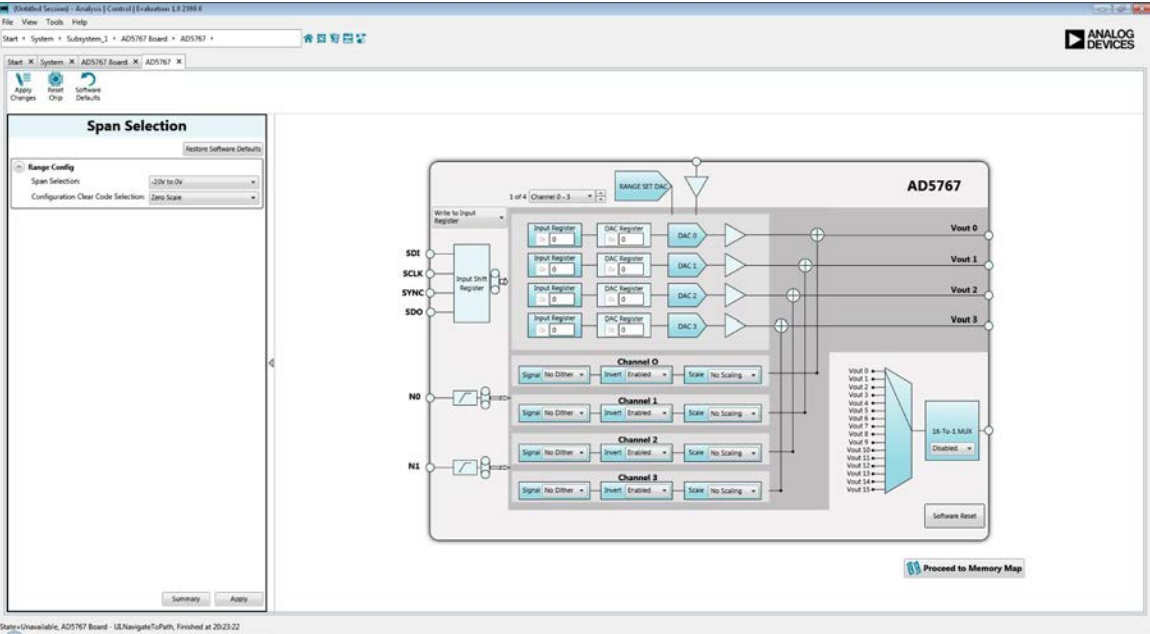


Figure 9. AD5767 Chip Tab

Address (Hex)	Name	Data (Hex)	Data (Binary)
0000	MONITOR_MUX	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0001	I2C_CTRL	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0002	DAC_INPUT_0	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0003	DAC_INPUT_1	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0004	DAC_INPUT_2	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0005	DAC_INPUT_3	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0006	DAC_INPUT_4	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0007	DAC_INPUT_5	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0008	DAC_INPUT_6	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0009	DAC_INPUT_7	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
000A	DAC_INPUT_8	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
000B	DAC_INPUT_9	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
000C	DAC_INPUT_10	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
000D	DAC_INPUT_11	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
000E	DAC_INPUT_12	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
000F	DAC_INPUT_13	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0010	DAC_INPUT_14	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0011	DAC_INPUT_15	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0012	SPI_DAC	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0013	SPI_REG	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0014	DAC_PASSWORD	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0015	DETHIER_PASSWORD	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0016	RESET	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0017	APPLY_DETHER_DAC0_DAC7	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0018	APPLY_DETHER_DAC8_DAC15	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0019	DETHIER_INVERT	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
001A	DETHIER_SCALE_DAC0_DAC7	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
001B	DETHIER_SCALE_DAC8_DAC15	0000	0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

Figure 10. AD5767 Memory Map Tab

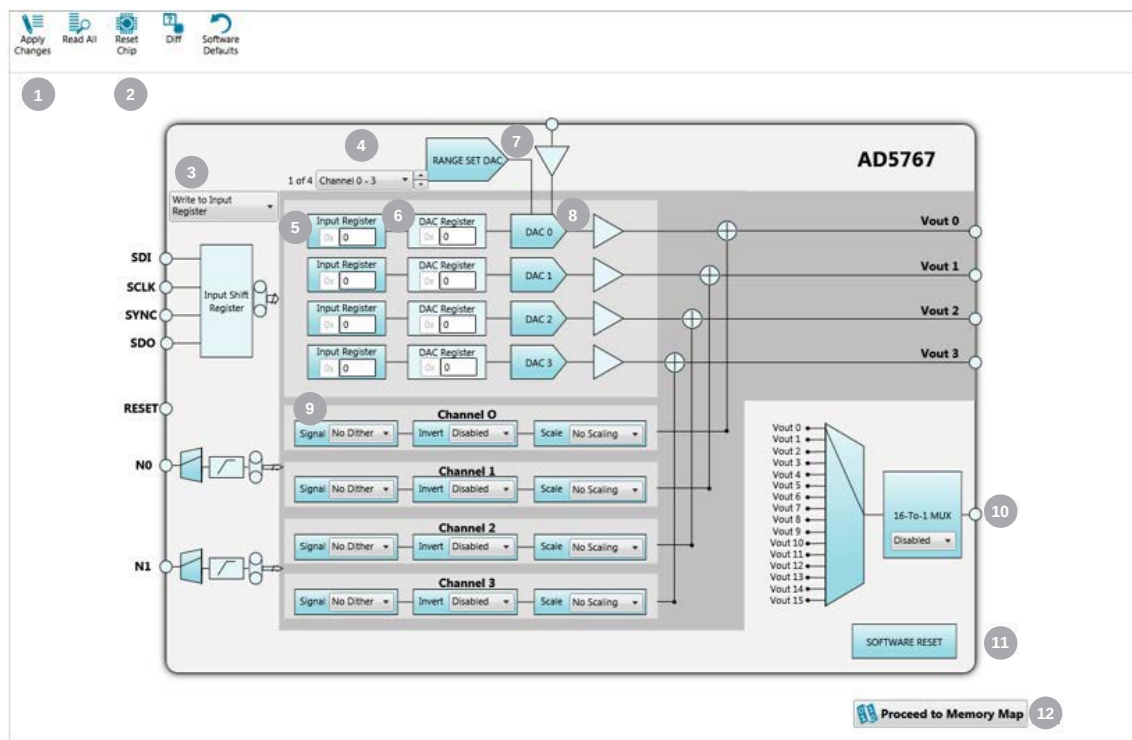


Figure 11. Main Window

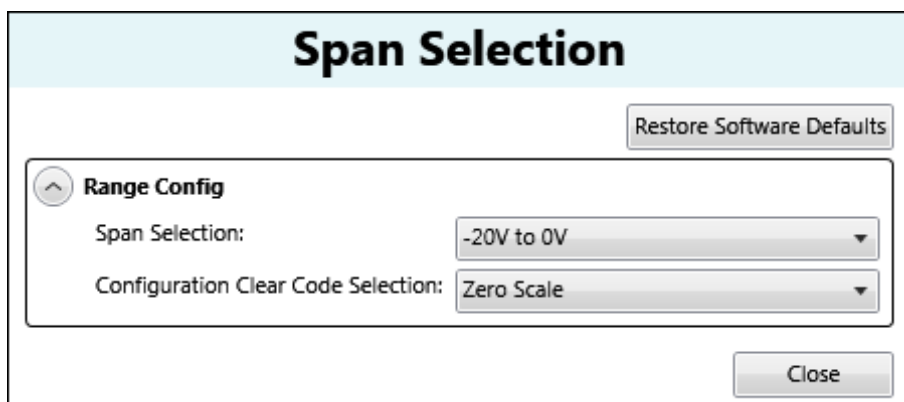
Figure 12. **Span Selection** Window

Table 6. GUI Options (See Figure 11)

Label No.	GUI Element	Description
1	Apply Changes	This button must be clicked to submit any changes on the GUI to the evaluation board hardware.
2	Reset Chip	Issues a hardware reset and reverts the software and hardware registers to their default settings.
3	Write to Input Register	Allows the user to write to the input register, write to the input register and the DAC register, or write to the input register and update all DAC registers.
4	Select output	Channels displayed. Allows the user to show Channel 0 to Channel 3, Channel 4 to Channel 7, Channel 8 to Channel 11, or Channel 12 to Channel 15 for V_{OUT} in the AD5767 chip tab.
5	Input Register	The user can input data to write to the input register. There is one input register per channel.
6	DAC Register	This is a graphical representation of the DAC register. There is one DAC register per channel.
7	RANGE SET DAC	Click RANGE SET DAC to select the output voltage range from the Span Selection window (see Figure 12).
8	DAC x	Click the DAC to apply a dither signal or to power down the selected channel.
9	Signal, Invert, and Scale	Allows the user to select the dither options for each channel.
10	16-To-1 MUX	Select which channel to route to the AD5767 MUX_OUT pin.
11	SOFTWARE RESET	Issues a software reset and reverts the software and hardware registers to their default settings.
12	Proceed to Memory Map	Click to open the AD5767 Memory Map tab (see Figure 10).

EVALUATION BOARD SCHEMATICS AND ARTWORK

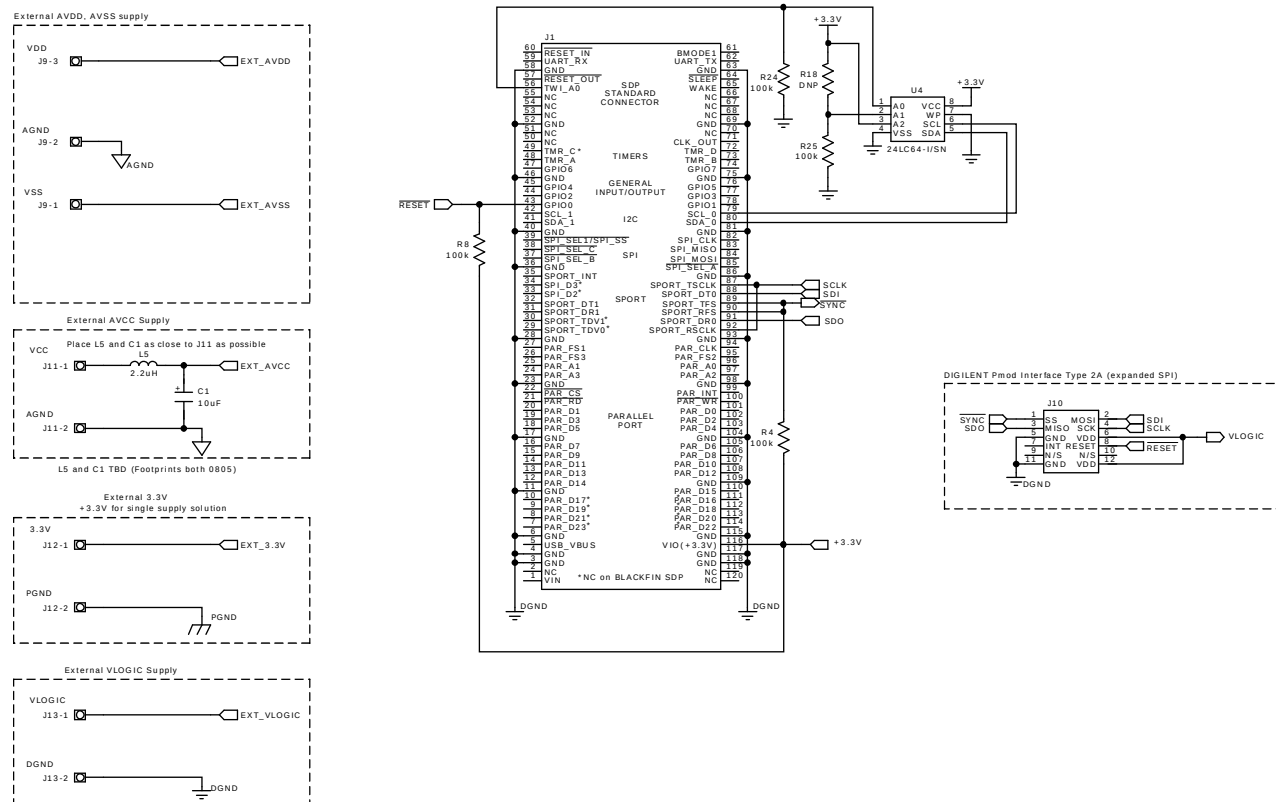


Figure 13. SDP Connector and Power Supply

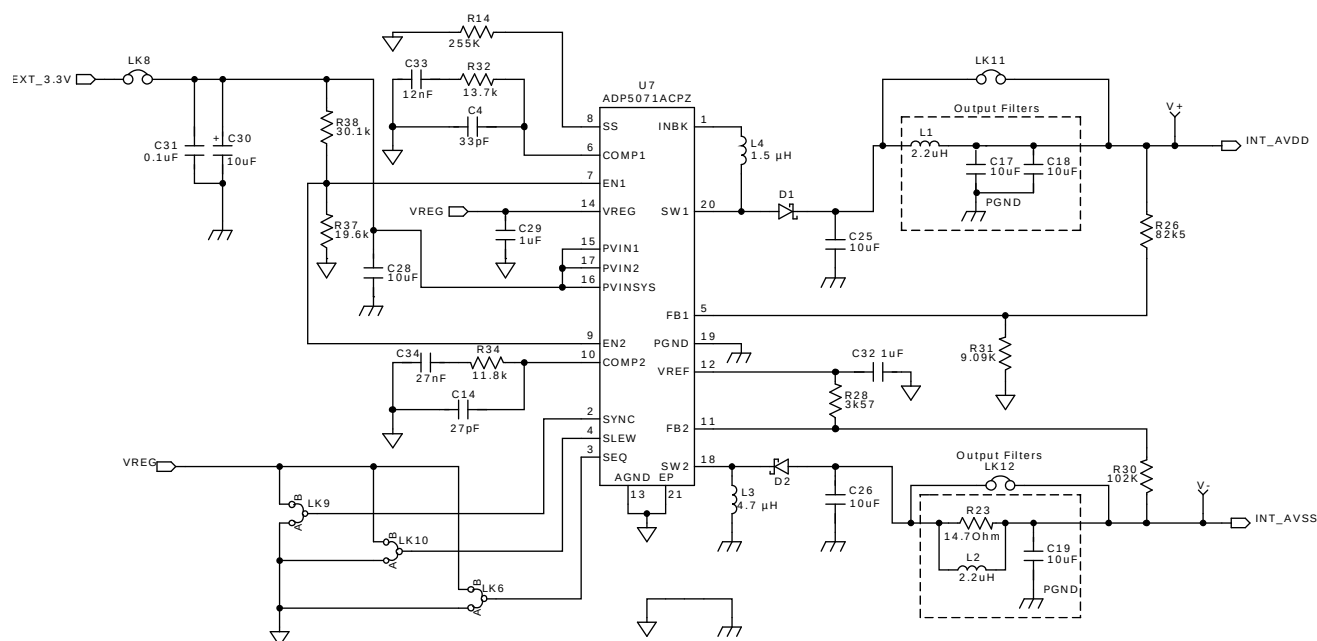


Figure 14. ADP5071 Power Solution

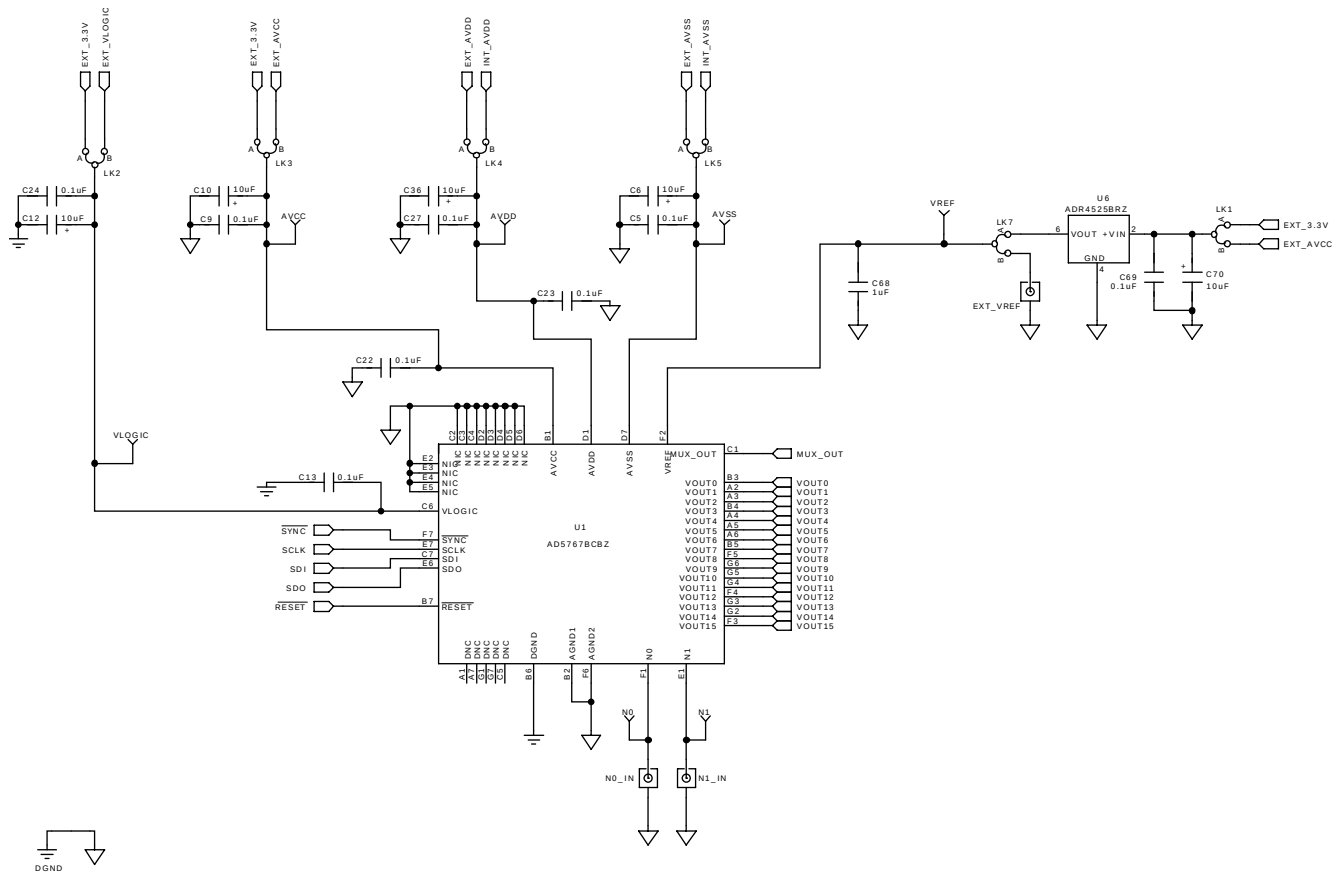
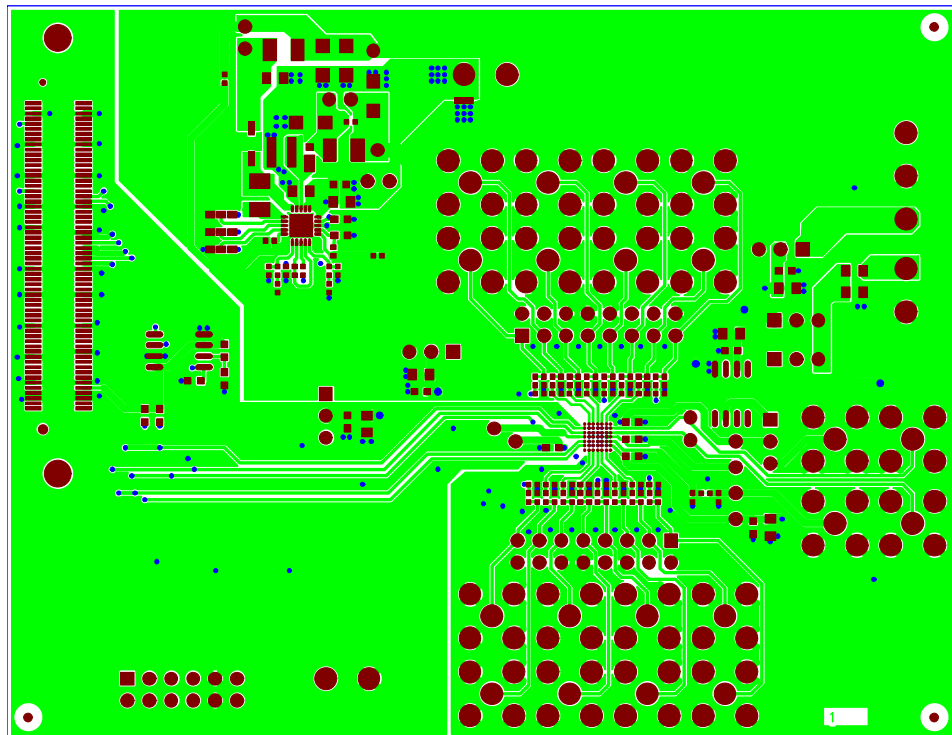
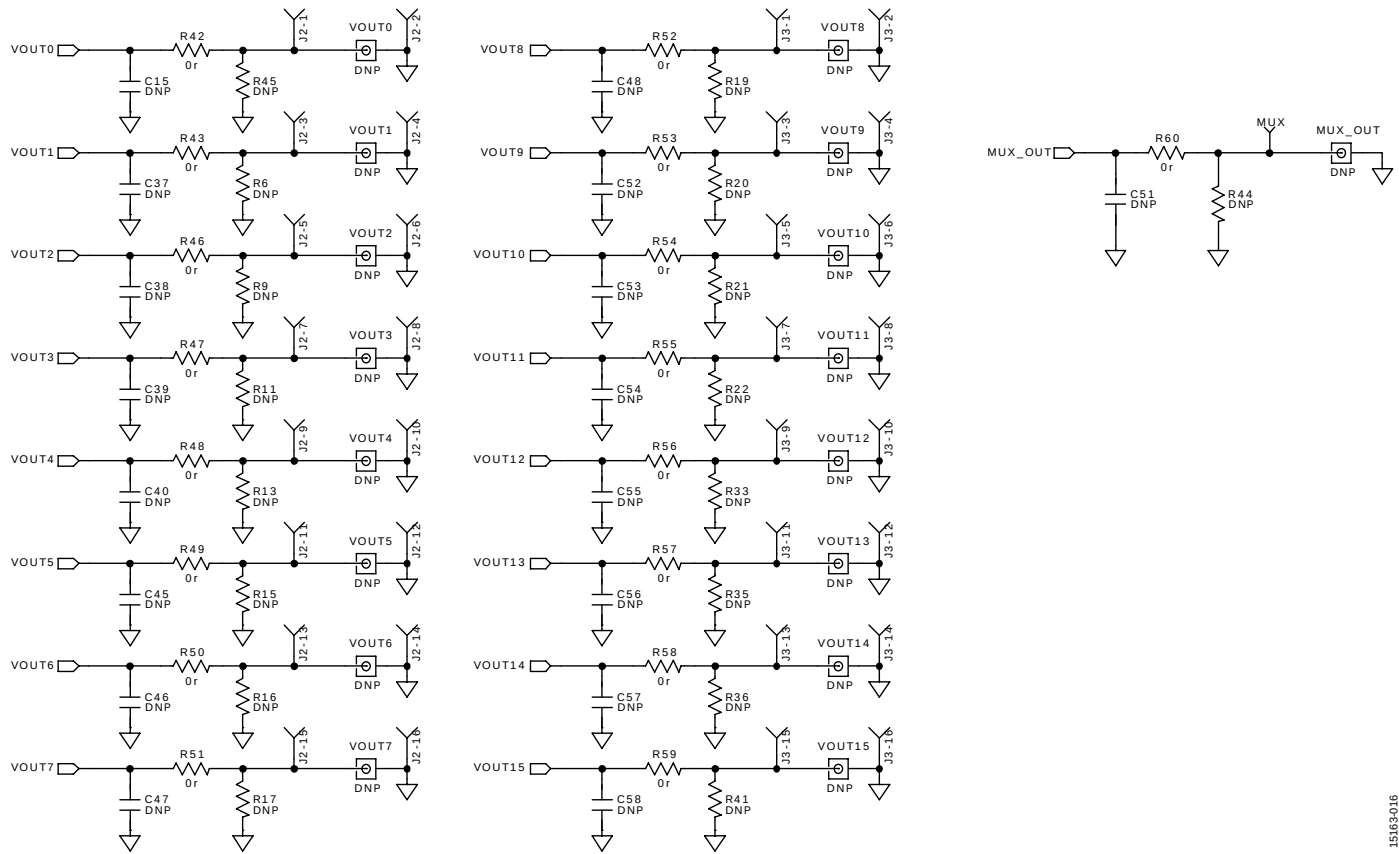
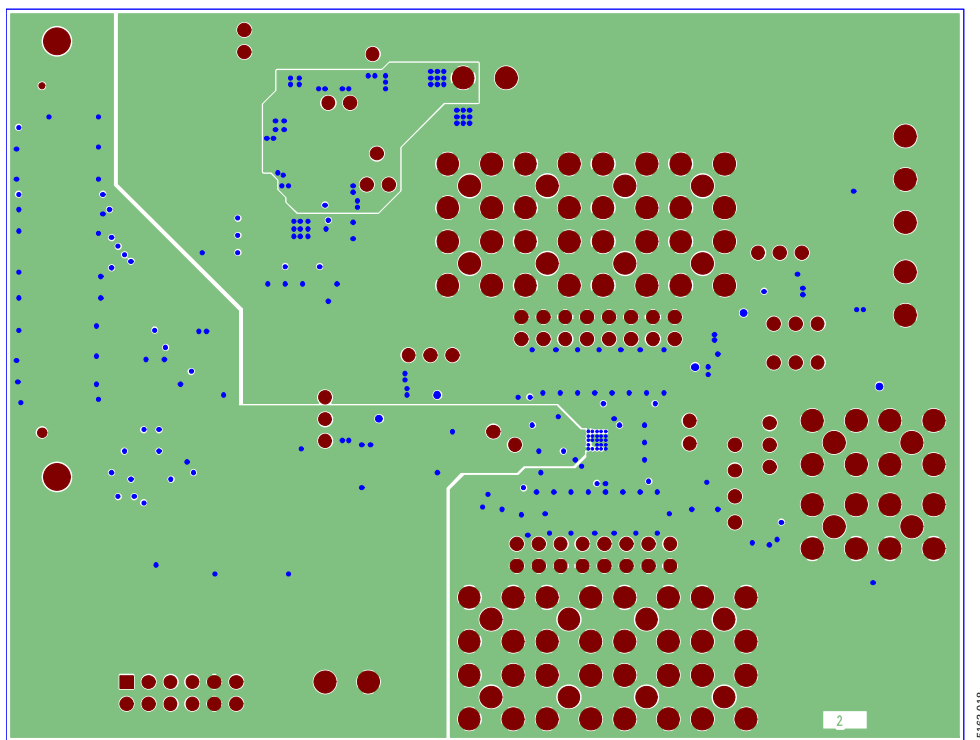


Figure 15. AD5767 (WLCSP) and External Reference

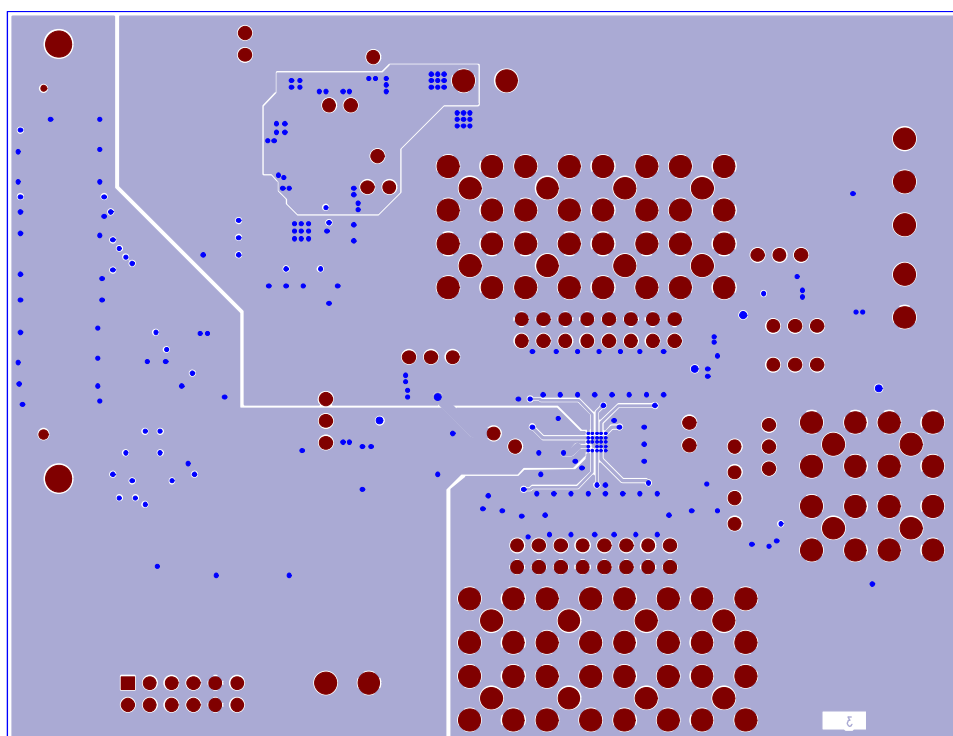
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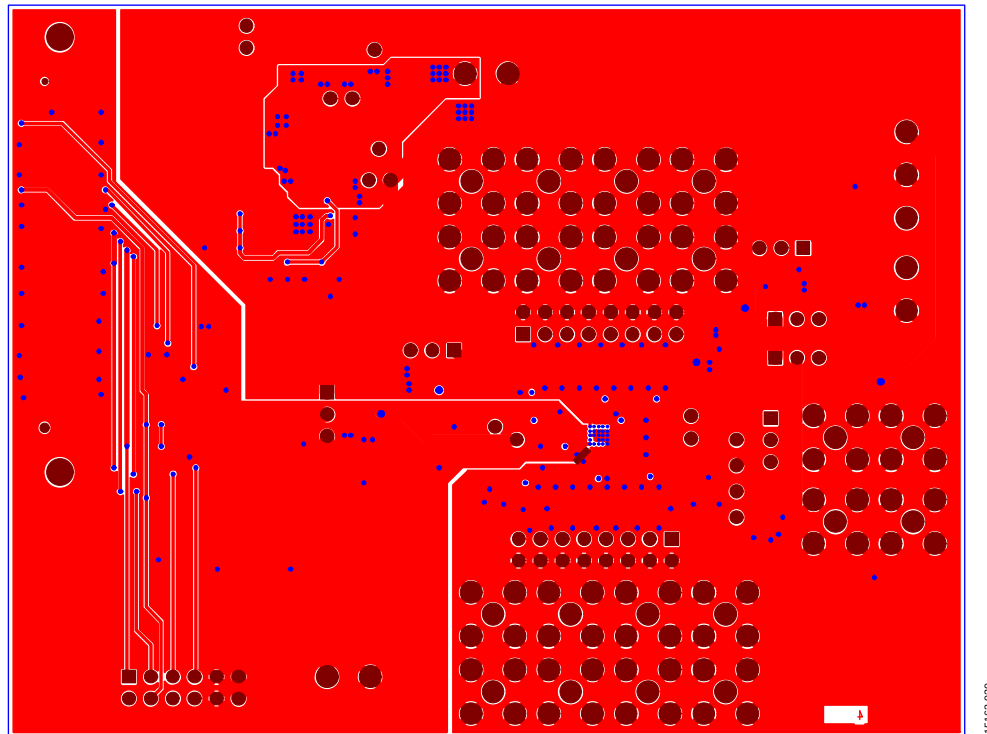
15163-018

Figure 18. Inner First PCB Layer



15163-019

Figure 19. Inner Second PCB Layer



15163-020

Figure 20. Bottom PCB Layer

ORDERING INFORMATION

BILL OF MATERIALS

Table 7.

Reference Designator	Description	Part Number	Stock Code
C1	Capacitor, 0805, X5R, 10 V, 10 μ F, $\pm$ 10%	GRM219R61A106KE44D	FEC 2346905
C4	Capacitor, 1210, C0G, 50 V, 33 pF, $\pm$ 10%	MC0402N330K500CT	FEC 1845741
C5 C9, C13, C22, C23, C24, C27, C31, C69	Capacitor, 0603, C0G, 50 V, 0.1 μ F, $\pm$ 10%	GRM188R71H104KA93D	FEC 8820023
C6, C10, C12, C30, C36, C70,	Capacitor, 0805, C0G, 50 V, 0.1 μ F, $\pm$ 10%	GRM21BR71A106KE51L	FEC 1828828
C14	Capacitor, 0402, C0G, 50 V, 27 pF, $\pm$ 10%	C0402C270K5GACTU	Digi-Key 399-8960-1-ND
C17, C18	Capacitor, 1206, X5R, 10 V, 10 μ F, $\pm$ 10%	C3216X5R1A106K160AB	FEC 1844306
C19, C26	Capacitor, 1206, X5R, 35 V, 10 μ F, $\pm$ 10%	GRM31CR6YA106KA12L	FEC 1797011
C25, C28	Capacitor, 0805, X5R, 10 V, 10 μ F, $\pm$ 10%	GRM21BR61A106KE19L	FEC 1828805
C29, C32	Capacitor, 0603, X5R, 6.3 V, 1 μ F, $\pm$ 10%	GRM188R60J105KA01D	FEC 9527699
C33	Capacitor, 0402, X7R, 16 V, 0.012 μ F, $\pm$ 10%	MC0402B123K160CT	FEC 1758886
C34	Capacitor, 0402, X5R, 16 V, 0.027 μ F, $\pm$ 10%	MC0402X273K160CT	FEC 1759382
C68	Capacitor, 0805, X7R, 50 V, 1 μ F, $\pm$ 10%	GRM21BR71H105KA12L	FEC 1735541
D1	Rectifier diode, single, 20 V, 500 mA, SOD-123, 2, 385 mV	MBR0520L	FEC 1467521
D2	Schottky diode	PD3S160-7	FEC 1843697
J1	120-way connector, 0.6 mm pitch	FX8-120S-SV(21)	FEC 1324660
J2, J3	16-pin (2 $\times$ 8), 0.1 inch pitch, single inline (SIL) header	M20-9980846	FEC 1022240
J9	3-pin terminal block (5 mm pitch)	CTB5000/3	FEC 151790
J10	PMOD connector	68021-212HLF	Digi-Key 609-3345-ND
J11, J12, J13	2-pin terminal block (5 mm pitch)	CTB5000/2	FEC 151789
L1, L2	Fixed inductor, 2.2 μ H, 1.6 A, 76 m Ω SMD	LQH32PN2R2NN0L	Digi-Key 490-5336-2-ND
L3	Surface-mount power inductor	XFL4020-472MEC	FEC 2289218
L4	Fixed inductor 1.5 μ H, 4.1 A, 46.8 m Ω	SPM4020T-1R5M	Digi-Key 445-172371-1-ND
L5	2.2 μ H shielded multilayer inductor	AIML-0805-2R2K-T	Digi-Key 535-11631-2-ND
LK1 to LK5, LK7	3-pin SIL header and shorting link	M20-9990345 & M7567-05	FEC 1022248 and FEC 150410
LK6, LK9, LK10	2-way resistor link option	MC 0.063W 0603 0R	FEC 9331662
LK8, LK11, LK12	2-pin (0.1 inch pitch) header and shorting shunt	M20-9990246	FEC 1022247 and FEC 150-411
R4, R8, R24, R25	Resistor, 100 k Ω , 0.063 W, 1%, 0603	MC0063W06031100K	FEC 9330402
R14	Surface-mount chip resistor, ceramic, MCMR series, 255 k Ω , 62.5 mW, $\pm$ 1%, 50 V	MCMR04X2553FTL	FEC 2072839
R23	Surface-mount chip resistor, thick film, AEC-Q200 CRCW series, 14.7 Ω , 63 mW, $\pm$ 1%, 50 V	CRCW040214R7FKED	FEC 2140591
R26	Resistor, 82.5 k Ω , 0.0625 W, 1%, 0402	MC00625W0402182K5	FEC 1803742
R28	Resistor, 3.57 k Ω , 0.0625 W, 1%, 0402	MC00625W040213K57	FEC 1803091
R30	Resistor, 102 k Ω , 0.0625 W, 1%, 0402	MC00625W04021102K	FEC 1803752
R31	Resistor, 9.09 k Ω , 0.0625 W, 1%, 0402	MC00625W040219K09	FEC 1803134
R32	Resistor, 13.7 k Ω , 0.0625 W, 1%, 50 V, 0402	MCMR04X1372FTL	FEC 2072621
R34	Resistor, 11.8 k Ω , 0.063 W, 1%, 50 V, 0402	CRCW040211K8FKED	FEC 2140865
R37	Resistor, 19.6 k Ω , 0.0625 W, 1%, 50 V, 0402	MC00625W0402119K6	FEC 1803680
R38	Resistor, 30.1 k Ω , 0.063 W, 1%, 50 V, 0402	CRCW040230K1FKED	FEC 1469704
R42, R43, R46 to R60	Resistor, 0402, 1%, 0 Ω	MC00625W040210R	FEC 1357983
U1	16-channel, 12-bit voltage output denseDAC	AD5767	AD5767BCBZ-WP
U4	64 kb I ² C serial EEPROM	24LC64-I/SN	FEC 9758070
U6	2.5 V voltage reference	ADR4525BRZ	ADR4525BRZ
U7	2 A/1.2 A dc to dc switching regulator with independent positive and negative outputs	ADP5071ACPZ	ADP5071ACPZ

NOTES



ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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