

MOSFET - Single N-Channel

150 V, 4.4 mΩ, 187 A

NVBL54D0N15MC

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- Power Tools, Battery Operated Vacuums
- UAV/Drones, Material Handling
- BMS/Storage, Home Automation

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V _{DSS}	Drain-to-Source Voltage			150	V
V _{GS}	Gate-to-Source Voltage			±20	V
I _D	Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25°C	187	A
			T _C = 100°C	132	
P _D	Power Dissipation R _{θJC} (Note 2)	Steady State	T _C = 25°C	316	W
			T _C = 100°C	158	
I _D	Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	22	A
			T _A = 100°C	15	
P _D	Power Dissipation R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	4	W
			T _A = 100°C	2	
I _{DM}	Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		900	A
T _J , T _{stg}	Operating Junction and Storage Temperature Range			-55 to +175	°C
I _S	Source Current (Body Diode)			263	A
E _{AS}	Single Pulse Drain-to-Source Avalanche Energy (I _{LPEAK} = 15.9 A)			2300	mJ
T _L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			260	°C

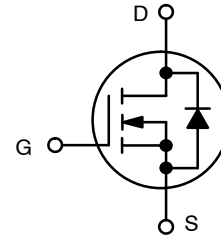
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface-mounted on FR4 board using 1 in² pad size, 2 oz Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

THERMAL RESISTANCE RATINGS

Symbol	Parameter	Max	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	0.5	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	35.8	

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
150 V	4.4 mΩ @ 10 V	187 A

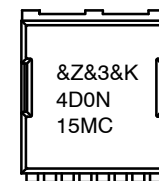


N-CHANNEL MOSFET



H-PSOF8L 11.68x9.80
MO-299A
CASE 100CU

MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 4D0N15MC = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
NVBL54D0N15MC	MO-299A (Pb-Free)	2000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVBL54D0N15MC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA		150	–	–	V
V _{(BR)DSS} / T _J	Drain-to-Source Breakdown Voltage Temperature Coefficient	I _D = 250 μA, ref to 25°C		–	30.23	–	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{GS} = 0 V, V _{DS} = 120 V	T _J = 25°C	–	–	1	μA
			T _J = 125°C	–	–	10	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = ±20 V		–	–	±100	nA

ON CHARACTERISTICS

V _{GS(TH)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 584 μA	2.5	3.7	4.5	V
V _{GS(TH)} / T _J	Negative Threshold Temperature Coefficient	I _D = 250 μA, ref to 25°C	–	–10.12	–	mV/°C
R _{DS(on)}	Drain-to-Source On Resistance	V _{GS} = 10 V, I _D = 80 A	–	3.1	4.4	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 5 V, I _D = 80 A	–	174	–	S
R _G	Gate-Resistance	T _A = 25°C	–	1.3	–	Ω

CHARGES & CAPACITANCES

C _{ISS}	Input Capacitance	V _{GS} = 0 V, f = 1 MHz, V _{DS} = 75 V	–	7490	–	pF
C _{OSS}	Output Capacitance		–	2055	–	
C _{RSS}	Reverse Transfer Capacitance		–	27.2	–	
Q _{G(TOT)}	Total Gate Charge	V _{GS} = 10 V, V _{DS} = 75 V, I _D = 80 A	–	90.4	–	nC
Q _{G(TH)}	Threshold Gate Charge		–	24.7	–	
Q _{GS}	Gate-to-Source Charge		–	40.2	–	
Q _{GD}	Gate-to-Drain Charge		–	12.6	–	
V _{GP}	Plateau Voltage		–	5.7	–	V

SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 3)

t _{d(ON)}	Turn-On Delay Time	V _{GS} = 10 V, V _{DS} = 75 V, I _D = 80 A, R _G = 6 Ω	–	47	–	ns
t _r	Rise Time		–	115	–	
t _{d(OFF)}	Turn-Off Delay Time		–	58	–	
t _f	Fall Time		–	11	–	

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	V _{GS} = 0 V, I _S = 80 A	T _J = 25°C	–	0.86	1.2	V
			T _J = 125°C	–	0.75	–	
t _{RR}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 80 A		–	84	–	ns
t _a	Charge Time			–	55	–	
t _b	Discharge Time			–	29	–	
Q _{RR}	Reverse Recovery Charge			–	180	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

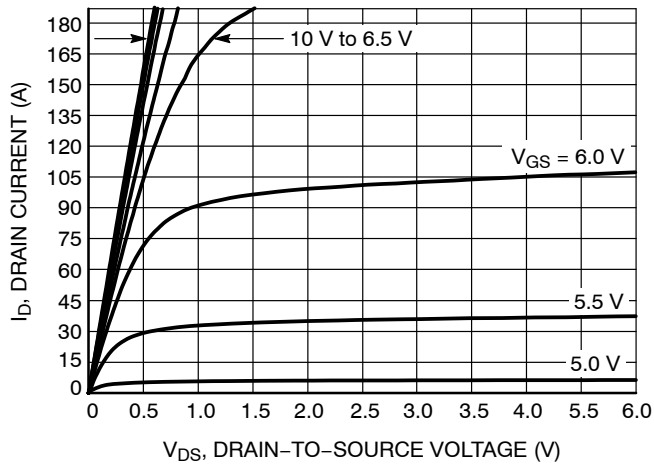


Figure 1. On-Region Characteristics

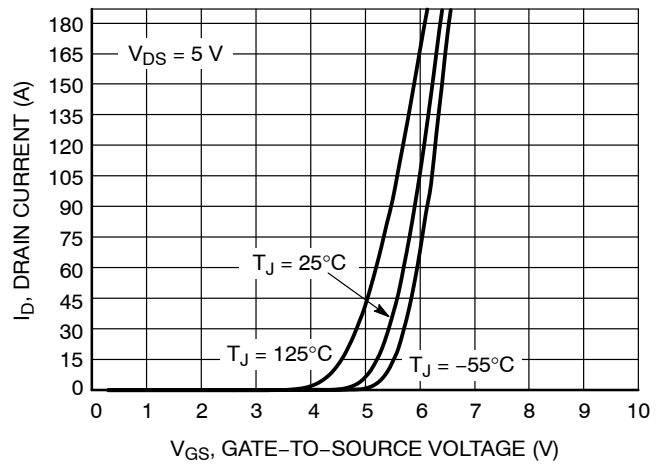


Figure 2. Transfer Characteristics

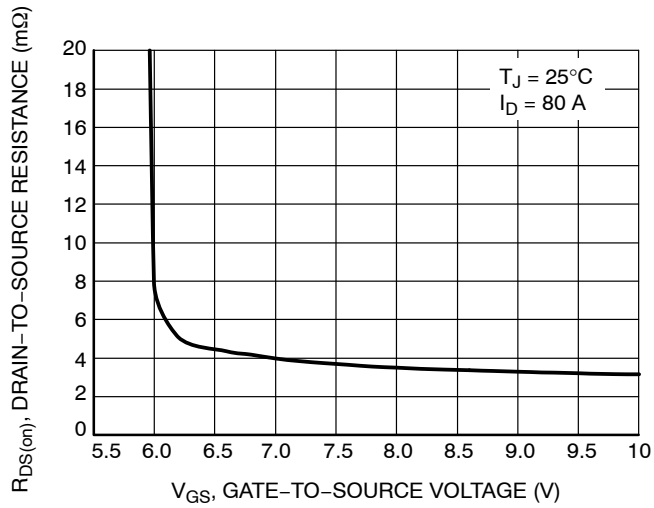


Figure 3. On-Resistance vs. V_{GS}

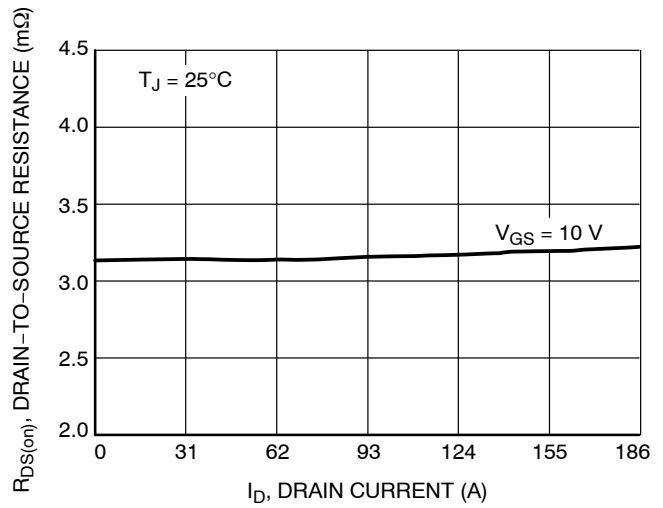


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

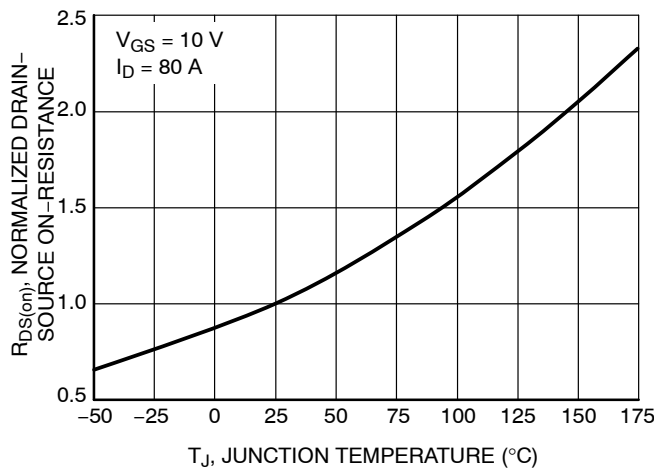


Figure 5. On-Resistance Variation with Temperature

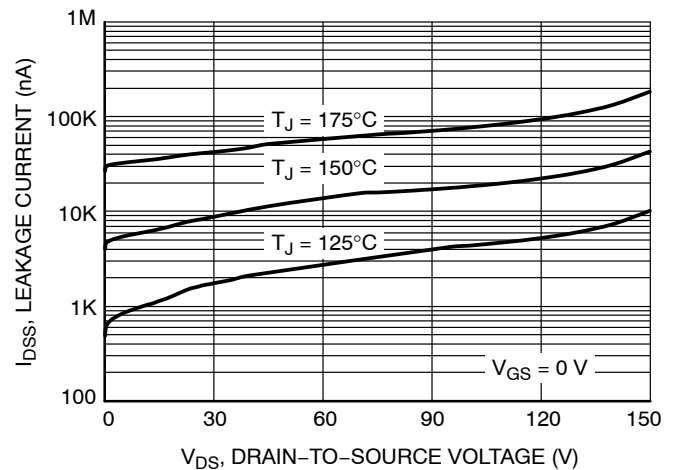


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

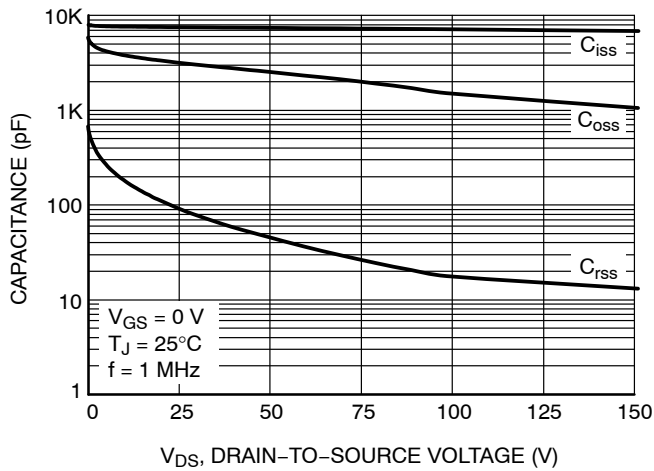


Figure 7. Capacitance Variation

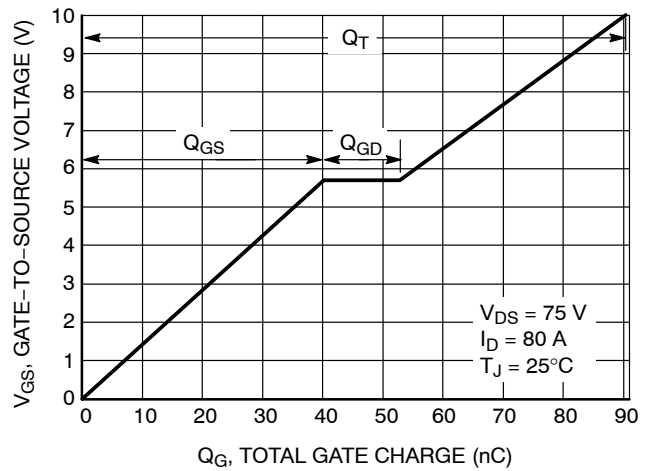


Figure 8. Gate-to-Source Voltage vs. Total Gate Charge

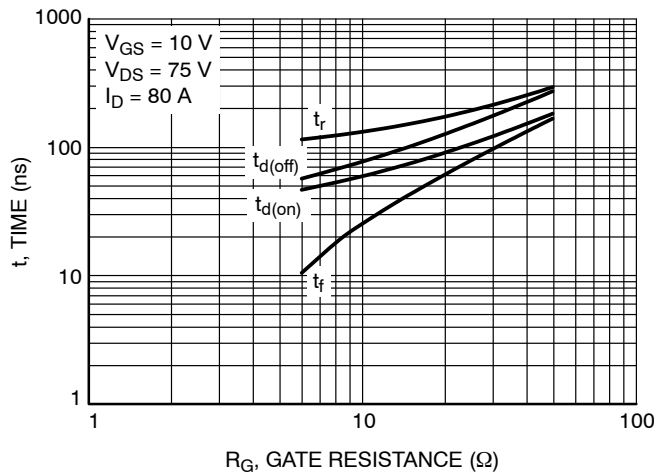


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

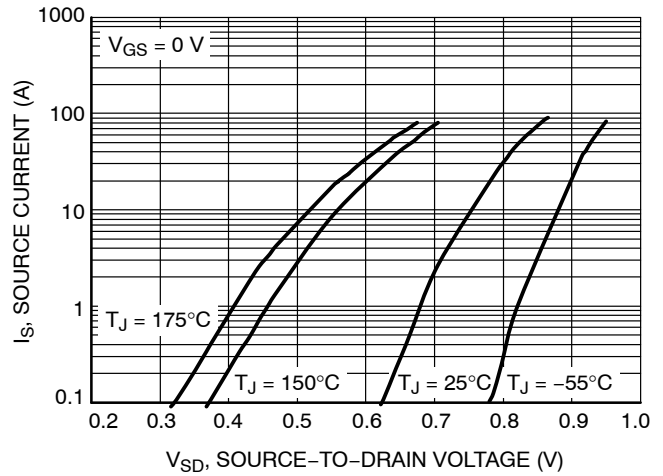


Figure 10. Diode Forward Voltage vs. Current

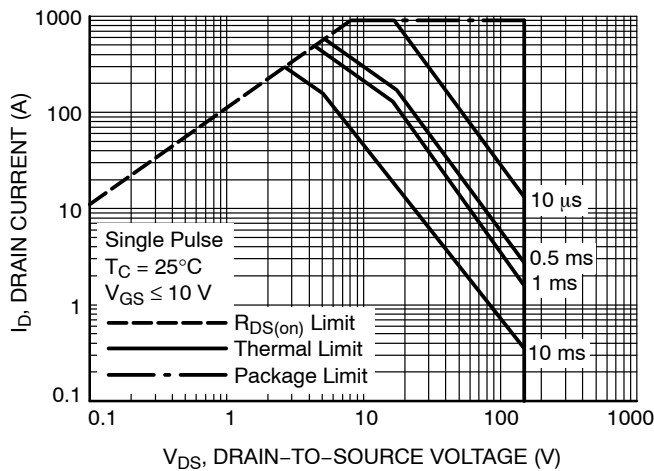


Figure 11. Maximum Rated Forward Biased Safe Operating Area

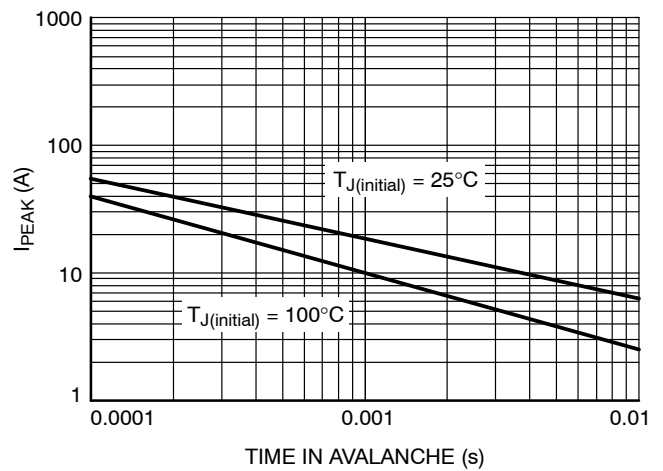


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

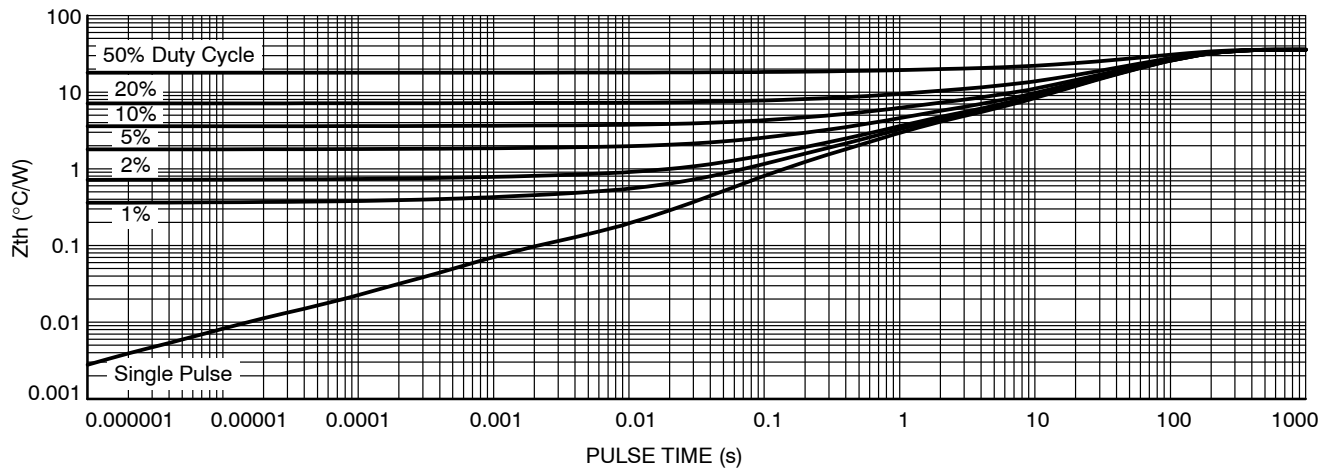
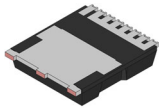
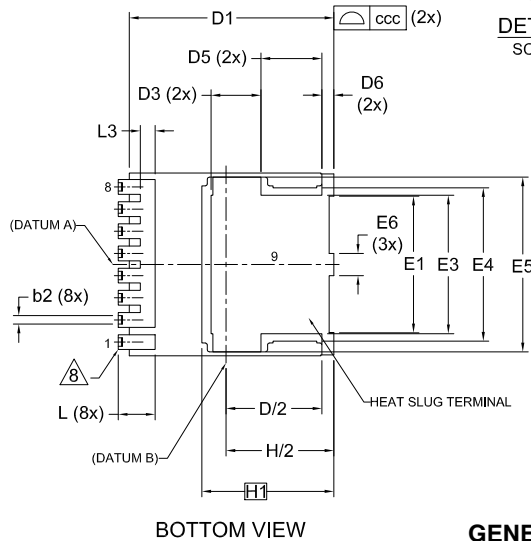
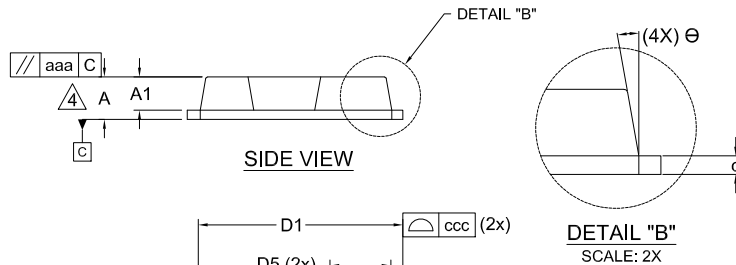
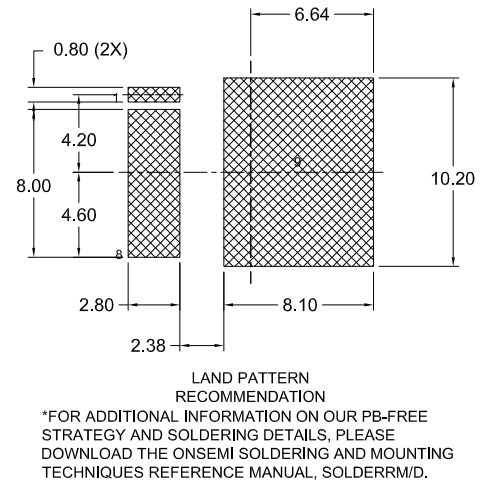
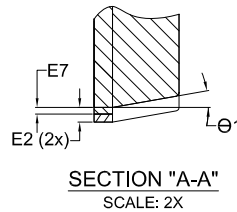
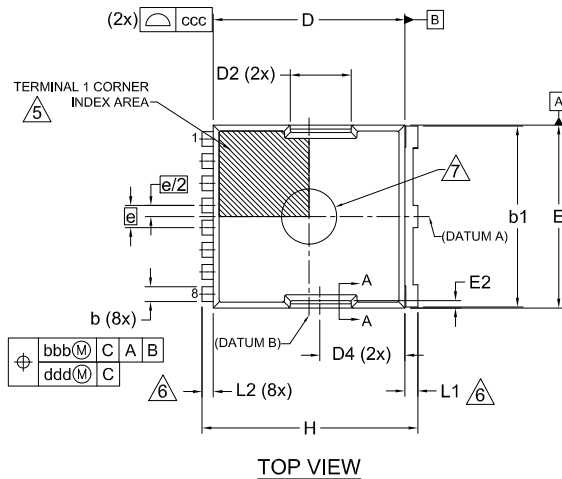


Figure 13. Thermal Characteristics (Junction-to-Ambient)



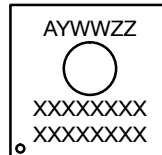
H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

DATE 30 JUL 2024



GENERIC
MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code



NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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