# Dual Digitally Controlled Potentiometer (XDCP™)

## FEATURES

- Two XDCPs in one package
- 2-wire serial interface
- Register oriented format, 8 registers total
  - —Directly write wiper position
  - —Read wiper position
  - —Store as many as four positions per pot
- Instruction format
  - —Quick transfer of register contents to resistor array
- Direct write cell
  - —Endurance–100,000 writes per bit per register
- Resistor array values
  - —2kΩ, 10kΩ, 50kΩ
- Resolution: 64 taps each pot
- 20 Ld plastic DIP and 20 Ld SOIC packages
- Pb-free plus anneal available (RoHS compliant)

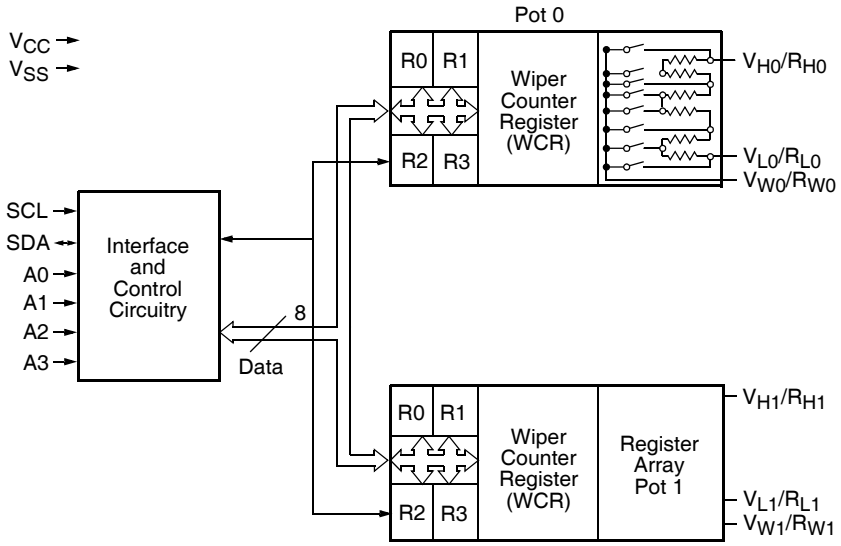
## DESCRIPTION

The X9221A integrates two digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated microcircuit.

The digitally controlled potentiometer is implemented using 63 resistive elements in a series array. Between each element are tap points connected to the wiper terminal through switches. The position of the wiper on the array is controlled by the user through the 2-wire bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and 2 non-volatile Data Registers (DR0:DR1) that can be directly written to and read by the user. The contents of the WCR controls the position of the wiper on the resistor array through the switches. Power up recalls the contents of DR0 to the WCR.

The XDCP can be used as a three-terminal potentiometer or as a two-terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

## BLOCK DIAGRAM






CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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## Ordering Information

| PART NUMBER | PART MARKING | $V_{CC}$ LIMITS (V) | $R_{TOTAL}$ (k) | TEMP RANGE (°C) | PACKAGE | PKG. DWG. # |
|---|---|---|---|---|---|---|
| X9221AYS | X9221AYS | 5 ±10% | 2 | 0 to +70 | 20 Ld SOIC (300MIL) | MDP0027 |
| X9221AYSZ (Note) | X9221AYS Z | | | 0 to +70 | 20 Ld SOIC (300MIL) (Pb-Free) | MDP0027 |
| X9221AYSI* | X9221AYSI | | | -40 to +85 | 20 Ld SOIC (300MIL) | MDP0027 |
| X9221AYSIZ* (Note) | X9221AYSI Z | | | -40 to +85 | 20 Ld SOIC (300MIL) (Pb-Free) | MDP0027 |
| X9221AWS* | X9221AWS | | 10 | 0 to +70 | 20 Ld SOIC (300MIL) | MDP0027 |
| X9221AWSZ* (Note) | X9221AWS Z | | | 0 to +70 | 20 Ld SOIC (300MIL) (Pb-Free) | MDP0027 |
| X9221AWSI* | X9221AWSI | | | -40 to +85 | 20 Ld SOIC (300MIL) | MDP0027 |
| X9221AWSIZ* (Note) | X9221AWSI Z | | | -40 to +85 | 20 Ld SOIC (300MIL) (Pb-Free) | MDP0027 |
| X9221AUP | X9221AUP | | 50 | 0 to +70 | 20 Ld PDIP | MDP0031 |
| X9221AUPZ (Note) | X9221AUPZ | | | 0 to +70 | 20 Ld PDIP (Pb-Free) | MDP0031 |
| X9221AUPI | X9221AUPI | | | -40 to +85 | 20 Ld PDIP | MDP0031 |
| X9221AUPIZ (Note) | X9221AUPIZ | | | -40 to +85 | 20 Ld PDIP (Pb-Free) | MDP0031 |
| X9221AUSI* | X9221AUSI | | | -40 to +85 | 20 Ld SOIC (300MIL) | MDP0027 |
| X9221AUSIZ* (Note) | X9221AUSI Z | | | -40 to +85 | 20 Ld SOIC (300MIL) (Pb-Free) | MDP0027 |

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## PIN DESCRIPTIONS

### *Host Interface Pins*

#### Serial Clock (SCL)

The SCL input is used to clock data into and out of the X9221A.

#### Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire-ORed with any number of open drain or open collector outputs. An open drain output requires the use of a pull-up resistor. For selecting typical values, refer to the guidelines for calculating typical values on the bus pull-up resistors graph.

#### Address

The Address inputs are used to set the least significant 4 bits of the 8-bit slave address. A match in the slave address serial data stream must be made with the Address input in order to initiate communication with the X9221A

### *Potentiometer Pins*

#### $V_H/R_H(V_{H0}/R_{H0}-V_{H1}/R_{H1})$, $V_L/R_L$ ($V_{L0}/R_{L0}-V_{L1}/R_{L1}$)

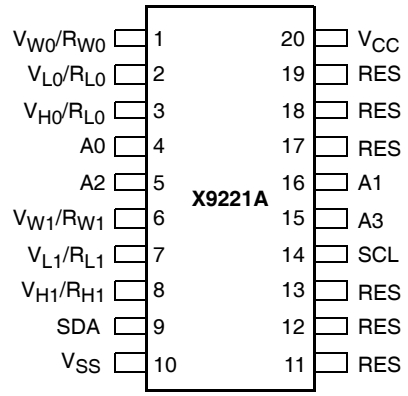
The $V_H/R_H$ and $V_L/R_L$ inputs are equivalent to the terminal connections on either end of a mechanical potentiometer.

#### $V_W/R_W$ ($V_{W0}/R_{W0}-V_{W1}/R_{W1}$)

The wiper outputs are equivalent to the wiper output of a mechanical potentiometer.

## PIN CONFIGURATION

DIP/SOIC






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## PIN NAMES

| Symbol | Description |
|---|---|
| SCL | Serial Clock |
| SDA | Serial Data |
| A0–A3 | Address |
| $V_{H0}/R_{H0}$-$V_{H1}/R_{H1}$, $V_{L0}/R_{H0}$-$V_{L1}/R_{L0}$ | Potentiometers (terminal equivalent) |
| $V_{W0}/R_{W0}$-$V_{W1}/R_{W1}$ | Potentiometers (wiper equivalent) |
| RES | Reserved (Do not connect) |

## PRINCIPLES OF OPERATION

The X9221A is a highly integrated microcircuit incorporating two resistor arrays, their associated registers and counters and the serial interface logic providing direct communication between the host and the XDCP potentiometers.

### Serial Interface

The X9221A supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is a master and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the X9221A will be considered a slave device in all applications.

### Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW periods ($t_{LOW}$). SDA state changes during SCL HIGH are reserved for indicating start and stop conditions.

### Start Condition

All commands to the X9221A are preceded by the start condition, which is a HIGH to LOW transition of SDA while SCL is HIGH ($t_{HIGH}$). The X9221A continuously monitors the SDA and SCL lines for the start condition, and will not respond to any command until this condition is met.

### Stop Condition

All communications must be terminated by a stop condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

### Acknowledge

Acknowledge is a software convention used to provide a positive handshake between the master and slave devices on the bus to indicate the successful receipt of data. The transmitting device, either the master or the slave, will release the SDA bus after transmitting eight bits. The master generates a ninth clock cycle and during this period the receiver pulls the SDA line LOW to acknowledge that it successfully received the eight bits of data. See Figure 7.

The X9221A will respond with an acknowledge after recognition of a start condition and its slave address and once again after successful receipt of the command byte. If the command is followed by a data byte the X9221A will respond with a final acknowledge.

### Array Description

The X9221A is comprised of two resistor arrays. Each array contains 63 discrete resistive segments that are connected in series. The physical ends of each array are equivalent to the fixed terminals of a mechanical potentiometer ($V_H/R_H$ and $V_L/R_L$ inputs).

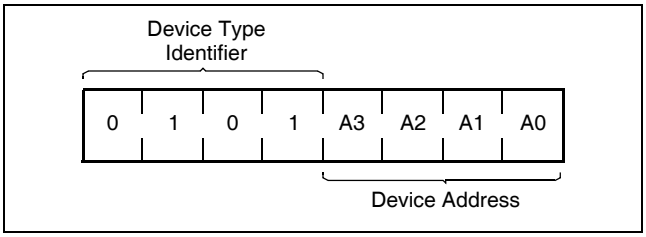
At both ends of each array and between each resistor segment is a FET switch connected to the wiper ($V_W/R_W$) output. Within each individual array only one switch may be turned on at a time. These switches are controlled by the Wiper Counter Register (WCR). The six least significant bits of the WCR are decoded to select, and enable, one of sixty-four switches.

The WCR may be written directly, or it can be changed by transferring the contents of one of four associated data registers into the WCR. These data registers and the WCR can be read and written by the host system.

### Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (refer to Figure 1 below). For the X9221A this is fixed as 0101[B].

**Figure 1. Slave Address**





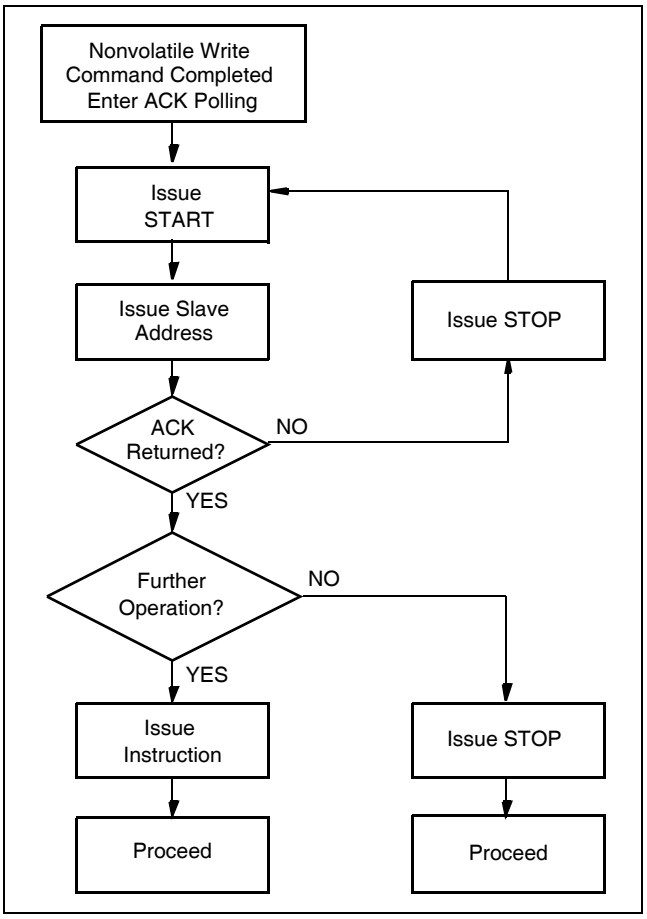

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The next four bits of the slave address are the device address. The physical device address is defined by the state of the A0-A3 inputs. The X9221A compares the serial data stream with the address input state; a successful compare of all four address bits is required for the X9221A to respond with an acknowledge.

### Acknowledge Polling

The disabling of the inputs, during the internal nonvolatile write operation, can be used to take advantage of the typical 5ms EEPROM write cycle time. Once the stop condition is issued to indicate the end of the nonvolatile write command the X9221A initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the device slave address. If the X9221A is still busy with the write operation no ACK will be returned. If the X9221A has completed the write operation an ACK will be returned and the master can then proceed with the next operation.

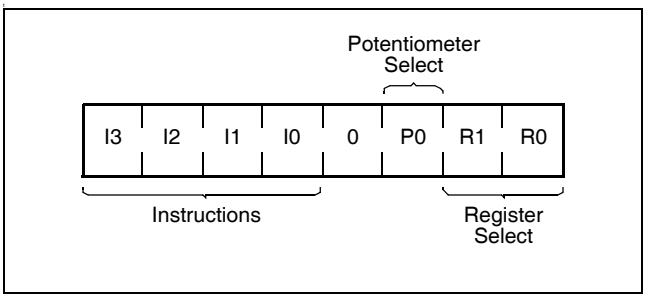
**Flow 1. ACK Polling Sequence**




### Instruction Structure

The next byte sent to the X9221A contains the instruction and register pointer information. The four most significant bits are the instruction. The next four bits point to one of two pots and when applicable they point to one of four associated registers. The format is shown below in Figure 2.

**Figure 2. Instruction Byte Format**




The four high order bits define the instruction. The sixth bit (P0) selects which one of the two potentiometers is to be affected by the instruction. The last two bits (R1 and R0) select one of the four registers that is to be acted upon when a register oriented instruction is issued.

Four of the nine instructions end with the transmission of the instruction byte. The basic sequence is illustrated in Figure 3. These two-byte instructions exchange data between the WCR and one of the data registers. A transfer from a data register to a WCR is essentially a write to a static RAM. The response of the wiper to this action will be delayed $t_{STPWV}$. A transfer from WCR's current wiper position to a data register is a write to nonvolatile memory and takes a minimum of $t_{WR}$ to complete. The transfer can occur between either potentiometer and their associated registers or it may occur between both of the potentiometers and one of their associated registers.

Four instructions require a three-byte sequence to complete. These instructions transfer data between the host and the X9221A; either between the host and one of the data registers or directly between the host and the WCR. These instructions are: Read WCR, read the current wiper position of the selected pot; Write WCR, change current wiper position of the selected pot; Read Data Register, read the contents of the selected nonvolatile register; Write Data Register, write a new value to the selected data register. The sequence of operations is shown in Figure 4.

The Increment/Decrement command is different from the other commands. Once the command is issued and the X9221A has responded with an acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine



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tuning capability to the host. For each SCL clock pulse ($t_{HIGH}$) while SDA is HIGH, the selected wiper will move one resistor segment towards the $V_H/R_H$ terminal. Similarly, for each SCL clock pulse while SDA is LOW, the selected wiper will move one resistor segment towards the $V_L/R_L$ terminal. A detailed illustration of the sequence and timing for this operation are shown in Figures 5 and 6 respectively.

**Figure 3. Two-Byte Command Sequence**

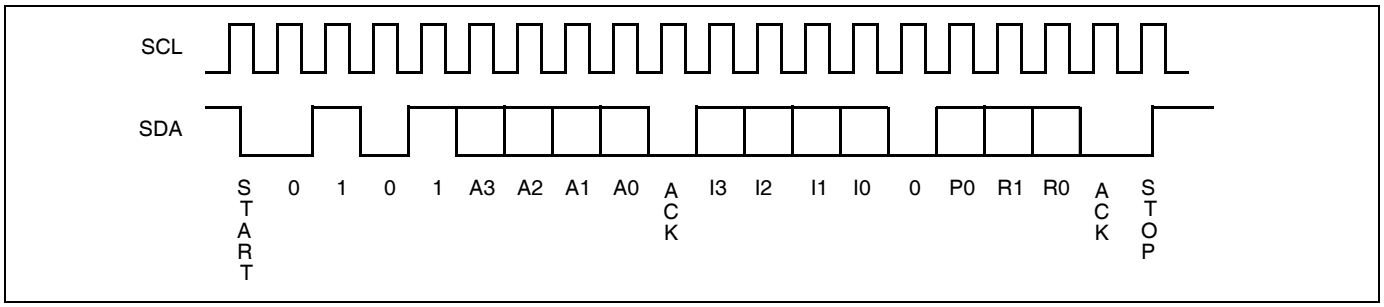



**Figure 4. Three-Byte Command Sequence**

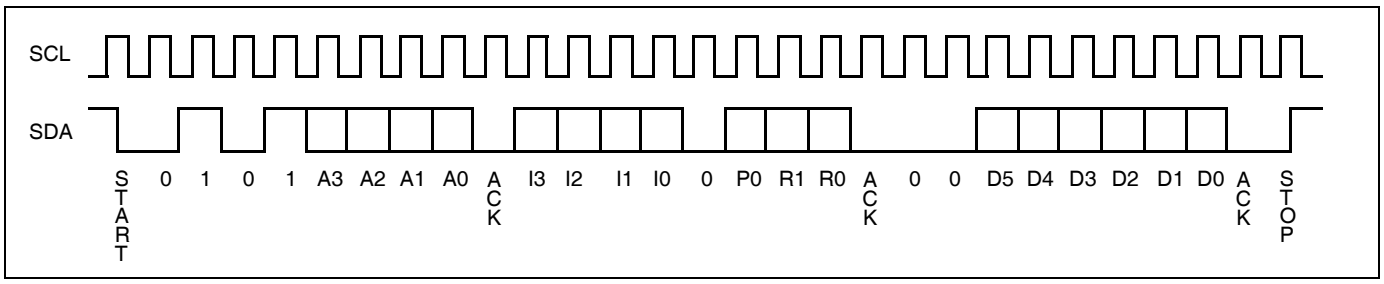
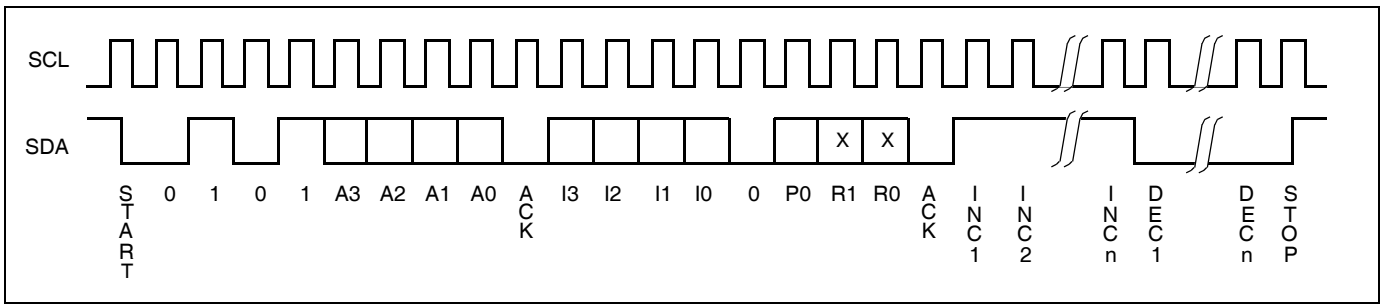



**Figure 5. Increment/Decrement Command Sequined**






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**Figure 6. Increment/Decrement Timing Limits**

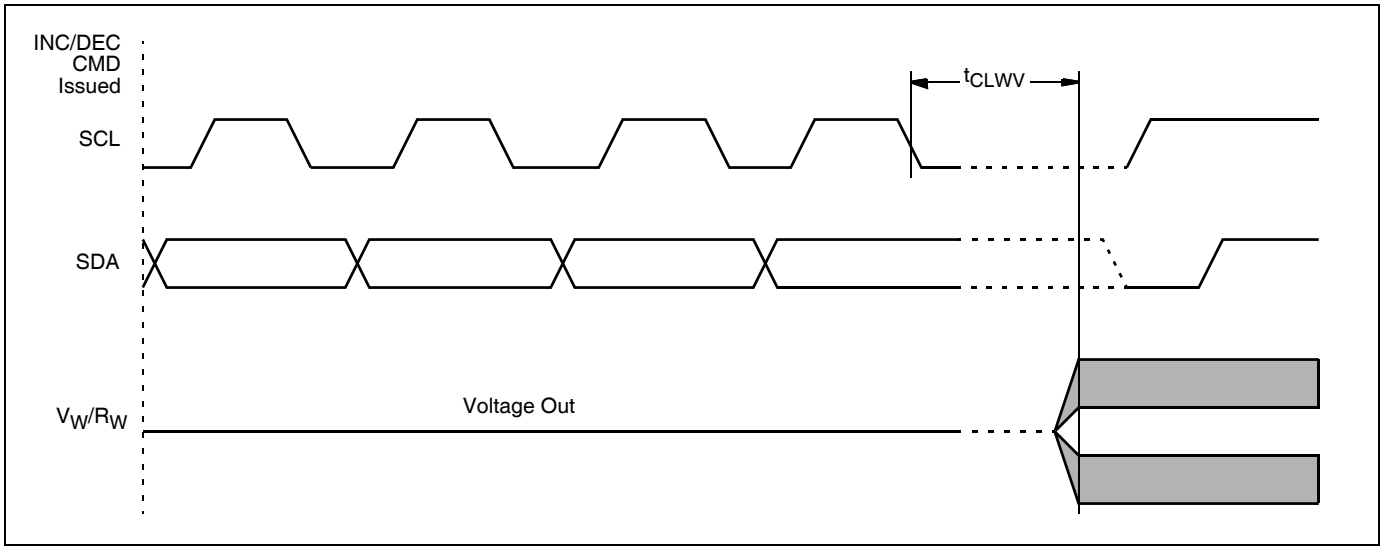



**Table 1. Instruction Set**

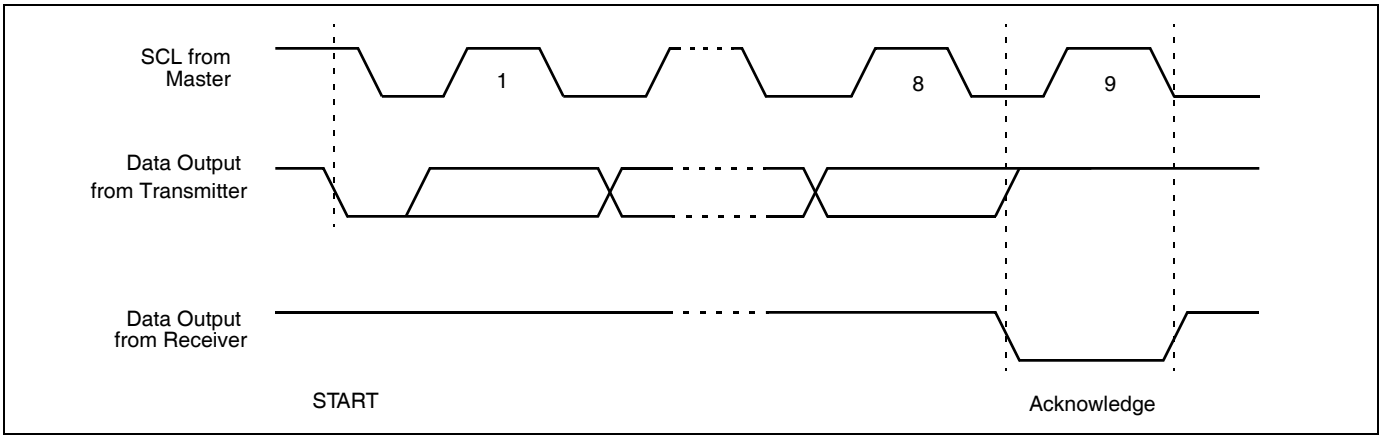
| Instruction | Instruction Format | | | | | | | | Operation |
|---|---|---|---|---|---|---|---|---|---|
| | $I_3$ | $I_2$ | $I_1$ | $I_0$ | 0 | $P_0$ | $R_1$ | $R_0$ | |
| Read WCR | 1 | 0 | 0 | 1 | 0 | 1/0 | N/A(7) | N/A | Read the contents of the Wiper Counter Register pointed to by $P_0$ |
| Write WCR | 1 | 0 | 1 | 0 | 0 | 1/0 | N/A | N/A | Write new value to the Wiper Counter Register pointed to by $P_0$ |
| Read Data Register | 1 | 0 | 1 | 1 | 0 | 1/0 | 1/0 | 1/0 | Read the contents of the Register pointed to by $P_0$ and $R_1$–$R_0$ |
| Write Data Register | 1 | 1 | 0 | 0 | 0 | 1/0 | 1/0 | 1/0 | Write new value to the Register pointed to by $P_0$ and $R_1$–$R_0$ |
| XFR Data Register to WCR | 1 | 1 | 0 | 1 | 0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the Register pointed to by $P_0$ and $R_1$–$R_0$ to its associated WCR |
| XFR WCR to Data Register | 1 | 1 | 1 | 0 | 0 | 1/0 | 1/0 | 1/0 | Transfer the contents of the WCR pointed to by $P_0$ to the Register pointed to by $R_1$–$R_0$ |
| Global XFR Data Register to WCR | 0 | 0 | 0 | 1 | N/A | N/A | 1/0 | 1/0 | Transfer the contents of the Data Registers pointed to by $R_1$–$R_0$ of both pots to their respective WCR |
| Global XFR WCR to Data Register | 1 | 0 | 0 | 0 | N/A | N/A | 1/0 | 1/0 | Transfer the contents of all WCRs to their respective data Registers pointed to by $R_1$–$R_0$ of both pots |
| Increment/Decrement Wiper | 0 | 0 | 1 | 0 | 0 | 1/0 | N/A | N/A | Enable Increment/decrement of the WCR pointed to by $P_0$ |

**Note:** (7) N/A = Not applicable or don't care; that is, a data register is not involved in the operation and need not be addressed (typical)



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**Figure 7. Acknowledge Response from Receiver**




## DETAILED OPERATION

Both XDCP potentiometers share the serial interface and share a common architecture. Each potentiometer is comprised of a resistor array, a wiper counter register and four data registers. A detailed discussion of the register organization and array operation follows.

### Wiper Counter Register

The X9221A contains two wiper counter registers (WCR), one for each XDCP potentiometer. The WCR can be envisioned as a 6-bit parallel and serial load counter with its outputs decoded to select one of sixty-four switches along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write WCR instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction; finally, it is loaded with the contents of its data register zero (R0) upon power-up.

The WCR is a volatile register; that is, its contents are lost when the X9221A is powered-down. Although the register is automatically loaded with the value in R0 upon power-up, it should be noted this may be different from the value present at power-down.

### Data Registers

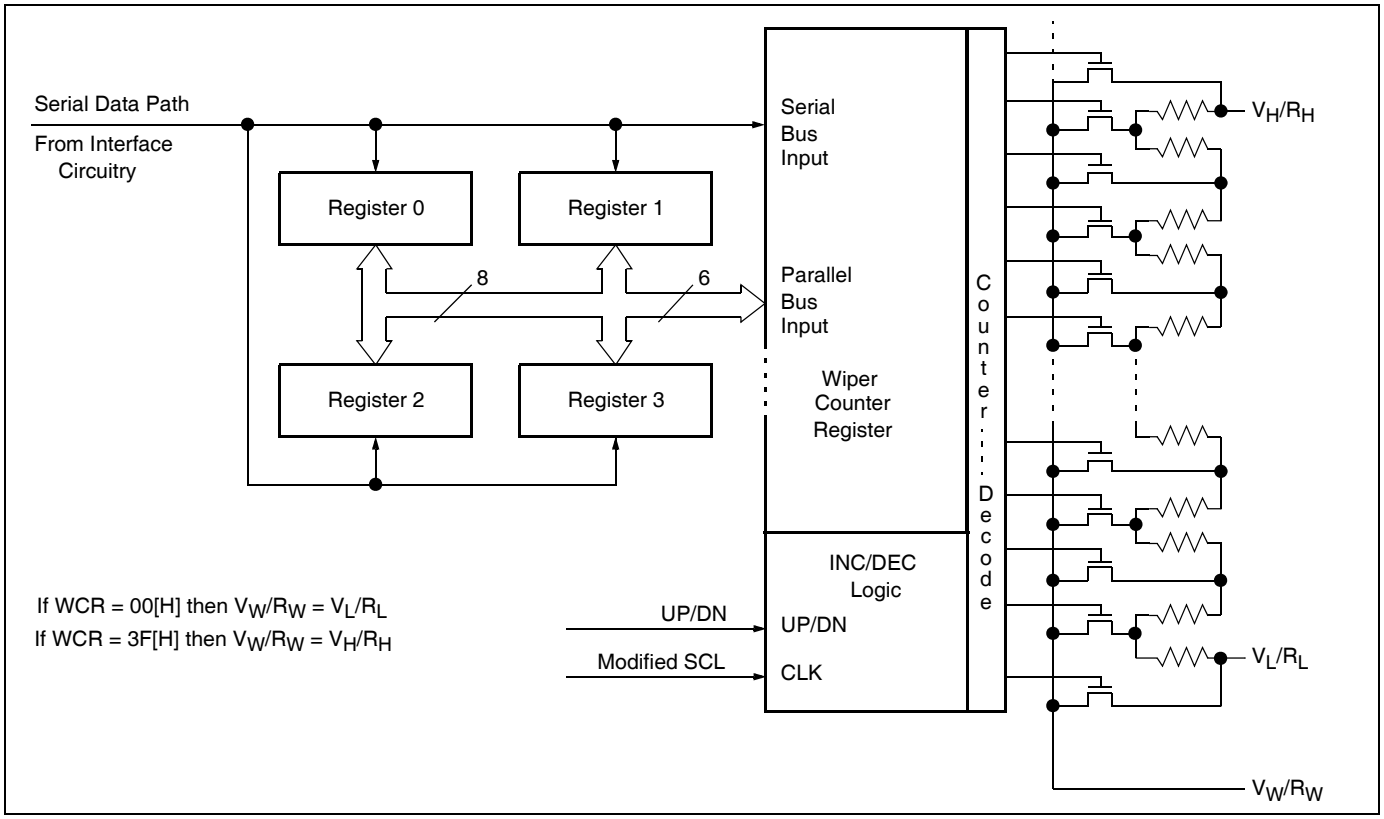
Each potentiometer has four nonvolatile data registers. These can be read or written directly by the host and data can be transferred between any of the four data registers and the WCR. It should be noted all operations changing data in one of these registers is a nonvolatile operation and will take a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, these registers can be used as regular memory locations that could possibly store system parameters or user preference data.



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**Figure 8. Detailed Potentiometer Block Diagram**






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## ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -65°C to +135°C
Storage Temperature ..... -65°C to +150°C
Voltage on SCK, SCL or Any Address
Input With Respect to $V_{SS}$ ..... -1V to +7V
Voltage on Any $V_H/R_H$, $V_W/R_W$ or $V_L/R_L$
Referenced to $V_{SS}$ ..... +6V / -4.3V
$\Delta V = |V_H/R_H – V_L/R_L|$ ..... 10.3V
Lead Temperature (soldering, 10s) ..... +300°C
$I_W$ (10s) ..... ±6mA

## COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

| Temp | Min. | Max. |
|---|---|---|
| Commercial | 0°C | +70°C |
| Industrial | -40°C | +85°C |

| Supply Voltage | Limits |
|---|---|
| X9221A | 5V ± 10% |

**ANALOG CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| $R_{TOTAL}$ | End to End Resistance | -20 | | +20 | % | |
| | Power Rating | | | 50 | mW | +25°C, each pot |
| $I_W$ | Wiper Current | -3 | | +3 | mA | |
| $R_W$ | Wiper Resistance | | 40 | 130 | Ω | Wiper Current = ±1mA |
| $V_{TERM}$ | Voltage on any $V_H/R_H$, $V_W/R_W$ or $V_L/R_L$ Pin | -3.0 | | +5 | V | |
| | Noise | | ≤120 | | dBV | Ref: 1V |
| | Resolution | | 1.6 | | % | See Note 5 |
| | Absolute Linearity(1) | -1 | | +1 | MI(3) | $V_{w(n)(actual} - V_{w(n)(expected)}$ |
| | Relative Linearity(2) | -0.2 | | +0.2 | MI(3) | $V_{w(n+1)} - [V_{w(n)} + MI]$ |
| | Temperature Coefficient | | ±300 | | ppm/°C | See Note 5 |
| | Radiometric Temperature Coefficient | | | ±20 | ppm/°C | See Note 5 |
| $C_H/C_L/C_W$ | Potentiometer Capacitances | | 10/10/25 | | pF | See circuit #3 |



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**D.C. OPERATING CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated.)

| Symbol | Parameter | Limits | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Unit | |
| $I_{CC}$ | Supply Current (Active) | | | 3 | mA | $f_{SCL}$ = 100kHz, SDA = Open, Other Inputs = $V_{SS}$ |
| $I_{SB}$ | $V_{CC}$ Current (Standby) | | 200 | 500 | µA | SCL = SDA = $V_{CC}$, Addr. = $V_{SS}$ |
| $I_{LI}$ | Input Leakage Current | | | 10 | µA | $V_{IN}$ = $V_{SS}$ to $V_{CC}$ |
| $I_{LO}$ | Output Leakage Current | | | 10 | µA | $V_{OUT}$ = $V_{SS}$ to $V_{CC}$ |
| $V_{IH}$ | Input HIGH Voltage | 2 | | $V_{CC}$ + 1 | V | |
| $V_{IL}$ | Input LOW Voltage | -1 | | 0.8 | V | |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 | V | $I_{OL}$ = 3mA |

**Notes:** (1) Absolute Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
(2) Relative Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
(3) MI = RTOT/63 or ($V_H$/$R_H$–$V_L$/$R_L$)/63, single pot

**ENDURANCE AND DATA RETENTION**

| Parameter | Min. | Unit |
|---|---|---|
| Minimum endurance | 100,000 | Data changes per bit per register |
| Data retention | 100 | years |

**CAPACITANCE**

| Symbol | Parameter | Max. | Unit | Test Conditions |
|---|---|---|---|---|
| $C_{I/O}$(5) | Input/output capacitance (SDA) | 8 | pF | $V_{I/O}$ = 0V |
| $C_{IN}$(5) | Input capacitance (A0, A1, A2, A3 and SCL) | 6 | pF | $V_{IN}$ = 0V |

**POWER-UP TIMING**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{PUR}$(6) | Power-up to initiation of read operation | | 1 | ms |
| $t_{PUW}$(6) | Power-up to initiation of write operation | | 5 | ms |
| $t_R V_{CC}$ | $V_{CC}$ Power-up ramp rate | 0.2 | 50 | V/ms |

**Notes:** (5) This parameter is periodically sampled and not 100% tested.
(6) $t_{PUR}$ and $t_{PUW}$ are the delays required from the time $V_{CC}$ is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

**Power Up Requirements** (Power up sequencing can affect correct recall of the wiper registers)

The preferred power-on sequence is as follows: First $V_{CC}$, then the potentiometer pins. It is suggested that $V_{CC}$ reach 90% of its final value before power is applied to the potentiometer pins. The $V_{CC}$ ramp rate specification should be met, and any glitches or slope changes in the $V_{CC}$ line should be held to <100mV if possible. Also, $V_{CC}$ should not reverse polarity by more than 0.5V.



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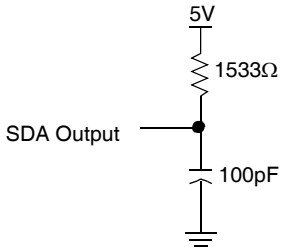
## A.C. CONDITIONS OF TEST

| | |
|---|---|
| Input pulse levels | $V_{CC}$ x 0.1 to $V_{CC}$ x 0.9 |
| Input rise and fall times | 10ns |
| Input and output timing levels | $V_{CC}$ x 0.5 |

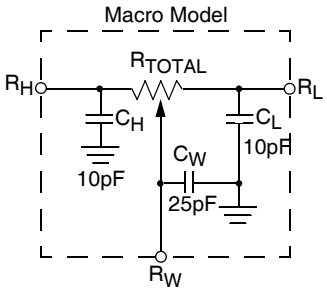
## SYMBOL TABLE

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be steady | Will be steady |
| | May change from LOW to HIGH | Will change from LOW to HIGH |
| | May change from HIGH to LOW | Will change from HIGH to LOW |
| | Don't Care: Changes Allowed | Changing: State Not Known |
| | N/A | Center Line is High Impedance |

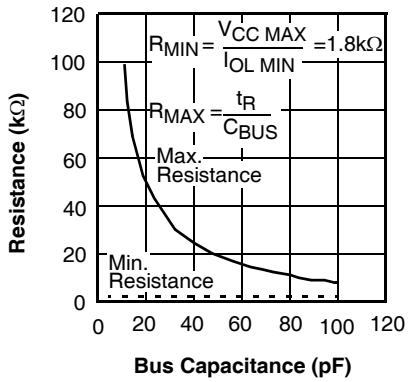
## Equivalent A.C. Test Circuit




## Circuit #3 SPICE Macro Model




## Guidelines for Calculating Typical Values of Bus Pull-Up Resistors






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**A.C. CHARACTERISTICS** (Over recommended operating conditions unless otherwise stated)

| Symbol | Parameter | Limits | | Unit | Reference Figure |
|---|---|---|---|---|---|
| | | Min. | Max. | | |
| $f_{SCL}$ | SCL clock frequency | 0 | 100 | kHz | 10 |
| $t_{LOW}$ | Clock LOW period | 4700 | | ns | 10 |
| $t_{HIGH}$ | Clock HIGH period | 4000 | | ns | 10 |
| $t_R$ | SCL and SDA rise time | | 1000 | ns | 10 |
| $t_F$ | SCL and SDA fall time | | 300 | ns | 10 |
| $T_i$ | Noise suppression time constant (glitch filter) | | 100 | ns | 10 |
| $t_{SU:STA}$ | Start condition setup time (for a repeated start condition) | 4700 | | ns | 10 & 12 |
| $t_{HD:STA}$ | Start condition hold time | 4000 | | ns | 10 & 12 |
| $t_{SU:DAT}$ | Data in setup time | 250 | | ns | 10 |
| $t_{HD:DAT}$ | Data in hold time | 0 | | ns | 10 |
| $t_{AA}$ | SCL LOW to SDA data out valid | 300 | 3500 | ns | 11 |
| $t_{DH}$ | Data out hold time | 300 | | ns | 11 |
| $t_{SU:STO}$ | Stop condition setup time | 4700 | | ns | 10 & 12 |
| $t_{BUF}$ | Bus free time prior to new transmission | 4700 | | ns | 10 |
| $t_{WR}$ | Write cycle time (nonvolatile write operation) | | 10 | ms | 13 |
| $t_{STPWV}$ | Wiper response time from stop generation | | 1000 | µs | 13 |
| $t_{CLWV}$ | Wiper response from SCL LOW | | 500 | µs | 6 |

## TIMING DIAGRAMS

**Figure 10. Input Bus Timing**

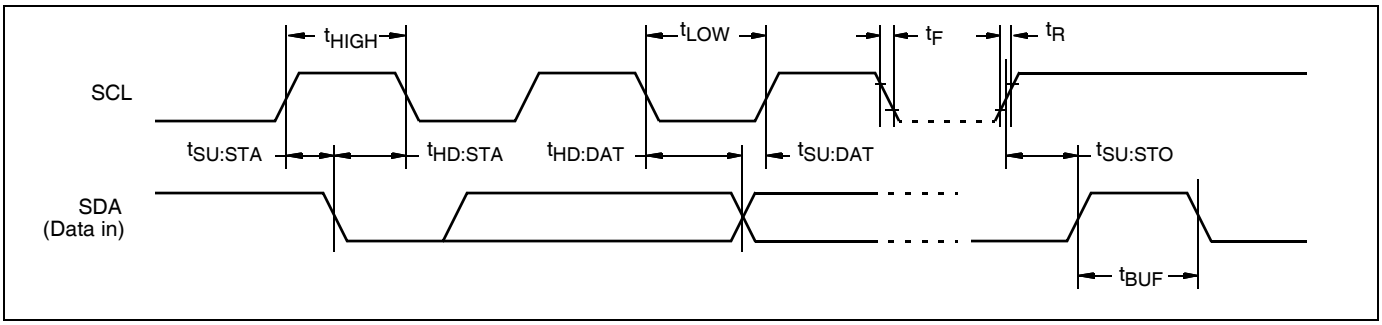
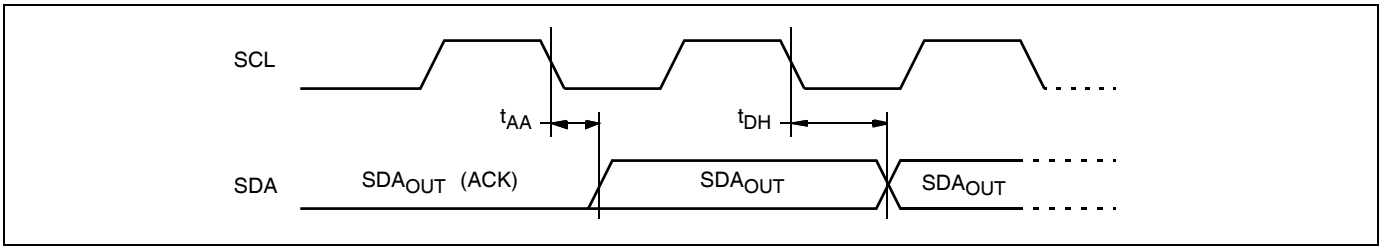



**Figure 11. Output Bus Timing**






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**Figure 12. Start Stop Timing**

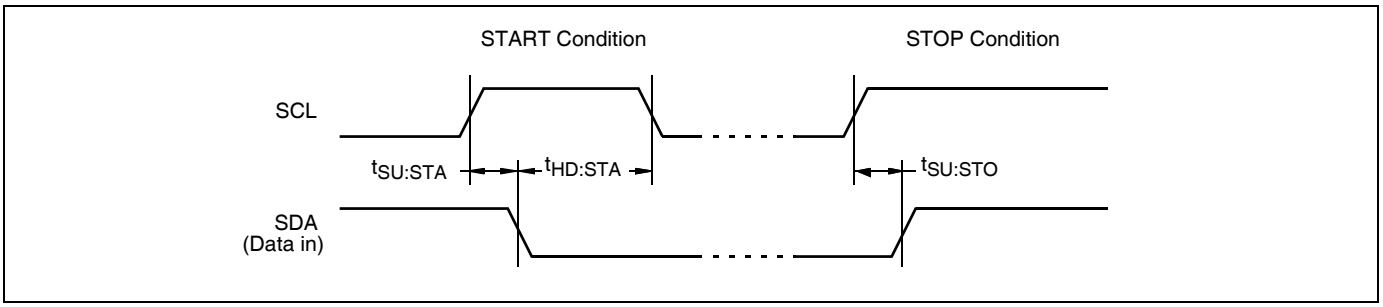
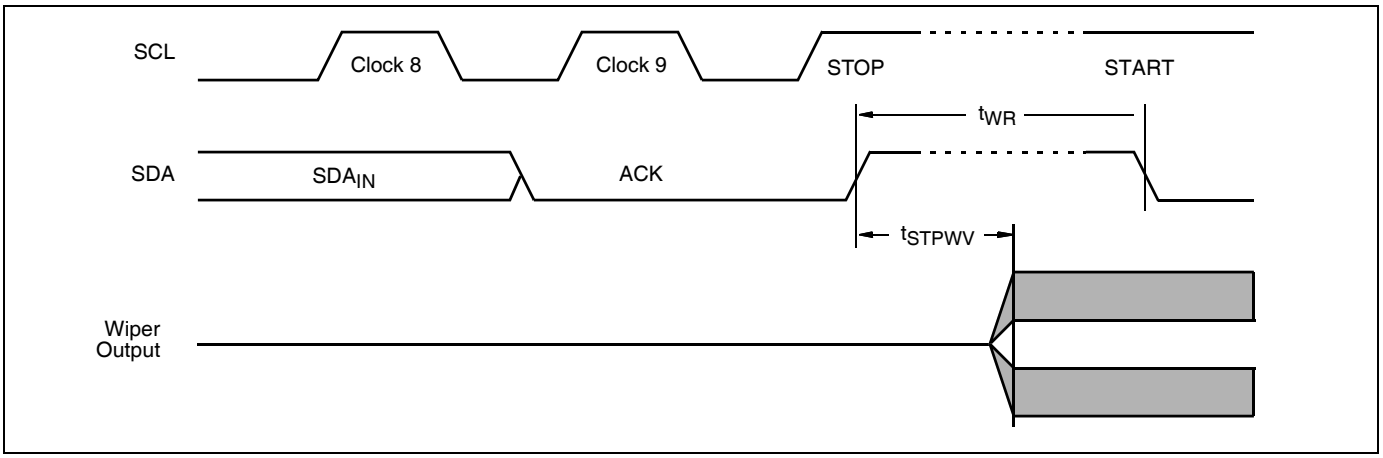


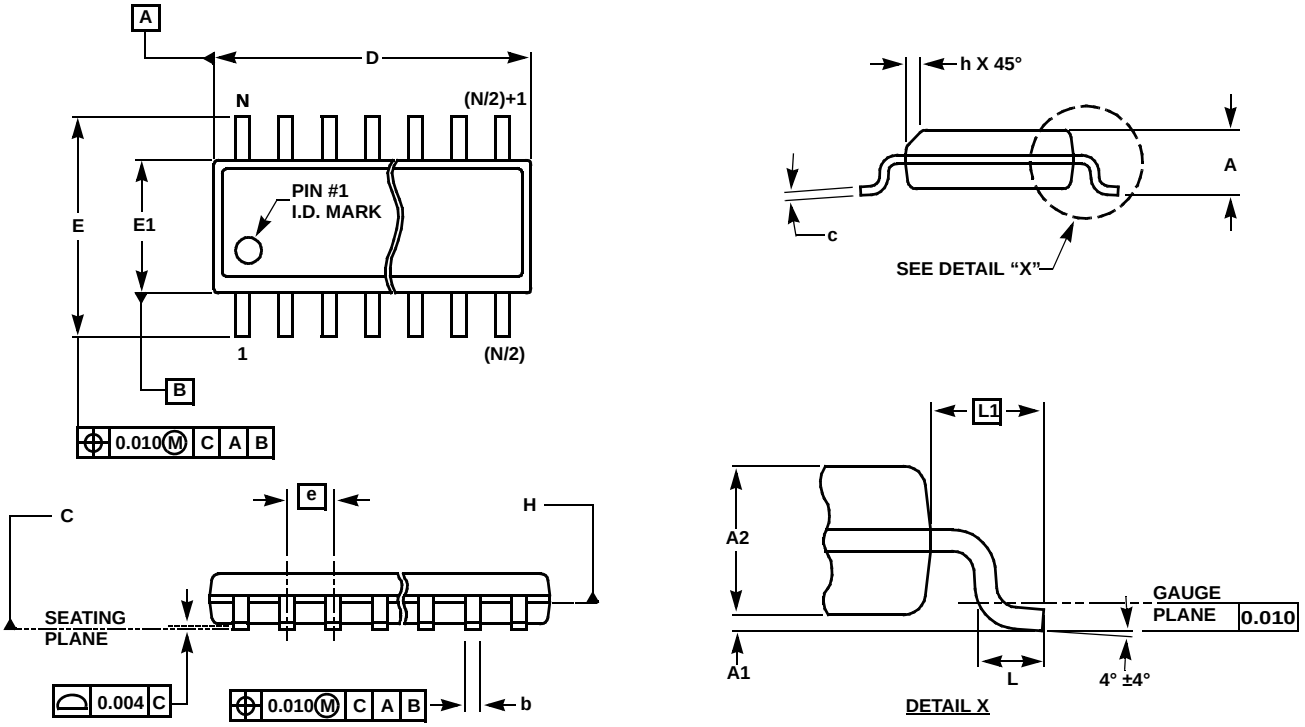

**Figure 13. Write Cycle and Wiper Response Timing**






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## Small Outline Package Family (SO)




### MDP0027

**SMALL OUTLINE PACKAGE FAMILY (SO)**

| SYMBOL | SO-8 | SO-14 | SO16 (0.150") | SO16 (0.300") (SOL-16) | SO20 (SOL-20) | SO24 (SOL-24) | SO28 (SOL-28) | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|---|---|
| A | 0.068 | 0.068 | 0.068 | 0.104 | 0.104 | 0.104 | 0.104 | MAX | - |
| A1 | 0.006 | 0.006 | 0.006 | 0.007 | 0.007 | 0.007 | 0.007 | ±0.003 | - |
| A2 | 0.057 | 0.057 | 0.057 | 0.092 | 0.092 | 0.092 | 0.092 | ±0.002 | - |
| b | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | 0.017 | ±0.003 | - |
| c | 0.009 | 0.009 | 0.009 | 0.011 | 0.011 | 0.011 | 0.011 | ±0.001 | - |
| D | 0.193 | 0.341 | 0.390 | 0.406 | 0.504 | 0.606 | 0.704 | ±0.004 | 1, 3 |
| E | 0.236 | 0.236 | 0.236 | 0.406 | 0.406 | 0.406 | 0.406 | ±0.008 | - |
| E1 | 0.154 | 0.154 | 0.154 | 0.295 | 0.295 | 0.295 | 0.295 | ±0.004 | 2, 3 |
| e | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | 0.050 | Basic | - |
| L | 0.025 | 0.025 | 0.025 | 0.030 | 0.030 | 0.030 | 0.030 | ±0.009 | - |
| L1 | 0.041 | 0.041 | 0.041 | 0.056 | 0.056 | 0.056 | 0.056 | Basic | - |
| h | 0.013 | 0.013 | 0.013 | 0.020 | 0.020 | 0.020 | 0.020 | Reference | - |
| N | 8 | 14 | 16 | 16 | 20 | 24 | 28 | Reference | - |

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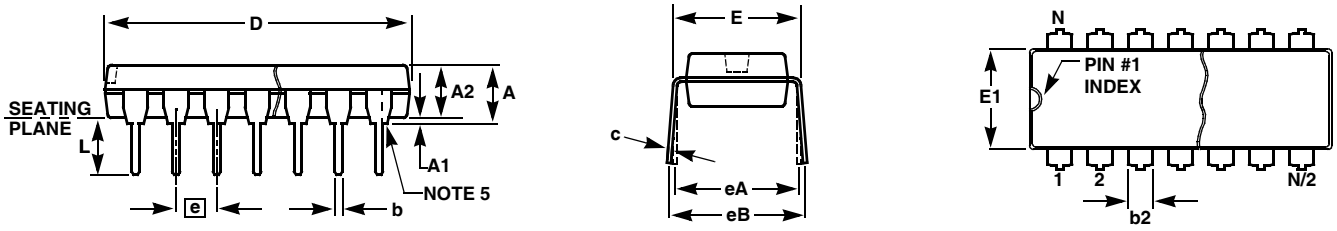
NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994



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## Plastic Dual-In-Line Packages (PDIP)




### MDP0031

**PLASTIC DUAL-IN-LINE PACKAGE**

| SYMBOL | PDIP8 | PDIP14 | PDIP16 | PDIP18 | PDIP20 | TOLERANCE | NOTES |
|---|---|---|---|---|---|---|---|
| A | 0.210 | 0.210 | 0.210 | 0.210 | 0.210 | MAX | |
| A1 | 0.015 | 0.015 | 0.015 | 0.015 | 0.015 | MIN | |
| A2 | 0.130 | 0.130 | 0.130 | 0.130 | 0.130 | ±0.005 | |
| b | 0.018 | 0.018 | 0.018 | 0.018 | 0.018 | ±0.002 | |
| b2 | 0.060 | 0.060 | 0.060 | 0.060 | 0.060 | +0.010/-0.015 | |
| c | 0.010 | 0.010 | 0.010 | 0.010 | 0.010 | +0.004/-0.002 | |
| D | 0.375 | 0.750 | 0.750 | 0.890 | 1.020 | ±0.010 | 1 |
| E | 0.310 | 0.310 | 0.310 | 0.310 | 0.310 | +0.015/-0.010 | |
| E1 | 0.250 | 0.250 | 0.250 | 0.250 | 0.250 | ±0.005 | 2 |
| e | 0.100 | 0.100 | 0.100 | 0.100 | 0.100 | Basic | |
| eA | 0.300 | 0.300 | 0.300 | 0.300 | 0.300 | Basic | |
| eB | 0.345 | 0.345 | 0.345 | 0.345 | 0.345 | ±0.025 | |
| L | 0.125 | 0.125 | 0.125 | 0.125 | 0.125 | ±0.010 | |
| N | 8 | 14 | 16 | 18 | 20 | Reference | |

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NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

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