VC-711

Differential (LVPECL, LVDS) Crystal Oscillator

Features

- Ultra Low Jitter Performance, 3rd OT or Fundamental Crystal Design
- Extended Operating Temperature Range, -40°C to 105°C Option
- 10 MHz to 220 MHz Output Frequencies
- Excellent Power Supply Rejection Ratio
- Enable/Disable
- 1.8 (LVDS), 2.5 or 3.3V operation
- Hermetically Sealed 6-Lead 7.0 mm × 5.0 mm LDFN Ceramic Package
- Product is compliant to RoHS directive and fully compatible with lead free assembly (excluding Solder Dipped/_SNPB option)

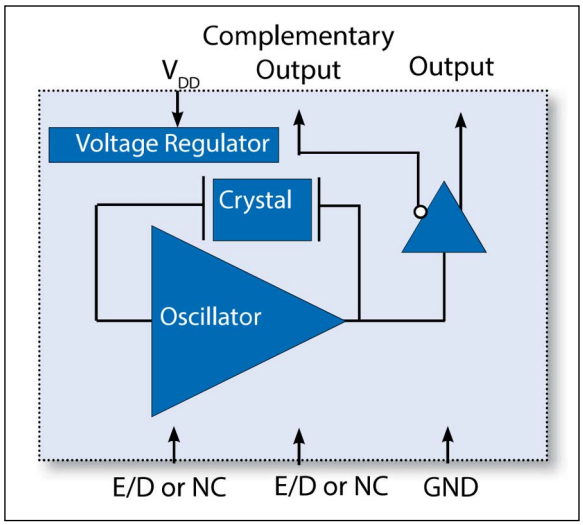
Applications

- Ethernet, GbE, Synchronous Ethernet
- PCIe
- Fiber Channel
- Enterprise Servers and Stoarge
- Test and Measurement
- GPON
- Clock source for ADC's, DAC's, FPGAs

General Description

Microchip's VC-711 Crystal Oscillator is a quartz stabilized, differential output oscillator, operating off either a 1.8V (LVDS), 2.5V, or 3.3V power supply in a hermetically sealed 6-Lead 7.0 mm × 5.0 mm LDFN ceramic package.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Supply Voltage ..... –0.5V to 5.0V
Enable/Disable Voltage ..... –0.5V to V_{DD} + 0.5V
ESD Rating, Human Body Model (Note 1) 1500V
ESD Rating, Charged Device Model (Note 1) 1500V

† Notice: Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied or any other excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Note 1: Although ESD protection circuitry has been designed into the VC-711, proper precautions should be taken when handling and mounting, Microchip employs a Human Body Model and Charged Device Model for ESD susceptibility testing and design evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry standard has been adopted for the CDM, a standard resistance of 1.5 kΩ and capacitance of 100 pF is widely used and therefor can be used for comparison purposes.

ELECTRICAL CHARACTERISTICS, LVPECL OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply						
Supply Voltage (Note 1)	V_{DD}	2.375	2.5	2.625	V	Ordering Option
		3.135	3.3	3.465		
2.5V Current Consumption	I_{DD}	—	—	61	mA	—
3.3V Current Consumption,		—	—	69		
Frequency						
Nominal Frequency	f_N	10	—	220	MHz	Ordering Option
Stability (Note 2)	—	—	—	±20	ppm	Ordering Option
		—	—	±25		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level Low (Note 3)	V_{OL}	V_{DD} – 1.810	—	V_{DD} – 1.620	V	—
Output Logic Level High (Note 3)	V_{OH}	V_{DD} – 1.025	—	V_{DD} – 0.880		
Output Rise and Fall Time (Note 3, Note 4)	t_r/t_f	—	—	450	ps	—
Load	—	50Ω into V_{DD} – 2.0V			—	—
Duty Cycle (Note 5)	DC	45	—	55	%	—

Note 1: The VC-711 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.
2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.
3: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.
4: Output rise and fall time will be 600 ps maximum for –40°C to +105°C operating temperature range.
5: Duty Cycle is measured as On/Time Period.
6: Measured using an Agilent E5052 Signal Source Analyzer at 25°C.
7: Outputs will be enabled if Enable/Disable is left open.

ELECTRICAL CHARACTERISTICS, LVPECL OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Phase Noise, 3.3V, 156.25 MHz (Note 6)	ϕ_N	—	–74	—	dBc/Hz	10 Hz
		—	–105	—		100 Hz
		—	–134	—		1 kHz
		—	–147	—		10 kHz
		—	–155	—		100 kHz
		—	–156	—		1 MHz
		—	–158	—		20 MHz
Phase Jitter, 156.25 MHz, 12 kHz to 20 MHz (Note 6)	ϕ_J	—	75	100	fs	—
Enable/Disable						
Outputs Enabled (Note 7)	V_{IH}	0.7 × V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3 × V_{DD}	V	—
Disable Time	t_D	—	—	200	ns	—
Enable/Disable Leakage Current	$I_{E/D}$	—	—	±200	uA	—
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85		
		–40	—	105		

Note 1: The VC-711 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-1 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time will be 600 ps maximum for –40°C to +105°C operating temperature range.

5: Duty Cycle is measured as On/Time Period.

6: Measured using an Agilent E5052 Signal Source Analyzer at 25°C.

7: Outputs will be enabled if Enable/Disable is left open.

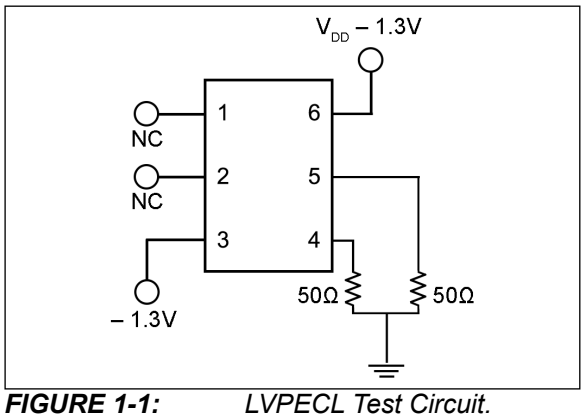


FIGURE 1-1: *LVPECL Test Circuit.*

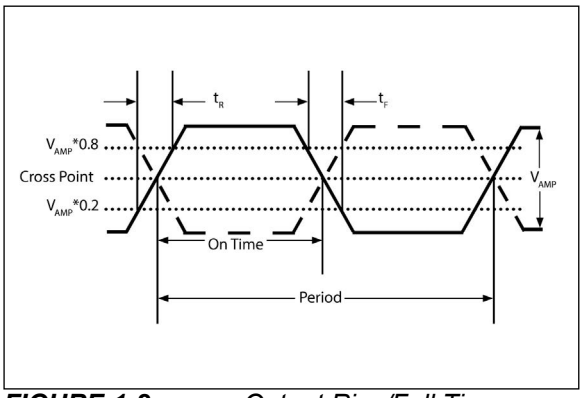


FIGURE 1-2: *Output Rise/Fall Time.*

ELECTRICAL CHARACTERISTICS, LVDS OPTION

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Supply						
Supply Voltage (Note 1)	V_{DD}	1.71	1.8	1.89	V	Ordering Option
		2.371	2.5	2.625		
		3.135	3.3	3.465		
1.8V Current Consumption	I_{DD}	—	—	21	mA	—
2.5V Current Consumption		—	—	29		
3.3V Current Consumption		—	—	33		
Frequency						
Nominal Frequency	f_N	10	—	220	MHz	Ordering Option
		100	—	175		1.8V
Stability (Note 2)	—	—	—	±20	ppm	Ordering Option
		—	—	±25		
		—	—	±50		
		—	—	±100		
Outputs						
Output Logic Level High (Note 3)	V_{OH}	—	1.43	1.6	V	—
Output Logic Level Low (Note 3)	V_{OL}	0.9	1.10	—		
Output Amplitude		247	350	454	mV	—
Differential Output Error		—	—	50	mV	—
Offset Voltage		1.125	1.25	1.375	V	—
Offset Voltage Error		—	—	50	mV	—
Output Leakage Current		—	—	10	µA	Outputs Disabled
Output Rise and Fall Time	t_r/t_f	—	—	450	ps	Note 3, Note 4
Load		100Ω Differential			—	—
Duty Cycle (Note 5)	DC	45	—	55	%	—
Phase Noise, 3.3V, 156.25 MHz (Note 6)	ϕ_N	—	–69	—	dBc/Hz	10 Hz
		—	–102	—		100 Hz
		—	–130	—		1 kHz
		—	–148	—		10 kHz
		—	–154	—		100 kHz
		—	–156	—		1 MHz
		—	–159	—		20 MHz

Note 1: The VC-711 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

3: Figure 1-3 defines the test circuit and Figure 1-2 defines these parameters.

4: Output rise and fall time will be 600 ps (max) for -40/105°C operating temperature range and 500 ps (max) for 1.8V.

5: Duty Cycle is defined as the On/Time Period.

6: Measured using an Agilent E5052 Signal Source Analyzer at 25°C.

7: Outputs will be enabled if Enable/Disable is left open.

ELECTRICAL CHARACTERISTICS, LVDS OPTION (CONTINUED)

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Phase Jitter, 156.25 MHz, 12 kHz to 20 MHz (Note 6)	ϕ_J	—	75	100	fs	—
Enable/Disable						
Outputs Enabled (Note 7)	V_{IH}	0.7 × V_{DD}	—	—	V	—
Outputs Disabled	V_{IL}	—	—	0.3 × V_{DD}	V	—
Disable Time	t_D	—	—	200	ns	—
Enable/Disable Leakage Current	$I_{E/D}$	—	—	±200	uA	
Start-Up Time	t_{SU}	—	—	10	ms	—
Operating Temperature	T_{OP}	–10	—	70	°C	Ordering Option
		–40	—	85		
		–40	—	105		

Note 1: The VC-711 power supply should be filtered. For example, a 10 µF, 0.1 µF, and 0.01 µF capacitor.

2: Includes calibration tolerance, operating temperature, supply voltage variations, aging, and IR reflow.

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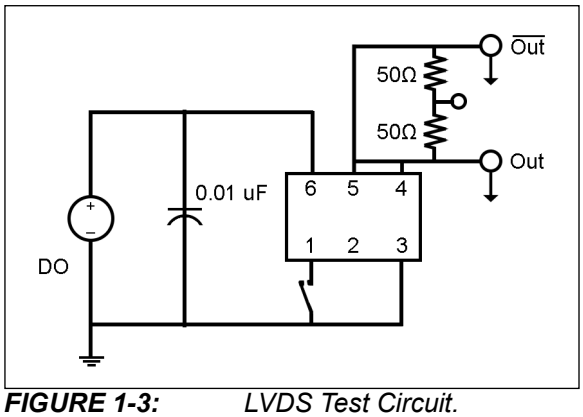


FIGURE 1-3: *LVDS Test Circuit.*

2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	E/D or NC	Enable/Disable or No Connection. (Note 1)
2	E/D or NC	Enable/Disable or No Connection. (Note 1)
3	GND	Electrical and lid ground.
4	f_O	Output frequency.
5	Cf_O	Complementary output frequency.
6	V_{DD}	Supply voltage.

Note 1: Enable/Disable can be provided on Pin 1 or Pin 2.

TABLE 2-2: ENABLE/DISABLE FUNCTION

E/D Pin	Output
High	Clock Output
Open	Clock Output
Low	High Impedance

3.0 APPLICATION DIAGRAMS

3.1 LVPECL Application Diagrams

The VC-711 incorporates a standard PECL output scheme, which are unterminated FET drains. There are numerous application notes on terminating and interfacing PECL logic and the two most common methods are a single resistor to ground, Figure 3-1, or for best 50Ω matching a pull-up/pull-down scheme as shown in Figure 3-2 should be used. AC coupling capacitors are optional, depending on the application and the input logic requirements of the next stage.

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

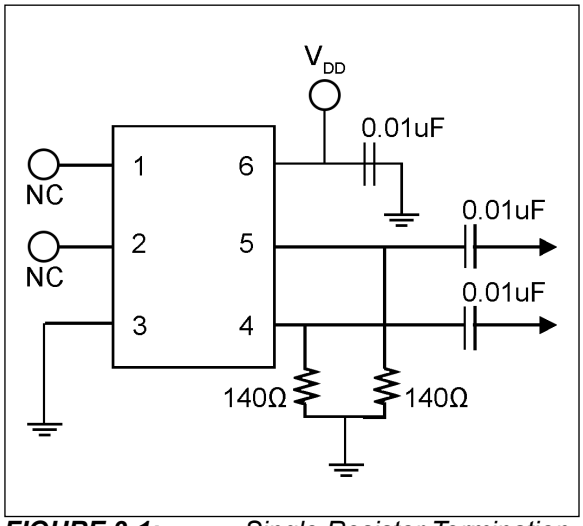


FIGURE 3-1: *Single Resistor Termination Scheme.*

Resistor values are typically 140Ω for 3.3V operation and 84Ω for 2.5V operation.

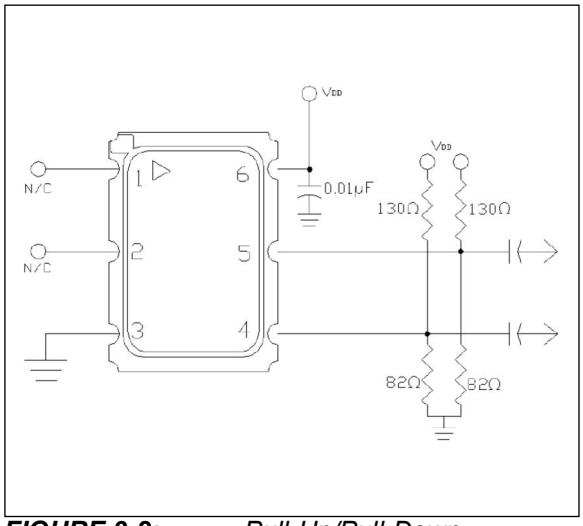


FIGURE 3-2: *Pull-Up/Pull-Down Termination.*

Resistor values shown are typical for 3.3 V operation. For 2.5V operation, the resistor to ground is 62Ω and the resistor to supply is 250Ω.

3.2 LVDS Application Diagrams

One of the most important considerations is terminating the Output and Complementary Outputs equally. An unused output should not be left unterminated, and if it one of the two outputs is left open it will result in excessive jitter on both. PC board layout must take this and 50Ω impedance matching into account. Load matching and power supply noise are the main contributors to jitter related problems.

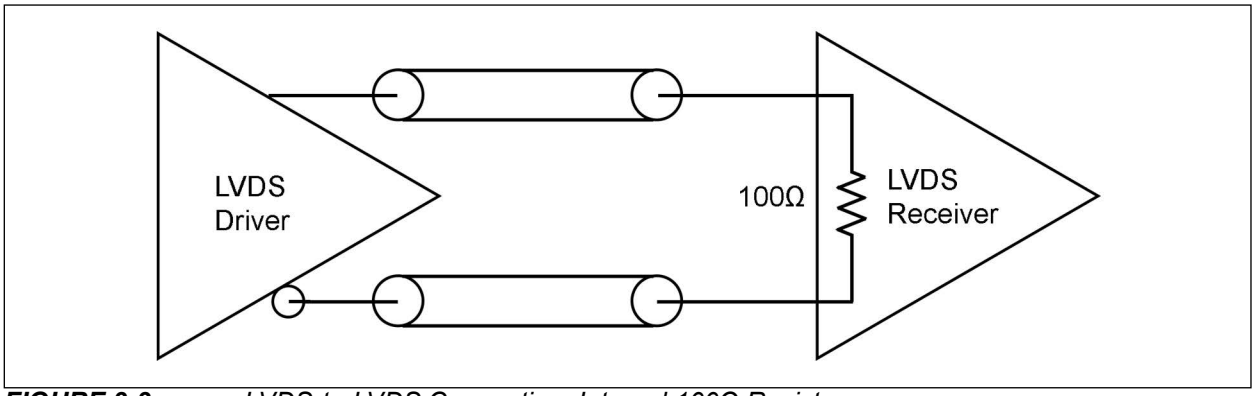


FIGURE 3-3: *LVDS-to-LVDS Connection, Internal 100Ω Resistor.*

Some LVDS structures have an internal 100Ω resistor on the input and do not need additional components. AC blocking capacitors can be used if the DC levels are incompatible.

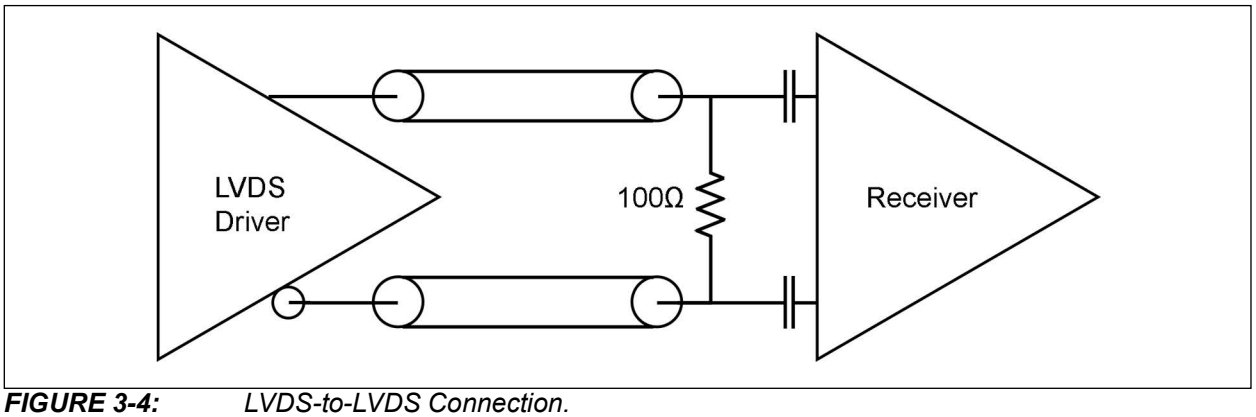


FIGURE 3-4: *LVDS-to-LVDS Connection.*

Some input structures may not have an internal 100Ω resistor on the input and will need an external 100Ω resistor for impedance matching. Also, the input may have an internal DC bias that may not be compatible with LVDS levels, AC blocking capacitors can be used.

4.0 RELIABILITY

Microchip qualification will include aging at various extreme temperatures, shock and vibration, temperature cycling, and IR reflow simulation. The VC-711 family is capable of meeting the following qualification tests.

TABLE 4-1: ENVIRONMENTAL COMPLIANCE

Parameter	Condition
Mechanical Shock	MIL-STD-883 Method 2002
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Fine and Gross Leak	MIL-STD-883 Method 1014
Rsistance to Solvents	MIL-STD-202 Method 2015
Moisture Sensitivity Level	MSL1
Contact Pads	Gold (0.3-1.0 um) over Nickel
Max Junction Temperature (θ_{JC}, bottom of case)	24°C/W, 150°C
Weight	182 mg

5.0 IR REFLOW

Devices are built using lead-free epoxy and can be subjected to standard lead free IR reflow conditions shown in Table 5-1. Contact pads are gold over nickel and lower maximum temperatures can also be used, such as 220°C.

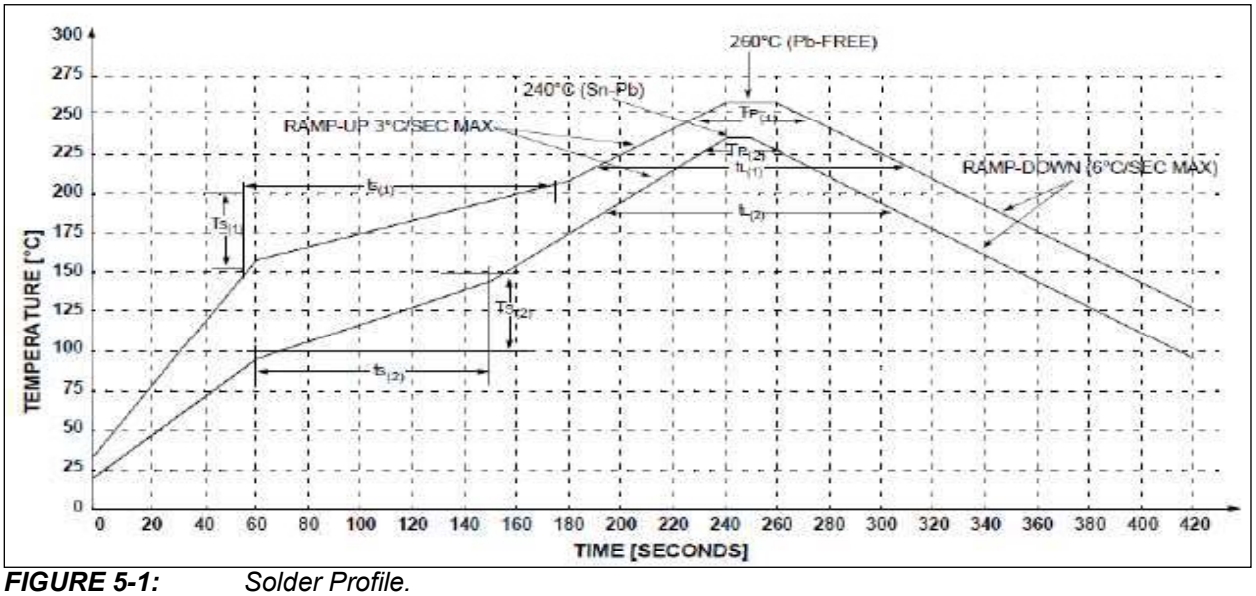


FIGURE 5-1: *Solder Profile.*

TABLE 5-1: REFLOW PROFILE

Symbol	Minimum	Maximum	Conditions
$T_{S(1)}$	150°C	200°C	Pb-Free
$T_{S(2)}$	100°C	150°C	_SNPB Option
$t_{S(1)}$	60 sec.	180 sec.	Pb-Free
$t_{S(2)}$	60 sec.	120 sec.	_SNPB Option
$t_{l(1)}$	60 sec.	150 sec.	Pb-Free
$t_{l(2)}$	60 sec.	150 sec.	_SNPB Option
$T_{p(1)}$	245°C	260°C	Pb-Free
$T_{p(2)}$	225°C	240°C	_SNPB Option

6.0 TAPE AND REEL

TABLE 6-1: TAPE AND REEL DIMENSIONS

Tape Dimensions (mm)						Reel Dimensions (mm)							
Dimension	W	F	Do	Po	P1	A	B	C	D	N	W1	W2	# per Reel
Tolerance	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Typ	Max	
VC-711	16	7.5	1.5	4	8	180	2	13	21	50	17	21	1000

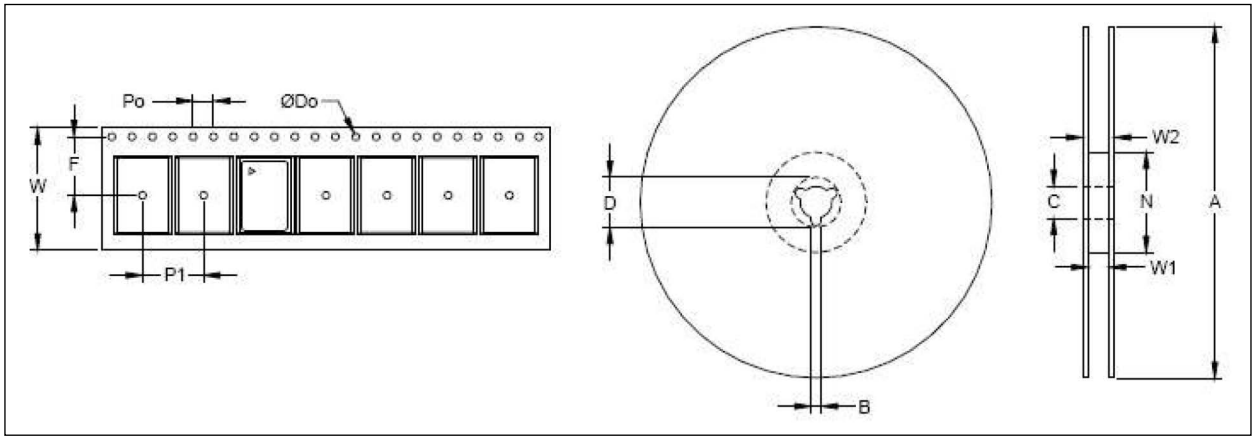


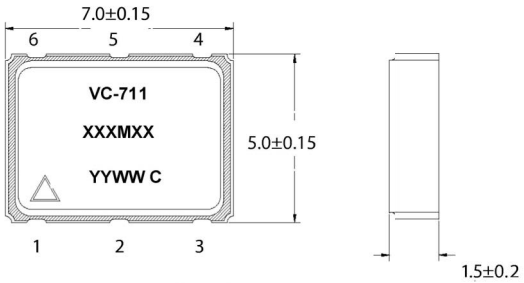
FIGURE 6-1: *Tape and Reel Diagram.*

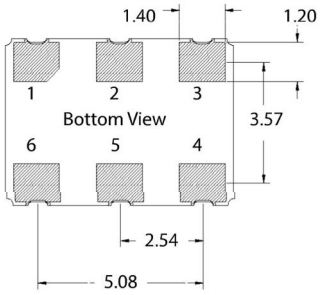
7.0 PACKAGING INFORMATION

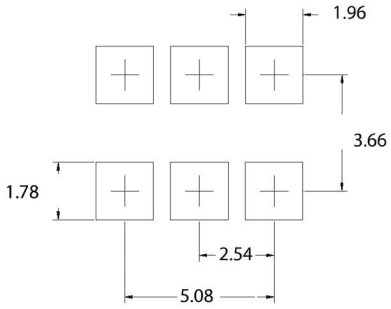
6-Lead 7 mm x 5 mm LDFN Package Outline and Recommended Land Pattern

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

Marking Information:
XXXMXX = Frequency (example: 100M00 = 100.000 MHz)
YY = Year of Manufacture
WW = Week of the Year
C = Manufacturing Location
▲ = Pin 1 Indicator







Pad Layout

Units are mm

APPENDIX A: REVISION HISTORY

Revision A (May 2025)

- Converted Vectron document VC-711 to Microchip data sheet template DS20007011A.
- Minor text changes throughout for clarity and correctness.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

Device	-X	X	X	-X	X	X	X	-XXXXXXXXXX	XX
Part No.	Power Supply	Output	Temp. Range	Stability	E/D Logic	E/D Pin	Custom Options	Frequency	Packaging

Device:	VC-711	=	Differential (LVPECL, LVDS) Crystal Oscillator in 6-Lead LDFN
Power Supply:	E	=	3.3 Vdc ±5%
	H	=	2.5 Vdc ±5%
	J	=	1.8 Vdc ±5% (LVDS)
Output:	C	=	LVPECL
	D	=	LVDS
Temperature Range:	W	=	–10°C to +70°C
	E	=	–40°C to +85°C
	F	=	–40°C to +105°C
Stability:	E	=	±20 ppm
	F	=	±25 ppm
	K	=	±50 ppm
	S	=	±100 ppm
Enable/Disable Logic:	A	=	Output Enabled with a Logic High or Open, Output is Disabled with a Logic Low
Enable/Disable Pin:	A	=	Pin 1 (Pin 2 = No Connect)
	B	=	Pin 2 (Pin 1 = No Connect)
Custom Options:	N	=	Standard option
Frequency:	xxxMxxxxxx	=	Frequency in MHz
Packaging:	TR	=	1000/Reel (LVPECL)
	<blank>	=	1000/Reel (LVDS)
	<blank>	=	Non-standard T/R or Cut Tape quantities (LVDS or LVPECL)
	_SNPB	=	Tin Lead Solder Dipped

Note 1: Not all combinations of options are available. Other specifications may be available upon request.

2: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

Examples:

a) VC-711-ECE-EAAN-156M250000TR:

VC-711, 3.3 Vdc, LVPECL Output, –40°C to +85°C Temp Range, ±20 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 156.25 MHz, 1000/Reel

b) VC-711-ECW-FAAN-160M000000:

VC-711, 3.3 Vdc, LVPECL Output, –10°C to +70°C Temp Range, ±25 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 160.00 MHz, 1/Non-standard T/R

c) VC-711-EDE-EAAN-50M000000TR:

VC-711, 3.3 Vdc, LVDS Output, –40°C to +85°C Temp Range, ±20 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 50.00 MHz, 1000/Reel

d) VC-711-HCE-FAAN-128M000000:

VC-711, 2.5 Vdc, LVPECL Output, –40°C to +85°C Temp Range, ±25 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 128.00 MHz, 1/Non-standard T/R

e) VC-711-HDW-KAAN-156M253900:

VC-711, 2.5 Vdc, LVDS Output, –10°C to +70°C Temp Range, ±50 ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 156.2539 MHz, 250/Non-standard T/R

f) VC-711-JDE-KAAN-156M250000:

VC-711, 1.8 Vdc, LVDS Output, –40°C to +85°C Temp Range, ± 50ppm Stability, Output Enabled, Pin 1 Enable/Disable, Standard Option, 156.25 MHz, 10/Non-standard T/R

TABLE 0-1: STANDARD OUTPUT FREQUENCIES

10.000000 MHz	25.000000 MHz	50.000000 MHz	100.000000 MHz	120.000000 MHz	125.000000 MHz
128.000000 MHz	155.000000 MHz	155.520000 MHz	156.250000 MHz	156.253900 MHz	160.000000 MHz
200.000000 MHz	—	—	—	—	—

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