High Performance 10-Bit Display Interface

AD9984A

FEATURES

10-bit, analog-to-digital converters
170 MSPS maximum conversion rate
Low PLL clock jitter at 170 MSPS
Automatic gain matching
Automated offset adjustment
2:1 input mux
Power-down via dedicated pin or serial register
4:4:4, 4:2:2, and DDR output format modes
Variable output drive strength
Odd/even field detection
External clock input
Regenerated Hsync output
Programmable output high impedance control
Hsyncs per Vsync counter
Sync-on-green (SOG) pulse filter
Pb-free package

APPLICATIONS

Advanced TVs
Plasma display panels
LCDTV
HDTV
RGB graphics processing
LCD monitors and projectors
Scan converters

FUNCTIONAL BLOCK DIAGRAM

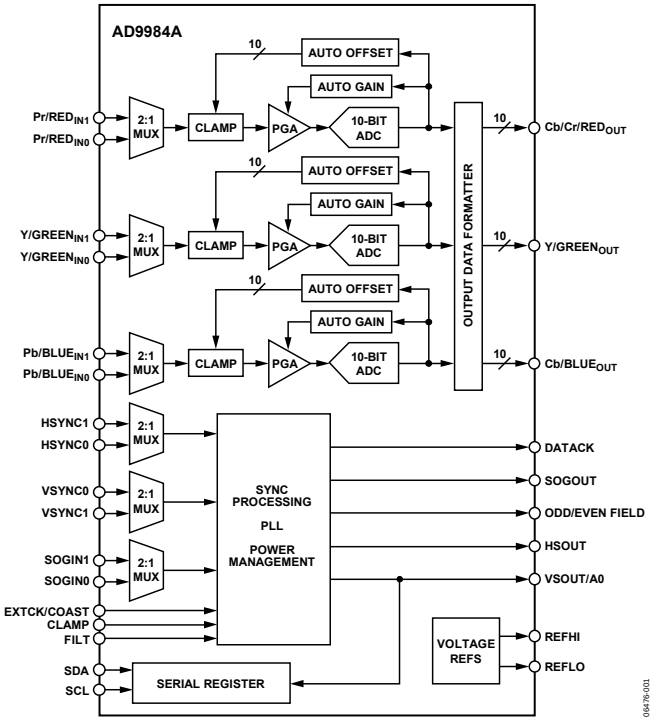

Figure 1.

GENERAL DESCRIPTION

The AD9984A is a complete 10-bit, 170 MSPS, monolithic analog interface optimized for capturing YPbPr video and RGB graphics signals. Its 170 MSPS encode rate capability and full power analog bandwidth of 300 MHz support all HDTV video modes up to 1080p, as well as graphics resolutions up to UXGA (1600 × 1200 at 60 Hz).

The AD9984A includes a 170 MHz triple ADC with an internal reference, a PLL, and programmable gain, offset, and clamp control. The user provides only a 1.8 V power supply and an analog input. Three-state CMOS outputs can be powered from 1.8 V to 3.3 V.

The AD9984A on-chip PLL generates a sample clock from the tri-level sync (for YPbPr video) or the horizontal sync (for RGB graphics). Sample clock output frequencies range from 10 MHz to 170 MHz. With internal coast generation, the PLL maintains its output frequency in the absence of a sync input. A 32-step sampling clock phase adjustment is provided. Output data, sync, and clock phase relationships are maintained.

The auto-offset feature can be enabled to automatically restore the signal reference levels and calibrate out any offset differences between the three channels. The auto channel-to-channel gain-matching feature can be enabled to minimize any gain mismatches between the three channels.

The AD9984A also offers full sync processing for composite sync and sync-on-green applications. A clamp signal is generated internally or can be provided by the user through the CLAMP input pin.

Fabricated in an advanced CMOS process, the AD9984A is provided in a space-saving, Pb-free, 80-lead low profile quad flat package (LQFP) or 64-lead lead frame chip scale package (LFCSP) and is specified over the 0°C to 70°C temperature range.

Rev. 0

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REVISION HISTORY

7/07—Revision 0: Initial Version

SPECIFICATIONS

ANALOG INTERFACE CHARACTERISTICS

V_D = 1.8 V, V_{DD} = 3.3 V, PV_D = 1.8 V, DAV_{DD} = 1.8 V, ADC clock = maximum conversion rate, full temperature range = 0°C to 70°C.

Table 1. Electrical Characteristics

Parameter	Temp	Test Level[1]	AD9984AKSTZ-140 AD9984AKCPZ-140 Min	Typ	Max	AD9984AKSTZ-170 AD9984AKCPZ-170 Min	Typ	Max	Unit
RESOLUTION									
Number of Bits				10			10		Bits
LSB Size				0.098			0.098		% of full scale (FS)
DC ACCURACY									
Differential Nonlinearity	25°C	I		±0.6	+1.8/−1.0		±0.7	+1.9/−1.0	LSB
	Full	VI			+1.9/−1.0			+2.0/−1.0	LSB
Integral Nonlinearity	25°C	I		±2.35	±7.0		±2.35	±8.5	LSB
	Full	VI			±9.0			±9.0	LSB
No Missing Codes	Full	VI		GNT[2]			GNT[2]		
ANALOG INPUT									
Input Voltage Range									
Minimum	Full	VI			0.5			0.5	V p-p
Maximum	Full	VI	1.0			1.0			V p-p
Gain Tempco	25°C	V		125			125		ppm/°C
Input Bias Current	25°C	IV			1			1	µA
	Full	IV			1			1	µA
Input Full-Scale Matching	Full	VI		1			1		% FS
Offset Adjustment Range	Full	VI		50			50		% FS
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	140			170			MSPS
Minimum Conversion Rate	Full	IV			10			10	MSPS
Clock to Data Skew (t_{SKEW})	Full	IV	−0.5		+2.0	−0.5		+2.0	ns
t_{BUFF}	Full	VI	4.7			4.7			µs
t_{STAH}	Full	VI	4.0			4.0			µs
t_{DHO}	Full	VI	0			0			µs
t_{DAL}	Full	VI	4.7			4.7			µs
t_{DAH}	Full	VI	4.0			4.0			µs
t_{DSU}	Full	VI	250			250			ns
t_{STASU}	Full	VI	4.7			4.7			µs
t_{STOSU}	Full	VI	4.0			4.0			µs
Maximum PLL Clock Rate	Full	VI	140			170			MHz
Minimum PLL Clock Rate	Full	IV			10			10	MHz
Sampling Phase Tempco	Full	IV		15			15		ps/°C
DIGITAL INPUTS									
Input Voltage, High (V_{IH})	Full	VI	1.0			1.0			V
Input Voltage, Low (V_{IL})	Full	VI			0.8			0.8	V
Input Current, High (I_{IH})	Full	V			−1.0			−1.0	µA
Input Current, Low (I_{IL})	Full	V			1.0			1.0	µA
Input Capacitance	25°C	V		2			2		pF
DIGITAL OUTPUTS									
Output Voltage, High (V_{OH})	Full	VI	V_{DD} − 0.1			V_{DD} − 0.1			V
Output Voltage, Low (V_{OL})	Full	VI			0.1			0.1	V
Duty Cycle (DATACK)	Full	IV	45	50	55	45	50	55	%
Output Coding				Binary			Binary		

Parameter	Temp	Test Level[1]	AD9984AKSTZ-140 AD9984AKCPZ-140 Min	Typ	Max	AD9984AKSTZ-170 AD9984AKCPZ-170 Min	Typ	Max	Unit
POWER SUPPLY									
V_D Supply Voltage	Full	IV	1.7	1.8	1.9	1.755	1.8	1.9	V
V_{DD} Supply Voltage	Full	IV	1.7	3.3	3.47	1.7	3.3	3.47	V
PV_D Supply Voltage	Full	IV	1.7	1.8	1.9	1.7	1.8	1.9	V
DAV_{DD} Supply Voltage	Full	IV	1.7	1.8	1.9	1.7	1.8	1.9	V
V_D Supply Current (I_D)	25°C	V		250			255		mA
V_{DD} Supply Current (I_{DD})	25°C	V		31			34		mA
PV_D Supply Current (IPV_D)	25°C	V		9			9		mA
DAV_{DD} Supply Current (IDA_{VDD})	25°C	V		16			19		mA
Total Power Dissipation	Full	VI			710			740	mW
Power-Down Supply Current	Full	VI		10			10		mA
Power-Down Dissipation	Full	VI		18			18		mW
DYNAMIC PERFORMANCE									
Analog Bandwidth, Full Power	25°C	V		300			300		MHz
Crosstalk	Full	V		60			60		dBc

[1] See the Explanation of Test Levels section.
[2] Guaranteed by design, not production tested.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
V_D	1.98 V
V_{DD}	3.6 V
PV_D	1.98 V
DAV_{DD}	1.98 V
Analog Inputs	V_D to 0.0 V
REFHI	V_D to 0.0 V
REFLO	V_D to 0.0 V
Digital Inputs	5 V to 0.0 V
Digital Output Current	20 mA
Operating Temperature Range	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Maximum Case Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

I. 100% production tested.

II. 100% production tested at 25°C and sample tested at specified temperatures.

III. Sample tested only.

IV. Parameter is guaranteed by design and characterization testing.

V. Parameter is a typical value only.

VI. 100% production tested at 25°C; guaranteed by design and characterization testing.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
80-Lead LQFP	35	16	°C/W
64-Lead LFCSP	35	16	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

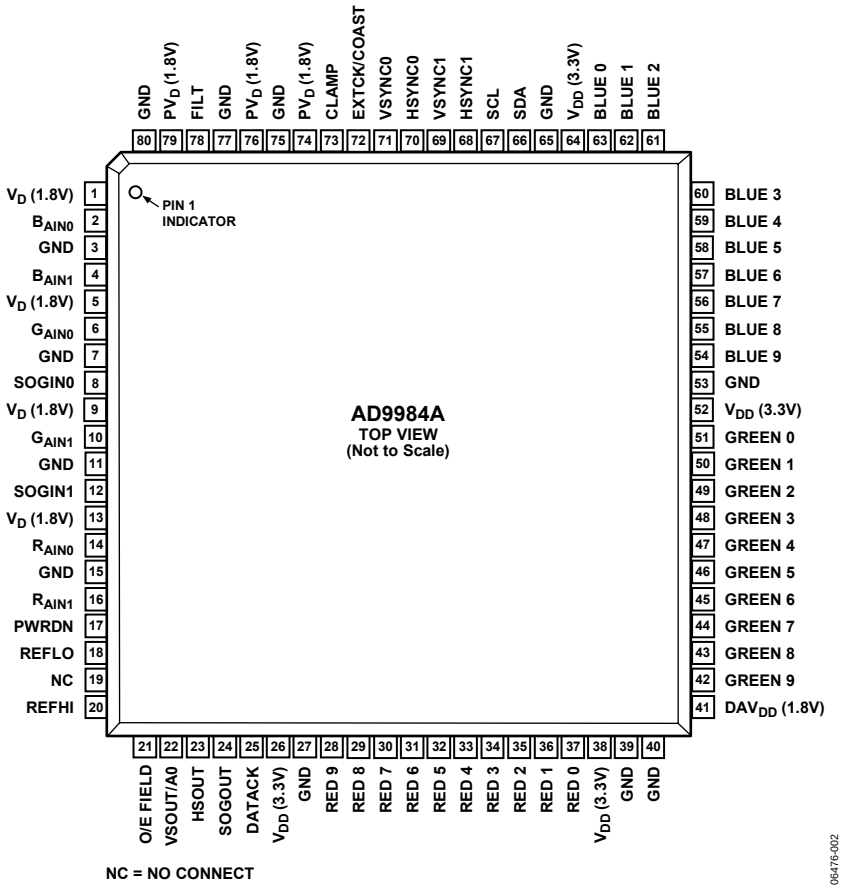


Figure 2. 80-Lead LQFP Pin Configuration

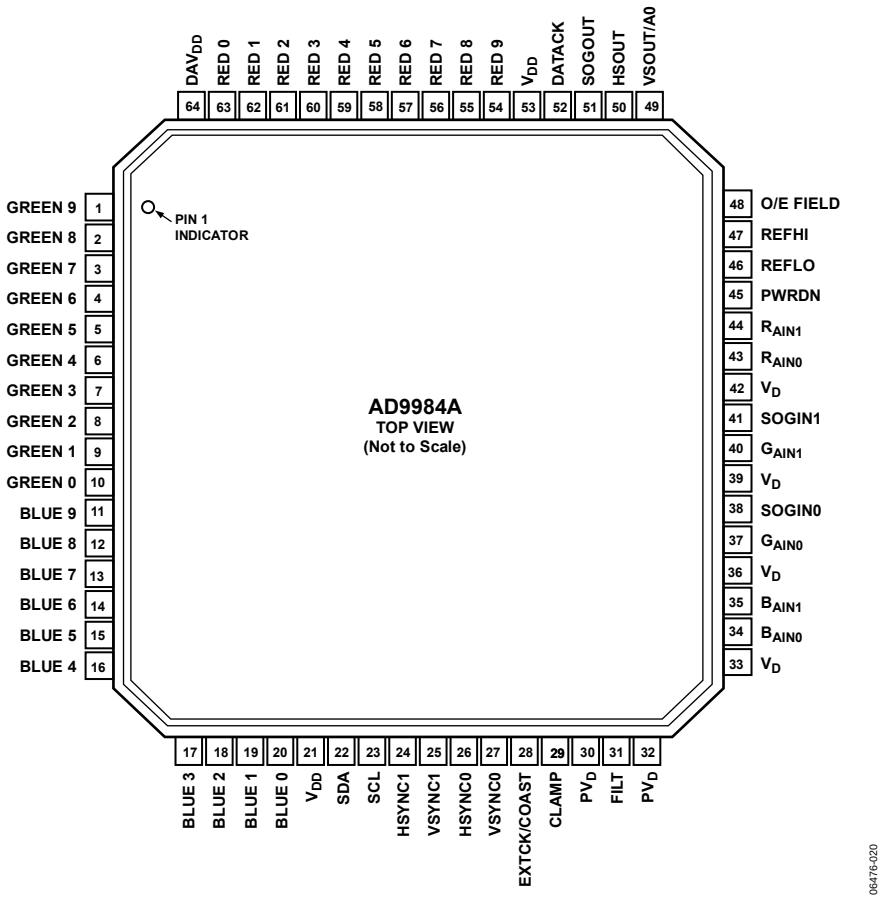


Figure 3. 64-Lead LFCSP Pin Configuration

Table 4. Complete Pin Configuration List

	Pin Number				
Pin Type	**80-Lead LQFP**	**64-Lead LFCSP**	**Mnemonic**	**Function**	**Value**
Inputs	14	43	R_{AIN0}	Channel 0 Analog Input for Converter R	0.0 V to 1.0 V
	16	44	R_{AIN1}	Channel 1 Analog Input for Converter R	0.0 V to 1.0 V
	6	37	G_{AIN0}	Channel 0 Analog Input for Converter G	0.0 V to 1.0 V
	10	40	G_{AIN1}	Channel 1 Analog Input for Converter G	0.0 V to 1.0 V
	2	34	B_{AIN0}	Channel 0 Analog Input for Converter B	0.0 V to 1.0 V
	4	35	B_{AIN1}	Channel 1 Analog Input for Converter B	0.0 V to 1.0 V
	70	26	HSYNC0	Horizontal Sync Input for Channel 0	3.3 V CMOS
	68	24	HSYNC1	Horizontal Sync Input for Channel 1	3.3 V CMOS
	71	27	VSYNC0	Vertical Sync Input for Channel 0	3.3 V CMOS
	69	25	VSYNC1	Vertical Sync Input for Channel 1	3.3 V CMOS
	8	38	SOGIN0	Input for Sync-on-Green Channel 0	0.0 V to 1.0 V
	12	41	SOGIN1	Input for Sync-on-Green Channel 1	0.0 V to 1.0 V
	72	28	EXTCK[1]	External Clock Input	3.3 V CMOS
	73	29	CLAMP	External Clamp Input Signal	3.3 V CMOS
	72	28	COAST[1]	External PLL Coast Signal Input	3.3 V CMOS
	17	45	PWRDN	Power-Down Control	3.3 V CMOS

Pin Type	Pin Number		Mnemonic	Function	Value
	80-Lead LQFP	64-Lead LFCSP			
Outputs	28 to 37	54 to 63	RED[9:0]	Outputs of Converter R; Bit 9 is the MSB	3.3 V CMOS
	42 to 51	1 to 10	GREEN[9:0]	Outputs of Converter G; Bit 9 is the MSB	3.3 V CMOS
	54 to 63	11 to 20	BLUE[9:0]	Outputs of Converter B; Bit 9 is the MSB	3.3 V CMOS
	25	52	DATACK	Data Output Clock	3.3 V CMOS
	23	50	HSOUT	Hsync Output Clock (Phase-aligned with DATACK)	3.3 V CMOS
	22	49	VSOUT[2]	Vsync Output Clock	3.3 V CMOS
	24	51	SOGOUT	Sync-on-Green Slicer Output	3.3 V CMOS
	21	48	O/E FIELD	Odd/Even Field Output	3.3 V CMOS
References	78	31	FILT	Connection for External Filter Components for Internal PLL	
	18	46	REFLO	Connection for External Capacitor for Input Amplifier	
	20	47	REFHI	Connection for External Capacitor for Input Amplifier	
Power Supply	1, 5, 9, 13	33, 36, 39, 42	V_D	Analog Power Supply	1.8 V
	26, 38, 52, 64	21, 53	V_{DD}	Output Power Supply	1.8 V to 3.3 V
	74, 76, 79	30, 32	PV_D	PLL Power Supply	1.8 V
	41	64	DAV_{DD}	Digital Logic Power Supply	1.8 V
	3, 7, 11, 15, 27, 39, 40, 53, 65, 75, 77, 80	N/A	GND	Ground	0 V
Control	66	22	SDA	Serial Port Data I/O	3.3 V CMOS
	67	23	SCL	Serial Port Data Clock (100 kHz maximum)	3.3 V CMOS
	22	49	A0[2]	Serial Port Address Input	3.3 V CMOS

[1] EXTCK and COAST share the same pin.
[2] VSOUT and A0 share the same pin.

Table 5. Pin Function Descriptions

Mnemonic	Function	Description
R_{AIN0}	Analog Input for the Red Channel 0	These high impedance inputs accept the red, green, and blue channel graphics signals, respectively. The three channels are identical and can be used for any colors, but colors are assigned for convenient reference. They accommodate input signals ranging from 0.5 V to 1.0 V full scale. Signals should be ac-coupled to these pins to support clamp operation. Refer to Figure 4 and Figure 5.
G_{AIN0}	Analog Input for the Green Channel 0	
B_{AIN0}	Analog Input for the Blue Channel 0	
R_{AIN1}	Analog Input for the Red Channel 1	
G_{AIN1}	Analog Input for the Green Channel 1	
B_{AIN1}	Analog Input for the Blue Channel 1	
HSYNC0	Horizontal Sync Input Channel 0	These inputs receive a logic signal that establishes the horizontal timing reference and provides the frequency reference for pixel clock generation. The logic sense of these pins can be automatically determined by the chip or manually controlled by Serial Register 0x12, Bits[5:4] (Hsync polarity). Only the leading edge of Hsync is used by the PLL; the trailing edge is used in clamp timing. When Hsync polarity = 0, the falling edge of Hsync is used. When Hsync polarity = 1, the rising edge is active. These inputs include a Schmitt trigger for noise immunity.
HSYNC1	Horizontal Sync Input Channel 1	
VSYNC0	Vertical Sync Input Channel 0	These inputs for vertical sync provide timing information for generation of the field (odd/even) and internal coast generation. The logic sense of this pin can be automatically determined by the chip or manually controlled by Serial Register 0x14, Bits[5:4] (Vsync polarity).
VSYNC1	Vertical Sync Input Channel 1	
SOGIN0	Sync-on-Green Input Channel 0	These inputs help process signals with embedded sync, typically on the green channel. These pins connect to a high speed comparator with an internally generated threshold. The threshold level can be programmed in 8 mV steps to any voltage between 8 mV and 256 mV above the negative peak of the input signal. The default voltage threshold is 128 mV. When connected to an ac-coupled graphics signal with embedded sync, a noninverting digital output is produced on SOGOUT. This output is usually a composite sync signal, containing both vertical and horizontal sync information that must be separated before passing the horizontal sync signal for Hsync processing. When not used, these inputs should be left unconnected. For more details about this function and how it should be configured, refer to the Sync-on-Green section.
SOGIN1	Sync-on-Green Input Channel 1	
CLAMP	External Clamp Input (Optional)	This logic input can be used to define the time during which the input signal is clamped to ground or midscale. It should be exercised when the reference dc level is known to be present on the analog input channels, typically during the back porch of the graphics signal. The CLAMP pin is enabled by setting the control bit clamp function to 1, (Register 0x18, Bit 4; default is 0). When disabled, this pin is ignored and the clamp timing is determined internally by counting a delay and duration from the trailing edge of the Hsync input. The logic sense of this pin can be automatically determined by the chip or controlled by clamp polarity (Register 0x1B, Bits[7:6]). When not used, this pin can be left unconnected (there is an internal pull-down resistor) and the clamp function programmed to 0.
EXTCK/COAST	External Clock (EXTCK)	This pin has dual functionality. EXTCK allows the insertion of an external clock source rather than the internally generated, PLL locked clock. EXTCK is enabled by programming Register 0x03, Bit 2 to 1. This EXTCK function does not affect the COAST function.
	Optional Coast Input to Clock Generator (COAST)	COAST can be used to cause the pixel clock generator to stop synchronizing with Hsync and continue to produce a clock at its current frequency and phase. This is useful when processing signals from sources that fail to produce Hsync pulses during the vertical interval. The coast signal is generally not required for PC-generated signals. The logic sense of this pin can be determined automatically or controlled by coast polarity (Register 0x18, Bits[7:6]). When this function and the EXTCK function are not used, this pin can be grounded and coast polarity programmed to 1. Input coast polarity defaults to 1 at power-up. This COAST function does not affect the EXTCK function.
PWRDN	Power-Down Control (PWRDN)	PWRDN allows for manual power-down control. If manual power-down control is selected (Register 0x1E, Bit 4),and this pin is not used, it is recommended to set the pin polarity (Register 0x1E, Bit 2) to active high and hardwire this pin to ground with a 10 kΩ resistor.
REFLO, REFHI	Input Amplifier Reference	REFLO and REFHI are connected together through a 10 µF capacitor. These are used for stability in the input ADC circuitry. See Figure 6.

Mnemonic	Function	Description
FILT	External Filter Connection	For proper operation, the pixel clock generator PLL requires an external filter. Connect the filter shown in Figure 8 to this pin. For optimal performance, minimize noise and parasitics on this node. For more information, see the PCB Layout Recommendations section.
HSOUT	Horizontal Sync Output	This pin is a reconstructed and phase-aligned version of the Hsync input. Both the polarity and duration of this output can be programmed via serial bus registers. By maintaining alignment with DATACK and the main data outputs (RED[9:0], GREEN[9:0], BLUE[9:0]), data timing with respect to Hsync can always be determined.
VSOUT/A0	Vertical Sync Output (VSOUT) Serial Port Address Input 0 (A0)	This pin has dual functionality. VSOUT can either be a separated Vsync from a composite signal or a direct pass through of the Vsync signal. The polarity of this output can be controlled via a serial bus bit. The placement and duration in all modes can be set by the graphics transmitter or the duration can be set by Register 0x14, Bit 1 and Register 0x15, Bits[7:0]. This VSOUT function does not affect the A0 function. A0 selects the LSB of the serial port device address, allowing two parts from Analog Devices, Inc., to be on the same serial bus. A high impedance (10 kΩ), external pull-up resistor enables this pin to be read at power-up as 1. This A0 function does not interfere with the VSOUT function. For more details on A0, see the description in the 2-Wire Serial Control Port section.
SOGOUT	Sync-On-Green Slicer Output	This pin outputs one of four possible signals (controlled by Register 0x1D, Bits[1:0]): raw SOGINx, raw HSYNCx, regenerated Hsync from the filter, or the filtered Hsync. See Figure 9 to view how this pin is connected. Other than slicing off SOG, the output from this pin receives no additional processing on the AD9984A. Vsync separation is performed via the sync separator.
O/E FIELD	Odd/Even Field Bit for Interlaced Video	This output identifies whether the current field (in an interlaced signal) is odd or even.
SDA	Serial Port Data I/O	Data I/O for the I²C® serial port.
SCL	Serial Port Data Clock	Clock for the I²C serial port.
RED[9:0] GREEN[9:0] BLUE[9:0]	Data Output, Red Channel Data Output, Green Channel Data Output, Blue Channel	The main data outputs. Bit 9 is the MSB. The delay from pixel sampling time to output is fixed. When the sampling time is changed by adjusting the phase register, the output timing is shifted as well. The DATACK and HSOUT outputs are also moved to maintain the timing relationship among the signals.
DATACK	Data Clock Output	This is the main clock output signal used to strobe the output data and HSOUT into external logic. Four possible output clocks can be selected with Register 0x20, Bits[7:6]. Three of these are related to the pixel clock (pixel clock, 90° phase-shifted pixel clock, and 2× frequency pixel clock). They are produced by the internal PLL clock generator or by EXTCK, and are synchronous with the pixel sampling clock. The fourth option for the data clock output is an internally generated 0.5× pixel clock. The sampling time of the internal pixel clock can be changed by adjusting the phase register (Register 0x04). When this is changed, the pixel-related DATACK timing is also shifted. The data (RED[9:0], GREEN[9:0], BLUE[9:0]), DATACK, and HSOUT outputs are moved to maintain the timing relationship among the signals.
V_D (1.8 V)	Main Power Supply	These pins supply power to the main elements of the circuit. They should be as quiet and as filtered as possible.
V_{DD} (1.8 V to 3.3 V)	Digital Output Power Supply	A large number of output pins (up to 35) switching at high speed (up to 170 MHz) generates large amounts of power supply transients (noise). These supply pins are identified separately from the V_D pins. As a result, special care must be taken to minimize output noise transferred into the sensitive analog circuitry. If the AD9984A is interfacing with lower voltage logic, V_{DD} can be connected to a lower supply voltage (as low as 1.8 V) for compatibility.
PV_D (1.8 V)	Clock Generator Power Supply	The most sensitive portion of the AD9984A is the clock generation circuitry. These pins provide power to the clock PLL and help the user design for optimal performance. The designer should provide quiet, noise-free power to these pins.
DAV_{DD} (1.8 V)	Digital Input Power Supply	This supplies power to the digital logic. It is recommended to connect this pin to the V_D supply.
GND	Ground	The ground return for all on-chip circuitry. It is recommended that the AD9984A be assembled on a single solid ground plane with careful attention to ground current paths.

THEORY OF OPERATION

The AD9984A is a fully integrated solution for capturing and digitizing analog RGB or YPbPr signals for display on advanced TVs, flat panel monitors, projectors, and other types of digital displays. Implemented in a high performance CMOS process, the interface can capture signals with pixel rates up to 170 MHz.

The AD9984A includes all necessary input buffering, signal dc restoration (clamping), offset and gain (brightness and contrast) adjustment, pixel clock generation, sampling phase control, and output data formatting. All controls are programmable via a 2-wire serial interface (I^2C). Full integration of these sensitive analog functions makes system design straightforward and less sensitive to the physical and electrical environment.

With a typical power dissipation of less than 900 mW and an operating temperature range of 0°C to 70°C, the device requires no special environmental considerations.

DIGITAL INPUTS

All digital inputs on the AD9984A operate to 3.3 V CMOS levels. The following digital inputs are 5 V tolerant (that is, applying 5 V to them does not cause any damage): HSYNC0, HSYNC1, VSYNC0, VSYNC1, SOGIN0, SOGIN1, SDA, SCL, and CLAMP.

ANALOG INPUT SIGNAL HANDLING

The AD9984A has six, high impedance, analog input pins for the red, green, and blue channels. They accommodate signals ranging from 0.5 V to 1.0 V p-p.

Signals are typically brought onto the interface board with a DVI-I connector, a 15-pin D connector, or RCA connectors. The AD9984A should be located as close as possible to the input connector. Signals should be routed using matched-impedance traces (normally 75 Ω) to the IC input pins.

At the input pins, the signal should be resistively terminated (75 Ω to the signal ground return) and capacitively coupled to the AD9984A inputs through 47 nF capacitors. These capacitors form part of the dc restoration circuit.

In an ideal world of perfectly matched impedances, the best performance can be obtained with the widest possible signal bandwidth. The wide bandwidth inputs of the AD9984A (300 MHz) can track the input signal continuously as it moves from one pixel level to the next and can digitize the pixel during a long, flat pixel time. In many systems, however, there are mismatches, reflections, and noise, which can result in excessive ringing and distortion of the input waveform. This makes it more difficult to establish a sampling phase that provides good image quality. A small inductor in series with the input is shown to be effective in rolling off the input bandwidth slightly and providing a high quality signal over a wider range of conditions. Using a high speed, signal chip, bead inductor (such as the Fair-Rite 2508051217Z0) in the circuit shown in Figure 4 provides good results in most applications.

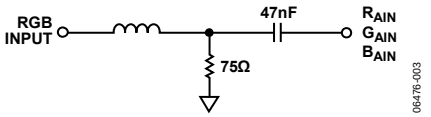


Figure 4. Analog Input Interface Circuit

HSYNC AND VSYNC INPUTS

The interface also accepts Hsync and Vsync signals, which are used to generate the pixel clock, clamp timing, and coast and field information. These can be either a sync signal directly from the graphics source, or a preprocessed TTL- or CMOS-level signal.

The Hsync input includes a Schmitt trigger buffer for immunity to noise and signals with long rise times. In typical PC-based graphic systems, the sync signals are simply TTL-level drivers feeding unshielded wires into the monitor cable. As such, no termination is required.

SERIAL CONTROL PORT

The serial control port is designed for 3.3 V logic; however, it is tolerant of 5 V logic signals. Refer to the 2-Wire Serial Control Port section for more information.

OUTPUT SIGNAL HANDLING

The digital outputs operate from 1.8 V to 3.3 V (V_{DD}).

CLAMPING

RGB Clamping

To properly digitize the incoming signal, the dc offset of the input must be adjusted to fit the range of the on-board ADCs.

Most graphics systems produce RGB signals with black at ground and white at approximately 0.75 V. However, if sync signals are embedded in the graphics, the sync tip is often at ground, black is at 300 mV, and white is at approximately 1.0 V. Some common RGB line amplifier boxes use emitter-follower buffers to split signals and increase drive capability. This introduces a 700 mV dc offset to the signal, which must be removed for proper capture by the AD9984A.

The key to clamping is to identify a portion (time) of the signal when the graphic system is known to be producing black. An offset is then introduced that results in the ADC producing a black output (Code 0x00) when the known black input is present. The offset then remains in place when other signal levels are processed, and the entire signal is shifted to eliminate offset errors.

In most PC graphics systems, black is transmitted between active video lines. With CRT displays, when the electron beam has completed writing a horizontal line on the screen (at the right side), the beam is deflected quickly to the left side of the screen (called horizontal retrace) and a black signal is provided to prevent the beam from disturbing the image.

In systems with embedded sync, a blacker-than-black signal (Hsync) is briefly produced to signal the CRT that it is time to begin a retrace. Because the input is not at black level at this time, it is important to avoid clamping during Hsync. Fortunately, there is usually a period following Hsync (called the back porch) where a good black reference is provided. This is the time when clamping should be done.

The clamp timing can be established by simply exercising the CLAMP pin at the appropriate time with clamp source (Register 0x18, Bit 4) = 1. The polarity of this signal is set by the clamp polarity bits (Register 0x1B, Bits[7:6]).

A simpler method of clamp timing employs the AD9984A internal clamp timing generator. The clamp placement register (Register 0x19) is programmed with the number of pixel periods that should pass after the trailing edge of Hsync before clamping starts. A second register, clamp duration (Register 0x1A), sets the duration of the clamp. These are both 8-bit values, providing considerable flexibility in clamp generation. Although Hsync duration can widely vary, the clamp timing is referenced to the trailing edge of Hsync because the back porch (black reference) always follows Hsync. An effective starting point for establishing clamping is to set the clamp placement to 0x04 (providing 4 pixel periods for the graphics signal to stabilize after sync) and set the clamp duration to 0x28 (giving the clamp 40 pixel periods to reestablish the black reference).

Clamping is accomplished by placing an appropriate charge on the external input coupling capacitor. The value of this capacitor affects the performance of the clamp. If it is too small, there is a significant amplitude change during a horizontal line time (between clamping intervals). If the capacitor is too large, it takes a long time for the clamp to recover from a large change in incoming signal offset. The recommended value (100 nF) results in recovering from a step error of 100 mV to within 1 LSB in 60 lines with a clamp duration of 20 pixel periods on a 85 Hz XGA signal.

YPbPr Clamping

YPbPr graphic signals are slightly different from RGB signals in that the dc reference level (black level in RGB signals) of color difference signals is at the midpoint of the video signal rather than at the bottom. The three inputs are composed of luminance (Y) and color difference (Pb and Pr) signals. For color difference signals, it is necessary to clamp to the midscale range of the ADC range (512) rather than to the bottom of the ADC range (0), while the Y channel is clamped to ground.

Clamping to midscale rather than ground can be accomplished by setting the clamp select bits in the serial bus register. Each of the three converters has its own selection bit to enable them to be independently clamped to midscale or ground. These bits are located in Register 0x18, Bits[3:1]. The midscale reference voltage is internally generated for each converter.

GAIN AND OFFSET CONTROL

The AD9984A contains three programmable gain amplifiers (PGAs), one for each of the three analog inputs. The range of the PGA is sufficient to accommodate input signals with inputs ranging from 0.5 V to 1.0 V full scale. The gain is set in three 9-bit registers, red gain (Register 0x05, Register 0x06), green gain (Register 0x07, Register 0x08), and blue gain (Register 0x09, Register 0x0A). For each register, a gain setting of 0d corresponds to the highest gain, while a gain setting of 511d corresponds to the lowest gain. Note that increasing the gain setting results in an image with less contrast.

The offset control shifts the analog input, resulting in a change in brightness. Three 11-bit registers, red offset (Register 0x0B, Register 0x0C), green offset (Register 0x0D, Register 0x0E), and blue offset (Register 0x0F, Register 0x10) provide independent settings for each channel. Note that the function of the offset register depends on whether auto-offset is enabled (Register 0x1B, Bit 5).

If manual offset is used, nine bits of the offset registers (for the red channel, Register 0x0B, Bits[6:0] plus Register 0x0C, Bits[7:6]) control the absolute offset added to the channel. The offset control provides ±255 LSBs of adjustment range, with 1 LSB of offset corresponding to 1 LSB of output code.

Automatic Offset

In addition to the manual offset adjustment mode, the AD9984A also includes circuitry to automatically calibrate the offset for each channel. By monitoring the output of each ADC during the back porch of the input signals, the AD9984A can self-adjust to eliminate any offset errors in its own ADC channels and any offset errors present on the incoming graphics or video signals.

To activate the auto-offset mode, set Register 0x1B, Bit 5 to 1. Next, the target code registers (Register 0x0B through Register 0x10) must be programmed. The values programmed into the target code registers should be the output code desired from the AD9984A during the back porch reference time.

For example, for RGB signals, all three registers are normally programmed to Code 2, while for YPbPr signals, the green (Y) channel is normally programmed to Code 2, and the blue and red channels (Pb and Pr) are normally set to 512. The target code registers have 11 bits per channel and are in twos complement format. This allows any value between −1024 and +1023 to be programmed. Although any value in this range can be programmed, the AD9984A offset range may not be able to reach every value. Intended target code values range from (but are not limited to) −160 to −1 and +1 to +160 when ground clamping, and 350 to 670 when midscale clamping. Note that a target code of 0 is not valid.

Negative target codes are included to duplicate a feature that is present with manual offset adjustment. The benefit that is mimicked is the ability to easily adjust brightness on a display. By setting the target code to a value that does not correspond to the ideal ADC range, the end result is an image that is brighter or darker. A target code higher than ideal results in a brighter image, whereas a target code lower than ideal results in a darker image.

The ability to program a target code offers a large degree of freedom and flexibility. Although all channels are set to either 1 or 512 in most cases, the flexibility to select other values makes it possible to insert intentional skews between channels. It also allows the ADC range to be skewed so that voltages outside of the normal range can be digitized. For example, setting the target code to 40 allows the sync tip, which is normally below black level, to be digitized and evaluated.

The internal logic for the auto-offset circuit requires 16 data clock cycles to perform its function. This operation is executed immediately after the clamping pulse. Therefore, it is important to end the clamping pulse signal at least 16 data clock cycles before active video. This is true whether using the AD9984A internal clamp circuit or an external CLAMP signal. The auto-offset function can be programmed to run continuously or on a one-time basis (see the 0x2C—Bit[4] Auto-Offset Hold section). In continuous mode, the update frequency can be programmed (Register 0x1B, Bits[4:3]). Continuous operation with updates every 192 Hsyncs is recommended.

Guidelines for basic auto-offset operation are shown in Table 6 and Table 7.

Table 6. RGB Auto-Offset Register Settings

Register	Value	Comments
0x0B	0x00	Sets red target to 4.
0x0C	0x80	Must be written.
0x0D	0x00	Sets green target to 4.
0x0E	0x80	Must be written.
0x0F	0x00	Sets blue target to 4.
0x10	0x80	Must be written.
0x18, Bits[3:1]	000	Sets red, green, and blue channels to ground clamp.
0x1B, Bits[5:3]	110	Selects update rate to every 192 clamps and enables auto-offset.

Table 7. YPbPr Auto-Offset Register Settings

Register	Value	Comments
0x0B	0x40	Sets Pr (red) target to 512.
0x0C	0x00	Must be written.
0x0D	0x00	Sets Y (green) target to 4.
0x0E	0x80	Must be written.
0x0F	0x40	Sets Pb (blue) target to 512.
0x10	0x00	Must be written.
0x18, Bits[3:1]	101	Sets Pb, Pr to midscale clamp and Y to ground clamp.
0x1B, Bits[5:3]	110	Selects update rate to every 192 clamps and enables auto-offset.

Automatic Gain Matching

The AD9984A includes circuitry to match the gains between the three channels to within 1% of each other. Matching the gains of each channel is necessary to achieve good color balance on a display. On products without this feature, gain matching is achieved by writing software that evaluates the output of each channel, calculates gain mismatches, and then writes values to the gain registers of each channel to compensate. With the auto gain matching function, this software routine is no longer needed. To activate auto gain matching, set Register 0x3C, Bits[2:0] to 110.

Auto gain matching has similar timing requirements to auto offset. It requires 16 data clock cycles to perform its function, starting immediately after the end of the clamp pulse. Unlike auto offset, auto gain matching does not require that these 16 clock cycles occur during the back porch reference time, although it is recommended. During auto gain matching operation, the data outputs of the AD9984A are frozen (held at the value they had just prior to operation). The auto gain matching function can be programmed to run continuously or on a one-time basis (see the 0x3C—Bit[3] Auto Gain Matching Hold section). In continuous mode, the update frequency can be programmed (Register 0x1B, Bits[4:3]). Continuous operation with updates every 192 Hsyncs is recommended.

SYNC-ON-GREEN

The sync-on-green inputs (SOGIN0, SOGIN1) operate in two steps. First, they set a baseline clamp level off the incoming video signal with a negative peak detector. Second, they set the voltage level of the SOG slicer's comparator (Register 0x1D, Bits[7:3]) with a variable trigger level to a programmable level (typically 128 mV) above the negative peak. Each sync-on-green input must be ac-coupled to the green analog input through its own capacitor. The value of the capacitor must be 1 nF ± 20%. If sync-on-green is not used, this connection is not required. The sync-on-green signal always has negative polarity.

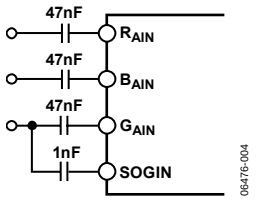


Figure 5. Typical Input Configuration

REFERENCE BYPASSING

REFLO and REFHI are connected to each other by a 10 µF capacitor (see Figure 6). These references are used by the input ADC circuitry.

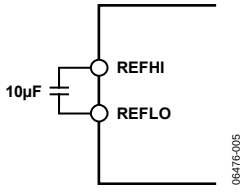


Figure 6. Input Amplifier Reference Capacitors

CLOCK GENERATION

A PLL is used to generate the pixel clock. The Hsync input provides a reference frequency to the PLL. A voltage controlled oscillator (VCO) generates a much higher pixel clock frequency. The pixel clock is divided by the PLL divide value (Register 0x01 and Register 0x02) and phase-compared with the Hsync input. Any error is used to shift the VCO frequency and maintain lock between the two signals.

The stability of this clock is a very important element in providing the clearest and most stable image. During each pixel time, the signal slews from the old pixel amplitude and settles at its new value; this is called the slewing time. Then, the input voltage stabilizes before the signal must slew to a new value; this is called the stable time. The ratio of the slewing time to the stable time is a function of the graphics DAC bandwidth and the bandwidth of the transmission system (cable and termination). This ratio is also a function of the overall pixel rate. If the dynamic characteristics of the system remain fixed, the slewing and settling time is likewise fixed. This time must be subtracted from the total pixel period, leaving the stable period. At higher pixel frequencies, the total cycle time is shorter and the stable pixel time becomes shorter as well.

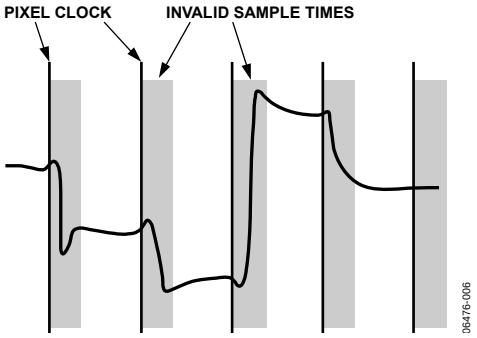


Figure 7. Pixel Sampling Times

Any jitter in the clock reduces the precision of the sampling time and it must also be subtracted from the stable pixel time. Considerable care has been taken in the design of the AD9984A clock generation circuit to minimize jitter. The clock jitter of the AD9984A is low in all operating modes, making the reduction in the valid sampling time due to jitter negligible.

The PLL characteristics are determined by the loop filter design, the PLL charge pump current, and the VCO range setting. The loop filter design is illustrated in Figure 8. Recommended settings of the VCO range and charge pump current for VESA standard display modes are listed in Table 10.

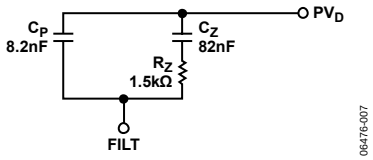


Figure 8. PLL Loop Filter Design

Four programmable registers are provided to optimize the performance of the PLL. These registers are the 12-bit divisor register, the 2-bit VCO range register, the 3-bit charge pump current register, and the 5-bit phase adjust register.

The 12-Bit Divisor Register

The input Hsync frequencies can accommodate any Hsync as long as the product of the Hsync and the PLL divisor falls within the operating range of the VCO. The PLL multiplies the frequency of the Hsync signal, producing pixel clock frequencies in the range of 10 MHz to 170 MHz. The divisor register controls the exact multiplication factor. This register can be set to any value between 2 and 4095 as long as the output frequency is within range.

The 2-Bit VCO Range Register

To improve the noise performance of the AD9984A, the VCO operating frequency range is divided into four overlapping regions. The VCO range register sets this operating range. The frequency ranges for the four regions are shown in Table 8.

Table 8. VCO Frequency Ranges

PV1	PV0	Pixel Clock Range (MHz)	KVCO Gain (MHz/V)
0	0	10 to 31[1]	150
0	1	31 to 62	150
1	0	62 to 124	150
1	1	124 to 170	150

[1] For frequencies of 18 MHz or lower, enable the VCO low range bit (Reg. 0x36[0]).

The 3-Bit Charge Pump Current Register

This register varies the current that drives the low-pass loop filter. The possible current values are listed in Table 9.

Table 9. Charge Pump Current/Control Bits

Ip2	Ip1	Ip0	Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

The 5-Bit Phase Adjust Register

The phase of the generated sampling clock can be shifted to locate an optimum sampling point within a clock cycle. The phase adjust register provides 32 phase-shift steps of 11.25° each. The Hsync signal with an identical phase shift is available through the HSOUT pin. Phase adjust is still available if an external pixel clock is used. The COAST pin or the internal coast is used to allow the PLL to continue to run at the same frequency in the absence of the incoming Hsync signal or during disturbances in Hsync (such as from equalization pulses). This can be used during the vertical sync period or at any other time that the Hsync signal is unavailable.

The polarity of the coast signal can be set through the coast polarity register (Register 0x18, Bits[6:5]). In addition, the polarity of the Hsync signal can be set through the Hsync polarity register (Register 0x12, Bits[5:4]). For both Hsync and coast, a value of 1 is active high. The internal coast function is driven off the Vsync signal, which is typically a time when Hsync signals can be disrupted with extra equalization pulses.

Table 10. Recommended VCO Range and Charge Pump and Current Settings for Standard Display Formats

Standard	Resolution	Refresh Rate (Hz)	Horizontal Frequency (kHz)	Pixel Rate (MHz)	PLL Divider	VCO Range	Current	VCO Gear (Reg.0x36[0])
VGA	640 × 480	60	31.500	25.175	800	00	101	0
		72	37.700	31.500	832	01	100	0
		75	37.500	31.500	840	01	100	0
		85	43.300	36.000	832	01	100	0
SVGA	800 × 600	56	35.100	36.000	1024	01	100	0
		60	37.900	40.000	1056	01	101	0
		72	48.100	50.000	1040	01	101	0
		75	46.900	49.500	1056	01	101	0
		85	53.700	56.250	1048	01	110	0
XGA	1024 × 768	60	48.400	65.000	1344	10	100	0
		70	56.500	75.000	1328	10	101	0
		75	60.000	78.750	1312	10	101	0
		80	64.000	85.500	1336	10	101	0
		85	68.300	94.500	1376	10	110	0
SXGA	1280 × 1024	60	64.000	108.000	1688	10	110	0
		75	80.000	135.000	1688	11	110	0
		85	91.100	157.500	1728	11	110	0
UXGA	1600 × 1200	60	75.000	162.000	2160	11	110	0
TV	480i	30	15.750	13.510	858	00	101	1
	480p	60	31.470	27.000	858	00	101	0
	576i	30	15.625	13.500	864	00	101	1
	576p	60	31.250	27.000	864	00	101	0
	720p	60	45.000	74.250	1650	10	101	0
	1035i	30	33.750	74.250	2200	10	101	0
	1080i	60	33.750	74.250	2200	10	101	0
	1080p	60	67.500	148.500	2200	11	101	0

SYNC PROCESSING

The inputs of the sync processing section of the AD9984A are combinations of digital Hsyncs and Vsyncs, analog sync-on-green or sync-on-Y signals, and an optional external coast signal. From these signals, the part generates a precise, jitter-free clock from its PLL, an odd/even-field signal, HSOUT and VSOUT signals, a count of Hsyncs per Vsync, and a programmable SOGOUT. The main sync processing blocks are the sync slicer, sync separator, Hsync filter, Hsync regenerator, Vsync filter, and coast generator.

- The sync slicer extracts the sync signal from the green graphics or luminance video signal that is connected to the SOGINx inputs, and outputs a digital composite sync.
- The sync separator extracts Vsync from the composite sync signal, which can come from either the sync slicer or the HSYNCx inputs.
- The Hsync filter is used to eliminate any extraneous pulses from the HSYNCx or SOGINx inputs, outputting a clean, low-jitter signal that is appropriate for mode detection and clock generation.
- The Hsync regenerator is used to recreate a clean, although not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync.
- The Vsync filter is used to eliminate spurious Vsyncs, maintain a stable timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output.
- The coast generator creates a robust coast signal to allow the PLL to maintain its frequency in the absence of Hsync pulses.

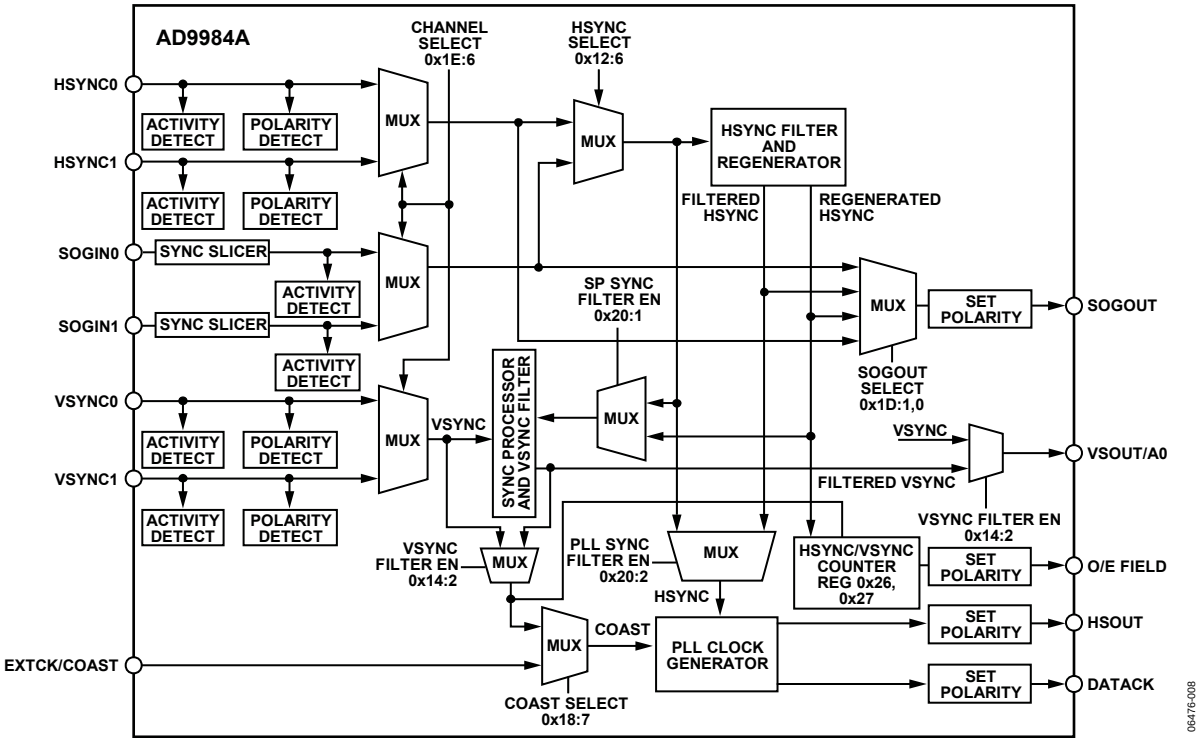


Figure 9. Sync Processing Block Diagram

Sync Slicer

The purpose of the sync slicer is to extract the sync signal from the green graphics or luminance video signal that is connected to the SOG input. The sync signal is extracted in a two step process. First, the SOG input is clamped to its negative peak, (typically 0.3 V below the black level). Next, the signal goes to a comparator with a variable trigger level (set by Register 0x1D, Bits[7:3]), but nominally 0.128 V above the clamped level. The sync slicer output is a digital composite sync signal containing both Hsync and Vsync information (see Figure 10).

Sync Separator

As part of sync processing, the sync separator's task is to extract Vsync from the composite sync signal. It works on the idea that the Vsync signal stays active for a much longer time than the Hsync signal. By using a digital low-pass filter and a digital comparator, the sync separator rejects pulses with small durations (such as Hsyncs and equalization pulses) and only passes pulses with large durations, such as Vsync (see Figure 10).

The threshold of the digital comparator is programmable for maximum flexibility. To program the threshold duration, write a value (N) to Register 0x11. The resulting pulse width is $N \times 200$ ns. If, for example, N = 5, the digital comparator threshold is 1 µs. Any pulse less than 1 µs is rejected, while any pulse greater than 1 µs passes through.

There are two factors to keep in mind when using the sync separator. First, the resulting clean Vsync output is delayed from the original Vsync by a duration equal to the digital comparator threshold ($N \times 200$ ns). Second, there is some variability to the 200 ns multiplier value. The maximum variability over all operating conditions is ±20% (160 ns to 240 ns). Because normal Vsync and Hsync pulse widths differ by a factor of approximately 500 or more, the 20% variability is not an issue.

Hsync Filter and Regenerator

The Hsync filter is used to eliminate any extraneous pulses from the Hsync or SOG inputs, outputting a clean, low jitter signal that is appropriate for mode detection and clock generation. The Hsync regenerator is used to recreate a clean, but not low jitter, Hsync signal that can be used for mode detection and counting Hsyncs per Vsync. The Hsync regenerator has a high degree of tolerance to extraneous and missing pulses on the Hsync input, but is not appropriate for use by the PLL in creating the pixel clock due to jitter.

The Hsync regenerator runs automatically and requires no setup to operate. The Hsync filter requires the setting up of a filter window. The filter window sets a periodic window of time around the regenerated Hsync leading edge where valid Hsyncs are allowed to occur. The general idea is that extraneous pulses on the sync input occur outside of this filter window and are thus, filtered out. To set the filter window timing, program a value (x) into Register 0x23. The resulting filter window time is $\pm x$ times 25 ns around the regenerated Hsync leading edge. Just as for the sync separator threshold multiplier, allow a ±20% variance in the 25 ns multiplier to account for all operating conditions (20 ns to 30 ns range).

A second output from the Hsync filter is a status bit (Register 0x25, Bit 1) that indicates if extraneous pulses are present on the incoming sync signal. Extraneous pulses are often included for copy protection purposes, so this status bit can be used to detect such pulses.

The filtered Hsync (rather than the raw HSYNCx/SOGINx signal) for pixel clock generation by the PLL is controlled by Register 0x20, Bit 2. The regenerated Hsync (rather than the raw HSYNCx/SOGINx signal) for the sync processing is controlled by Register 0x20, Bit 1. Using the filtered Hsync and regenerated Hsync is recommended. See Figure 11 for an illustration of a filtered Hsync.

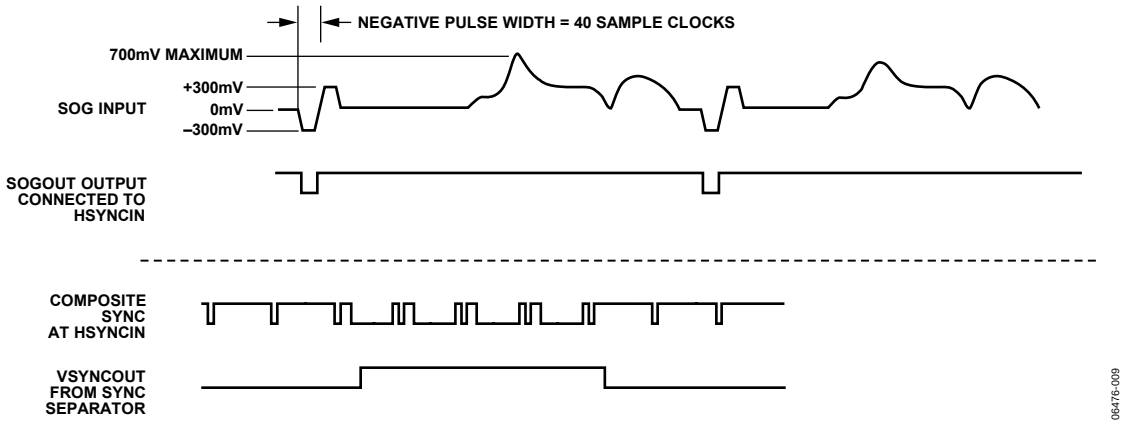


Figure 10. Sync Slicer and Sync Separator Output

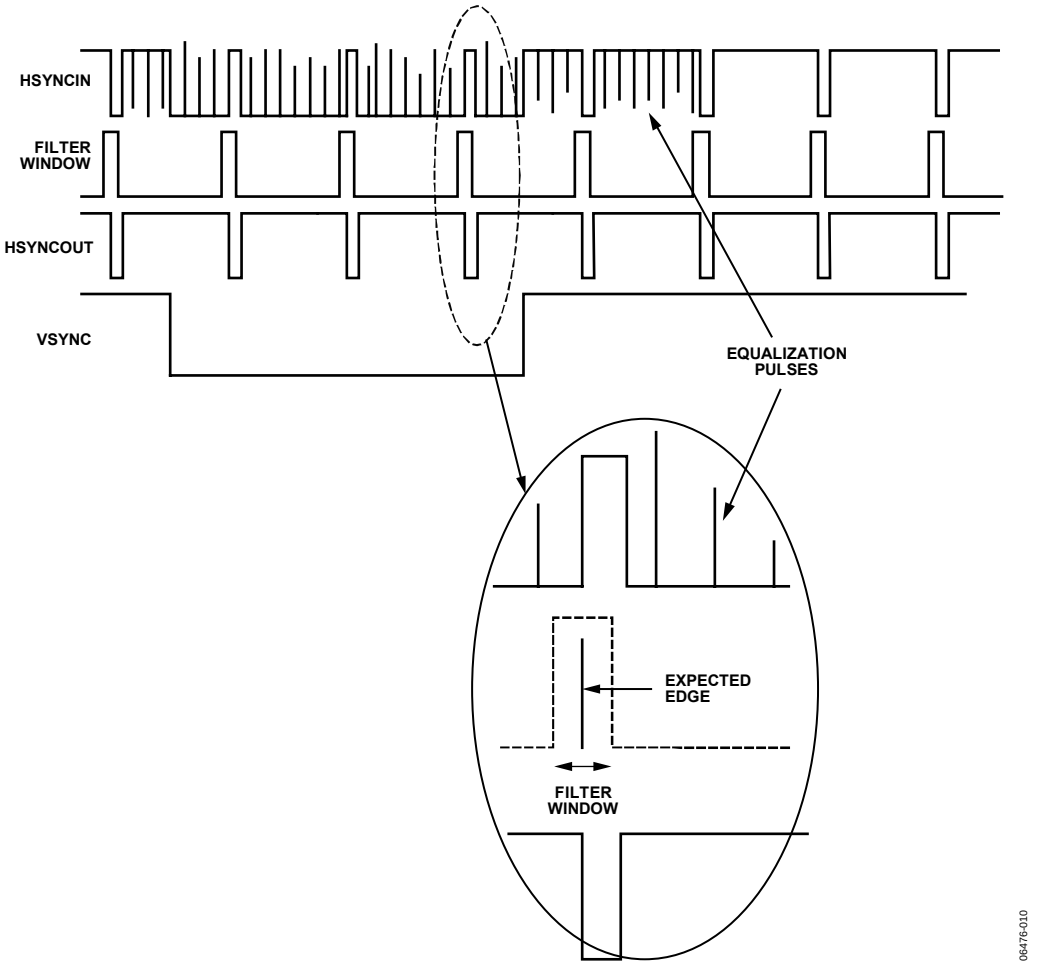


Figure 11. Sync Processing Filter

Vsync Filter and Odd/Even Fields

The Vsync filter is used to eliminate spurious Vsyncs, maintain a stable timing relationship between the Vsync and Hsync output signals, and generate the odd/even field output.

The filter works by examining the placement of Vsync with respect to Hsync and if necessary, shifting it in time slightly. The goal is to keep the Vsync and Hsync leading edges from switching at the same time, thus eliminating confusion as to when the first line of a frame occurs. Register 0x14, Bit 2 enables the Vsync filter. Use of the Vsync filter is recommended for all cases, including interlaced video, and is required when using the Hsyncs per Vsync counter. Figure 12 and Figure 13 illustrate even/odd field determination in two situations.

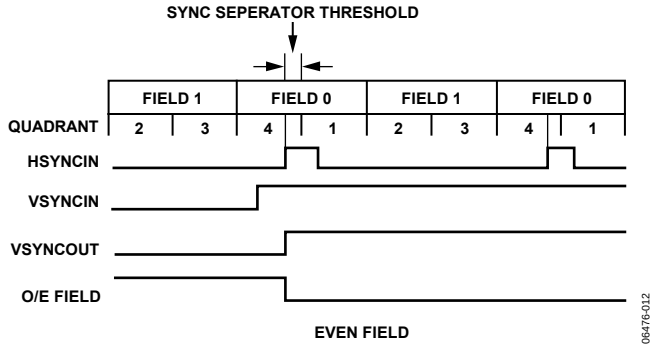


Figure 12. Even Field

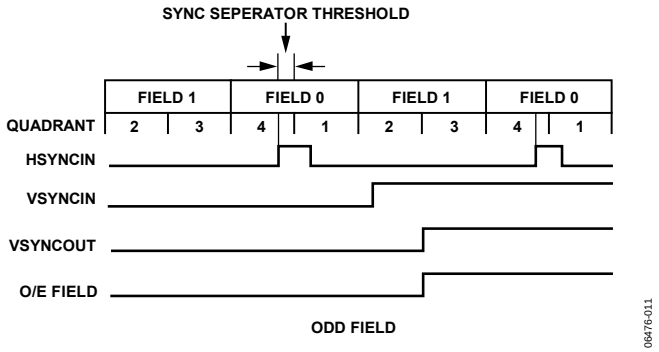


Figure 13. Odd Field

POWER MANAGEMENT

To meet display requirements for low standby power, the AD9984A includes a power-down mode. The power-down state can be controlled manually (via Pin 17 or Register 0x1E, Bit 3), or automatically by the chip. If automatic control is selected (Register 0x1E, Bit 4 =1), the AD9984A's decision is based on the status of the following sync detect bits in Register 0x24: Bit 2, Bit 3, Bit 6, and Bit 7. If either an Hsync or a sync-on-green input is detected on any input, the chip powers up; otherwise, it powers down. For manual control, the AD9984A allows flexibility of control through both a dedicated pin and a register bit. For the dedicated pin, a hardware watchdog circuit controls power-down, while software controls power-down for the register bit. With manual power-down control, the polarity of the power-down pin must be set (Register 0x1E, Bit 2) whether the pin is used or not. If unused, it is recommended to set the polarity to active high and hardwire the pin to ground with a 10 kΩ resistor.

In power-down mode, several circuits continue to operate normally. The serial register and sync detect circuits maintain power so that the AD9984A can be woken up from its power-down state. The band gap circuit maintains power because it is needed for sync detection. The sync-on-green and SOGOUT functions continue to operate because SOGOUT is needed when sync detection is performed by a secondary chip. All of these circuits require minimal power to operate. Typical standby power on the AD9984A is about 50 mW.

There are two options that can be selected when in power-down. These are controlled by Bit 0 and Bit 1 in Register 0x1E. Bit 0 controls whether the SOGOUT pin is in high impedance or not. In most cases, the user does not place SOGOUT in high impedance during normal operation. The option to put SOGOUT in high impedance is included mainly to allow for factory testing modes. Bit 1 keeps the AD9984A powered up while placing only the outputs in high impedance. This option is useful when the data outputs from two chips are connected on a PCB and the user wants to switch instantaneously between the two.

Table 11.Power-Down Control and Mode Descriptions

	Inputs			
Mode	**Auto Power-Down Control[1]**	**Power-Down[2]**	**Sync Detect[3]**	**Powered on/Comments**
Power-Up	1	X	1	Everything.
Power-Down	1	X	0	Only the serial bus, sync activity detect, SOG, band gap reference.
Power-Up	0	0	X	Everything.
Power-Down	0	1	X	Only the serial bus, sync activity detect, SOG, band gap reference.

[1] Auto power-down control is set by Register 0x1E, Bit 4.
[2] Power-down is controlled by OR'ing Pin 17 with Register 0x1E, Bit 3. The polarity of Pin 17 is set by Register 0x1E, Bit 2.
[3] Sync detect is determined by OR'ing Register 0x24, Bit 2, Bit 3, Bit 6, and Bit 7.

TIMING DIAGRAMS

The timing diagrams in Figure 14 to Figure 17 show the operation of the AD9984A. The output data clock signal is created so that its rising edge always occurs between data transitions and can be used to latch the output data externally. There is a pipeline in the AD9984A that must be flushed before valid data becomes available. This means six data sets are present before valid data is available.

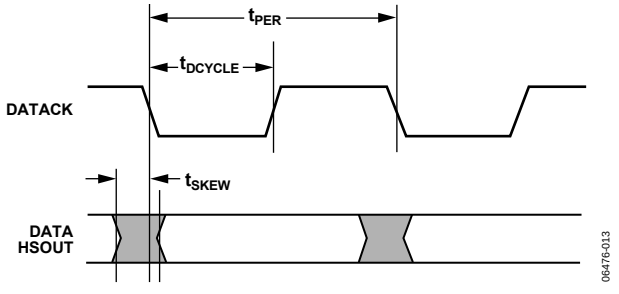


Figure 14. Output Timing

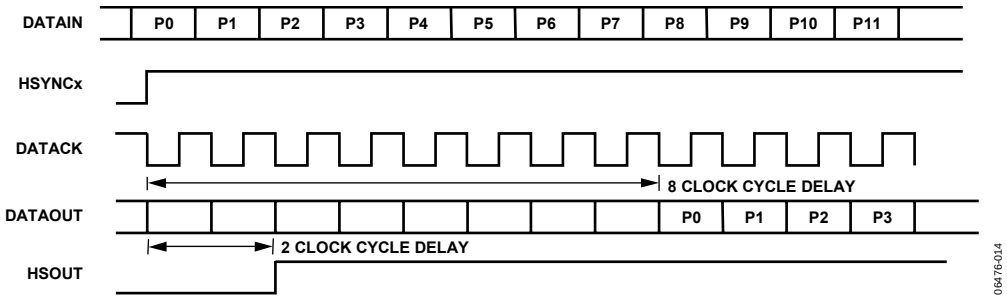


Figure 15. 4:4:4 Timing Mode

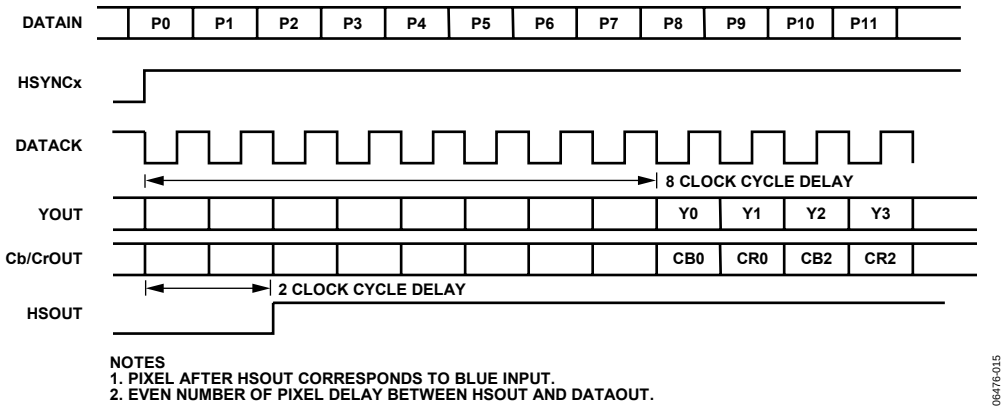


Figure 16. 4:2:2 Timing Mode

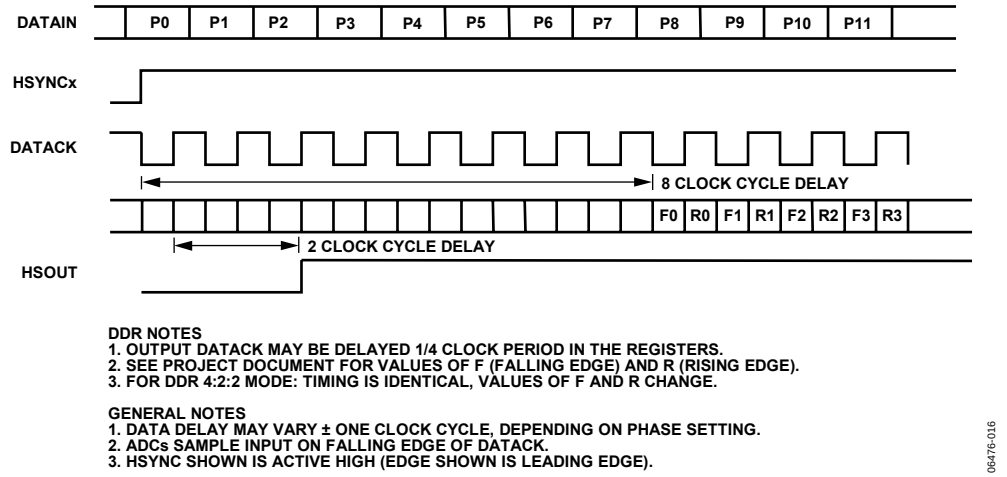


Figure 17. Double Data Rate (DDR) Timing Mode

HSYNC TIMING

The Hsync is processed in the AD9984A to eliminate ambiguity in the timing of the leading edge with respect to the phase-delayed pixel clock and data.

The Hsync input is used as a reference to generate the pixel sampling clock. The sampling phase can be adjusted with respect to Hsync through a full 360° in 32 steps via the phase adjust register (to optimize the pixel sampling time). Display systems use Hsync to align memory and display write cycles. Therefore, it is important to have a stable timing relationship between the Hsync output (HSOUT) and data clock (DATACK).

Three things happen to Hsync in the AD9984A. First, the polarity of Hsync input is determined and, as a result, has a known output polarity. The known output polarity can be programmed either active high or active low (Register 0x12, Bit 3). Second, HSOUT is aligned with DATACK and data outputs. Third, the duration of HSOUT (in pixel clocks) is set via Register 0x13. HSOUT is the sync signal that should be used to drive the rest of the display system.

COAST TIMING

In most computer systems, the Hsync signal is provided continuously on a dedicated wire. In these systems, the COAST input and function are unnecessary and should not be used.

In some systems, however, Hsync is disturbed during the vertical sync period (Vsync). In some cases, Hsync pulses disappear. In other systems, such as those that employ composite sync (Csync) signals or embedded sync-on-green, Hsync can include equalization pulses or other distortions during Vsync. To avoid upsetting the clock generator during Vsync, it is important to ignore these distortions. If the pixel clock PLL sees extraneous pulses, it attempts to lock to this new frequency, and changes frequency by the end of the Vsync period. It then takes a few lines of correct Hsync timing to recover at the beginning of a new frame, resulting in a tearing of the image at the top of the display.

The COAST input is provided to eliminate this problem. It is an asynchronous input that disables the PLL input and holds the clock at its current frequency. The PLL can free run for several lines without significant frequency drift. Coast can be generated internally by the AD9984A (see Register 0x18) or can be provided externally by the graphics controller.

When internal coast is selected (Register 0x18, Bit 7 = 0, and Register 0x14, Bits[7:6] to select source), Vsync is used as a basis for determining the position of coast. The internal coast signal is enabled a programmed number of Hsync periods before the periodic Vsync signal (Precoast Register 0x16), and it is dropped a programmed number of Hsync periods after Vsync (Postcoast Register 0x17). It is recommended that the Vsync filter be enabled when using the internal coast function to allow the AD9984A to precisely determine the number of Hsyncs/Vsync and their location. In many applications where disruptions occur and coast is used, values of 2 for precoast and 10d for postcoast are sufficient to avoid most extraneous pulses.

OUTPUT FORMATTER

The output formatter is capable of generating several output formats to be presented to the 30 data output pins. The output formats and the pin assignments for each format are listed in Table 12. In addition, there are several clock options for the output clock. The user can select the pixel clock, a 90° phase-shifted pixel clock, a 2× pixel clock, or a 0.5× pixel clock for test purposes. The output clock can also be inverted.

Data output is available as 30-pin RGB or YCbCr, or, if either 4:2:2 or 4:4:4 DDR is selected, a secondary channel is available. This secondary channel is always 4:2:2 DDR. It contains the same video data as the primary channel and can be utilized by either another display or storage device. Depending on the choice of output modes, the primary output can be 30 pins, 20 pins, or as few as 15 pins.

Mode Descriptions

4:4:4

All channels come out with their 10 data bits at the same time. Data is aligned to the negative edge of the clock for easy capture. This is the normal 30-bit output mode for RGB or 4:4:4 YCbCr.

4:2:2

Red and green channels contain 4:2:2 formatted data (20 pins) with Y data on the green channel and Cb, Cr data on the red channel. Data is aligned to the negative edge of the clock. The blue channel contains the secondary channel with Cb, Y, Cr, Y formatted 4:2:2 DDR data. The data edges are aligned to both edges of the pixel clock, therefore, using a 90° clock may be necessary to capture the DDR data.

4:4:4 DDR

This mode puts out full 4:4:4 data on 15 bits of the red and green channels, thus saving 15 pins. The first half (RGB[14:0]) of the 30-bit data is sent on the rising edge and the second half (RGB[29:15]) is sent on the falling edge. DDR 4:2:2 data is sent on the blue channel, as in 4:2:2 mode.

RGB[29:0] = R[9:0] + G[9:0] + B[9:0], so
RGB[29:15] = R[9:0] + G[9:5] and
RGB[14:0] = G[4:0] + B[9:0]

Table 12. Output Formats[1]

Port	Red										Green										Blue									
Bit	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0
4:4:4	Red/Cr										Green/Y										Blue/Cb									
4:2:2[2]	Cb, Cr										Y										DDR 4:2:2 ↑Cb,Cr ↓Y,Y									
4:4:4 DDR	DDR ↑G[4:0]					DDR ↑B[9:0]										N/A					DDR 4:2:2 ↑Cb,Cr									
	DDR ↓R[9:0]										DDR ↓G[9:5]					N/A					DDR 4:2:2 ↓Y,Y									

[1] Arrows in table indicate clock edge. Rising edge of clock = ↑, falling edge = ↓.
[2] For 4:2:2 modes, Cb is sent before Cr.

2-WIRE SERIAL CONTROL PORT

A 2-wire serial control interface is provided with the AD9984A. Up to two AD9984A devices can be connected to the 2-wire serial interface with each device having a unique address.

The 2-wire serial interface comprises a clock (SCL) and a bi-directional data (SDA) pin. The analog flat panel interface acts as a slave for receiving and transmitting data over the serial interface. When the serial interface is not active, the logic levels on SCL and SDA are pulled high by external pull-up resistors.

Data received or transmitted on the SDA line must be stable for the duration of the positive-going SCL pulse. Data on SDA must change only when SCL is low. If SDA changes state while SCL is high, the serial interface interprets that action as a start or stop sequence.

The following are the five components to serial bus operation:

- Start signal
- Slave address byte
- Base register address byte
- Data byte to read or write
- Stop signal

When the serial interface is inactive (SCL and SDA are high), communication is initiated by sending a start signal. The start signal is a high-to-low transition on SDA while SCL is high. This signal alerts all slaved devices that a data transfer sequence is coming.

The first 8 bits of data transferred after a start signal comprise a 7-bit slave address (the first seven bits) and a single R/$\overline{W}$ bit (the eighth bit). The R/$\overline{W}$ bit indicates the direction of data transfer, read from 1 or write to 0 on the slave device. If the transmitted slave address matches the address of the device, the AD9984A acknowledges the match by bringing SDA low on the ninth SCL pulse. If the addresses do not match, the AD9984A does not acknowledge it.

Table 13. Serial Port Addresses

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1
A6 (MSB)	A5	A4	A3	A2	A1	A0
1	0	0	1	1	0	0
1	0	0	1	1	0	1

DATA TRANSFER VIA SERIAL INTERFACE

For each byte of data read or written, the MSB is the first bit in the sequence.

If the AD9984A does not acknowledge the master device during a write sequence, the SDA remains high so the master can generate a stop signal. If the master device does not acknowledge the AD9984A during a read sequence, the AD9984A interprets this as end of data. The SDA remains high so the master can generate a stop signal.

Writing data to specific control registers of the AD9984A requires writing to the 8-bit address of the control register of interest after the slave address has been established. This control register address is the base address for subsequent write operations. After the initial data byte is written, the base address auto-increments by one for each additional data byte. If more bytes are transferred than available addresses, the address does not increment and remains at its maximum value of 0x44. Any base address higher than 0x44 does not produce an acknowledge signal. Data is read from the control registers of the AD9984A in a similar manner. Reading requires two data transfer operations.

- The base address must be written with the R/$\overline{W}$ bit of the slave address byte low to set up a sequential read operation. Reading (the R/$\overline{W}$ bit of the slave address byte high) begins at the previously established base address. The address of the read register auto-increments after each byte is transferred.
- To terminate a read/write sequence to the AD9984A, a stop signal must be sent. A stop signal comprises a low-to-high transition of SDA while SCL is high.

A repeated start signal occurs when the master device driving the serial interface generates a start signal without first generating a stop signal to terminate the current communication. This is used to change the mode of communication (read, write) between the slave and master without releasing the serial interface lines.

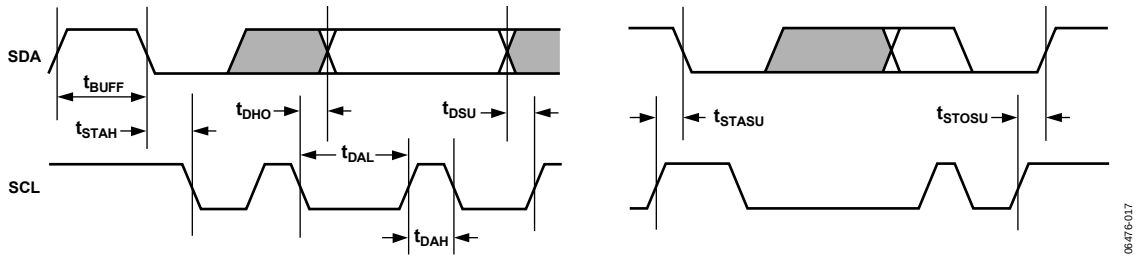


Figure 18. Serial Port Read/Write Timing

Serial Interface Read/Write Examples

Write to One Control Register

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Data byte to base address
5. Stop signal

Write To Four Consecutive Control Registers

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Data byte to base address
5. Data byte to (base address + 1)
6. Data byte to (base address + 2)
7. Data byte to (base address + 3)
8. Stop signal

Read from One Control Register

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Start signal
5. Slave address byte (R/$\overline{W}$ bit = high)
6. Data byte from base address
7. Stop signal

Read from Four Consecutive Control Registers

1. Start signal
2. Slave address byte (R/$\overline{W}$ bit = low)
3. Base address byte
4. Start signal
5. Slave address byte (R/$\overline{W}$ bit = high)
6. Data byte from base address
7. Data byte from (base address + 1)
8. Data byte from (base address + 2)
9. Data byte from (base address + 3)
10. Stop signal

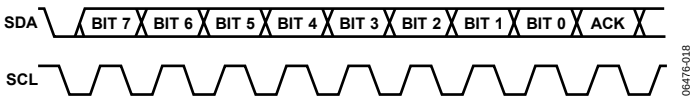


Figure 19. Serial Interface—Typical Byte Transfer

2-WIRE SERIAL REGISTER MAP

The AD9984A is initialized and controlled by a set of registers that determine the operating modes. An external controller is employed to write and read the control registers through the 2-wire serial interface port.

Table 14. Control Register Map

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
0x00	RO	7:0	0010 0000	Chip Revision	An 8-bit register that represents the silicon revision level.
0x01	R/$\overline{W}$	7:0	0110 1001	PLL Div MSBs	The 8 MSBs (Bits[11:4] of the PLL Divider. Larger values mean the PLL operates at a faster rate. This register should be loaded first when a change is needed. (This gives the PLL more time to lock).[1]
0x02	R/$\overline{W}$	7:4	1101 ****	PLL Div LSBs	The 4 LSBs (Bits[3:0]) of the PLL Divider. Links to the PLL Div MSB to make a 12-bit register.[1]
0x03	R/$\overline{W}$	7:6	01** ****	VCO/CPMP	VCO Range Select. Chooses the VCO frequency range (see the Clock Generation section).
		5:3	**00 1***		Charge Pump Current. Varies the current that drives the low-pass filter (see the Clock Generation section).
		2	**** *0**		External Clock Enable.
0x04	R/$\overline{W}$	7:3	1000 0***	Phase Adjust	ADC Clock Phase Adjust. Larger values mean more delay. (1 LSB = T/32).
0x05	R/$\overline{W}$	6:0	*100 0000	Red Gain MSBs	The 7 MSBs of the Red Channel Gain Control. Controls ADC input range (contrast) of each respective channel. Larger values give less contrast.
0x06	R/$\overline{W}$	7:6	00** ****	Red Gain LSBs	The 2 LSBs of the Red Channel Gain Control. Links with Register 0x05 to form the 9-bit red gain that controls the ADC input range (contrast) of the red channel. A lower value corresponds to a higher gain.[1]
0x07	R/$\overline{W}$	6:0	*100 0000	Green Gain MSBs	The 7 MSBs of the Green Channel Gain Control. Controls ADC input range (contrast) of each respective channel. Larger values give less contrast.
0x08	R/$\overline{W}$	7:6	00** ****	Green Gain LSBs	The 2 LSBs of the Green Channel Gain Control. Links to Register 0x07 to form the 9-bit green gain that controls the ADC input range (contrast) of the green channel. A lower value corresponds to a higher gain.[1]
0x09	R/$\overline{W}$	6:0	*100 0000	Blue Gain MSBs	The 7 MSBs of the Blue Channel Gain Control. Controls ADC input range (contrast) of each respective channel. Larger values give less contrast.
0x0A	R/$\overline{W}$	7:6	00** ****	Blue Gain LSBs	The 2 LSBs of the Blue Channel Gain Control. Links to Register 0x09 to form the 9-bit blue gain that controls the ADC input range (contrast) of the blue channel. A lower value corresponds to a higher gain.[1]
0x0B	R/$\overline{W}$	7:0	0100 0000	Red Offset MSBs	The 8 MSBs of the Red Channel Offset Control. Controls dc offset (brightness) of each respective channel. Larger values decrease brightness.[1]
0x0C	R/$\overline{W}$	7:5	000* ****	Red Offset LSBs	The 3 LSBs of the Red Channel Offset Control. Links to Register 0x0B to form the 11-bit red offset that controls the dc offset (brightness) of the red channel in auto-offset mode.
0x0D	R/$\overline{W}$	7:0	0100 0000	Green Offset MSBs	The 8 MSBs of the Green Channel Offset Control. Controls dc offset (brightness) of each respective channel. Larger values decrease brightness.[1]
0x0E	R/$\overline{W}$	7:5	000* ****	Green Offset LSBs	The 3 LSBs of the Green Channel Offset Control. Links to Register 0x0D to form the 11-bit green offset that controls the dc offset (brightness) of the green channel in auto-offset mode.
0x0F	R/$\overline{W}$	7:0	0100 0000	Blue Offset MSBs	The 8 MSBs of the Blue Channel Offset Control. Controls dc offset (brightness) of each respective channel. Larger values decrease brightness.[1]
0x10	R/$\overline{W}$	7:5	000* ****	Blue Offset LSBs	The 3 LSBs of the Blue Channel Offset Control. Links to Register 0x0F to form the 11-bit blue offset that controls the dc offset (brightness) of the blue channel in auto-offset mode.
0x11	R/$\overline{W}$	7:0	0010 0000	Sync Separator Threshold	Sets the threshold of the sync separator's digital comparator.
0x12	R/$\overline{W}$	7	0*** ****	Hsync Control	Hsync Source Override. 0 = The chip determines the active Hsync source. 1 = The active Hsync source is set by Reg. 0x12, Bit 6.

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
		6	*0** ****		Hsync Source Select. Determines the source of the Hsync for PLL and sync processing. This bit is used only if Reg. 0x12, Bit 7 is set to 1 or if both syncs are active. 0 = Hsync is from HSYNCx input pin. 1 = Hsync is from SOG.
		5	**0* ****		Hsync Input Polarity Override. 0 = The chip selects the Hsync input polarity. 1 = The input polarity of Hsync is controlled by Reg. 0x12, Bit 4.
		4	***1 ****		Hsync Input Polarity. This bit is used only if Reg. 0x12, Bit 5 is set to 1. 0 = Hsync input polarity is negative. 1 = Hsync input polarity is positive.
		3	**** 1***		Hsync Output Polarity. Sets the polarity of the Hsync output signal (HSOUT). 0 = HSOUT polarity is negative. 1 = HSOUT polarity is positive.
0x13	R/$\overline{W}$	7:0	0010 0000	Hsync Duration	Sets the number of pixel clocks that HSOUT is active.
0x14	R/$\overline{W}$	7	0*** ****	Vsync Control	Vsync Source Override. 0 = The chip determines the active Vsync source. 1 = The active Vsync source is set by Reg. 0x14, Bit 6.
		6	*0** ****		Vsync Source Select. Determines the source of Vsync for sync processing. This bit is used only if Reg. 0x14, Bit 7 is set to 1. 0 = Vsync is from the VSYNCx input pin. 1 = Vsync is from the sync separator.
		5	**0* ****		Vsync Input Polarity Override. 0 = The chip selects Vsync input polarity. 1 = The input polarity of Vsync is set by Reg. 0x14, Bit 4.
		4	***1 ****		Vsync Input Polarity. This bit is used only if Reg. 0x14, Bit 5 is set to 1. 0 = Vsync input polarity is negative. 1 = Vsync input polarity is positive.
		3	**** 1***		Vsync Output Polarity. Sets the polarity of the output Vsync signal (VSOUT). 0 = VSOUT polarity is negative. 1 = VSOUT polarity is positive.
		2	**** *0**		Vsync Filter Enable. This needs to be enabled when using the Hsync to Vsync counter. 0 = The Vsync filter is disabled. 1 = The Vsync filter is enabled.
		1	**** **0*		Vsync Duration Block Enable. This is designed to be used with the Vsync filter. 0 = Vsync output duration is unchanged. 1 = Vsync output duration is set by Register 0x15.
0x15	R/$\overline{W}$	7:0	0000 1010	Vsync Duration	Sets the number of Hsyncs that Vsync out is active. This is only used if Reg. 0x14, Bit 1 is set to 1.
0x16	R/$\overline{W}$	7:0	0000 0000	Precoast	The number of Hsync periods to coast prior to Vsync.
0x17	R/$\overline{W}$	7:0	0000 0000	Postcoast	The number of Hsync periods to coast after Vsync.
0x18	R/$\overline{W}$	7	0*** ****	Coast and Clamp Control	Coast Source. Determines the source of the coast signal. 0 = Using internal coast generated from Vsync. 1 = Using external coast signal from COAST pin.
		6	*0** ****		Coast Polarity Override. 0 = The chip selects the coast polarity. 1 = The polarity of the coast signal is set by Reg. 0x18, Bit 5.
		5	**1* ****		Coast Polarity. This bit is used only if Reg. 0x18, Bit 6 is set to 1. 0 = Coast polarity is negative. 1 = Coast polarity is positive.
		4	***0 ****		Clamp Source Select. Determines the source of the clamp timing. 0 = Uses the internal clamp generated from Hsync. 1 = Uses the external CLAMP signal.

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
		3	**** 0***		Red Clamp Select. 0 = Clamp the red channel to ground. 1 = Clamp the red channel to midscale.
		2	**** *0**		Green Clamp Select. 0 = Clamp the green channel to ground. 1 = Clamp the green channel to midscale.
		1	**** **0*		Blue Clamp Select. 0 = Clamp the blue channel to ground. 1 = Clamp the blue channel to midscale.
		0	**** ***0		Must be set to 0 for proper operation.
0x19	R/$\overline{W}$	7:0	0000 1000	Clamp Placement	Places the clamp signal an integer number of clock periods after the trailing edge of the Hsync signal.
0x1A	R/$\overline{W}$	7:0	0010 0000	Clamp Duration	Number of clock periods that the clamp signal is actively clamping.
0x1B	R/$\overline{W}$	7	0*** ****	Clamp and Offset	Clamp Polarity Override. 0 = The chip selects the clamp polarity. 1 = The polarity of the clamp signal is set by Reg. 0x1B, Bit 6.
		6	*1** ****		Clamp Polarity. This bit is used only if Reg. 0x1B, Bit 7 is set to 1. 0 = Clamp polarity is negative. 1 = Clamp polarity is positive.
		5	**0* ****		Auto-Offset Enable. 0 = Auto-offset is disabled. 1 = Auto-offset is enabled (offsets become the desired clamp code).
		4:3	***1 1***		Auto-Offset Update Frequency. This selects how often the auto-offset circuit operates. 00 = Every 3 clamps. 01 = Every 48 clamps. 10 = Every 192 clamps. 11 = Every 3 Vsync periods.
		2:0	**** *011		Must be written to default (011) for proper operation.
0x1C	R/$\overline{W}$	7:0	1111 1111	Test Register 0	Must be set to 0xFF for proper operation.
0x1D	R/$\overline{W}$	7:3	0111 1***	SOG Control	SOG Slicer Comparator Threshold. Sets the voltage level of SOG slicer's comparator.
		2	**** *0**		SOGOUT Polarity. Sets the polarity of the signal on the SOGOUT pin. 0 = SOGOUT polarity is negative. 1 = SOGOUT polarity is positive.
		1:0	**** **00		SOGOUT Select. 00 = Raw SOGINx. 01 = Raw HSYNCx. 10 = Regenerated Hsync from sync filter. 11 = Filtered Hsync from sync filter.
0x1E	R/$\overline{W}$	7	*** ****	Input and Power Control	Channel Select Override. 0 = The chip determines which input channels to use. 1 = The input channel selection is determined by Reg. 0x1E, Bit 6.
		6	*0** ****		Channel Select. This is used only if Reg. 0x1E, Bit 7 is set to 1, or if syncs are present on both channels. 0 = Channel 0 syncs and data are selected. 1 = Channel 1 syncs and data are selected.
		5	**1* ****		Programmable Bandwidth. 0 = Low analog input bandwidth (~7 MHz). 1 = High analog input bandwidth (~300 MHz).
		4	***1 ****		Power-Down Control Select. 0 = Manual power-down control. 1 = Auto power-down control.
		3	**** 0***		Power-Down. 0 = Normal operation. 1 = Power-down.

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
		2	**** *0**		Power-Down Pin Polarity. Sets the polarity of the signal on the PWRDN pin. 0 = PWRDN polarity is negative. 1 = PWRDN polarity is positive.
		1	**** **0*		Power-Down Fast Switching Control. 0 = Normal power-down operation. 1 = The chip stays powered up, and the outputs are put in high impedance mode.
		0	**** ***0		SOGOUT High Impedance Control. 0 = SOGOUT operates as normal during power-down. 1 = SOGOUT is in high impedance during power-down.
0x1F	R/$\overline{W}$	7:5	100* ****	Output Select 1	Output Mode. 100 = 4:4:4 RGB mode. 101 = 4:2:2 YCbCr mode. 110 = 4:4:4 DDR mode.
		4	***1 ****		Primary Output Enable. 0 = Primary output is in high impedance state. 1 = Primary output is enabled.
		3	**** 0***		Secondary Output Enable. 0 = Secondary output is in high impedance state. 1 = Secondary output is enabled.
		2:1	**** *10*		Output Drive Strength. Applies to all outputs except VSOUT. 00 = Low output drive strength. 01 = Medium output drive strength. 1x = High output drive strength.
		0	**** ***0		Output Clock Invert. Applies to all clocks output on DATACK. 0 = Noninverted Pixel Clock. 1 = Inverted Pixel Clock.
0x20	R/$\overline{W}$	7:6	0*** ****	Output Select 2	Output Clock Select. 00 = Pixel clock. 01 = 90° phase-shifted pixel clock. 10 = 2× pixel clock. 11 = 0.5× pixel clock.
		5	*0** ****		Output High Impedance. 0 = Normal outputs. 1 = All outputs except SOGOUT in high impedance mode.
		4	**0* ****		SOGOUT High Impedance. 0 = Normal drive. 1 = SOGOUT pin is in high impedance mode.
		3	***0 ****		Field Output Polarity. Sets the polarity of the field output signal. 0 = Active low is an even field, active high is an odd field. 1 = Active low is an odd field, active high is an even field.
		2	**** 1***		PLL Sync Filter Enable. 0 = PLL uses raw HSYNCx/SOGINx. 1 = PLL uses filtered Hsync/SOG.
		1	**** *0**		Sync Processing Input Select. Selects the sync source for the sync processor. 0 = Sync processing uses raw HSYNCx/SOGINx. 1 = Sync processing uses regenerated Hsync from sync filter.
		0	**** ***0		Must be set to 1 for proper operation.
0x21	R/$\overline{W}$	7:0	0010 0000		Must be set to default for proper operation.
0x22	R/$\overline{W}$	7:0	0011 0010		Must be set to default for proper operation.
0x23	R/$\overline{W}$	7:0	0000 1010	Sync Filter Window Width	Sets the window of time around the regenerated Hsync leading edge (in 25 ns steps) that sync pulses are allowed to pass through.
0x24	RO	7	_*** ****	Sync Detect	HSYNC0 Detection. 0 = HSYNC0 is not active. 1 = HSYNC0 is active.

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
		6	*_** ****		HSYNC1 Detection. 0 = HSYNC1 is not active. 1 = HSYNC1 is active.
		5	**_* ****		VSYNC0 Detection. 0 = VSYNC0 is not active. 1 = VSYNC0 is active.
		4	***_ ****		VSYNC1 Detection. 0 = VSYNC1 is not active. 1 = VSYNC1 is active.
		3	**** _***		SOGIN0 Detection. 0 = SOGIN0 is not active. 1 = SOGIN0 is active.
		2	**** *_**		SOGIN1 Detection. 0 = SOGIN1 is not active. 1 = SOGIN1 is active.
		1	**** **_*		COAST Detection. 0 = External COAST is not active. 1 = External COAST is active.
		0	**** ***_		CLAMP Detection. 0 = External CLAMP is not active. 1 = External CLAMP is active.
0x25	RO	7	_*** ****	Sync Polarity Detect	HSYNC0 Polarity. 0 = HSYNC0 polarity is negative. 1 = HSYNC0 polarity is positive.
		6	*_** ****		HSYNC1 Polarity. 0 = HSYNC1 polarity is negative. 1 = HSYNC1 polarity is active high.
		5	**_* ****		VSYNC0 Polarity. 0 = VSYNC0 polarity is negative. 1 = VSYNC0 polarity is positive.
		4	***_ ****		VSYNC1 Polarity. 0 = VSYNC1 polarity is negative. 1 = VSYNC1 polarity is positive.
		3	**** _***		COAST Polarity. 0 = External COAST is negative. 1 = External COAST is positive.
		2	**** *_**		CLAMP Polarity. 0 = External CLAMP is negative. 1 = External CLAMP polarity is positive.
		1	**** **_*		Extraneous Pulse Detection. 0 = No extraneous pulses detected on Hsync. 1 = Extraneous pulses detected on Hsync.
		0	**** ***_		Sync Filter Lock. 0 = Sync filter unlocked 1 = Sync filter locked.
0x26	RO	7:0		Hsyncs per Vsync MSBs	MSBs of Hsyncs per Vsync count.
0x27	RO	7:4		Hsyncs per Vsync LSBs	LSBs of Hsyncs per Vsync count.
0x28	R/$\overline{W}$	7:0	1011 1111	Test Register 1	Must be written to 0xBF for proper operation.
0x29	R/$\overline{W}$	7:0	0000 0010	Test Register 2	Must be written to 0x02 for proper operation.
0x2A	RO	7:0		Test Register 3	Read only bits for future use.
0x2B	RO	7:0		Test Register 4	Read only bits for future use.
0x2C	R/$\overline{W}$	7:5	000* ****	Offset Hold	Must be written to default for proper operation.

Hex Address	Read/Write, Read Only	Bits	Default Value	Register Name	Description
		4	***0 ****		Auto-Offset Hold. Disables the auto-offset and holds the feedback result. 0 = Continuous update. 1 = One time update.
		3:0	**** 0000		Must be written to default for proper operation.
0x2D	R/$\overline{W}$	7:0	1111 0000	Test Register 5	Must be written to 0xE8 for proper operation.
0x2E	R/$\overline{W}$	7:0	1111 0000	Test Register 6	Must be written to 0xE0 for proper operation.
0x34	R/$\overline{W}$	2	**** *0**	SOG Filter	SOG Filter Enable. When enabled, filters out SOG inputs less than 250 ns. 0 = SOG filter disabled. 1 = SOG filter enabled.
0x36	R/$\overline{W}$	0	**** ***0	VCO Gear	VCO Gear Select. Adds another range to the VCO. Used for lower frequencies only. 0 = Disable low VCO gear. 1 = Enable low VCO gear.
0x3C	R/$\overline{W}$	7:4	0000 ****	Auto Gain	Test Bits. Must be set to default for proper operation.
		3	**** 0***		Auto Gain Matching Hold. 0 = Disables auto gain updates and holds the current auto offset values. 1 = Allows auto gain to continuously update.
		2:0	**** *000		Auto Gain Matching Enable. 000 = Auto gain matching is disabled. 110= Auto gain matching is enabled.

[1] Functions with more than eight control bits, such as PLL divide ratio, gain, and offset, are only updated when the LSBs are written to (for example, Register 0x02 for PLL divide ratio).

2-WIRE SERIAL CONTROL REGISTERS

CHIP IDENTIFICATION

0x00—Bits[7:0] Chip Revision

This is an 8-bit register that represents the silicon revision.

PLL DIVIDER CONTROL

0x01—Bits[7:0] PLL Divide Ratio MSBs

These are the 8 MSBs of the 12-bit PLL divide ratio (PLLDIV). The PLL derives a pixel clock from the incoming Hsync signal. The pixel clock frequency is then divided by an integer value, such that the output is phase-locked to Hsync. This PLLDIV value determines the number of pixel times (pixels plus horizontal blanking overhead) per line. This is typically 20% to 30% more than the number of active pixels in the display.

The 12-bit value of the PLL divider supports divide ratios from 2 to 4095 as long as the output frequency is within range. The higher the value loaded in this register, the higher the resulting clock frequency with respect to a fixed Hsync frequency.

VESA has established some standard timing specifications that assist in determining the value for PLLDIV as a function of horizontal and vertical display resolution and frame rate (see Table 10). However, many computer systems do not precisely conform to the recommendations. As a result, these numbers should be used only as a guide. The display system manufacturer should provide automatic or manual means for optimizing PLLDIV. An incorrectly set PLLDIV usually produces one or more vertical noise bars on the display. The greater the error, the greater the number of bars produced.

The power-up default value of PLLDIV is 1693. PLLDIVM = 0x69, PLLDIVL = 0xDX.

The AD9984A updates the full divide ratio only when the LSBs are written. Writing to this register by itself does not trigger an update.

0x02—Bits[7:4] PLL Divide Ratio LSBs

These are the four LSBs of the 12-bit PLL divide ratio (PLLDIV). The power-up default value of PLLDIV is 1693. PLLDIVM = 0x69, PLLDIVL = 0xDX.

CLOCK GENERATOR CONTROL

0x03—Bits[7:6] VCO Range Select

These two bits establish the operating range of the clock generator. VCO range must be set to correspond to the desired operating frequency (incoming pixel rate). The PLL gives the best jitter performance at high frequencies. For this reason, to output low pixel rates and still achieve good jitter performance, the PLL operates at a higher frequency, but then divides down the clock rate afterwards. See Table 15 for the pixel rates of each VCO range setting. The PLL output divisor is automatically selected with the VCO range setting. The power-up default value is 01.

Table 15. VCO Range Select Bits

Value	Result (Pixel Rates)
00	10 to 31
01	31 to 62
10	62 to 124
11	124 to 170

0x03—Bits[5:3] Charge Pump Current

These three bits establish the current driving the loop filter in the clock generator. The current must be set to correspond with the desired operating frequency. The power-up default value is current = 001.

Table 16. Charge Pump Current Bits

Ip2	Ip1	Ip0	Result (Current)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

0x03—Bit[2] External Clock Enable

This bit determines the source of the pixel clock.

Table 17. External Clock Enable Bit

Value	Result
0	Internally generated clock.
1	Externally provided clock signal.

A Logic 0 enables the internal PLL that generates the pixel clock from an externally provided Hsync.

A Logic 1 enables the external EXTCK input pin. In this mode, the PLL divide ratio (PLLDIV) is ignored. The clock phase adjust (Phase) is still functional. The power-up default value is EXTCK = 0.

PHASE ADJUST

0x04—Bits[7:3] ADC Clock Phase Adjust

These bits adjust the phase for the DLL to generate the ADC clock. The 5-bit value adjusts the sampling phase in 32 steps across one pixel time. Each step represents an 11.25° shift in sampling phase. The power-up default is 16.

INPUT GAIN

The AD9984A can accommodate input signals with a full-scale range between 0.5 V and 1.0 V p-p. Setting the red, green, or blue channel gain to 511 corresponds to an input range of 1.0 V. A red, green, or blue channel gain of 0 establishes an input range of 0.5 V. Note that increasing gain results in the picture having less contrast (the input signal uses fewer available converter codes).

0x05—Bits[6:0] Red Channel Gain Control MSBs

This register contains the 7-bit MSBs of the red channel gain control. Values written to this register are not updated until the LSB register (Register 0x06) has also been written to. The power-up default is 1000000.

0x06 —Bits[7:6] Red Channel Gain Control LSBs

This register contains the 2-bit LSBs of the red channel gain control. Along with the 7 MSBs of gain control in Register 0x05, there are 9 bits of gain control. Default power-up value is 00.

0x07—Bits[6:0] Green Channel Gain Control MSBs

This register contains the 7-bit MSBs of the green channel gain control. Register update requires writing 0x00 to Register 0x08.

0x08—Bits[7:6] Green Channel Gain Control LSBs

This register contains the 2-bit LSBs of the green channel gain control. Along with the 7 MSBs of gain control in Register 0x07, there are 9 bits of gain control. Default power-up value is 00.

0x09—Bits[6:0] Blue Channel Gain Control MSBs

This register contains the 7-bit MSBs of the blue channel gain control. Register update requires writing 0x00 to Register 0x0A.

0x0A—Bits[7:6] Blue Channel Gain Control LSBs

This register contains the 2-bit LSBs of the blue channel gain control. Along with the 7 MSBs of gain control in Register 0x09, there are 9 bits of gain control. Default power-up value is 00.

INPUT OFFSET

The offset control shifts the analog input, resulting in a change in brightness. Note that the function of the red, blue, or green channel offset registers depends on whether auto-offset is enabled (Register 0x1B, Bit 5).

If auto-offset is disabled, nine bits of the offset registers (Bits[6:0] of the offset MSB register plus Bits[7:6] of the following register) control the absolute offset added to the channel (for the red channel, Register 0x0B, Bits[6:0] plus Register 0x0C, Bits[7:6]) control the absolute offset added to the channel. The offset control provides a ±255 LSBs of adjustment range, with 1 LSB of offset corresponding to 1 LSB of output code.

If auto-offset is enabled, the 11-bit offset (comprised of the 8 bits of the MSB register and Bits[7:5] of the following LSB register) determines the clamp target code. The 11-bit offset consists of 1 sign bit plus 10 bits. If the register is programmed to 530d, the output code is equal to 530d at the end of the clamp period. Note that incrementing the offset register setting by 1 LSB adds 1 LSB of offset, regardless of the auto-offset setting.

0x0B—Bits[7:0] Red Channel Offset Control MSBs

This register is the 8-bit MSBs of the red channel offset control. Along with the 3 LSBs in the red channel offset in Register 0x0C, there are 11 bits of dc offset control in the red channel. Values written to this register are not updated until the LSB register (Register 0x0C) has also been written to.

0x0C—Bits[7:5] Red Channel Offset Control LSBs

This register contains the 3-bit LSBs of the red channel offset control. Combining these bits with the 8 bits of MSBs in Register 0x0B creates 11 bits of offset control.

0x0D—Bits[7:0] Green Channel Offset Control MSBs

This register contains the 8-bit MSBs of the green channel offset control. Update of this register occurs only when Register 0x0E is also written to.

0x0E—Bits[7:5] Green Channel Offset Control LSBs

This register contains the 3-bit LSBs of the green channel offset control. Combining these bits with the 8 bits of MSBs in the Register 0x0D makes 11 bits of offset control.

0x0F—Bits[7:0] Blue Channel Offset Control MSBs

The 8-bit blue channel offset control. Update of this register occurs only when Register 0x10 is also written to.

0x10—Bits[7:5] Blue Channel Offset Control LSBs

The LSBs of the blue channel offset control combine with the 8 bits of MSBs in the Register 0x0F to make 11 bits of offset control.

HSYNC CONTROL

0x11—Bits[7:0] Sync Separator Threshold

This register sets the threshold of the sync separator's digital comparator. The value written to this register is multiplied by 200 ns to get the threshold value. Therefore, if a value of 5 is written, the digital comparator threshold is 1 µs and any pulses less than 1 µs are rejected by the sync separator. There is some variability to the 200 ns multiplier value. The maximum variability over all operating conditions is ±20% (160 ns to 240 ns). Because normal Vsync and Hsync pulse widths differ by a factor of about 500 or more, the 20% variability is not an issue. The power-up default value is 32d.

0x12—Bit[7] Hsync Source Override

This bit is the Hsync source override. Setting this bit to 0 allows the chip to determine the active Hsync source. Setting it to 1 uses Bit 6 of Register 0x12 to determine the active Hsync source. Power-up default value is 0.

Table 18. Hsync Source Override Bit

Value	Result
0	Hsync source determined by chip.
1	Hsync source determined by user (Register 0x12, Bit 6).

0x12—Bit[6] Hsync Source Select

This bit selects the source of the Hsync for PLL and sync processing (only if Bit 7 of Register 0x12 is set to 1 or if both syncs are active). Setting this bit to 0 specifies the Hsync from the input pin. Setting it to 1 selects Hsync from SOG. Power-up default is 0.

Table 19. Hsync Source Select Bit

Value	Result
0	HSYNCx input.
1	Hsync from SOG.

0x12—Bit[5] Hsync Input Polarity Override

This bit determines whether the chip selects the Hsync input polarity or if it is specified. Setting this bit to 0 allows the chip to automatically select the polarity of the input Hsync. Setting it to 1 indicates that Bit 4 of Register 0x12 specifies the polarity. Power-up default is 0.

Table 20. Hsync Input Polarity Override Bit

Value	Result
0	Hsync polarity determined by chip.
1	Hsync polarity determined by user (Register 0x12, Bit 4).

0x12—Bit[4] Hsync Input Polarity

If Bit 5 of Register 0x12 is 1, the value of this bit specifies the polarity of the input Hsync. Setting this bit to 0 indicates a negative Hsync input polarity. Setting this bit to 1 indicates a positive Hsync input polarity. Power-up default is 1.

Table 21. Hsync Input Polarity Bit

Value	Result
0	Hsync input polarity is negative.
1	Hsync input polarity is positive.

0x12—Bit[3] Hsync Output Polarity

This bit sets the polarity of the Hsync output (HSOUT). Setting this bit to 0 indicates a negative HSOUT polarity. Setting this bit to 1 indicates a positive HSOUT polarity.

Table 22. Hsync Output Polarity Bit

Value	Result
0	HSOUT polarity is negative.
1	HSOUT polarity is positive.

0x13—Bits[7:0] Hsync Duration

This 8-bit register sets the duration of the HSOUT pulse. The leading edge of the Hsync output is triggered by the internally generated, phase-adjusted, PLL feedback clock. The AD9984A then counts a number of pixel clocks equal to the value in this register. This triggers the trailing edge of HSOUT, which is also phase-adjusted.

VSYNC CONTROL

0x14—Bit[7] Vsync Source Override

This bit is the active Vsync override. Setting this to 0 allows the chip to determine the active Vsync source, setting it to 1 uses Bit 6 of Register 0x14 to determine the active Vsync source. Power-up default value is 0.

Table 23. Vsync Source Override Bit

Value	Result
0	Vsync source determined by chip.
1	Vsync source determined by user (Register 0x14, Bit 6).

0x14—Bit[6] Vsync Source Select

This bit selects the source of the Vsync for sync processing only if Bit 7 of Register 0x14 is set to 1. Setting Bit 6 to 0 specifies the Vsync from the input pin. Setting it to 1 selects Vsync from the sync separator. Power-up default is 0.

Table 24. Vsync Source Select Bit

Value	Result
0	Vsync from VSYNCx input pin.
1	Vsync from sync separator.

0x14—Bit[5] Vsync Input Polarity Override

This bit sets whether the chip selects the Vsync input polarity or if it is specified. Setting this bit to 0 allows the chip to automatically select the polarity of the input Vsync. Setting this bit to 1 indicates that Bit 4 of Register 0x14 specifies the polarity. Power-up default is 0.

Table 25. Vsync Input Polarity Override Bit

Value	Result
0	Vsync polarity determined by chip.
1	Vsync polarity determined by user (Register 0x14, Bit 4).

0x14—Bit[4] Vsync Input Polarity

If Bit 5 of Register 0x14 is 1, the value of this bit specifies the polarity of the input Vsync. Setting this bit to 0 indicates a negative Vsync input polarity. Setting this bit to 1 indicates a positive Vsync input polarity. Power-up default is 1.

Table 26. Vsync Input Polarity Bit

Value	Result
0	Vsync input polarity is negative.
1	Vsync input polarity is positive.

0x14—Bit[3] Vsync Output Polarity

This bit sets the polarity of the Vsync output (VSOUT). Setting this bit to 0 indicates a negative VSOUT polarity. Setting this bit to 1 indicates a positive VSOUT polarity. Power-up default is 1.

Table 27. Vsync Output Polarity Bit

Value	Result
0	VSOUT polarity is negative.
1	VSOUT polarity is positive.

0x14—Bit[2] Vsync Filter Enable

This bit enables the Vsync filter allowing precise placement of the Vsync with respect to the Hsync and facilitating the correct operation of the Hsyncs/Vsync count.

Table 28. Vsync Filter Enable Bit

Value	Result
0	Vsync filter disabled.
1	Vsync filter enabled.

0x14—Bit[1] Vsync Duration Block Enable

This enables the Vsync duration block, which is designed to be used with the Vsync filter. Setting the bit to 0 leaves the Vsync output duration unchanged. Setting the bit to 1 sets the Vsync output duration based on Register 0x15. Power-up duration is 0.

Table 29. Vsync Duration Block Enable Bit

Value	Result
0	Vsync output duration is unchanged.
1	Vsync output duration is set by Register 0x15.

0x15—Bits[7:0] Vsync Duration

This register is used to set the output duration of the Vsync, and is designed to be used with the Vsync filter. This is valid only if Register 0x14, Bit 1 is set to 1. Power-up default is 10d.

COAST AND CLAMP CONTROLS

0x16—Bits[7:0] Precoast

This register allows the internally generated coast signal to be applied prior to the Vsync signal. This is necessary in cases where pre-equalization pulses are present. The step size for this control is one Hsync period. For precoast to work correctly, it is necessary for both the Vsync filter (Register 0x14, Bit 2) and sync processing filter (Register 0x20, Bit 1) to either be enabled or disabled. The power-up default is 00.

0x17—Bits[7:0] Postcoast

This register allows the internally generated coast signal to be applied following the Vsync signal. This is necessary in cases where post equalization pulses are present. The step size for this control is one Hsync period. For postcoast to work correctly, it is necessary for both the Vsync filter (Register 0x14, Bit 2) and sync processing filter (Register 0x20, Bit 1) to be enabled or disabled. The power-up default is 00.

0x18—Bit[7] Coast Source

This bit is used to select the active coast source. The choices are the COAST input pin or Vsync. If Vsync is selected, the additional decision of using the VSYNCx input pin or the output from the sync separator needs to be made (Register 0x14, Bits[7:6]).

Table 30. Coast Source Bit

Value	Result
0	Vsync (internal coast).
1	COAST pin.

0x18—Bit[6] Coast Polarity Override

This register is used to override the internal circuitry that determines the polarity of the coast signal going into the PLL. The power-up default setting is 0.

Table 31. Coast Polarity Override Bit

Value	Result
0	Coast polarity determined by chip.
1	Coast polarity determined by user (Register 0x18, Bit 5).

0x18—Bit[5] Input Coast Polarity

This register sets the input coast polarity when Bit 6 of Register 0x18 is 1. The power-up default setting is 1.

Table 32. Input Coast Polarity Bit

Value	Result
0	Coast polarity is negative.
1	Coast polarity is positive.

0x18—Bit[4] Clamp Source Select

This bit determines the source of clamp timing. A 0 enables the clamp timing circuitry controlled by clamp placement and clamp duration. The clamp position and duration is counted from the leading edge of Hsync. A 1 enables the external CLAMP input pin. The three channels are clamped when the clamp signal is active. The polarity of clamp is determined by the CLAMP polarity bit. The power-up default setting is 0.

Table 33. Clamp Source Select Bit

Value	Result
0	Internally generated clamp.
1	Externally provided clamp signal (CLAMP).

0x18—Bit[3] Red Clamp Select

This bit determines whether the red channel is clamped to ground or to midscale. The power-up default setting is 0.

Table 34. Red Clamp Select Bit

Value	Result
0	Clamp to ground.
1	Clamp to midscale.

0x18—Bit[2] Green Clamp Select

This bit determines whether the green channel is clamped to ground or to midscale. The power-up default setting is 0.

Table 35. Green Clamp Select Bit

Value	Result
0	Clamp to ground.
1	Clamp to midscale.

0x18—Bit[1] Blue Clamp Select

This bit determines whether the blue channel is clamped to ground or to midscale. The power-up default setting is 0.

Table 36. Blue Clamp Select Bit

Value	Result
0	Clamp to ground.
1	Clamp to midscale.

0x18—Bit[0]

Must be set to 0 for proper operation.

0x19—Bits[7:0] Clamp Placement

An 8-bit register that sets the position of the internally generated clamp. When clamp source select = 0 (Register 0x18, Bit 4), a clamp signal is generated internally at a position established by this register and for a duration set by the clamp duration register (Register 0x1A). Clamping is started at the clamp placement count of pixel periods after the trailing edge of Hsync. The clamp placement can be programmed to any value between 1 and 255. A value of 0 is not supported.

The clamp should be placed during a time that the input signal presents a stable black-level reference, usually the back porch period between Hsync and the image. When clamp source = 1, this register is ignored. Power-up default setting is 8.

0x1A—Bits[7:0] Clamp Duration

An 8-bit register that sets the duration of the internally generated clamp. When the clamp source select is 0 (Register 0x18, Bit 4), a clamp signal is generated internally at a position established by the clamp placement register (Register 0x19) for a duration set by this clamp duration register. Clamping begins a clamp placement count (Register 0x19) of pixel periods after the trailing edge of Hsync. The clamp duration can be programmed to any value between 1 and 255. A value of 0 is not supported.

For the best results, the clamp duration should be set to include the majority of the black reference signal time that follows the Hsync signal trailing edge. Insufficient clamping time can produce brightness changes at the top of the screen, and a slow recovery from large changes in the average picture level (APL) or brightness. When EXTCLMP = 1, this register is ignored. Power-up default setting is 20d.

0x1B—Bit[7] Clamp Polarity Override

This bit is used to override the internal circuitry that determines the polarity of the clamp signal. The power-up default setting is 0.

Table 37. Clamp Polarity Override Bit

Value	Result
0	Clamp polarity determined by chip.
1	Clamp polarity determined by user (Register 0x1B, Bit 6).

0x1B—Bit[6] Clamp Polarity

This bit indicates the polarity of the clamp signal only if Bit 7 of Register 0x1B = 1. The power-up default setting is 1.

Table 38. Clamp Polarity Bit

Value	Result
0	Clamp polarity is negative.
1	Clamp polarity is positive.

0x1B—Bit[5] Auto-Offset Enable

This bit selects between auto-offset mode and manual offset mode (auto-offset disabled). See the Automatic Offset section for more information. The power-up default setting is 0.

Table 39. Auto-Offset Enable Bit

Value	Result
0	Auto-offset is disabled.
1	Auto-offset is enabled (manual offset mode).

0x1B—Bits[4:3] Auto-Offset Update Frequency

These bits control how often the auto-offset circuit is updated (if enabled). Updating every 192 Hsyncs recommended. The power-up default setting is 11.

Table 40. Auto-Offset Update Frequency Bits

Value	Result
00	Update offset every 3-clamp periods.
01	Update offset every 48-clamp periods.
10	Update offset every 192-clamp periods.
11	Update offset every 3 Vsync periods.

0x1B—Bits[2:0]

Must be written to 011 for proper operation.

0x1C—Bits[7:0] Test Register 0

Must be set to 0xFF for proper operation.

SOG CONTROL

0x1D—Bits[7:3] SOG Slicer Comparator Threshold

These register bits adjust the comparator threshold of the SOG slicer in steps of 8 mV, with the minimum setting equaling 8 mV and the maximum setting equaling 256 mV. The power-up default setting is 15d and corresponds to a threshold value of 128 mV.

0x1D—Bit[2] SOGOUT Polarity

This bit sets the polarity of the SOGOUT signal. The power-up default setting is 0.

Table 41. SOGOUT Polarity Bit

Value	Result
0	SOGOUT polarity is negative.
1	SOGOUT polarity is positive.

0x1D—Bits[1:0] SOGOUT Select

These register bits control what is output on the SOGOUT pin. Options are the raw SOGINx from the slicer (that is, the unprocessed SOG signal produced from the sync slicer), the raw HSYNCx, the regenerated Hsync from the sync filter that can generate missing syncs due to coasting or drop-out, or finally, the filtered Hsync that excludes extraneous syncs that do not occur within the sync filter window. The power-up default setting is 0.

Table 42. SOGOUT Select Bits

Value	Result
00	Raw SOGINx.
01	Raw HSYNCx.
10	Regenerated Hsync from sync filter.
11	Filtered Hsync from sync filter.

INPUT AND POWER CONTROL

0x1E—Bit[7] Channel Select Override

This bit provides an override to the automatic input channel selection. Power-up default setting is 0.

Table 43. Channel Select Override Bit

Value	Result
0	Channel input source determined by chip.
1	Channel input source determined by user, (Register 0x1E, Bit 6).

0x1E—Bit[6] Channel Select

This bit selects the active input channel if Bit 7 of Register 0x1E is 1. This selects between Channel 0 data and syncs or Channel 1 data and syncs. Power-up default setting is 0.

Table 44. Channel Select Bit

Value	Result
0	Channel 0 data and syncs are selected.
1	Channel 1 data and syncs are selected.

0x1E—Bit[5] Programmable Bandwidth

This bit selects between a low or high input bandwidth; having a low input bandwidth is useful in limiting noise for lower frequency inputs. The power-up default setting is 1. Low analog input bandwidth is ~7 MHz; high analog input bandwidth is ~300 MHz.

Table 45. Programmable Bandwidth Bit

Value	Result
0	Low analog input bandwidth.
1	High analog input bandwidth.

0x1E—Bit[4] Power-Down Control Select

This bit determines whether power-down is controlled manually or automatically by the chip. If automatic control is selected (by setting this bit to 1), the AD9984A's decision is based on the status of the some of the sync detect bits (Register 0x24, Bit 2, Bit 3, Bit 6, and Bit 7). If either an Hsync or a sync-on-green input is detected on any input, the chip powers up or powers down. For manual control, the AD9984A allows the flexibility of control through both a dedicated pin and a register bit. The dedicated pin allows a hardware watchdog circuit to control power-down, whereas the register bit allows power-down to be controlled by software. With manual power-down control, the polarity of the power-down pin must be set (Register 0x1E, Bit 2) whether it is used or not. If unused, it is recommended to set the polarity to active high and hardwire the pin to ground with a 10 kΩ resistor.

Table 46. Power-Down Control Select Bit

Value	Result
0	Manual power-down control (user determines power-down).
1	Auto power-down control (chip determines power-down).

0x1E—Bit[3] Power-Down

This bit is used to manually place the chip in power-down mode. It is only used if manual power-down control is selected (Register 0x1E, Bit 4 = 0). Both the state of this register bit and the power-down pin (Pin 17) are used to control manual power-down. (See the Power Management section for more details on power-down.)

Table 47. Power-Down Bit

Value	Pin 17	Result
0	0	Normal operation.
1	X	Power-down.

0x1E—Bit[2] Power-Down Pin Polarity

This bit defines the polarity of the power-down pin (Pin 17). It is only used if manual power-down control is selected (Register 0x1E, Bit 4 = 0).

Table 48. Power-Down Pin Polarity Bit

Value	Result
0	PWRDN polarity is negative.
1	PWRDN polarity is positive.

0x1E—Bit[1] Power-Down Fast Switching Control

This bit controls a special fast switching mode. With this bit, the AD9984A can stay active during power-down and only puts the outputs in high impedance. This option is useful when the data outputs from two chips are connected on a PCB and the user wants to instantaneously switch between the two.

Table 49. Power-Down Fast Switching Control Bit

Value	Result
0	Normal power-down operation.
1	The chip stays powered up, and the outputs are put in high impedance mode.

0x1E—Bit[0] SOGOUT High Impedance Control

This bit controls whether or not the SOGOUT output pin is in high impedance when in power-down mode. In most cases, SOGOUT is not put in high impedance during normal operation because it is usually needed for sync detection by the graphics controller. The option to put SOGOUT in high impedance is included mainly to allow for factory testing modes.

Table 50. SOGOUT High Impedance Control Bit

Value	Result
0	The SOGOUT operates as normal during power-down.
1	The SOGOUT is in high impedance during power-down.

OUTPUT CONTROL

0x1F—Bits[7:5] Output Mode

These bits choose between three options for the output mode. In 4:4:4 mode, RGB is standard. In 4:2:2 mode, YCbCr is standard, which reduces the number of output pins from 30 to 20. In 4:4:4 DDR output mode, the data is in RGB mode, but changes on every clock edge. The power-up default setting is 100.

Table 51. Output Mode Bits

Value	Result
100	4:4:4 RGB mode.
101	4:2:2 YCbCr mode.
110	4:4:4 DDR mode.

0x1F—Bit[4] Primary Output Enable

This bit places the primary output in active or high impedance mode. The power-up default setting is 1.

Table 52. Primary Output Enable Bit

Value	Result
0	Primary output is in high impedance mode.
1	Primary output is enabled.

0x1F—Bit[3] Secondary Output Enable

This bit places the secondary output in active or high impedance mode.

The secondary output is designated when using either 4:2:2 or 4:4:4 DDR. In these modes, the data on the blue output channel is the secondary output while the output data on the red and green channels are the primary output. Secondary output is always a DDR YCbCr data mode. See the Output Formatter section and Table 12. The power-up default setting is 0.

Table 53. Secondary Output Enable Bit

Value	Result
0	Secondary output is in high impedance mode.
1	Secondary output is enabled.

0x1F—Bits[2:1] Output Drive Strength

These two bits select the drive strength for all the high speed digital outputs (except VSOUT, A0, and O/E FIELD). Higher drive strength results in faster rise/fall times and, in general, makes it easier to capture data. Lower drive strength results in slower rise/fall times and helps to reduce EMI and digitally generated power supply noise. The power-up default setting is 10.

Table 54. Output Drive Strength Bits

Value	Result
00	Low output drive strength.
01	Medium output drive strength.
1x	High output drive strength.

0x1F—Bit[0] Output Clock Invert

This bit allows inversion of the output clock. The power-up default setting is 0.

Table 55. Output Clock Invert Bit

Value	Result
0	Noninverted pixel clock.
1	Inverted pixel clock.

0x20—Bits[7:6] Output Clock Select

These bits selects the optional output clocks such as a fixed 40 MHz internal clock, a 2× clock, a 90° phase-shifted clock, or the normal pixel clock. The power-up default setting is 00.

Table 56. Output Clock Select Bits

Value	Result
00	Pixel clock.
01	90° phase-shifted pixel clock.
10	2× pixel clock.
11	0.5× pixel clock.

0x20—Bit[5] Output High Impedance

This bit puts all outputs (except SOGOUT) in a high impedance state. The power-up default setting is 0.

Table 57. Output High Impedance Bit

Value	Result
0	Normal outputs.
1	All outputs (except SOGOUT) in high impedance mode.

0x20—Bit[4] SOGOUT High Impedance

This bit allows the SOGOUT pin to be placed in high impedance mode. The power-up default setting is 0.

Table 58. SOGOUT High Impedance Bit

Value	Result
0	Normal drive.
1	SOGOUT pin is in high impedance mode.

0x20—Bit[3] Field Output Polarity

This bit sets the polarity of the field output bit. The power-up default setting is 1.

Table 59. Field Output Polarity Bit

Value	Result
0	Active low = even field, active high = odd field.
1	Active low = odd field, active high = even field.

SYNC PROCESSING

0x20—Bit[2] PLL Sync Filter Enable

This bit selects which signal the PLL uses. It can select between raw versions of HSYNCx/SOGINx and filtered versions of Hsync/SOG. The filtering of the Hsync and SOG can eliminate nearly all extraneous transitions that have traditionally caused PLL disruption. The power-up default setting is 0.

Table 60. PLL Sync Filter Enable Bit

Value	Result
0	PLL uses raw HSYNCx or SOGINx.
1	PLL uses filtered Hsync or SOG.

0x20—Bit[1] Sync Processing Input Select

This bit selects whether the sync processor uses a raw sync or a regenerated Hsync for the following functions: coast, Hsyncs per Vsync count, field detection, and Vsync duration counts. Using the regenerated Hsync is recommended.

Table 61. Sync Processing Input Select Bit

Value	Result
0	Sync processing uses raw HSYNCx or SOGINx.
1	Sync processing uses the internally regenerated Hsync.

0x20—Bit[0]

Must be set to 1 for proper operation.

0x21—Bits[7:0]

Must be set to default.

0x22—Bits[7:0]

Must be set to default.

0x23—Bits[7:0] Sync Filter Window Width

This 8-bit register sets the window of time for the regenerated Hsync leading edge (in 25 ns steps) and the time that sync pulses are allowed to pass through. Therefore, with the default value of 10, the window width is ±250 ns. The goal is to set the window width to reject extraneous pulses (see the Sync Processing section). As with the sync separator threshold, the 25 ns multiplier value is somewhat variable. The maximum variability over all operating conditions is ±20% (20 ns to 30 ns).

DETECTION STATUS

0x24—Bit[7] HSYNC0 Detection

This bit is used to indicate when activity is detected on the HSYNC0 input pin. If HSYNC0 is held high or low, activity is not detected. The sync processing block diagram (Figure 9) shows where this function is implemented.

Table 62. HSYNC0 Detection Bit

Value	Result
0	No activity detected.
1	Activity detected.

0x24—Bit[6] HSYNC1 Detection

This bit is used to indicate when activity is detected on the HSYNC1 input pin. If HSYNC1 is held high or low, activity is not detected. Figure 9 shows where this function is implemented.

Table 63. HSYNC1 Detection Results

Value	Result
0	No activity detected.
1	Activity detected.

0x24—Bit[5] VSYNC0 Detection

This bit is used to indicate when activity is detected on the VSYNC0 input pin. If VSYNC0 is held high or low, activity is not detected. Figure 9 shows where this function is implemented.

Table 64. VSYNC0 Detection Results

Value	Result
0	No activity detected.
1	Activity detected.

0x24—Bit[4] VSYNC1 Detection

This bit is used to indicate when activity is detected on the VSYNC1 input pin. If VSYNC1 is held high or low, activity is not detected. Figure 9 shows where this function is implemented.

Table 65. VSYNC1 Detection Bit

Value	Result
0	No activity detected.
1	Activity detected.

0x24—Bit[3] SOGIN0 Detection

This bit is used to indicate when activity is detected on the SOGIN0 pin. If SOGIN0 is held high or low, activity is not detected. Figure 9 shows where this function is implemented.

Table 66. SOGIN0 Detection Bit

Value	Result
0	No activity detected.
1	Activity detected.

0x24—Bit[2] SOGIN1 Detection

This bit is used to indicate when activity is detected on the SOGIN1 input pin. If SOGIN1 is held high or low, activity is not detected. Figure 9 shows where this function is implemented.

Table 67. SOGIN1 Detection Bit

Value	Result
0	No activity detected.
1	Activity detected.

0x24—Bit[1] COAST Detection

This bit detects activity on the EXTCK/COAST pin. It indicates that one of the two signals is active, but it does not indicate which one. A dc signal is not detected.

Table 68. COAST Detection Bit

Value	Result
0	No activity detected.
1	Activity detected.

0x24—Bit[0] CLAMP Detection

This bit is used to indicate when activity is detected on the external CLAMP pin. If external CLAMP is held high or low, activity is not detected.

Table 69. CLAMP Detection Bit

Value	Result
0	No activity detected.
1	Activity detected.

POLARITY STATUS

0x25—Bit[7] HSYNC0 Polarity

This bit indicates the polarity of HSYNC0 input.

Table 70. HSYNC0 Polarity Bit

Value	Result
0	HSYNC0 polarity is negative.
1	HSYNC0 polarity is positive.

0x25—Bit[6] HSYNC1 Polarity

This bit indicates the polarity of HSYNC1 input.

Table 71. HSYNC1 Polarity Bit

Value	Result
0	HSYNC1 polarity is negative.
1	HSYNC1 polarity is positive.

0x25—Bit[5] VSYNC0 Polarity

This bit indicates the polarity of VSYNC0 input.

Table 72. VSYNC0 Polarity Bit

Value	Result
0	VSYNC0 polarity is negative.
1	VSYNC0 polarity is positive.

0x25—Bit[4] VSYNC1 Polarity

This bit indicates the polarity of VSYNC1 input.

Table 73. VSYNC1 Polarity Bit

Value	Result
0	VSYNC1 polarity is negative.
1	VSYNC1 polarity is positive.

0x25—Bit[3] COAST Polarity

This bit indicates the polarity of the external COAST signal.

Table 74. COAST Polarity Bit

Value	Result
0	COAST polarity is negative.
1	COAST polarity is positive.

0x25—Bit[2] CLAMP Polarity

This bit indicates the polarity of the CLAMP signal.

Table 75. CLAMP Polarity Bit

Value	Result
0	CLAMP polarity is negative.
1	CLAMP polarity is positive.

0x25—Bit[1] Extraneous Pulse Detection

A second output from the Hsync filter, this status bit tells whether extraneous pulses are present on the incoming sync signal. Often, extraneous pulses are used for copy protection, so this status bit can be used for this purpose.

Table 76. Extraneous Pulse Detection Bit

Value	Result
0	No extraneous pulses detected during active Hsync.
1	Extraneous pulses detected during active Hsync.

0x25—Bit[0] Sync Filter Lock

When this bit is set to 1, the sync filter is locked. When set to 0, the sync filer is unlocked.

HSYNC COUNT

0x26—Bits[7:0] Hsyncs per Vsync MSBs

This register contains the 8 MSBs of the 12-bit counter that reports the number of Hsyncs per Vsync on the active input. It is useful for determining the mode and is an aid in setting the PLL divide ratio.

0x27—Bits[7:4] Hsyncs per Vsync LSBs

This register contains the four LSBs of the 12-bit counter that reports the number of Hsyncs per Vsync on the active input.

TEST REGISTERS

0x28—Bits[7:0] Test Register 1

Must be written to 0xBF for proper operation.

0x29—Bits[7:0] Test Register 2

Must be written to 0x02 for proper operation.

0x2A—Bits[7:0] Test Register 3

Read only bits for future use.

0x2B—Bits[7:0] Test Register 4

Read only bits for future use.

0x2C—Bits[7:5] Offset Hold

Must be written to default 0x00 for proper operation.

0x2C—Bit[4] Auto-Offset Hold

This bit controls whether the auto-offset function runs continuously or only once and holds the result. Continuous updates are recommended because they allow the AD9984A to compensate for drift over time, temperature, and so on. If one-time updates are preferred, they should be performed every time the part is powered up and when there is a mode change. To perform a one-time update, auto-offset must first be enabled (Register 0x1B, Bit 5). Next, this bit (auto-offset hold) must first be set to 0 to let the auto-offset function operate and settle to a final value. Auto-offset hold should then be set to 1 to hold the offset values that the auto circuitry calculates. The AD9984A auto-offset circuit's maximum settle time is 10 updates. For example, if the update frequency is set to once every 192 Hsyncs, the maximum settling time is 1920 Hsyncs (10 × 192 Hsyncs).

Table 77. Auto-Offset Hold Bit

Value	Result
0	Allows auto-offset to continuously update.
1	Disables auto-offset updates and holds the current auto-offset values.

0x2C—Bits[3:0]

Must be written to 0x0 for proper operation.

0x2D—Bits[7:0] Test Register 5

Read/write bits for future use. Must be written to 0xE8 for proper operation.

0x2E—Bits[7:0] Test Register 6

Read/write bits for future use. Must be written to 0xE0 for proper operation.

0x34—Bit[2] SOG Filter Enabler

When this bit is set to 1, the SOG does not pass pulses less than 250 ns in width. This reduces spurious signals that can improperly drive the PLL circuit. Default for this bit is 0 or off.

0x36—Bit[0] VCO Gear Select

This bit allows the VCO to select a lower gear to run lower pixel clocks while remaining in a more linear range.

Table 78. VCO Gear Select Bit

Value	Result
0	Normal VCO setting.
1	Enables lower VCO clock output.

0x3C—Bits[7:4] Test Bits

Must be set to 0x0 for proper operation.

0x3C—Bit[3] Auto Gain Matching Hold

This bit controls whether the auto gain matching function runs continuously or runs once and holds the result. Continuous updates are recommended because they allow the AD9984A to compensate for drift over time, temperature, and so on.

If one-time updates are preferred, they should be performed every time the part is powered up and when there is a mode change. To perform a one-time update, auto gain matching must first be enabled (Register 0x3C, Bits[2:0]). Next, this bit (auto gain matching hold) must first be set to 1 to let the auto gain matching function operate and settle to a final value.

The auto gain matching hold bit should then be set to 0 to hold the gain values that the auto circuitry calculates. The AD9984A auto gain matching circuit's maximum settle time is 10 updates. For example, if the update frequency is set to once every 64 Hsyncs, the maximum settling time would be 640 Hsyncs (10 × 64 Hsyncs).

Table 79. Auto Gain Matching Hold Bit

Value	Result
0[1]	Disables auto gain updates and holds the current auto gain values.
1	Allows auto gain to update continuously.

[1]The power-up default setting is 0.

0x3C—Bits[2:0] Auto Gain Matching Enable

These bits enable or disable the auto gain matching function.

Table 80. Auto Gain Matching Enable Bits

Value	Result
000	Auto gain matching disabled.
110	Auto gain matching enabled.

PCB LAYOUT RECOMMENDATIONS

The AD9984A is a high precision, high speed, analog device. To achieve the maximum performance from the part, it is important to have a well laid-out board. The section provides a guide for designing a board using the AD9984A.

ANALOG INTERFACE INPUTS

Use the following layout techniques on the graphics inputs:

- Minimize the trace length running into the graphics inputs. This is accomplished by placing the AD9984A as close as possible to the graphics VGA connector. Long input trace lengths are undesirable because they pick up noise from the board and other external sources.
- Place the 75 Ω termination resistors (see Figure 4) as close as possible to the AD9984A chip. Any additional trace length between the termination resistors and the input of the AD9984A increases the magnitude of reflections, which corrupts the graphics signal.
- Use 75 Ω matched impedance traces. Trace impedances other than 75 Ω also increase the chance of reflections.
- The AD9984A has a very high input bandwidth (300 MHz). While desirable for acquiring a high resolution PC graphics signal with fast edges, it also means that it captures any high frequency noise. Therefore, it is important to reduce the amount of noise that is coupled to the inputs. Avoid running any digital traces near the analog inputs.
- Due to the high bandwidth of the AD9984A, using a low-pass filter with the analog inputs can help to reduce noise. (for many applications, filtering is unnecessary.) Experiments have shown that placing a ferrite bead (specifically, the Fair-Rite 2508051217Z0) in series prior to the 75 Ω termination resistor is helpful in filtering excess noise. However, an application could work best with a different bead value. Alternatively, placing a 100 Ω to 120 Ω resistor between the 75 Ω termination resistor and the input coupling capacitor is beneficial.

Power Supply Bypassing

It is recommended to bypass each power supply pin with a 0.1 µF capacitor. An exception is when two or more supply pins are adjacent to each other. For these groupings of powers/grounds, it is only necessary to have one bypass capacitor. The fundamental idea is to have a bypass capacitor within ~0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the AD9984A, because doing so interposes resistive vias in the path.

The bypass capacitors should be physically located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the capacitor pads, down to the power plane, is generally the best approach.

It is particularly important to maintain low noise and good stability of the PV_D (the clock generator supply). Abrupt changes in PV_D can result in similar changes in sampling clock phase and frequency. This can be avoided by paying careful attention to regulation, filtering, and bypassing. It is desirable to provide separate regulated supplies for each of the analog circuitry groups (V_D and PV_D).

Some graphic controllers use substantially different levels of power when active (during active picture time), and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PV_D, from a different, cleaner, power source (for example, from a 12 V supply).

It is also recommended to use a single ground plane for the entire board. Experience has repeatedly shown that noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For these cases, place at least a single ground plane under the part. The location of the split should be at the receiver of the digital outputs. In this case, it is even more important to place components wisely because the current loops become much longer (current takes the path of least resistance). An example of a current loop is power plane to AD9984A to digital output trace, to digital data receiver, to digital ground plane, to analog ground plane.

PLL

Place the PLL loop filter components as close to the FILT pin as possible. Do not place any digital or other high frequency traces near these components. Use the values suggested in the data sheet with 10% tolerances or less.

OUTPUTS (BOTH DATA AND CLOCKS)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance and require more instantaneous current to drive, which creates more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor of 50 Ω to 200 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside of the AD9984A. If series resistors are used, place them as close to the AD9984A pins as possible (although try not to add vias or extra length to the output trace to get the resistors closer).

If possible, limit the capacitance driven by each digital output to less than 10 pF. This is easily accomplished by keeping traces short and connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside of the AD9984A and creates more digital noise on its power supplies.

DIGITAL INPUTS

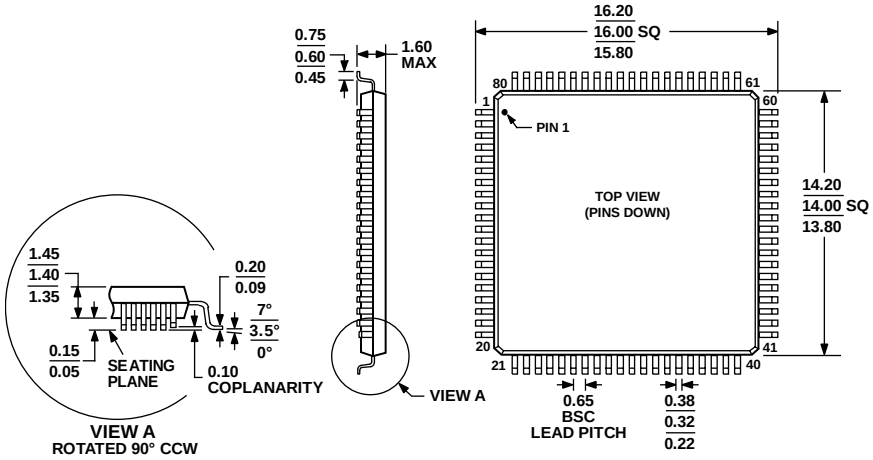
Digital inputs on the AD9984A (HSYNC0, HSYNC1, VSYNC0, VSYNC1, SOGIN0, SOGIN1, SDA, SCL, and CLAMP) are designed to work with 3.3 V signals, but are tolerant of 5 V signals. Therefore, no extra components need to be added if using 5 V logic.

Any noise that gets onto the Hsync input trace adds jitter to the system. Therefore, minimize the trace length and do not run any digital or other high frequency traces near it.

Reference Bypass

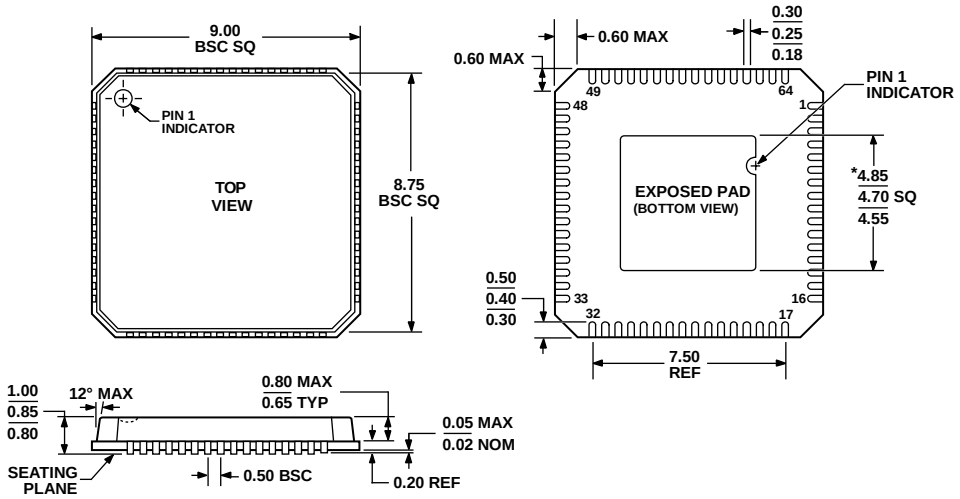
The AD9984A has two reference voltages that must be bypassed for proper operation of the ADC. REFLO and REFHI are connected to each other through a 10 µF capacitor. These references are used by the ADC circuitry to assure the greatest stability. Place them as close to the AD9984A pin as possible.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-026-BEC

Figure 20. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters



*COMPLIANT TO JEDEC STANDARDS MO-220-VMMD-4
EXCEPT FOR EXPOSED PAD DIMENSION

Figure 21. 64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
9 mm x 9 mm Body, Very Thin Quad
(CP-64-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD9984AKSTZ-140[1]	0°C to 70°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD9984AKSTZ-170[1]	0°C to 70°C	80-Lead Low Profile Quad Flat Package [LQFP]	ST-80-2
AD9984AKCPZ-140[1]	0°C to 70°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9984AKCPZ-170[1]	0°C to 70°C	64-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-64-1
AD9984A/PCBZ[1]		Evaluation Board [LQFP]	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

Purchase of licensed I²C components of Analog Devices or one of its sublicensed Associated Companies conveys a license for the purchaser under the Philips I²C Patent Rights to use these components in an I²C system, provided that the system conforms to the I²C Standard Specification as defined by Philips.

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