Datasheet

IrDA Controller LSI built-in Ir remote control

BU92747XXX Series

General Description

BU92747XXX series is IrDA controller LSI built-in Ir remote control.
Compatible with IrDA Physical layer version 1.0, 1.1, 1.2, 1.3, transmission control is possible between 2.4kbps to 4Mbps.
Built-in remote transmission formatter.
Infrared transmission formatter that compatible with each maker's formats is possible.

Features

- Data transfer speed (bps)
  - IrDA SIR: 2.4kbps, 9.6kbps, 19.2kbps, 38.4kbps, 57.6kbps and 115.2kbps
  - IrDA MIR: 0.576Mbps, 1.152Mbps
  - IrDA FIR: 4Mbps
  - IrSimple
- Detection, removal and insertion of preamble, start flag and stop flag in FIR mode
- Detection, removal and insertion of start flag and stop flag in MIR mode
- Detection and occurrence of CRC
- Interface
  - 16-bit data bus
  - Interrupt $\overline{\text{INTR}}$ (IrDA controller)
  - Address $A_{0\text{-}3}$
  - Control signals $\overline{\text{CS}}$, $\overline{\text{RD}}$ and $\overline{\text{WR}}$
- Built-in 2560 × 2byte FIFO buffer (for transmission and reception
- Accessible as a memory device connected to the bus
- Power down mode setting possible for transmission and reception
- Operation at V_{DD}=1.62 to 1.98V
- Input clock of 48MHz for external input clock or crystal input clock
- Ir remote control function
  - Serial 2-lines SDA, and SCL
  - Programmable carrier frequency
  - Programmable length of header
  - Programmable length of data Hi
  - Programmable length of data Lo
  - Programmable length of end part
  - Programmable arbitrary length of output data bit
  - Programmable frame
  - Continuous data transmission
  - Interrupt function $\overline{\text{NIRQ}}$

Applications

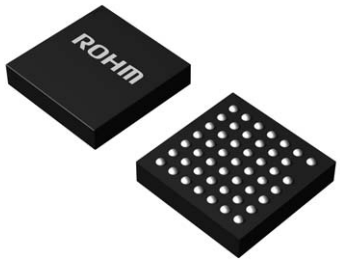
- IrDA transmission control.
- Remote transmission formatter

Key Specifications

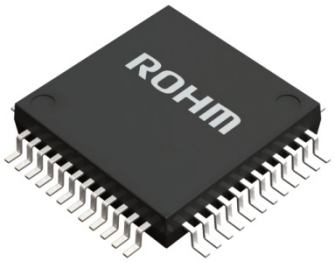
- Absolute maximum rating V_{DD} : -0.3 V to 4.5V
- Power supply voltage : 1.62V to 1.98V
- Input voltage H level : 1.62V ～ 3.6V
- Input clock frequency : 48MHz(within I100ppm)
- Clock input current consumption : 30mA(Max)
- Standby current : 10μA (Max)
- Operating temperature range : -40℃ to +85℃
- Allowable loss VBGA048W040 : 570mW (Max)
  VQFP48C : 900mW (Max)

Package

	W(Typ.) x D(Typ.) x H(Max.)
VBGA048W040	4.0mm x 4.0mm x 0.9mm



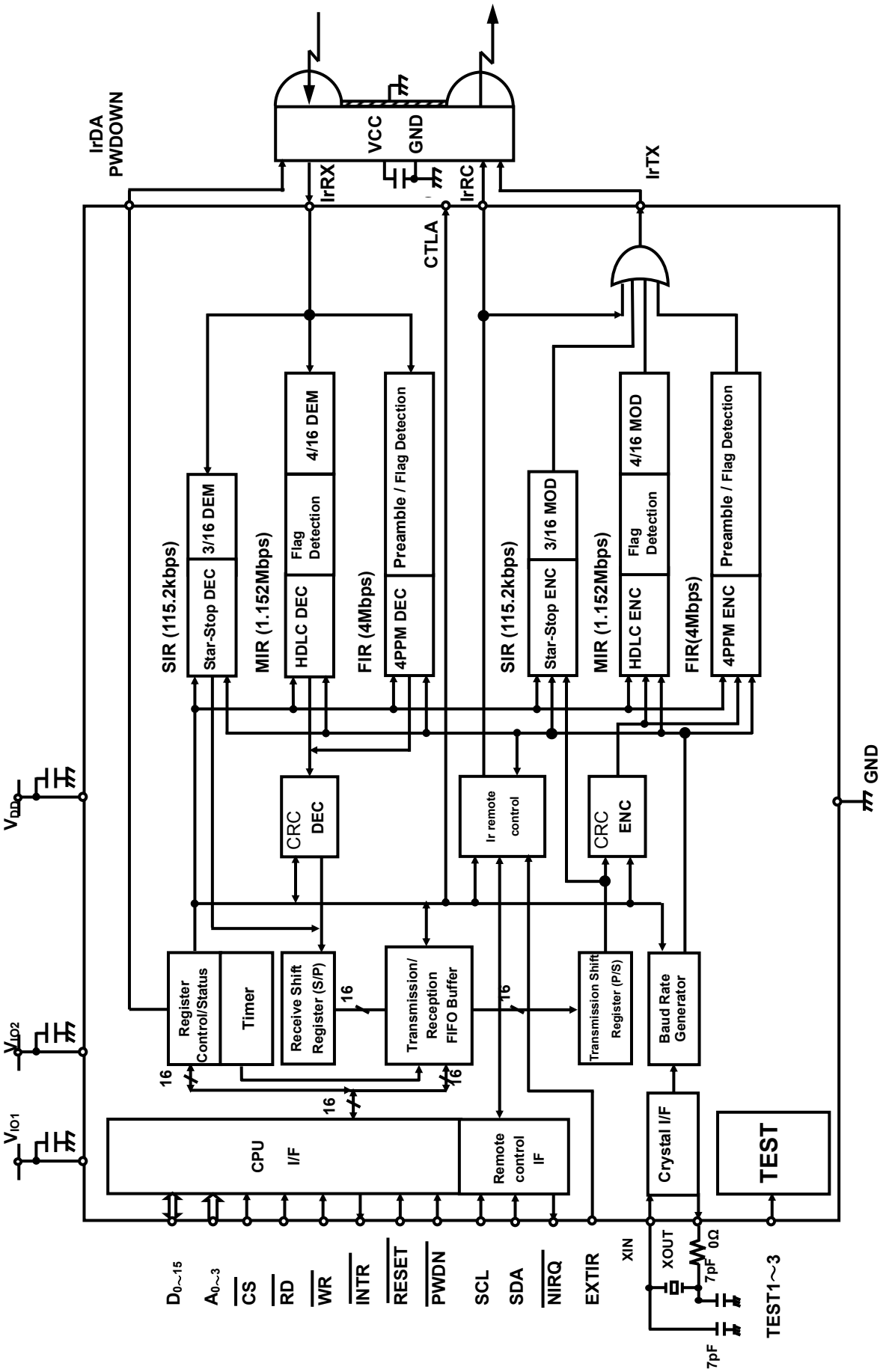
VQFP48C	9.00mm x 9.00mm x 1.60mm



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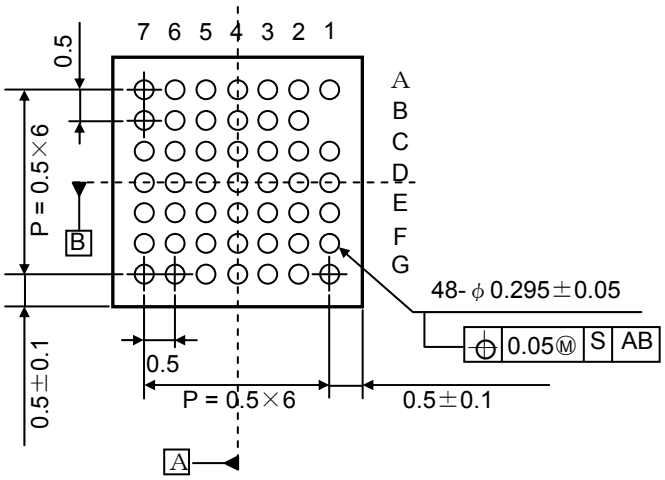
●Typical Application Circuit



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●**VBGA048W040 Pin Configuration**



(unit : mm)
number of balls : 48

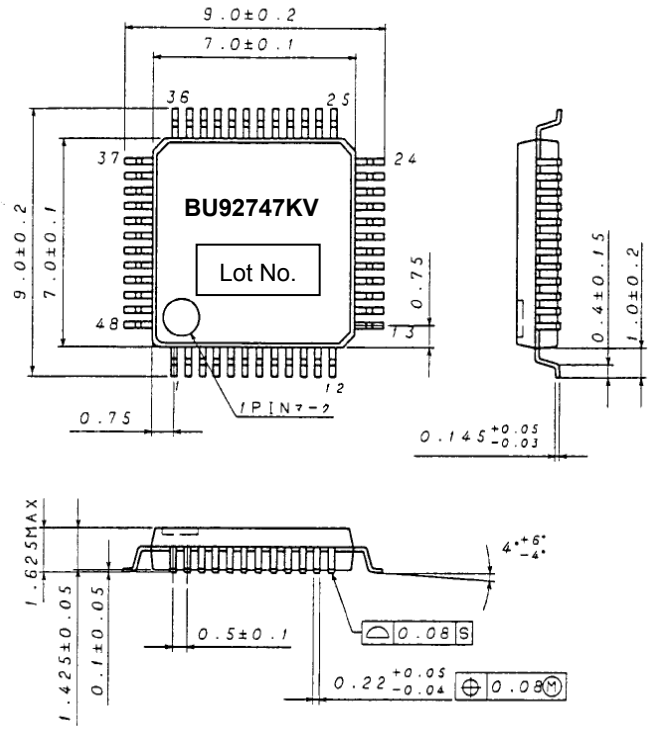
●**VBGA048W040 Land Matrix Table**

Land Matrix No.	Pin Name	Land Matrix No.	Pin Name	Land Matrix No.	Pin Name	Land Matrix No.	Pin Name
A1	$\overline{\text{PWDN}}$	C1	V_{IO2}	E1	A_2	G1	GND
A2	XOUT	C2	$\overline{\text{NIRQ}}$	E2	A_1	G2	D_5
A3	SCL	C3	$\overline{\text{RESET}}$	E3	A_0	G3	D_4
A4	IrRC	C4	(NC)	E4	D_{15}	G4	D_3
A5	IrTX	C5	EXTIR	E5	D_{14}	G5	D_2
A6	IrRX	C6	V_{IO1}	E6	D_{13}	G6	D_1
A7	GND	C7	$\overline{\text{RD}}$	E7	D_{12}	G7	D_0
(NC)	(NC)	D1	V_{IO1}	F1	D_{11}		
B2	XIN	D2	A_3	F2	V_{DD}		
B3	SDA	D3	TEST1	F3	D_{10}		
B4	CTLA	D4	TEST2	F4	D_9		
B5	IrDAPWDN	D5	TEST3	F5	D_8		
B6	V_{DD}	D6	$\overline{\text{INTR}}$	F6	D_7		
B7	$\overline{\text{WR}}$	D7	$\overline{\text{CS}}$	F7	D_6		

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●VQFP48C Pin Configuration



(unit : mm)

●VQFP48C Land Matrix Table

Land Matrix No.	Pin Name	Land Matrix No.	Pin Name	Land Matrix No.	Pin Name	Land Matrix No.	Pin Name
1	$\overline{PWDN}$	13	GND	25	D_0	37	GND
2	$\overline{RESET}$	14	D_5	26	D_6	38	IrRX
3	$\overline{NIRQ}$	15	A_0	27	D_{14}	39	EXTIR
4	V_{IO2}	16	D_4	28	D_{12}	40	IrTX
5	TEST2	17	D_{10}	29	D_{13}	41	IrDAPWDOWN
6	A_3	18	D_9	30	$\overline{INTR}$	42	CTLA
7	V_{IO1}	19	D_3	31	$\overline{CS}$	43	IrRC
8	TEST1	20	D_{15}	32	TEST3	44	(NC)
9	A_2	21	D_2	33	$\overline{RD}$	45	SCL
10	A_1	22	D_8	34	V_{IO1}	46	SDA
11	D_{11}	23	D_1	35	$\overline{WR}$	47	XOUT
12	V_{DD}	24	D_7	36	V_{DD}	48	XIN

●Pin Descriptions

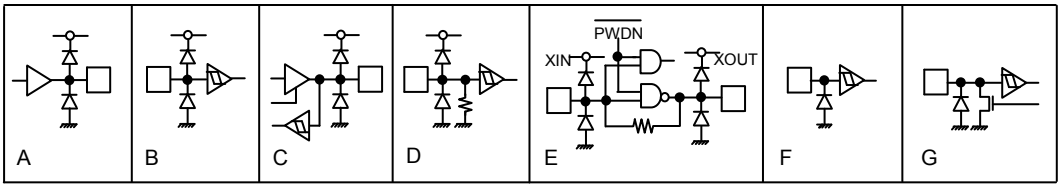
Pin name	I / O	Condition of after reset	Pin Function	Circuit Diagram
IrRX	I	-	IrDA Receive Input Pin	B
EXTIR	I	-	Signal Input Pin in SM2="H" (Input Signal is outputted to IrTX or IrRC)	B
IrTX	O	L	IrDA and remote control Transmission Output Pin Transmission IrDA when RC_EN= "L" Transmission remote control when RC_EN="H", RC_MODE="H"	A
D_{0-15}	I / O	Input	Data I/O Pin	C
A_{0-3}	I	-	Address Input Pin	B
$\overline{CS}$	I	-	Chip Select Pin. Low (L) Active The read/write signal goes “Active” in a Low period.	B
$\overline{RD}$	I	-	Read Signal Input Pin. Low (L) Active	B

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Pin name	I / O	Condition of after reset	Pin Function	Circuit Diagram
$\overline{WR}$	I	-	Write Signal Input Pun. Low (L) Active	B
$\overline{INTR}$	O	H	CPU Interrupt Request Output Pin. (IrDA Controller) The signal goes “Low” when an interrupt condition takes place. (note) Read EIR register at once and do appropriate processing when the interrupt request is occurred. When processing to the interrupt request is delayed, it is not likely to be able transmission/ reception it normally.	A
$\overline{RESET}$	I	-	Reset Input Pin. Low (L) Active The signal causes the internal register settings, etc. to be initialized.	B
$\overline{PWDN}$	I	-	Power Down Mode Setting. Low (L) Active When set to Low (L), this signal causes the wait status and sets the low dissipation current mode. After the power down mode is removed, $\overline{RESET}$=L must set to Low until crystal clock oscillation becomes stable (about 2 or 3 ms). After that $\overline{RESET}$ must set to High. Take it into consideration that this period depends on the crystal in use.	B
IrRC	O	L	Remote control transmission Output pin Transmission remote control when RC_EN= "H", RC_MODE= "L"	A
CTLA	O	L	Control Signal Output Pin	A
SCL	I	-	Serial clock	F
SDA	I/O	Input	Serial data I/O Pin	G
$\overline{NIRQ}$	O	H	CPU Interrupt Request Output Pin (Ir remote control) The signal goes “Low” when an interrupt condition takes place.	A
XIN/CLK48M	I	-	Crystal IN / External CLK Input	E
XOUT	O	-	Crystal OUT (N.C when external input clock is used)	E
TEST1-3	I	-	Test pins (These pins must be GND during normal operation.)	D
IrDA PWDOWN	O	H	IrDA module control signal output pin These pins must be OPEN for IrDA modules having no power-down pin.	A
V_{DD}	-	-	Power supply pin	-
V_{IO1}	-	-	Interface power supply voltage1	-
V_{IO2}	-	-	Interface power supply voltage2	-
GND	-	-	Ground pin	-

●Equivalent Circuit Diagram



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●Reset

Reset of IrDA controller and Ir remote control is common. In the case of crystal CLK oscillation, CLK isn't stable both just after the power supply is turned on and after the power down is reset. Therefore, RESET should be set to keep L for 2 or 3 msec until CLK becomes stable, and then RESET should be set to H after CLK stabilize.
(Make sure that the unstable period of CLK depends on Crystal and circuit constants etc.)

●Input clock

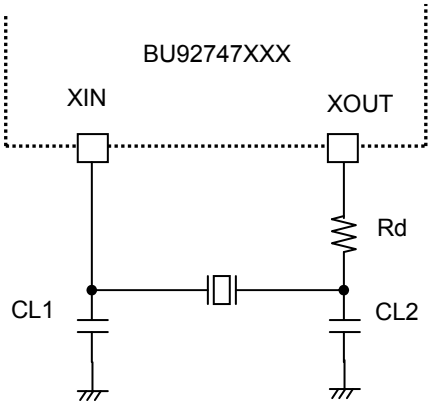
Input clock frequency is 48MHz.The tolerance is within ±100ppm.
The basis of the Duty ratio is 50% , and make it within ±30%.

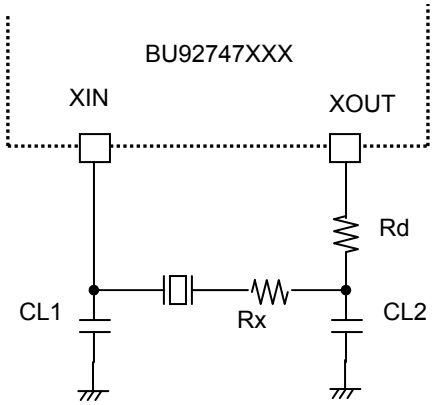
●About the IrSimple reception

Data is transmitted more one-sidedly than the sending side at the IrSimple-Uni-mode. The error interrupt such as OE_EI and DEX_EI is generated when processing and the received data reading speed to interrupt request (INTR:L) are slow etc. and it is not likely to be able to receive it normally. It is necessary to set the interrupt processing and the reading speed, etc. at which the entire system is considered on the HOST side.

●Example of crystal-oscillator circuit configuration

Please decide final circuitry and the constant after consulting the crystal-oscillator manufacturer.



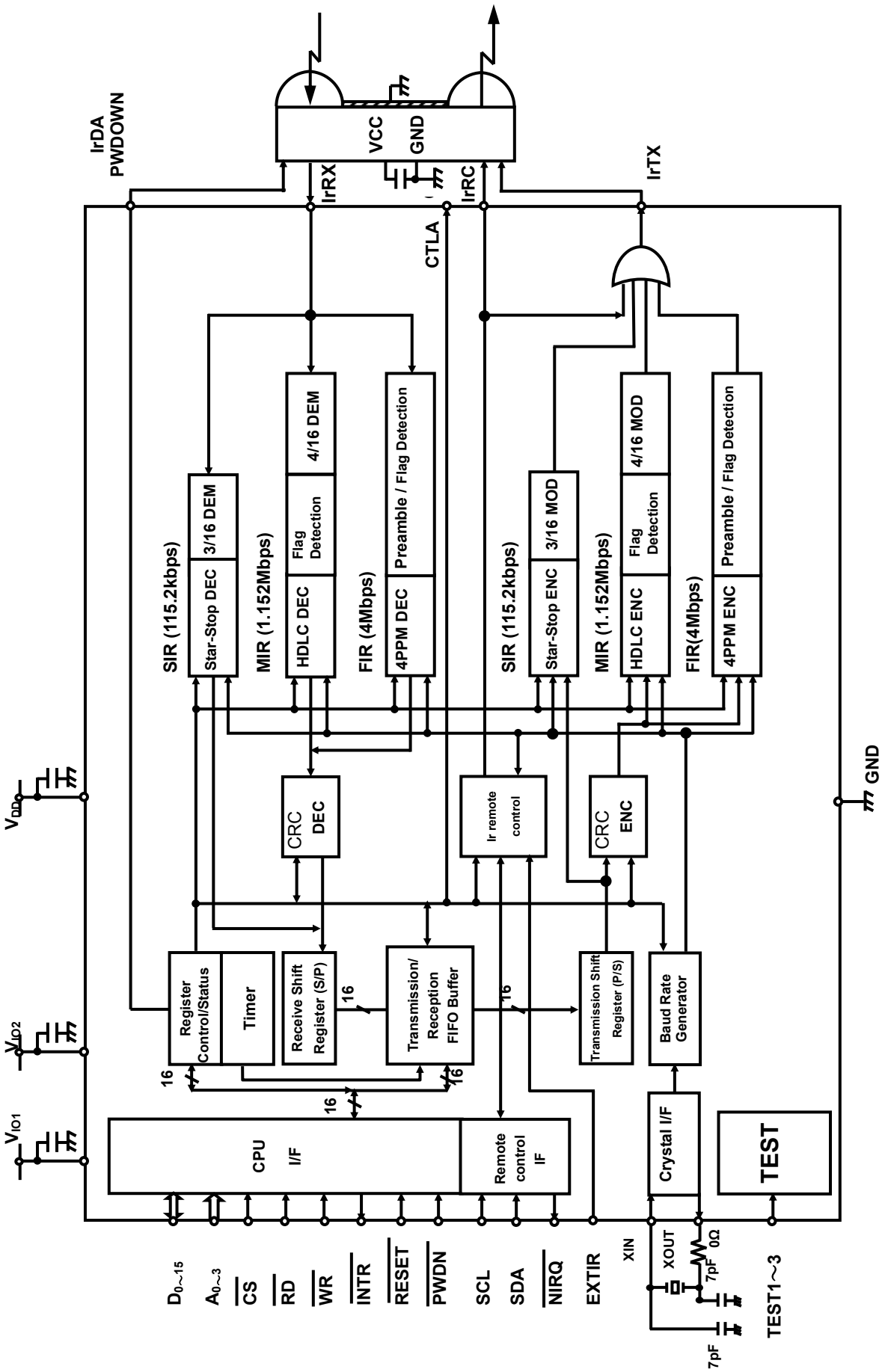


Example of suppressing excitation power

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●Block Diagram/ Application Circuit



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●Absolute Maximum Ratings

Ta=25°C unless otherwise stated

Parameter	Symbol	Limits	Unit
Supply voltage(Note1)	V_{DD}	-0.3 to +2.5	V
Interface supply voltage1(Note1)	V_{IO1}	-0.3 to +4.5	V
Interface supply voltage2(Note1)	V_{IO2}	-0.3 to +4.5	V
Input voltage(Note1)	V_{IN}	-0.3 to $V_{IO1, 2}$+0.3	V
Power dissipation(Note2) VBGA048W040	Pd	0.57	W
Power dissipation(Note3) VQFP48C	Pd	0.90	W
Operating temperature range	T_{OPR}	-40 to +85	℃
Storage temperature range	T_{STG}	-55 to +125	℃

(Note1)It applies to all pins based on the GND pin.
(Note2)Measured value with conformity substrate to SEMI (114.3mm×76.2mm×1.6mm, 4layer)
5.7mW/℃decrease over Ta=25℃use
(Noete3)Measured value with ROHM Standard Board (170.0mm×70.0mm×1.6mm, 1layer)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

●Recommended Operating Ratings

Parameter	Symbol	Limits			Unit
		Min.	Typ.	Max.	
Supply voltage	V_{DD}	1.62	1.8	1.98	V
Interface supply voltage1	V_{IO1}	1.62	1.8	3.6	V
Interface supply voltage2(Note1)	V_{IO2}	1.62	1.8	3.6	V

(Note1)V_{IO2} is connected with XIN/CLK48M, Xout, $\overline{PWDN}$, $\overline{NIRQ}$ and $\overline{RESET}$.

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●**Electrical Characteristics (DC Characteristics)**

Ta=25°C, V_{DD}=1.8V, V_{IO1}=1.8V, V_{IO2}=1.8V and GND=0V unless otherwise stated.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Dissipation current 1	$I_{DD}1$	—	0.1	10	μA	For input with no output load = 0V
Dissipation current 2	$I_{DD}2$	—	10	30	mA	For XIN = 48MHz
Digital high-level input voltage	V_{IH}	0.75×V_{IO}	—	—	V	
Digital low-level input voltage	V_{IL}	—	—	0.25×V_{IO}	V	
Digital high-level input current	I_{IH}	—	—	10	μA	Input voltage level 1.8V
		—	—	100	μA	Input voltage level 1.8V TEST1-3
Digital low-level input current	I_{IL}	—	—	10	μA	Input voltage level GND
Digital high-level output voltage	V_{OH}	V_{IO}−0.6	—	—	V	$\overline{INTR}$, $D_{0\sim15}$, IrDA$\overline{PWDOWN}$ IrTX, IrRC, $\overline{NIRQ}$, CTLA IOH=-1mA
Digital low-level output voltage	V_{OL}	—	—	0.6	V	$\overline{INTR}$, $D_{0\sim15}$, IrDA$\overline{PWDOWN}$ IrTX, IrRC, SDA, $\overline{NIRQ}$, CTLA IOL=1mA

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●**IrDA controller (parallel I/F) AC Characteristics**

Ta=25°C, V_{DD}=1.8V, V_{IO1}=1.8V, V_{IO2}=1.8V and GND=0V unless otherwise stated.

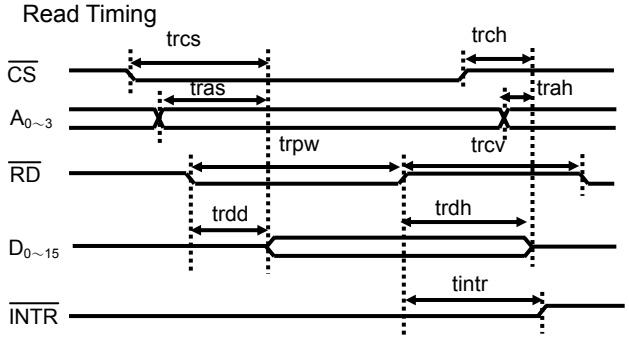
Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
Read pulse width	trpw	90	–	–	ns	
Read data delay time	trdd	–	–	60	ns	
Read address setup time	tras	–	–	70	ns	
Write address setup time	twas	70	–	–	ns	
Read address hold time	trah	0	–	–	ns	
Read data hold time	trdh	0	–	20	ns	
Read/write recovery time	trcv	60	–	–	ns	
Read chip select setup time	trcs	–	–	70	ns	
Write chip select setup time	twcs	70	–	–	ns	
Read chip select hold time	trch	0	–	–	ns	
Write chip select hold time	twch	6	–	–	ns	
Write address hold time	twah	10	–	–	ns	
Write pulse width	twpw	60	–	–	ns	
Write data setup time	twds	60	–	–	ns	
Write data hold time	twdh	10	–	–	ns	
Interrupt clear time	tintr	–	–	110	ns	
SIR pulse width	tspw	–	19.5	–	µs	For settings of 3/16 pulse width and baud rate of 9.6kbps
		–	1.6	–	µs	For setting of 1.6µs pulse width
MIR pulse width	tmpw	–	208.3	–	ns	For 1.152Mbps
FIR single pulse width	tfpw	–	125	–	ns	
FIR double pulse width	tfdpw	–	250	–	ns	
Reset pulse width	trstw	70	–	–	ns	

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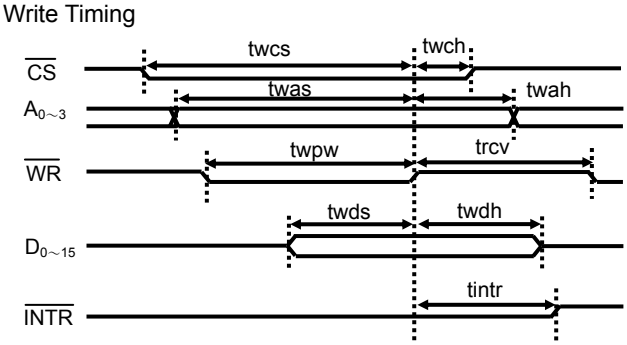
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●Timing Diagram

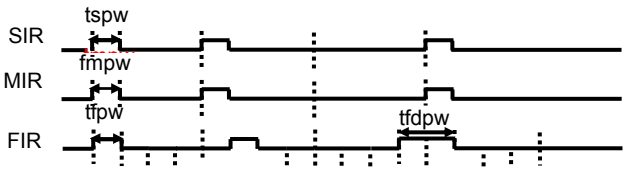
Read Timing



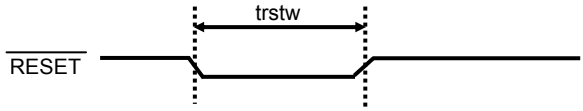
Write Timing



Infrared Ray (IR) Interface Timing



Reset Timing

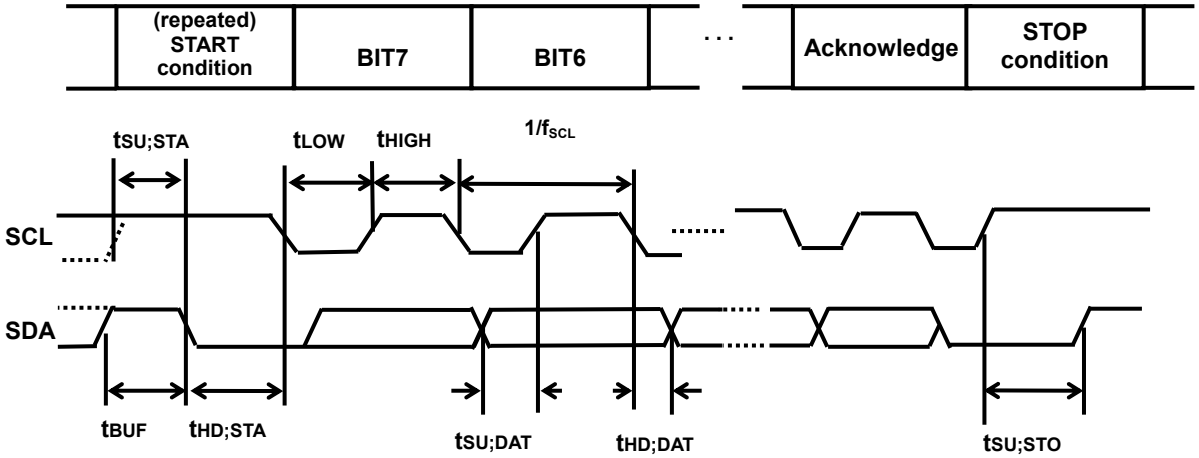


●Ir remote control (serial I/F) AC Characteristics

Ta=25°C, V_{DD}=1.8V, V_{IO1}=1.8V, V_{IO2}=1.8V and GND=0V unless otherwise stated.

Parameter	Symbol	Limits			Unit	Conditions
		Min.	Typ.	Max.		
SCL clock frequency	fSCL	-	-	400	kHz	
Bus free time	tBUF	1.3	-	-	µs	
Set-up time for (repeated) START condition	tSU;STA	0.6	-	--	µs	
Hold time (repeated) START condition	tHD;STA	0.6	-	-	µs	
SCL LOW time	tLOW	1.3	-	-	µs	
SCL HIGH time	tHIGH	0.6	-	-	µs	
Data setup time	tSU;DAT	100	-	-	ns	
Data hold time	tHD;DAT	0	-	-	ns	
Setup time for STOP condition	tSU;STO	0.6	−	−	µs	

●Timing Diagram



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●IrDA Controller Functional Description

・Mode description Three IrDA communication modes (SIR, MIR and FIR) can be set.
For details of each mode, check the following table.

Mode	Baud rate	BOF	Information portion	CRC	EOF	Insertion and deletion of preamble
SIR	2.4k to 115.2kbps	SW	SW	SW	SW	―
MIR	0.576M, 1.152Mbps	HW	SW	HW	HW	―
FIR	4Mbps	HW	SW	HW	HW	HW

※ SW : Software (set by IrLAP)
※ HW : Hardware (set by BU92747XXX)

・Transmission/reception method The following settings for transmission/reception can be made by setting RX_EN, TX_EN, TX_CON, and RX_CON in the control register to 0 and 1.

TX_CON	RX_CON	AUTO_FLV_CP	TX_EN	RX_EN	Mode
0	0	0	0	0	Idle mode(Note1)
0	0	0	0	1	Reception mode
0	0	0	1	0	Transmission mode
0	0	1	0	1	Automation many windows receive mode
0	1	0	0	1	Many windows receive mode
1	0	0	0	0	Many windows transmit mode

(Note1)Default
※ Other setting is inhibited.

●Time-out

Interrupt requests are issued when a time-out occurs in the FIFO buffer under the following conditions:

1 Condition causing an MIR and FIR receive time-out
When one or more bytes of data is present in the FIFO buffer, the CPU does not read the FIFO buffer data even though 64μs has elapsed after the last writing of data into the FIFO buffer from the receive shift register.

2 Condition causing an SIR receives time-out
When one or more bytes of data is present in the receive FIFO buffer, the CPU does not read the FIFO buffer data even though the Tout time has elapsed after the last writing of data into the FIFO buffer from the receive shift register.
Tout = 4 × (1 / Baud rate) × 10

3 Condition causing an MIR and FIR transmission time-out
The CPU does not access the FIFO buffer for 1ms or more in the transmission mode.
(Except for the condition of FTLV≦FLV)

4 Condition causing a many windows transmission mode time-out
The CPU does not write data for 1ms in many windows transmit mode, after setting FTLV or writing a former DATA.
(Except for the condition of FTLV≦(FLV - FLVⅡ))

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●**IrDA Controller Register Set**

Register name	Description
TXD	Transmit Data Register
RXD	Receive Data Register
IER	Interrupt setting register
EIR	Interrupt source display register
MCR	Communication mode setting register
PWR/FIT	Transmission pulse width setting register / Transmission frame interval setting register
TRCR	Transmission reception setting register
FTLV	FIFO transmission data count setting register
FLV	FIFO data count register
FLVⅡ	FIFO data count register in many windows receive mode / Transmission frame data count register
FLVⅢ	FIFO data count register in many windows receive mode
FLVⅣ	FIFO data count register in many windows receive mode
TRCRⅡ	TXE_C / WRE_C clear register
TXE_C	TXE count register in many windows transmit mode
WRE_C	WRE count register in many windows transmit mode

Address Bus				add	Register Name	R/W		Function of each bits													
								Bit No.													
A3	A2	A1	A0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	00	TXD/ RXD	R/W	ALL	TXD15 /RXD15	TXD14 /RXD14	TXD13 /RXD13	TXD12 /RXD12	TXD11 /RXD11	TXD10 /RXD10	TXD9 /RXD9	TXD8 /RXD8	TXD7 /RXD7	TXD6 /RXD6	TXD5 /RXD5	TXD4 /RXD4	TXD3 /RXD3	TXD2 /RXD2	TXD1 /RXD1	TXD0 /RXD0
0	0	0	1	01	IER	R/W	SIR	–	–	–	–	–	–	–	–	FE_IE	EOF _IE	OE_IE	–	TXE _IE	TO_IE	EOFRX _IE	DRX _IE
							MIR				RDE _IE	WRE _IE	RDUE _IE	DEX _IE	RDOE _IE	AC_IE			CRC _IE			STFRX _IE	–
							FIR									DECE _IE							
0	0	1	0	02	EIR	R	SIR	–	–	–	–	–	–	–	–	FE_EI	EOF _EI	OE_EI	–	TXE _EI	TO_EI	EOFRX _EI	DRX _EI
							MIR				RDE _EI	WRE _EI	RDUE _EI	DEX _EI	RDOE _EI	AC_EI			CRC _EI			STFRX _EI	–
							FIR									DECE _EI							
0	0	1	1	03	MCR	R/W	ALL	–	–	–	CTLA	RC_ MODE	RC _EN	–	–	DRS2	DRS1	DRS0	–	–	SM2	SM1	SM0

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Address Bus				add	Register Name	R/W		Function of each bits													
								Bit No.													
A3	A2	A1	A0					15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	0	0	04	PWR/ FIT	R/W	SIR	DIS2	DIS1	DIS0	–	–	–	–	–	FPW2	FPW1	FPW0	MPW3	MPW2	MPW1	MPW0	SPW
							MIR					FIT3	FIT2	FIT1	FIT0								
							FIR																
0	1	0	1	05	TRCR	R/W	SIR	–	–	–	–	–	1byte Read	TXPWD	RXPWD	–	IrPD	MS_EN	FCLR	–	–	RX_EN	TX_EN
							MIR	TX_NUM	TX_CON	FLV_CP	RX_CON	AUTO_FLV_CP	—			M_STA				IR_PLS	S_EOT		
							FIR									—							
0	1	1	0	06	FTLV	R/W	ALL	–	–	–	FTLV12	FTLV11	FTLV10	FTLV9	FTLV8	FTLV7	FTLV6	FTLV5	FTLV4	FTLV3	FTLV2	FTLV1	FTLV0
0	1	1	1	07	FLV	R	ALL	–	–	–	FLV12	FLV11	FLV10	FLV9	FLV8	FLV7	FLV6	FLV5	FLV4	FLV3	FLV2	FLV1	FLV0
1	0	0	0	08	FLVⅡ	R	MIR/ FIR	–	–	–	FLVⅡ12	FLVⅡ11	FLVⅡ10	FLVⅡ9	FLVⅡ8	FLVⅡ7	FLVⅡ6	FLVⅡ5	FLVⅡ4	FLVⅡ3	FLVⅡ2	FLVⅡ1	FLVⅡ0
1	0	0	1	09	FLVⅢ	R	MIR/ FIR	–	–	–	FLVⅢ12	FLVⅢ11	FLVⅢ10	FLVⅢ9	FLVⅢ8	FLVⅢ7	FLVⅢ6	FLVⅢ5	FLVⅢ4	FLVⅢ3	FLVⅢ2	FLVⅢ1	FLVⅢ0
1	0	1	0	0A	FLVⅣ	R	MIR/ FIR	–	–	–	FLVⅣ12	FLVⅣ11	FLVⅣ10	FLVⅣ9	FLVⅣ8	FLVⅣ7	FLVⅣ6	FLVⅣ5	FLVⅣ4	FLVⅣ3	FLVⅣ2	FLVⅣ1	FLVⅣ0
1	0	1	1	0B	TRCRⅡ	W	MIR/ FIR	–	–	–	–	–	–	–	–	–	–	–	–	–	–	WRE_C_CLR	TXE_C_CLR
1	1	0	0	0C	TXE_C	R	MIR/ FIR	–	–	–	–	–	–	–	TXE_C8	TXE_C7	TXE_C6	TXE_C5	TXE_C4	TXE_C3	TXE_C2	TXE_C1	TXE_C0
1	1	0	1	0D	WRE_C	R	MIR/ FIR	–	–	–	–	–	–	–	WRE_C8	WRE_C7	WR_C6	WRE_C5	WRE_C4	WR_C3	WRE_C2	WRE_C1	WRE_C0

※ —: Unused bit. When read, the value is 0.

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●TXD / RXD: Transmit/Receive Data Register

TXD/RXD shares the same address.
TXD is accessed when transmission data is written and is used as a transmission data hold register.
When the FIFO buffer is effective, it works as the first storage register of TX_FIFO.
RXD is accessed when received data is read out and is used as a receive data storage register.
When the FIFO buffer is effective, it also works as the last storage register of RX_FIFO. Neither reading from TXD nor writing to RXD can be performed.

●IER: Interrupt Enable Register

IER is used to control (enable) various kinds of interrupts.
All 13 bits correspond to interrupts so that they can be controlled independently.
Once system reset takes place, all the bits are set to "0". Each interrupt can be enabled by writing “1” to the corresponding bit.

IER0: DRX_IE (Data Receiver Interrupt Enable)

When one-byte received data has been transmitted in SIR mode from the receive shift register to the FIFO buffer, this bit sets an interrupt as a data read request.

IER1:

This bit works as EOFRX_IE in SIR mode or as STFRX_IE in MIR, FIR mode.

EOFRX_IE: (End of Frame Receiver Interrupt Enable)
Sets an interrupt as a data read request when EOF (C1) data has been written to FIFO.

STFRX_IE: (Stop Flag Receiver Interrupt Enable)
Sets a data read request when a Stop Flag has been detected during data reception.

IER2: TO_IE (Timeout Interrupt Enable)

This bit sets an interrupt for time-out.

IER3: TXE_IE (Transmitter Empty Interrupt Enable)

This bit sets an interrupt that takes place after both transmission FIFO buffer and transmission shift register are emptied and frame transmission is completed during data transmission.

IER4: CRC_IE (CRC Error Interrupt Enable)

This bit is effective in MIR and FIR mode. It sets an interrupt that takes place at CRC error occurrence.
In SIR mode, this bit is ignored but must be set to “0".

IER5: OE_IE (Overrun Error Interrupt Enable)

This bit sets an error at overrun (Overrun error occurs when the receive FIFO buffer becomes full and the next data is completely received in the receive register).

IER6: EOF_IE (End of Frame Interrupt Enable)

This bit sets an interrupt that takes place when FIFO is emptied in reading the last byte (EOF <h’C1> in SIR mode or last byte in frame information in MIR and FIR mode) of data written to FIFO in receive mode.

IER7:

This bit works FE_IE in SIR mode, AC_IE in MIR mode and DECE_IE in FIR mode.

FE_IE: (Framing Error Interrupt Enable)
Sets an interrupt that occurs when the stop bit of received data is not detected.

AC_IE: (Abort Condition Interrupt Enable)
Sets an interrupt that occurs when the received data of abort condition.

DECE_IE: (Decode Error Interrupt Enable)
Sets an interrupt that occurs for a decode error during data reception.

IER8: RDOE_IE (Read Overrun Error Interrupt Enable)

This bit is effective in many windows receive mode (MIR and FIR) and Auto_FLV_CP mode.
This bit sets as a register that tells too much reading of ex-frame data, when read the FIFO data.

IER9: DEX_IE (Data Exist Interrupt Enable)

This bit is effective in many windows receive mode (MIR and FIR) and A AUTO_FLV_CP mode. Do not set "1" in the other modes. When the setting is not done to FLV_CP=1 until the data of the next frame is received after Stop Flag of a front frame is received, interrupt is set.
reading receive data after generating the RDE_EI interruption (FLVⅡ value becomes 0) at the AUTO_ FLV_CP mode.

IER10: RDUE_IE (Read Underrun Error Interrupt Enable)

This bit is effective in many windows receive mode (MIR and FIR). Do not set "1" in the other modes.
This bit sets as a register that notifies the reading leaving of the front frame data FLVⅡ ≠0 to be when the value of FLV is copied to FLVⅡ with FLV_CP=1 (TRCR13).

IER11: WRE_IE (Write Enable Interrupt Enable)

This bit is effective in many windows transmit mode. Do not set "1" in the other modes.
This bit sets as a register that tells the CPU to be able to write next frame data in many windows transmit mode.

IER12 : RDE_IE(Read Enable Interrupt Enable)

This bit is effective in the AUTO_FLV_CP mode. Do not set "1" in the other modes.
This bit sets as a register that notifies to read it the reception frame data at the AUTO_FLV_CP mode.

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●EIR: Event Identification Register

EIR indicates an interrupt source at interrupt occurrence. All 13 bits corresponds to interrupts (interrupt array) set in IER. When an interrupt is invalid, the corresponding bits of EIR (status register) are set to “1” at event occurrence.
At system reset, all bits are reset to “0". In addition, this register is cleared to“0” when the CPU reads data in the register.

EIR0: DRX_EI (Data Receiver Event Identification)

This bit is set to “1” when one-byte received data is transmitted from the receive shift register to the FIFO buffer in SIR mode.

EIR1:

This bit works as EOFRX_EI in SIR mode and STFRX_EI in MIR and FIR mode.

EOFRX_EI: (End of Frame Receiver Event Identification)
Sets an interrupt as a data read request when EOF (C1) data has been written to FIFO.

STFRX_EI: (Stop Flag Receiver Event Identification)
Sets an interrupt as a data read request when a Stop Flag has been detected during reception.

EIR2: TO_EI (Timeout Event Identification)

This bit is set to“1” for time-out.

EIR3: TXE_EI (Transmitter Empty Event Identification)

This bit is set to “1” when both transmissions FIFO buffer and transmission shift register are emptied and frame transmission is completed during data transmission. （This bit is set to “1” only when FIFO buffer becomes empty by transmitting data.
If this bit is cleared by FCLR, it remains “0”.）

EIR4: CRC_EI (CRC Error Event Identification)

This bit is set to “1” at CRC error occurrence.

EIR5: OE_EI (Overrun Error Event Identification)

This bit is set to “1” at overrun error occurrence.

EIR6: EOF_EI (End of frame Event Identification)

This bit is set to “1” when FIFO is emptied in reading the last byte (EOF <h’C1> in SIR mode or last byte in frame information in MIR and FIR mode) of data written to FIFO in receive mode.
In many windows receive mode, interrupt occurs in every reading the last byte.

EIR7:

This bit is set to “1” as FE_EI in SIR mode, AC_IE in MIR mode or as DECE_EI in FIR mode.

FE_EI: (Framing Error Event Identification)
This bit is set to“1” when the stop bit of received data is not detected.

AC_EI: (Abort Condition Event Identification)
This bit is set to“1” when the received data of abort condition.

DECE_EI: (Decode Error Event Identification)
This bit is set to “1” when a decode error occurs during data reception.

EIR8: RDOE_EI (Read Overrun Error Event Identification)

This bit is effective in many windows receive mode (MIR and FIR) and AUTO_FLV_CP mode.
This bit is set to “1” in condition of FLVⅡ<0 as a register which tells too much reading of ex-frame data, when read the FIFO data.
In the case, all data in FIFO is automatically reset by BU92747XXX, and it becomes FLV=FLVⅡ=0.

EIR9: DEX_EI (Data Exist Event Identification)

This bit is effective in many windows receive mode (MIR and FIR) and AUTO_FLV_CP mode.
When the setting is not done to FLV_CP=1 until the data of the next frame is received after Stop Flag of a front frame is received, interrupt is set. In that case, all data that exists in FIFO in the hard independence is reset, and it becomes FLV=FLVⅡ= FLVⅢ=FLVⅣ =0.
This bit is set to "1" as a frame error when the Start Flag reception of the frame will start one after another by the time CPU finishes reading receive data after generating the RDE_EI interruption at the AUTO_ FLV_CP mode

EIR10: RDUE_EI (Read Underrun Error Event Identification)

This bit is effective in many windows receive mode (MIR and FIR).
This bit is set to "1" as a register that notifies the reading leaving of the front frame data FLVⅡ ≠ 0 to be when the value of FLV is copied to FLVⅡ with FLV_CP=1 (TRCR13).

EIR11: WRE_EI (Write Enable Event Identification)

This bit is effective in many windows transmit mode.
This bit is set to "1" as a register which tells the CPU to be able to write next frame data in many windows transmit mode.

EIR12 : RDE_EI(Read Enable Event Identification)

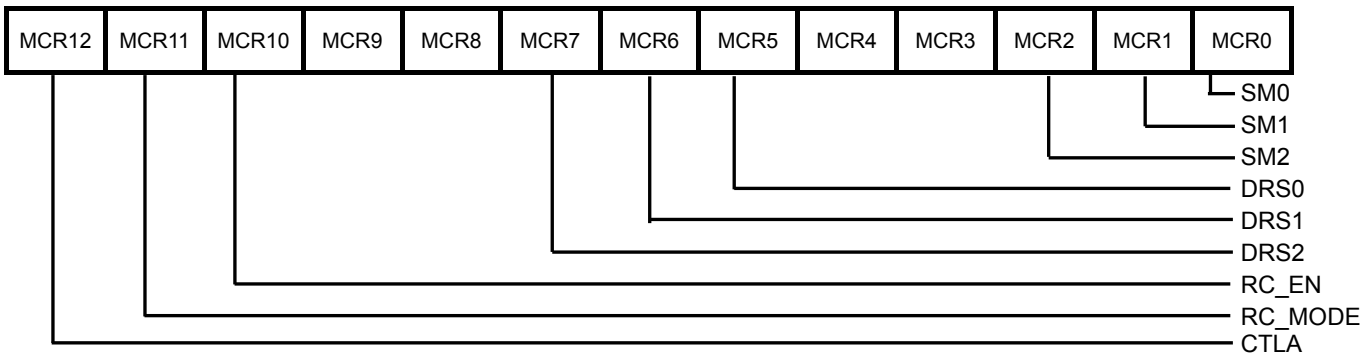
This bit is effective in the AUTO_FLV_CP mode. Do not set "1" in the other modes.
This bit is set to "1" as a register that notifies to read it the reception frame data at the AUTO_FLV_CP mode.

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●MCR: Mode Control Register

MCR sets various communication modes.



MCR0, 1: SM0, 1(Select Mode0, 1)

Combinations of SM1 and SM0 set the communication modes listed below.

SM1	SM0	mode
0	0	SIR (Note1)
0	1	MIR
1	0	FIR
1	1	FIR

(Note1) Default

MCR2: SM2

When this bit is set to "1", the signal inputted into EXTIR Pin is outputted from IrTX or IrRC.

MCR5～7 : DRS(Data Rate Select)

Combinations of DRS2 to DRS0 set the baud rates listed below for each communication mode.

DRS2～0	SIR	MIR	FIR
000	2.4kbps	Disable (1.152Mbps)	Disable (4Mbps)
001	Disable (4.8kbps)	0.576Mbps	Disable (4Mbps)
010	9.6kbps(Note1)	1.152Mbps	4Mbps
011	19.2kbps	Disable (1.152Mbps)	Disable (4Mbps)
100	38.4kbps	Disable (1.152Mbps)	Disable (4Mbps)
101	57.6kbps	Disable (1.152Mbps)	Disable (4Mbps)
110	115.2kbps	Disable (1.152Mbps)	Disable (4Mbps)
111	Disable (9.6kbps)	Disable (1.152Mbps)	Disable (4Mbps)

(Note1) Default

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MCR10: RC_EN (REMCON_Enable)

This bit set the mode listed below (SM2 = 0)

RC_EN	mode
0	IrDA controller(Note1)
1	Ir remote control

(Note1) Default

MCR11: RC_MODE (REMCON_MODE)

Output Pin is selected by this bit when SM2 is set to "1".
RC_MODE becomes invalid in RC_EN=0, and the IrDA signal is output from the IrTX pin.

RC_MODE	Remote control signal output pin
0	IrRC
1	IrTX(Note1)

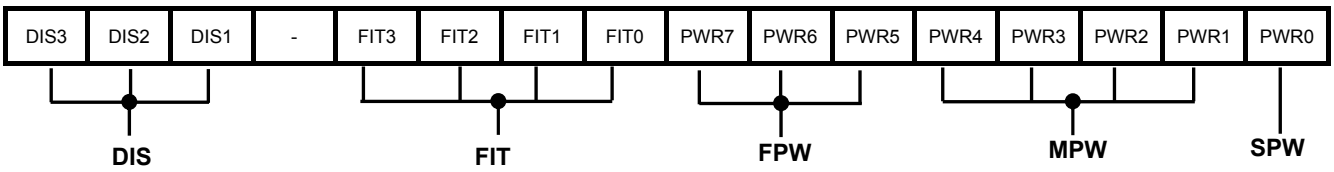
(Note1) Default

MCR12: CTLA (Control_A)

When this bit is set to "1", CTLA Output Pin is set to "Hi". When this bit is set to "0", CTLA Output Pin is set to "Lo".
This bit is set to "0" after reset.

●PWR/FIT: Pulse Width Register/Frame Interval Time

The PWR/FIT register sets the IrTX output pulse width, and frame interval time.



PWR0: SPW (SIR Pulse Width)

This bit is effective in the SIR mode.
When this bit is set to "0", the Hi pulse of about 1.6μs is outputted (default).
When this bit is set to "1", the Hi pulse of 3/16 of a baud cycle is outputted.

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PWR4～1 : MPW3～0（MIR Pulse Width)

This bit is effective in the MIR mode.
Any of the MIR pulse widths listed in the following table is defined by a combination of MPW3 to MPW0.

MPW3～0	MIR Pulse Width[ns]
0000	145.8
0001	166.7
0010	187.5
0011	208.3 (Note1)
0100	229.2
0101	250.0
0110	270.8
0111	291.7
1000	312.5
1001	354.2
1010	395.8
1011	437.5
1100	479.2
1101	520.8
1110	562.5
1111	604.2

(Note1) Default

FIT3～0 :FIT3～0(Frame Interval Times)

This bit is effective in the many windows transmit mode.
Any of the Frame interval time listed in the following table is defined by a combination of FIT3 to FIT0.

FIT3～0	Frame Interval Time[μs]
0000	100(Note1)
0001	200
0010	300
0011	400
0100	500
0101	600
0110	800
0111	1000
1000	1200
1001	1400
1010	1600
1011	1800
1100	2000
1101	2200
1110	2400
1111	2600

(Note1) Default

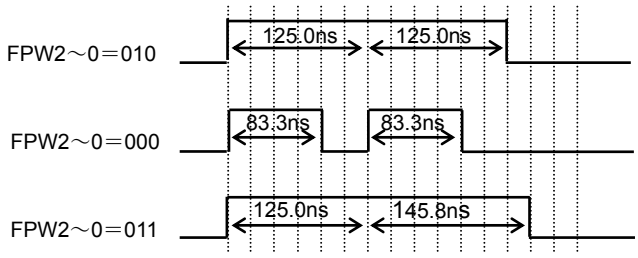
PWR7～5 : FPW2～0(FIR Pulse Width)

This bit is effective in the FIR mode.
any of the FIR pulse widths listed in the following table is defined by a combination of FPW2 to FPW0.

FPW2～0	FIR Pulse Width[ns]
000	83.3
001	104.2
010	125.0(Note1)
011	145.8
100	—
101	—
110	—
111	—

(Note1) Default

A duplicate pulse has a waveform shown below.



DIS2～0 : DIS2～0(Distinction Register)

Model distinction register (read only)

Combinations of FPW2 to FPW0 set to "001" at BU92747XXX.

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●TRCR: Transmit / Receive Control Register

The TRCR register sets various environments for transmission and reception.

TRCR0: TX_EN (Transmit Enable)

When this bit is set to “1”, the transmission mode is set.
When this bit is set to “0”, all data within the FIFO buffer is transmitted, and then transmission is terminated.
When the relation between the number of registers set in the FTLV register and the FLV register (register indicating the amount of data within the buffer) is FLV ≥ FTLV, then TX_EN=0 is automatically set and data transmission is terminated after all data within the FIFO buffer is transmitted.
(Do not set TX_EN and RX_EN to 1 even though this setting causes data reception to take precedence over data transmission.)

TRCR1: RX_EN (Receive Enable)

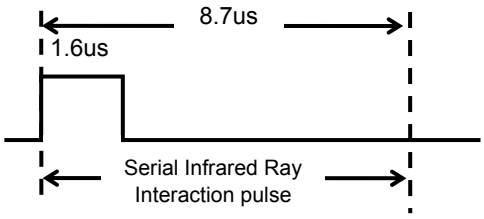
When this bit is set to “1”, the receive mode is set.
When this bit is set to “0”, data reception is terminated. When the last data is odd byte at SIR reception, it must be “C1” (EOF).
(When "C1" data of EOF is written on the LSB side of FIFO at the SIR mode, "00" is inserted in the MSB side by independence and the increment does the FIFO pointer.)
In addition, when the receive mode is terminated once and set again after received data has been read at FIR reception, the next reception is started.
(RX_CON=1and RX_EN=1, or AUTO_FLV_CP=1 and RX_EN=1, this bit doesn't have to be set to the receiving mode again.)

TRCR2: S_EOT (Set End of Transmission)

This bit is effective in MIR and FIR mode. When This bit is set to ”1”, the next data written to the FIFO buffer (2-byte data only) is recognized as the last data and CRC and STF are added just after that data to send a frame.
After frame transmission this bit is automatically set to “0". This bit cannot be used in SIR mode.

TRCR3: IR_PLS (IrDA Pulse)

This bit is effective in MIR mode, FIR mode and many windows transmit mode (MIR and FIR). When this bit is set to “1”, an interaction pulse is transmitted just after the frame being transmitted. After transmission, IR_PLS is automatically set to “0". This bit cannot be used in SIR mode.



TRCR4: FCLR (FIFO clear)

When this bit is set to “1”, WP (Write Point) and RP (Read Point) within the FIFO buffer are initialized.
After completion of initialization, this bit is automatically set to “0".

TRCR5: MS_EN (Mode Select Enable)

This bit is used to switch the communication mode of the Rohm IrDA module RPM971/972.
When this bit is set to “1”, the operation mode of the IrDA module is changed according to the current operation mode of BU92747XXX. Upon completion of operation, MS_EN is automatically set to “0".

When BU92747XXX has been set in the FIR mode, IrDA Module is changed to the FIR mode:
1. The IrDA PWDOWN and IrTX pins are set to “High (H)".
2. After about 200ns have elapsed, the IrDA PWDOWN pin is set to “Low (L)".
3. After about 200ns have elapsed, the IrTX pin is set to “Low (L)” for 200µs.

When BU92747XXX has been set in the SIR/MIR mode, IrDA Module is changed to the SIR mode:
1. The IrDA PWDOWN pin is set to "High (H)” and the IrTX pin is set to “Low (L)".
2. After about 200ns have elapsed, the IrDA PWDOWN pin is set to “Low (L)”.
3. After about 200ns have elapsed, the IrTX pin is set to “Low (L)” for 200µs.

(When TRCR3 and TRCR5 is set to “1” at the same time, TRCR5 takes precedence.)

TRCR6: IrPD (IrDA POWER DOWN)

When this bit is set to “1”, the IrDA PWDOWN pin is set to “Hi”.
When this bit is set to “0”, the IrDA PWDOWN pin is set to “Lo”.
At system reset, this bit is set to "1". (When TRCR5 and TRCR6 is set to “1” at the same time, TRCR6 takes precedence.)

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TRCR7: M_STA (MIR Start Flag times)

This bit controls start flag times in MIR mode.
When this bit is set to "0", start flag is 7E × 2 times (Default).
When this bit is set to "1", start flag is 7E × 4times.

TRCR8: RXPWD (RXD Power down)

When this bit is set to "1", the receive demodulation block is set to the power-down mode. Usually, RXPWD is set to “0".

TRCR9: TXPWD (TXD Power down)

When this bit is set to "1", the transmission demodulation block is set to the power-down mode. Usually, TXPWD is set to “0”.

TRCR10: 1byteRead

This bit is effective in SIR mode.
When this bit is set to “1", 1-byte received data is written to the FIFO LSB and “00” is written to the FIFO MSB, resulting in 16-bit data h00xx. (Data is written to the only FIFO LSB 8bits)
When this bit is set to “0”, 2-byte received data is written to the FIFO 16 bits.

For 1byteRead="1"

FIFO write map

	MSB	LSB
word 0	h'00	h'AA
word 1	h'00	h'BB
	h'00	h'CC
	.	.
	.	.
	.	.

For 1byteRead="0"

FIFO write map

	MSB	LSB
word 0	h'BB	h'AA
word 1	h'DD	h'CC
	h'FF	h'EE
	.	.
	.	.
	.	.

TRCR11:AUTO_FLV_CP

AUTO_FLV_CP (Automation many windows receive mode) change register. TRCR13 (FLV_CP) is processed by the automatic operation. The register of IER/EIR8, 9, and 12 , FLVⅡ, FLVⅢ, and FLVⅣ becomes effective by setting "1" to this bit at the MIR, FIR mode.

TRCR12: RX_CON

When this bit is set to "1", the mode becomes many windows receive mode.
In the MIR, FIR mode IER/EIR8.9.10 and FLVⅡ register are available.
In the SIR mode, FIFO pointer is increased by itself after EOF"C1" data is written FIFO LSB.
At the same moment, "00" is written to FIFO MSB.

TRCR13: FLV_CP

This bit is effective in many windows receive mode (MIR and FIR).
When this bit is set to "1", the data is copied from FLV to FLVⅡ. After the action, this bit is set to “0” automatically.

TRCR14 : TX_CON

When this bit is set to "1", the mode becomes many windows transmit mode. Data frame begins to be transmitted in the condition of FLV≧FTLV. FLV is data number written in FIFO, FTLV is data number transmitted.
At the same moment, WRE_EI that means the CPU is able to write next frame data is set to "1".
The rotation of these actions enables to transmit many windows.

TRCR15 : TX_NUM

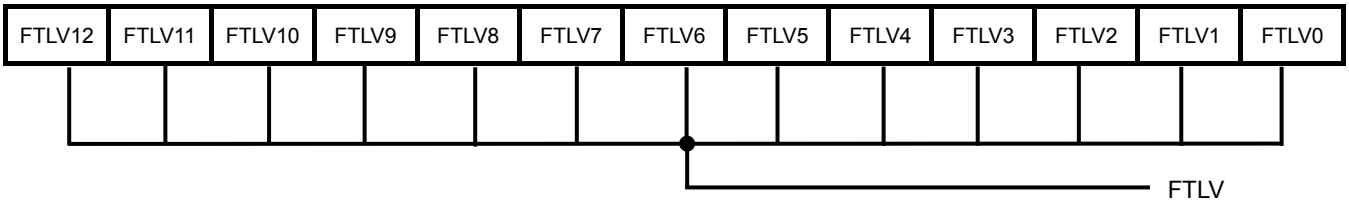
This bit is effective in the many windows transmit mode (TX_CON=1).
When the frame begins to be transmitted in the many windows transmit mode, this bit is set to "1" at the same time automatically. This bit is reset when TX_CON is set to "0".

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●FT: FIFO Trigger Level

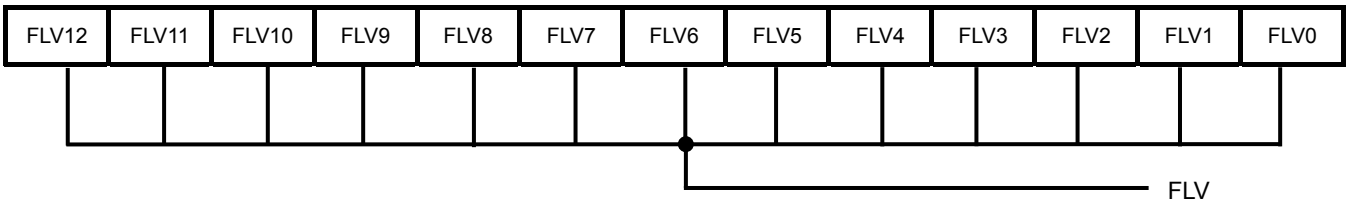
The FTLV register sets the number of data items to be written to FIFO.



This register sets the number of transmission data items in a range from 0 to 5119.
Set the number of transmission data items in this register before transmission.

●FLV: FIFO Level

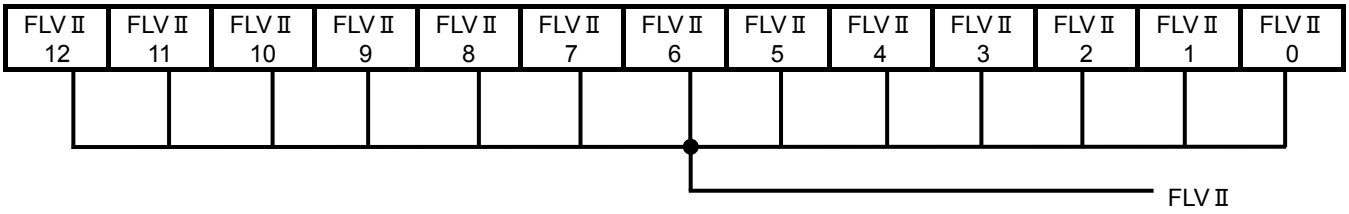
The FLV register indicates the number of data items in FIFO.



This register indicates the number of data items stored in the FIFO buffer in a range from 0 to 5119.
At the end of data transmission, FLV is automatically set to 0. (Because data writing by CPU takes place in units of even bytes, an even number (byte) is indicated during data transmission.)

●FLVⅡ: FIFO Level

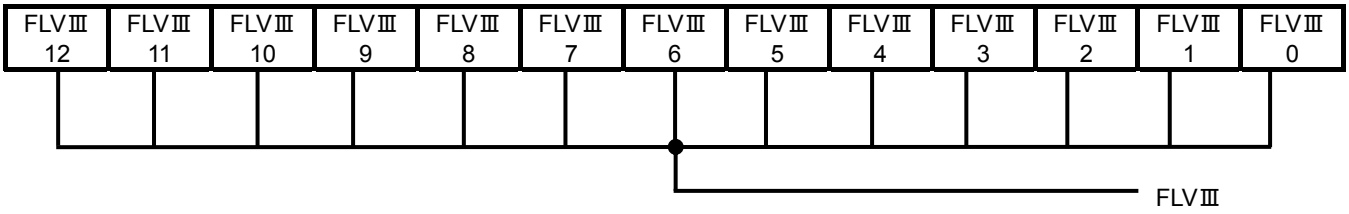
The FLVⅡ register indicates the number of data items in FIFO.



In the MIR and FIR many windows receive mode or AUTO_FLV_CP mode, the number of preceding frame data is indicated by any number from 0 to 5119.
In the many windows transmit mode, the number of transmitting frame data is indicated by any number from 0 to 5119.

●FLVⅢ: FIFO Level

The FLVⅢ register indicates the number of data items in FIFO.



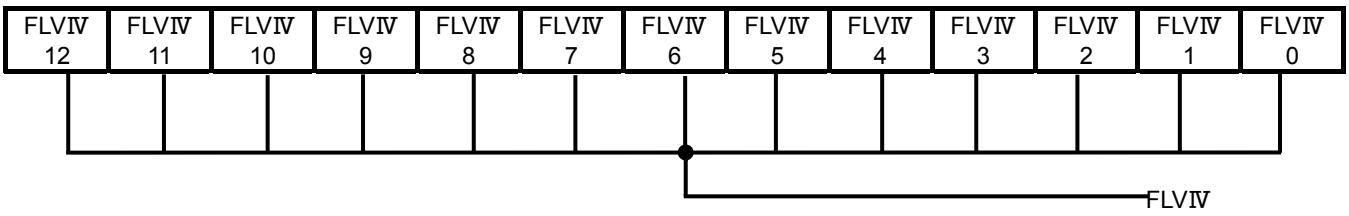
When data exists in FLVⅡ, FLVⅢ indicates the number of data bytes of the following frames that do the reception completion in AUTO_FLV_CP mode.

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●FLVⅣ: FIFO Level

The FLVⅣ register indicates the number of data items in FIFO.



When data exists in FLVⅢ, FLVⅣ indicates the number of data bytes of the following frames that do the reception completion in AUTO_FLV_CP mode.

●TRCRⅡ: Transmit / Receive Control Register

TRCRⅡ is a register that sets each environment of the transmission and the reception.

TRCRⅡ1 : TXE_C_CLR (TXE_EI Counter Clear)

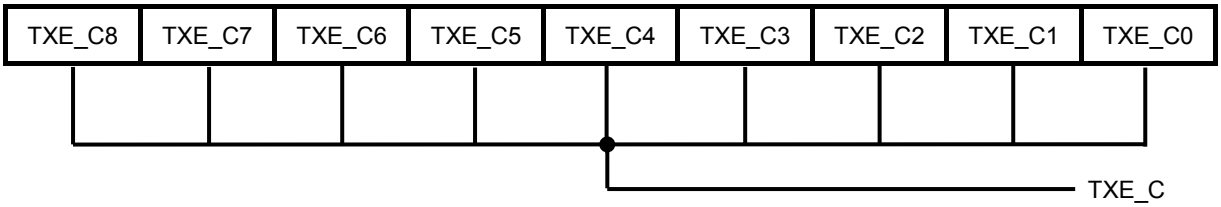
When this bit is set to “1”, TXE_EI Counter is cleared.
After it clears, this bit is set to “0” automatically.

TRCRⅡ2 : WRE_C_CLR (WRE_EI Counter Clear)

When this bit is set to “1”, WRE_EI Counter is cleared.
After it clears, this bit is set to “0” automatically.

●TXE_C: TXE_EI Counter

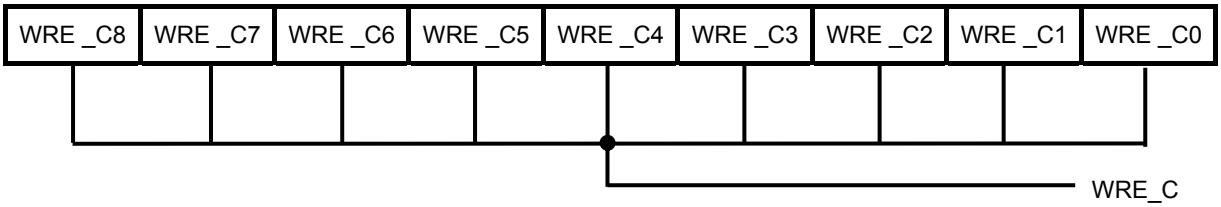
TXE_C is a register that counts the generation frequency of TXE_EI.



TXE_C is effective in many windows transmit mode.
The initial value is 0.
TXE_C is initialized by TXE_C_CLR=1 or transmit / receive mode change.

●WRE_C: WRE_EI Counter

WRE_C is a register that counts the generation frequency of WRE_EI.



WRE_C is effective in many windows transmit mode.
The initial value is 0.
WRE_C is initialized by WRE_C_CLR=1 or transmit / receive mode change.

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●Ir Remote Control Functional Description

The MCR register (MCR10:RC_EN) set to "1" when Ir remote control function is used.

Serial 2- lines Interface

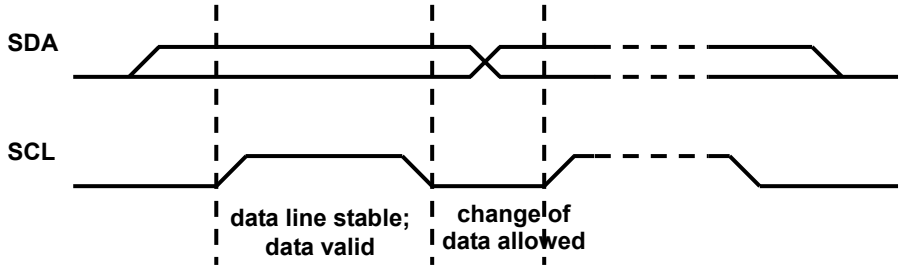
BU92747XXX is controlled by serial 2-lines slave interface. The address (slave address) is “1110111”.

A7	A6	A5	A4	A3	A2	A1	W/R
1	1	1	0	1	1	1	0/1

slave address

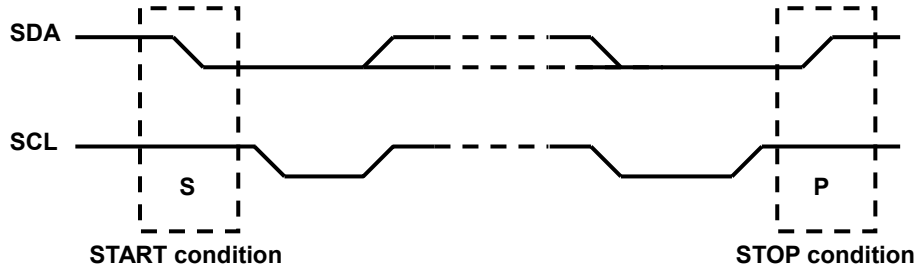
TRANSFER

During “H” period of SCL, one data bit is transferred. The data on the SDA line must be stable during the HIGH period of the clock, as changes in the data line at this time will be interpreted as a control signal.



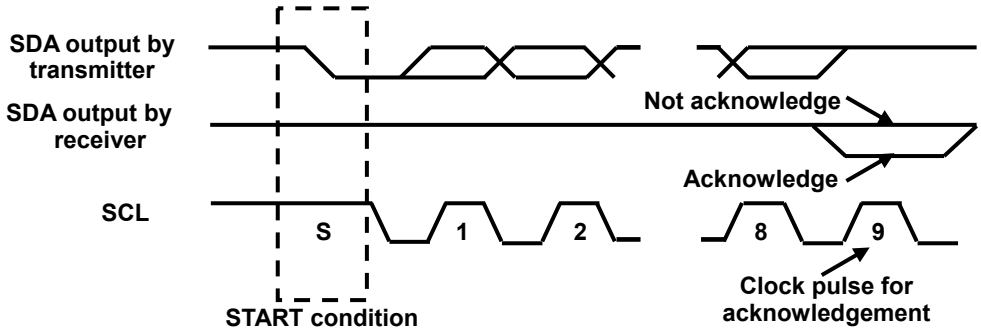
START AND STOP CONDITIONS

Both data and clock lines remain HIGH when the bus is not busy. A HIGH to LOW transition of the data line, while the clock is HIGH is defined as the START (S) condition. A LOW to HIGH transition of the data line while the clock is HIGH is defined as the STOP (P) condition.



ACKNOWLEDGE

After the occurrence of START condition, each 8-bits has to be followed. A receiver must generate an acknowledgement by pulling down the SDA line after the reception of each byte. In this event the transmitter leaves the SDA line.

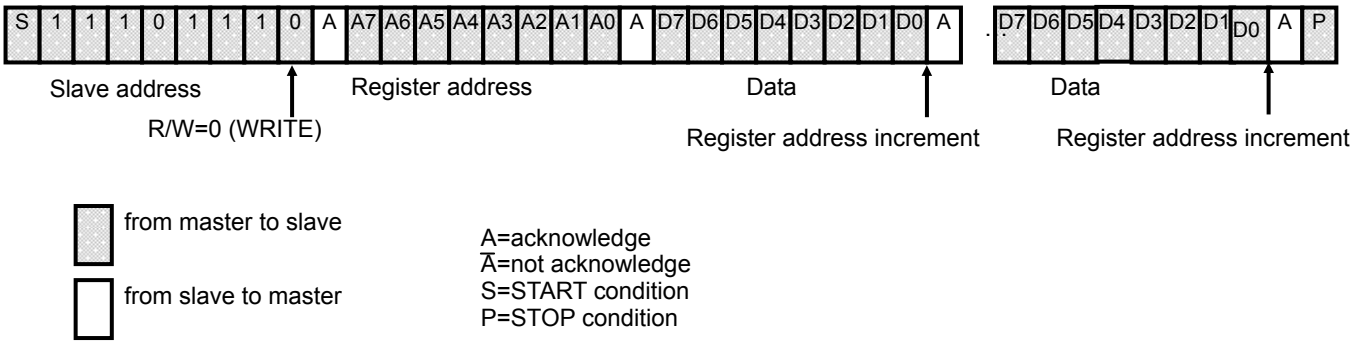


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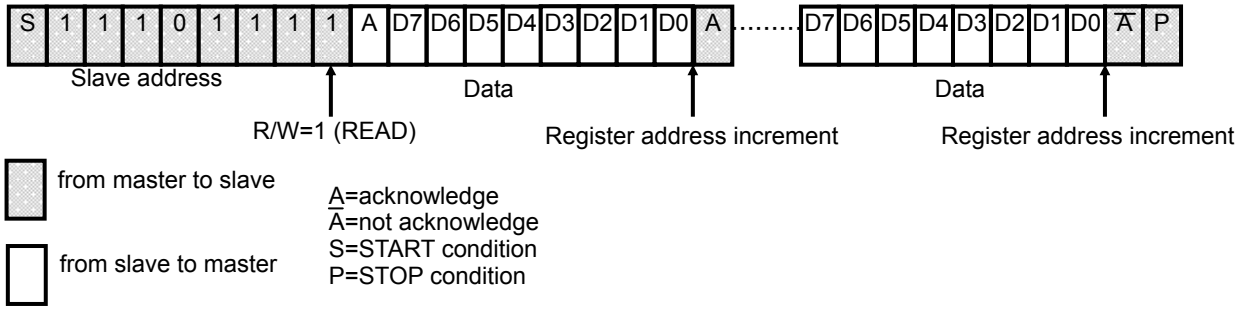
REGISTER WRITING PROTOCOL

The following sentence is about writing protocol. After transmitting the slave address and WRITE command (first byte), the register address of BU92747XXX is transferred (second byte). The third byte is the register data of this register address (second byte). After the register data (third byte), it is possible to send the register data consecutively. The address is automatically increased. But the next register address becomes 00h when the register address becomes final address (3Fh). After finishing the transmission, the register address is increased.



REGISTER READING PROTOCOL

After the slave address and R/W bit are written, register data is read from the fllowing byte. This data is the register data of the address which is followed the last access address. Subsequently , the register data of the increased address is read. But the following register address becomes 00h when the register address becomes final address. After the transmission is finished, the register address is incresed.

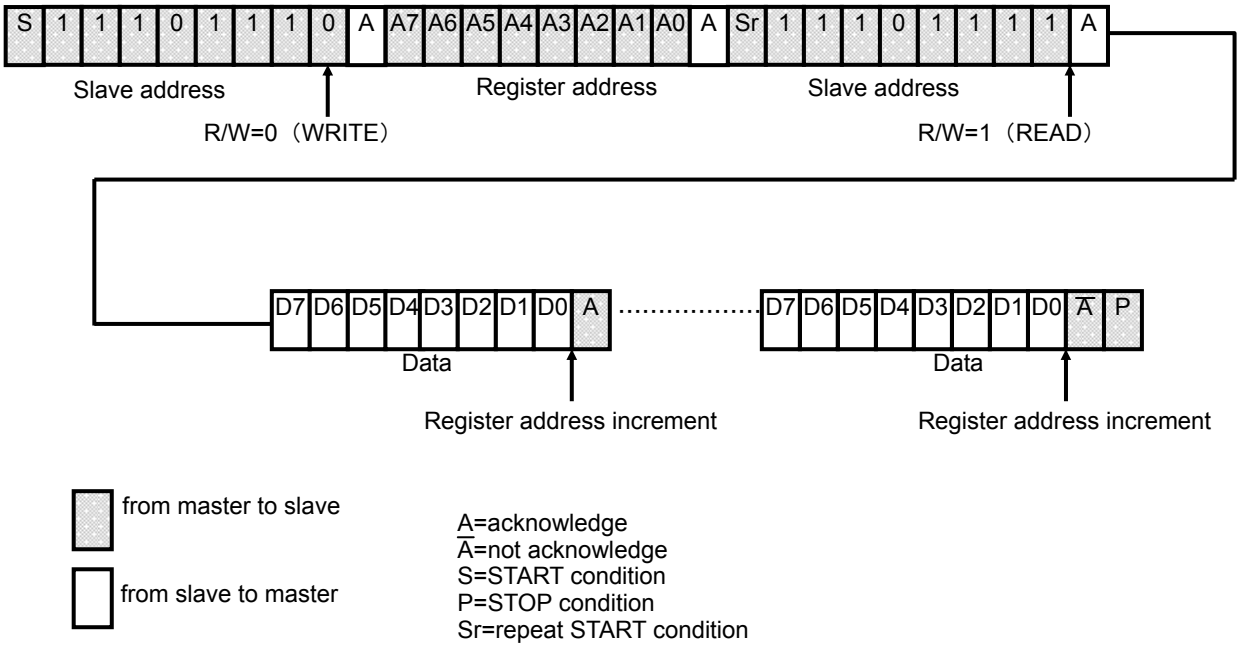


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COMPLEX PROTOCOL

If the repeated START condition is occurred after the register address is set, the register data of following address is read. Subsequently, the register data of the increased address is read. But the following register address becomes 00h when the register address becomes final address. After the transmission is finished, the register address is increased.



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●**Ir Remote Control Register Set**

Address	Initial Value	R/W	D7	D6	D5	D4	D3	D2	D1	D0
00h	00h	R/W	-	-	Opm	Divs	Irqe	Inv1	Inv0	Pwr
01h	01h	R/W	-	-	Frmb	Frme	Rpt			
02h	00h	R/W	Base							
03h	01h	R/W	-	-	-	-	-	-	-	Clo1
04h	19h	R/W	Clo0							
05h	00h	R/W	-	-	-	-	-	-	-	Chi1
06h	8Fh	R/W	Chi 0							
07h	00h	R/W	-	-	Hlo1					
08h	ABh	R/W	Hlo0							
09h	01h	R/W	-	-	Hhi1					
0Ah	58h	R/W	Hhi0							
0Bh	00h	R/W	-	-	D0lo1					
0Ch	14h	R/W	D0lo0							
0Dh	00h	R/W	-	-	D0hi1					
0Eh	14h	R/W	D0hi0							
0Fh	00h	R/W	-	-	D1lo1					
10h	14h	R/W	D1lo0							
11h	00h	R/W	-	-	D1hi1					
12h	3Ch	R/W	D1hi0							
13h	00h	R/W	-	-	EndLen1					
14h	14h	R/W	EndLen0							
15h	20h	R/W	BitLen							
16h	00h	R/W	FrmLen1							
17h	00h	R/W	FrmLen0							
18h	00h	R/W	Out0							
19h	00h	R/W	Out1							
1Ah	00h	R/W	Out2							
1Bh	00h	R/W	Out3							
1Ch	00h	R/W	Out4							
1Dh	00h	R/W	Out5							
1Eh	00h	R/W	Out6							
1Fh	00h	R/W	Out7							
20h	00h	R/W	Out8							
21h	00h	R/W	Out9							
22h	00h	R/W	Out10							
23h	00h	R/W	Out11							
24h	00h	R/W	Out12							
25h	00h	R/W	Out13							
26h	00h	R/W	Out14							
27h	00h	R/W	Out15							
28h	00h	W	-	-	-	-	-	-	-	Irqc
29h	00h	W	-	-	-	-	-	-	-	Send
2Ah	00h	W	-	-	-	-	-	-	-	Rst
2Bh	00h	R/W	-	-	-	-	-	-	-	Regs
2Ch～3Fh	-	-	Reserved							

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●DESCRIPTION OF REGISTER FUNCTION

Address 00h (Read/Write)

	Description	Initial value	Operation
D5 (Opm)	Selection of operational mode	0	Operational mode 0: When transmission buffer is null, interrupt is generated. 1: When output register data is transmitted to transmission buffer, interrupt is generated.
D4 (Divs)	Selection of divider	0	Divider in the system clock generator 0: Carrier divider. 1: Base clock divider. The system clock frequency is a reference of period setting for each part except carrier part (Clo, Chi).
D3 (Irqe)	Permission of interrupt	0	Interrupt mode 0: Mask Mode, $\overline{\text{NIRQ}}$ pin output “HIGH”. 1: Permit Mode, $\overline{\text{NIRQ}}$ pin output “LOW” when this bit is “1” and the transmission buffer is null.
D2 (Inv1)	Data output period, reversal of Lo period (Data1)	0	Data1 output format 0: In Data1 output, Lo part follows carrier freq. 1: In Data1 output, carrier freq. follows Lo part.
D1 (Inv0)	Data output period, revered of Lo period (Data0)	0	Data0 output format 0: In Data0 output, Lo part follows carrier freq. 1: In Data0 output, carrier freq. follows Lo part.
D0 (Pwr)	Control of clock buffer	0	Clock buffer (CLKI pin) power down control 0: Power down to stop the internal clock. DOUT pin outputs “LOW” and NIRQ pin outputs “HIGH”. 1: Power up.

Address 01h (Read/Write)

	Description	Initial value	Operation
D5 (Frmb)	Base of frame interval	0	Base of frame interval 0: A start of header is selected as base of frame interval. 1: Ah end of End parts selected as base of frame interval. Frame interval (FrmLen) sets up a time from base of frame interval to the following start of header.
D4 (Frme)	Control of frame interval	0	Frame interval 0: Disable 1: Enable, It enables the time interval to set from the current transmission data to the next data.
D3-D0 (Rpt)	Repetition times	1h	IrRC (or IrTX) output times control The setting value of this register is the repetition times (When Rpt=0h, the repetition times is 16). In case of setting this register, set Frme and FrmLen.

Address 02h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Base)	Base clock frequency dividing	00h	Base clock frequency control (Base clock cycle) = 1/ (XIN input freq.÷3) [Sec] (Base=00h), (Base clock cycle) = (2×Base) / (XIN input freq.÷3) [sec] (except for above).

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Address 03h (Read/Write)

	Description	Initial value	Operation
D0 (Clo1)	Period of carrier Lo (MSB)	1	Carrier “Lo” (Clo) period control with Clo0

Address 04h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Clo0)	Period of carrier Lo (Lower 8 bit)	19h	Carrier “Lo” (Clo) period control with Clo1 (Period of carrier lo) = (2^8xClo1+Clo0) / (XIN input freq.÷3) [Sec]

Address 05h (Read/Write)

	Description	Initial value	Operation
D0 (Chi1)	Period of carrier Hi (MSB)	0	Carrier “Hi” (Chi) period control with Chi0

Address 06h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Chi0)	Period of carrier Hi (Lower 8 bit)	8Fh	Carrier “Hi” (Chi) period control with Chi1 (Period of carrier Hi) = (2^8xChi1+Chi0) / (XIN input freq.÷3) [Sec]

・(System clock freq.) = 1 / (Period of carrier Lo + Period of carrier Hi) [Hz] (Divs = 0)
・(System clock freq.) = 1 / (Base clock cycle) [Hz] (Divs = 1)

Address 07h (Read/Write)

	Description	Initial value	Operation
D5-D0 (Hlo1)	Period of header Lo part (Upper 6bit)	00h	Header “Lo” (Hlo) period control with Hlo0

Address 08h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Hlo0)	Period of header Lo part (Lower 8 bit)	ABh	Header “Lo” (Hlo) period control with Hlo1 (Period of header Lo) = (2^8x Hlo1+Hlo0) / (system clock freq.) [Sec]

Address 09h (Read/Write)

	Description	Initial value	Operation
D5-D0 (Hhi1)	Period of header Hi part (Upper 6bit)	01h	Header “Hi” (Hhi) period control with Hhi0

Address 0Ah (Read/Write)

	Description	Initial value	Operation
D7-D0 (Hhi0)	Period of header Hi part (Lower 8 bit)	58h	Header “Hi” (Hhi) period control with Hhi1 (Period of header Hi) = (2^8x Hhi1+Hhi0) / (system clock freq.) [Sec]

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Address 0Bh (Read/Write)

	Description	Initial value	Operation
D5-D0 (D0lo1)	Period of Data0 Lo part (Upper 6bit)	00h	Data0 “Lo” (D0lo) period control with D0lo0

Address 0Ch (Read/Write)

	Description	Initial value	Operation
D7-D0 (D0lo0)	Period of Data0 Lo part (Lower 8 bit)	14h	Data0 “Lo” (D0lo) period control with D0lo1 (Period of Data0 lo) = (2^8x D0lo1+D0lo0) / (system clock freq.) [sec]

Address 0Dh (Read/Write)

	Description	Initial value	Operation
D5-D0 (D0hi1)	Period of Data0 Hi part (Upper 6bit)	00h	Data0 “Hi” (D0hi) period control with D0hi0

Address 0Eh (Read/Write)

	Description	Initial value	Operation
D7-D0 (D0hi0)	Period of Data0 Hi part (Lower 8 bit)	14h	Data0 “Hi” (D0hi) period control with D0hi1 (Period of Data0 lo) = (2^8x D0hi1+D0hi0) / (system clock freq.) [sec]

Address 0Fh (Read/Write)

	Description	Initial value	Operation
D5-D0 (D1lo1)	Period of Data1 Lo part (Upper 6bit)	00h	Data1 “Lo” (D1lo) period control with D1lo0

Address10h (Read/Write)

	Description	Initial value	Operation
D7-D0 (D1lo0)	Period of Data1 Lo part (Lower 8 bit)	14h	Data1 “Lo” (D1lo) period control with D1lo1 (Period of Data1 Lo) = (2^8x D1lo1+D1lo0) / (system clock freq.) [sec]

Address 11h (Read/Write)

	Description	Initial value	Operation
D5-D0 (D1hi1)	Period of Data1 Hi part (Upper 6bit)	00h	Data1 “Hi” (D1hi) period control with D1hi1

Address 12h (Read/Write)

	Description	Initial value	Operation
D7-D0 (D1hi0)	Period of Data1 Hi part (Lower 8 bit)	3Ch	Data 1 “Hi” (D1hi) period control with D1hi0 (Period of Data1 Hi)=(2^8x D1hi1+D1hi0)/(system clock freq.) [sec]

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Address13h (Read/Write)

	Description	Initial value	Operation
D5-D0 (EndLen1)	Period of End part (Upper 6bit)	00h	End period control with EndLen0

Address 14h (Read/Write)

	Description	Initial value	Operation
D7-D0 (EndLen0)	Period of End part (Lower 8 bit)	14h	End period control with EndLen1 (Period of End) = (2^8x EndLen1+EndLen0) / (system clock freq.) [sec]

Address 15h (Read/Write)

	Description	Initial value	Operation
D7-D0 (BitLen)	Output bit length of data part	20h	Output bit length of data part control The output data is transferred from Out0 with LSB first. When BitLen=00h, there are no data parts.

Address16h (Read/Write)

	Description	Initial value	Operation
D7-D0 (FrmLen1)	Frame interval (Upper 8bit)	00h	Frame interval control with FrmLen0

Address 17h (Read/Write)

	Description	Initial value	Operation
D7-D0 (FrmLen0)	Frame interval (Lower 8 bit)	00h	Frame interval control with FrmLen1 (Frame interval)=(2^8x FrmLen1+FrmLen0)/(system clock frequency) [sec] When the frame interval is controlled, the frame interval must be set more than the following value: (Hhi+Hlo)+max{(D0hi+D0lo), (D1hi+D1ho)}×(BitLen)+(EndLen)+4 (The max function returns the greater one in the brace.)

Address 18h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out0)	Output data	00h	Output data of Out0 The output data is transferred from Out0 with LSB first. Setting data bit “1”: Output Data1 (from IrRC or IrTX pin) Setting data bit “0”: Output Data0 (from IrRC or IrTX pin)

Address 19h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out1)	Output data	00h	Output data of Out1

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Address 1Ah (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out2)	Output data	00h	Output data of Out2

Address 1Bh (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out3)	Output data	00h	Output data of Out3

Address 1Ch (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out4)	Output data	00h	Output data of Out4

Address 1Dh (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out5)	Output data	00h	Output data of Out5

Address 1Eh (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out6)	Output data	00h	Output data of Out6

Address 1Fh (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out7)	Output data	00h	Output data of Out7

Address 20h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out8)	Output data	00h	Output data of Out8

Address 21h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out9)	Output data	00h	Output data of Out9

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Address 22h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out10)	Output data	00h	Output data of Out10

Address 23h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out11)	Output data	00h	Output data of Out11

Address 24h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out12)	Output data	00h	Output data of Out12

Address 25h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out13)	Output data	00h	Output data of Out13

Address 26h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out14)	Output data	00h	Output data of Out14

Address 27h (Read/Write)

	Description	Initial value	Operation
D7-D0 (Out15)	Output data	00h	Output data of Out15

Address 28h (Write)

	Description	Initial value	Operation
D0 (Irqc)	Clear the internal interrupt	0	1: The internal interrupt is cleared.

Address 29h (Write)

	Description	Initial value	Operation
D0 (Send)	Start the transmission	0	1: The register setting is forwarded to the transmission buffer, and the transmission starts in the IrRC (or IrTX) pin. After forwarding to the transmission buffer, this bit is set “0”. At the same time, the internal interrupt is cleared.

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Address 2Ah (Write)

	Description	Initial value	Operation
D0 (Rst)	Remote control Reset	0	0: Normal operation 1: Reset. When the condition of serial bus is STOP, this bit is set “0”. The operation of this bit must not do with the operation of another address. This operation must be realized by accessing only this address on a sequence of the data transmission of serial (from START condition to STOP condition).

Address 2Bh (Write)

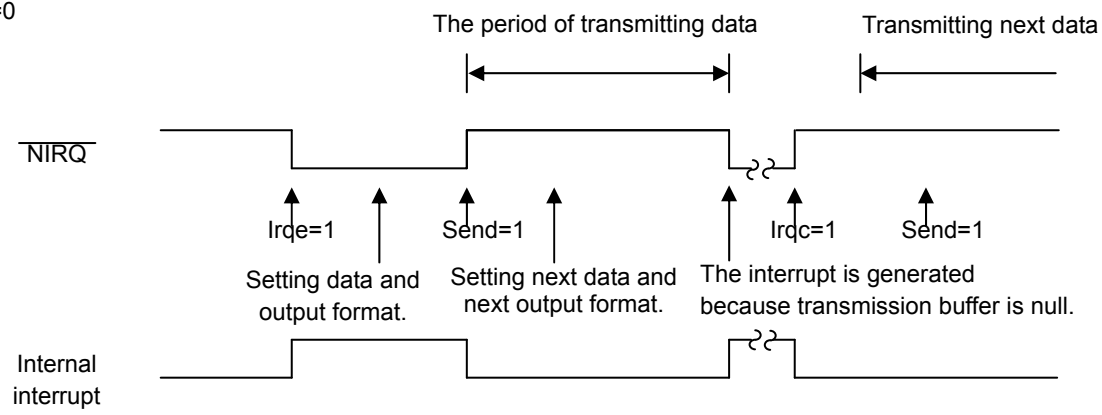
	Description	Initial value	Operation
DO (Regs)	Selection of forwarding to transmission buffer	0	Transmitting from output data register to transmission buffer only once or repeatedly 0: 128 bits data in Out0~Out15 is forwarded to transmission buffer only once. Then data bit length that is specified by BitLen is outputted to IrRC (or IrTX), and End part is outputted to IrRC (or IrTX) pin. 1: It is repeated that 128 bits data in Out0~Out15 is forwarded to transmission buffer. After 128 bits data of transmission buffer is outputted to IrRC (or IrTX), 128 bits data of Out0~Out15 is forwarded to transmission buffer and the data of transmission buffer is outputted to IrRC (or IrTX) again.

Address 2Ch-3Fh

Reserved.

●INTERRUPT FUNCTION

Opm=0

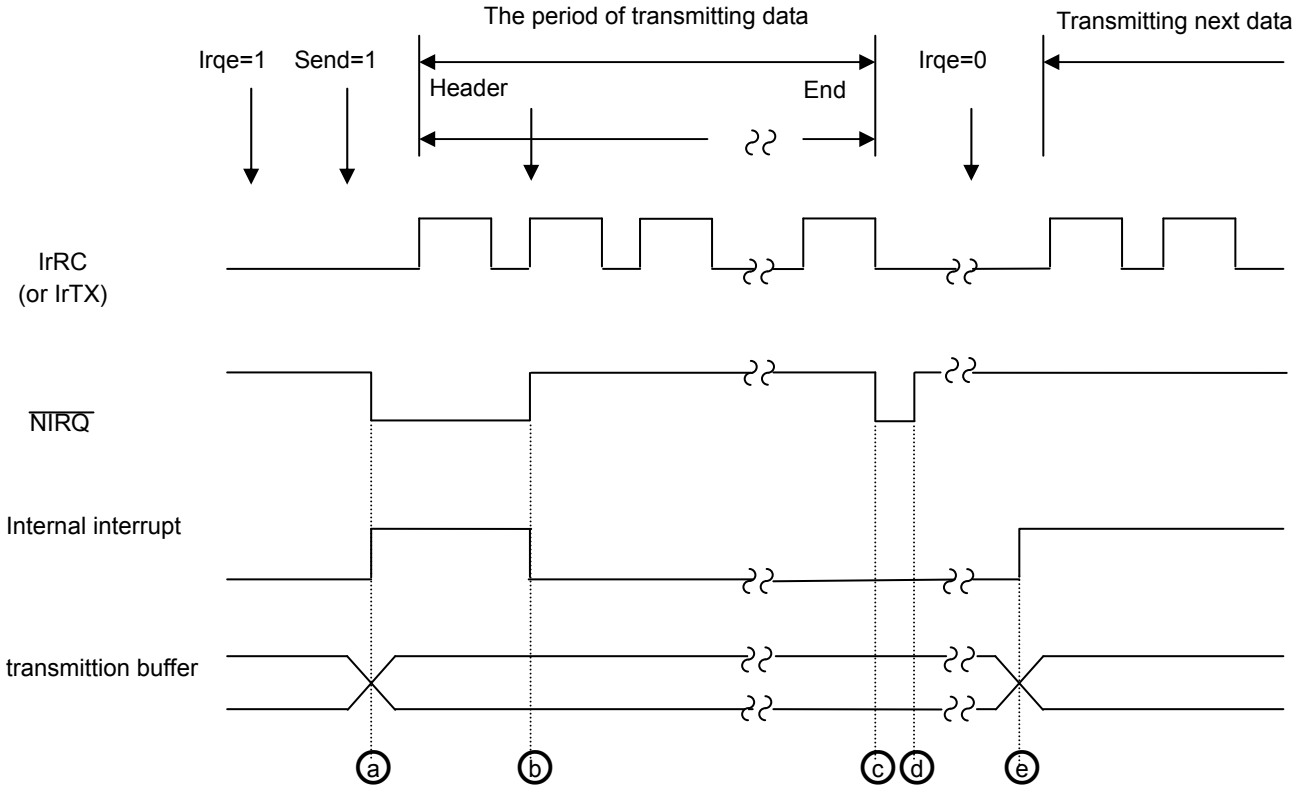


When transmission buffer is null, internal interrupt is generated.
After the reset is canceled, transmission buffer becomes null.
When Send bit is set to “1”, the setting data is forwarded to the transmission buffer, and starts the transmission in IrRC (or IrTX) pin.
When the data is forward to the transmission buffer, the interrupt is cleared.
Also, when Irqc bit is set “1”, the interrupt is cleared.
When Irqe bit is set “1”, NIRQ pin outputs the interrupt condition because the internal interrupt is permitted.
When Irqe bit is set “0”, NIRQ pin outputs “HIGH” because the internal interrupt is masked.

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Opm=1



With forwarding value of output data register to the transmission buffer, it is enabled to update the output data register. Therefore internal interrupt is generated (refer ⓐ in the figure).

- Regs bit sets “0”: if Send bit sets “1”, the value of output data register is forwarded to the transmission buffer and internal interrupt is generated.
- Regs bit sets “1”: If Send bit sets “1”, the value of output data register is forwarded to the transmission buffer and internal interrupt factor is generated. Afterward, the value of output data register is forwarded to the transmission buffer when the last bit of transmission buffer is outputted. As often as this transmission is finished, internal interrupt is generated.

Afterward, finished End part output, interrupt is generated (refer ⓒ in the figure).

When Irqc bit sets “1”, interrupt is cleared (refer ⓑ and ⓓ in the figure).

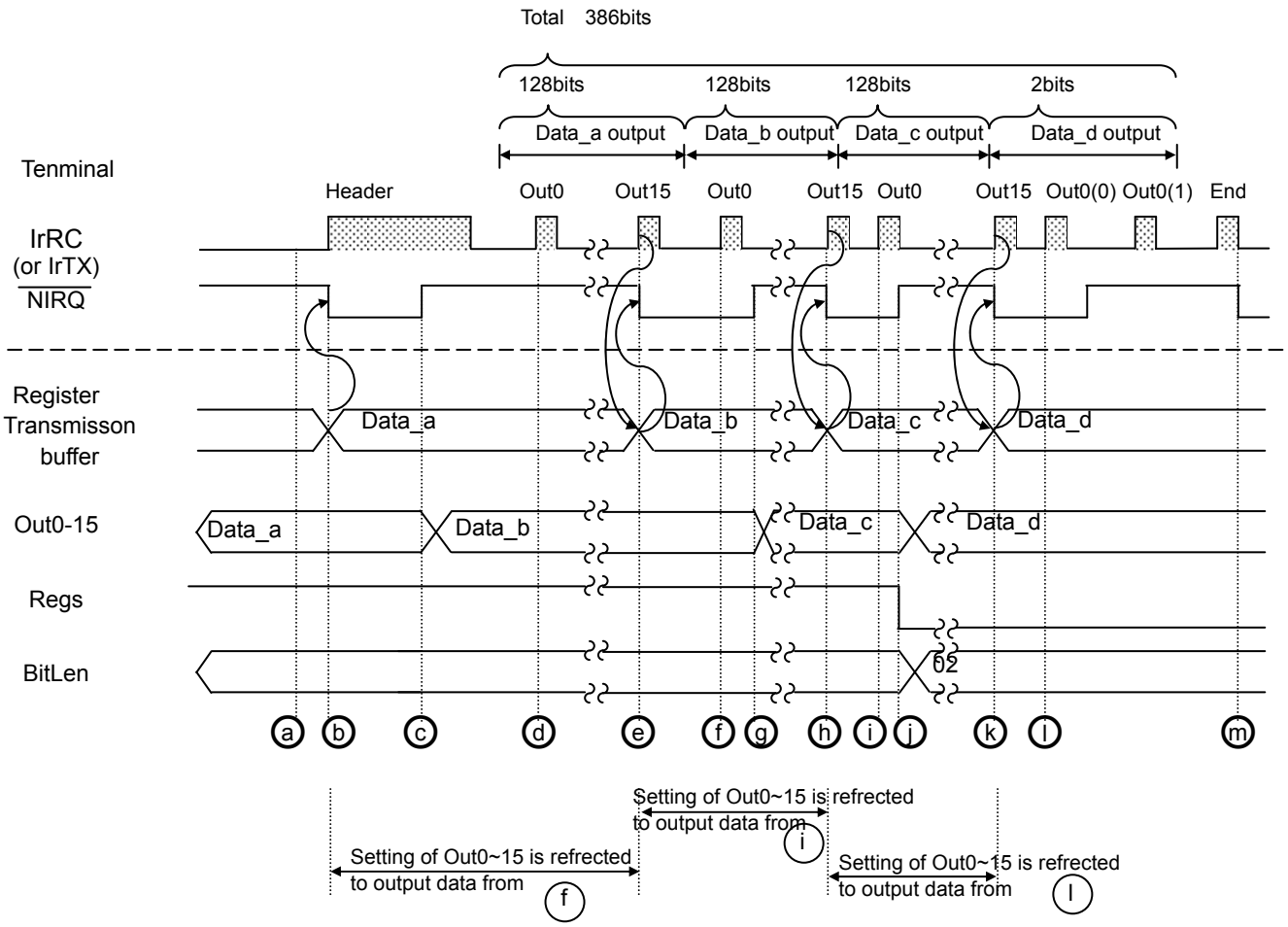
When Irqe bit sets “1”, internal interrupt is permitted. Therefore with generating the internal interrupt, NIRQ pin outputs ”LOW” (refer ⓐ and ⓒ in the figure).

When Irqe bit sets “0”, NIRQ pin fixes “HIGH” (refer ⓔ in the figure).

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●SETTIG MORE THAN 128BITS DATA



This is an example that data length of one frame is 386 bits.

a. Register setting is Irqe=1, i.e. it is permitted interrupt, Regs=1, i.e. it is repeated to forward output data register to transmission buffer, and Out0~15=Data_a, i.e. it is set output data register to Data_a as transmission data. Then to set Send=1, the transmission is started.
b. After the transmission is started, Out0~15 is forwarded to transmission buffer. Then, interrupt is generated (NIRQ="LOW"), and it is informed to update Out0~15.
c. After Irqc=1, i.e. it is cleared internal interrupt, Out0~15 set to Data_b.
d. After header part output is finished, Data_a in transmission buffer is outputted from IrRC(or IrTx) pin.
e. When the last bit of Data_a is outputted, Data_b in Out0~15 is forwarded to transmission buffer. Then interrupt is generated, and it is informed to update Out0~15.
f. After Data_a output is finished, Data_b in transmission buffer is outputted to IrRC (or IrTx) pin.
g. After internal interrupt is cleared, Out0~15 set to Data_c.
h. When the last bit of Data_b is outputted, Data_c in Out0~15 is forwarded to transmission buffer. Then interrupt is generated, and it is informed to update Out0~15.
i. After Data_b output is finished, Data_c of transmission buffer is outputted to IrRC (or IrTx) pin.
j. Internal interrupt is cleared. Then register setting is Regs=0, i.e. it is to forwarded output data register to transmission buffer once, and BitLen=02h, i.e. data bit length is 2bits.
k. When the last bit of Data_c is outputted, Data_d in Out0~15 is forwarded to transmission buffer. Then interrupt is generated. For Regs=0 and BitLen=02h, finished Data_c output, next output is 2bits of Data_d.
l. After Data_b output is finished, 2bits of Data_d in transmission buffer is outputted to IrRC (or ITtx) pin, then End
m. A sequence of sending is finished, and then interrupt is generated.

To repeat above e-g, it is enabled to send more than 128 bits data length.

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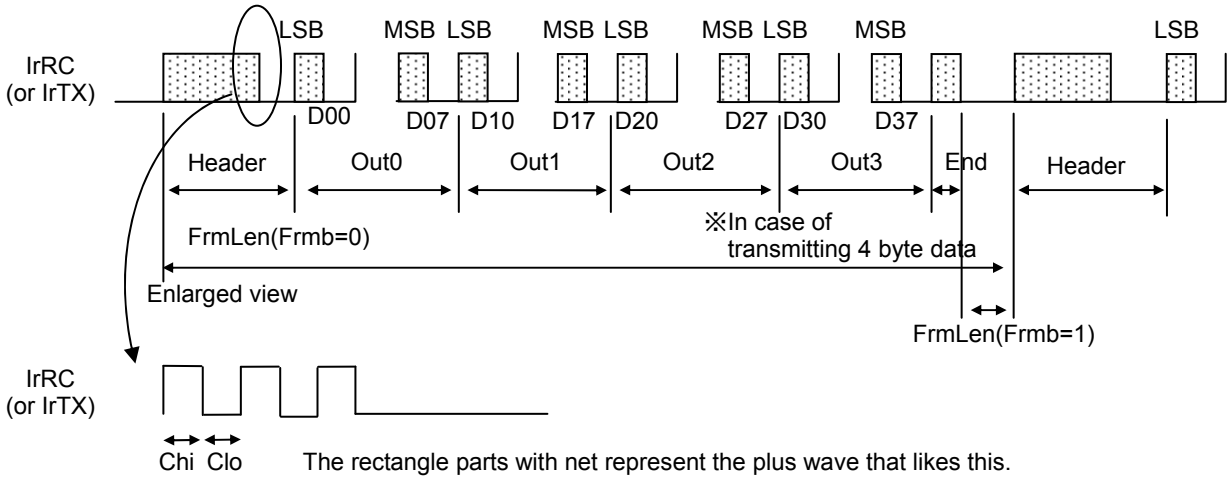
Note 1 When it is sent the data of more than 128 bits, if data output is sent several times in the way to set Rpt register, the frame output after the 2nd frame output is different from the 1st frame output. In the above example, if Rpt=2, the 2nd frame output is “Header + 2bits in Data_d + End part”. If 1st frame output is repeated. After 1st frame output is finished, it needs to re-set Reg=1 and Out0-15.

Note 2 When start of header is selected as base of frame interval (Frmb=0), It is the possibility that the time to send a series of data from header to End part is out of the FrmLen’s range. To avoid such a case, end of End part as base of frame interval is selected (Frmb=1).

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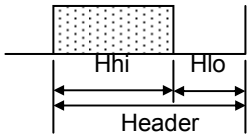
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●OUTPUT FORMAT



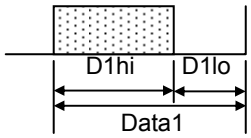
The rectangle parts with net represent the plus wave that likes this.

※Header part

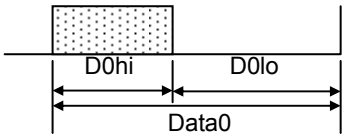


※Data part

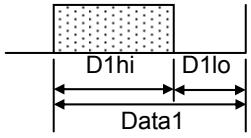
Data1(Inv1=0, Inv0=0)



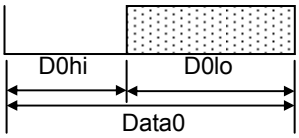
Data 0(Inv1=0, Inv0=0)



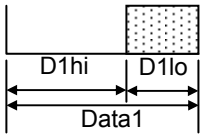
Data 1(Inv1=0, Inv0=1)



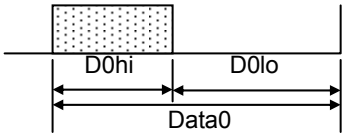
Data 0(Inv1=0, Inv0=1)



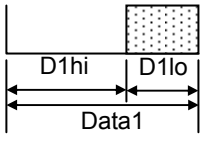
Data 1(Inv1=1, Inv0=0)



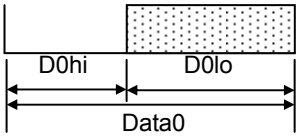
Data 0(Inv1=1, Inv0=0)



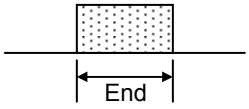
Data 1(Inv1=1, Inv0=1)



Data 0(Inv1=1, Inv0=1)



※End part



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●**INITIAL VALUE OF REGISTER**

Register name	Register setting	Time		Condition
	Initial value	Initial value	unit	
Base	00h	0.0625	μs	XIN=48MHz
Clo1, Clo0	1h, 19h	17.56	μs	XIN=48MHz
Chi1, Chi0	0h, 8Fh	8.94	μs	XIN=48MHz
Hlo1, Hlo0	00h, ABh	4.5	ms	carrier frequency＝37.9kHz, Divs=0
Hhi1, Hhi0	01h, 58h	9.1	ms	carrier frequency＝37.9kHz, Divs=0
D0lo1, D0lo0	00h, 14h	530	μs	carrier frequency＝37.9kHz, Divs=0
D0hi1, D0hi0	00h, 14h	530	μs	carrier frequency＝37.9kHz, Divs=0
D1lo1, D1lo0	00h, 14h	530	μs	carrier frequency＝37.9kHz, Divs=0
D1hi1, D1hi0	00h, 3Ch	1590	μs	carrier frequency＝37.9kHz, Divs=0
EndLen1,EndLen0	00h, 14h	530	μs	carrier frequency＝37.9kHz, Divs=0
BitLen	20h	32	bit	
FrmLen1, FrmLen0	00h, 00h	0	μs	carrier frequency＝37.9kHz, Divs=0

●**RANGE OF REGISTER SETTING (Divs=0)**

Register name	The enable range of register setting		Time (XIN=48MHz)		Condition
	min	max	min	max	
Base	00h	FFh	0.0625	31.875	μS
Clo1, Clo0	0h, 01h	1h, FFh	0.0625	31.938	μS
Chi1, Chi0	0h, 01h	1h, FFh	0.0625	31.938	μS
Hlo1, Hlo0	00h, 00h,	3Fh, FFh	0	16383	carrier cycle
Hhi1, Hhi0	00h, 00h,	3Fh, FFh	0	16383	carrier cycle
D0lo1, D0lo0	00h, 01h,	3Fh, FFh	1	16383	carrier cycle
D0hi1, D0hi0	00h, 01h,	3Fh, FFh	1	16383	carrier cycle
D1lo1, D1lo0	00h, 01h,	3Fh, FFh	1	16383	carrier cycle
D1hi1, D1hi0	00h, 01h,	3Fh, FFh	1	16383	carrier cycle
EndLen1,EndLen0	00h, 01h,	3Fh, FFh	0	16383	carrier cycle
BitLen	00h	80h	0	128	bit
FrmLen1, FrmLen0	①	FFh, FFh	①	65535	carrier cycle

※Don't set the data that is out of the range in these registers, because it doesn't guarantee the operation.
① applies the following expression: (Hhi+Hlo)+max{(D0hi+D0lo), (D1hi+D1ho)}×(Bit Len)+(End Len)+4 (Frmb=0),4 (Frmb=1)

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●Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

In the construction of this IC, P-N junctions are inevitably formed creating parasitic diodes or transistors. The operation of these parasitic elements can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions which cause these parasitic elements to operate, such as applying a voltage to an input pin lower than the ground voltage should be avoided. Furthermore, do not apply a voltage to the input pins when no power supply voltage is applied to the IC. Even if the power supply voltage is applied, make sure that the input pins have voltages within the values specified in the electrical characteristics of this IC.

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●Ordering Information

B U 9 2 7 4 7 X X X	E 2

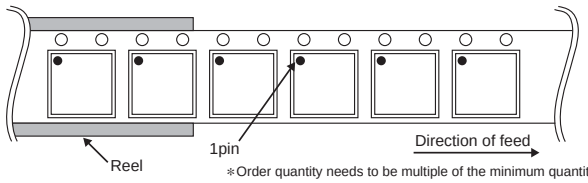
- Part Number
- Package
  GUW:VBGA048W040
  KV:VQFP48C
- Packaging and forming specification
  E2: Embossed tape and reel
  Blank: Tray

●Physical Dimension Tape and Reel Information

VBGA048W040

<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

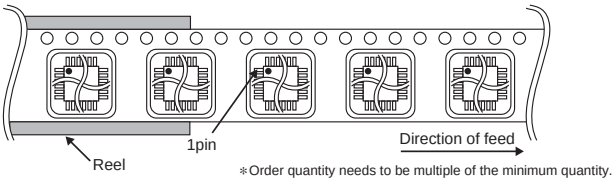


∗Order quantity needs to be multiple of the minimum quantity.

VQFP48C

<Tape and Reel information>

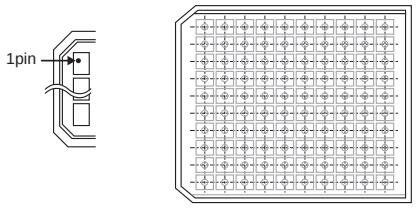
Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

<Tape and Reel information>

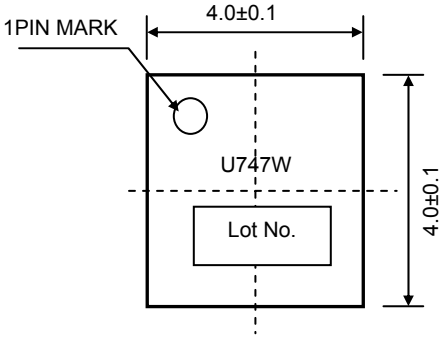
Container	Tray
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray



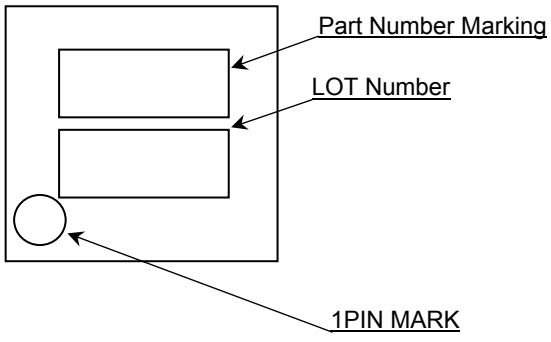
∗Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram

VBGA048W040 (TOP VIEW)



VQFP48C (TOP VIEW)



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●Revision History

Date	Revision	Changes
24.Jun.2015	001	New Release

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Notice

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1. Our Products are designed and manufactured for application in ordinary electronic equipments (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

QR code printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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