TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74AC299P, TC74AC299F

8-Bit PIPO Shift Register with Asynchronousclear

The TC74AC299 is an advanced high speed CMOS 8-BIT PIPO SHIFT REGISTER fabricated with silicon gate and double-layer metal wiring $\rm C^2MOS$ technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It has a four modes (HOLD, SHIFT LEFT, SHIFT RIGHT and LOAD DATA) controlled by the two selection inputs (S0, S1).

When one or both enable ($\overline{G1}$, $\overline{G2}$) are high, the eight I/O outputs are forced to the high-impedance state; however, sequential operation or clearing of the register is not affected.

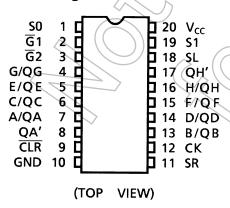
All inputs are equipped with protection circuits against static discharge or transient excess voltage.

Features (Note 1)(Note 2)

- High speed: $f_{max} = 150 \text{ MHz}$ (typ.) at $V_{CC} = 5 \text{ V}$
- Low power dissipation: $I_{CC} = 8 \mu A \text{ (max)}$ at $T_a = 25 \text{°C}$
- High noise immunity: $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (min)
- Symmetrical output impedance: $|I_{OH}| = I_{OL} = 24$ mA (min) Capability of driving 50 Ω transmission lines.
- Balanced propagation delays: t_{pLH} ≈ t_{pHL}
- Wide operating voltage range: V_{CC} (opr) = 2 to 5.5 V
- Pin and function compatible with 74F299
 - Note 1: Do not apply a signal to any bus terminal when it is in the output mode. Damage may result.

Note 2: All floating (high impedance) bus terminals must have their input levels fixed by means of pull up or pull down resistors.

Pin Assignment



DIP20-P-300-2.54A TC74AC299F SOP20-P-300-1.27A

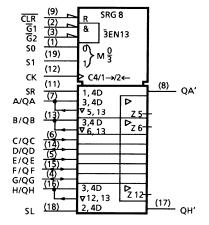
Weight

DIP20-P-300-2.54A SOP20-P-300-1.27A : 1.30 g (typ.)

: 0.22 g (typ.)

Start of commercial production 1988-05

IEC Logic Symbol



Truth Table

| Mode | Inputs | | | | | | | | < \ . | uts/ puts _ | Outputs | |
|-------|--------|--------------|----------------|--------------|--|-----|--------|-----|-------|----------------|---------|-----|
| | CLR | - I SPIECT I | | | tputs Control | | Serial | | | | -04 | |
| | | S1 | S0 | G1 (Note) | G2 (Note) | CK | SL | SR | A/QA | H/QH | QA' | QH' |
| | L | Н | Н | Х | Х | X | X | Х | Z | Z | | L |
| Clear | L | L | Х | L | L | X(| X | Х | L | (/Ľ/ | ∫) L | L |
| | L | Х | L | L | L < | (X) | X | X | (4 |)) | / L | L |
| Hold | Н | L | L | L | ١ | X | X | X | QA0 | Q H0 | QA0 | QH0 |
| Shift | Н | L | Н | L | (| 7 | Х | Н | ¥ | QGn | Н | QGn |
| Right | Н | L | Н | L | Ĺ. | | Х | , L | | QGn | L | QGn |
| Shift | Н | Н | L | L (| (L\ | | Н | X | QBn | Н | QBn | Н |
| Left | Н | Ι | L | L | Y) | | L | X | QBn | L | QBn | L |
| Load | Η | Η | Ξ ⁽ | (X)/ | \(\sigma \times \times \times \tag{\text{\tin}\text{\tetx{\text{\tetx{\text{\text{\text{\text{\text{\text{\text{\text{\text{\text{\texi}\text{\text{\text{\text{\text{\text{\texi}\text{\text{\text{\texi}\text{\text{\texi}\text{\text{\text{\text{\text{\text{\text{\texi}\text{\texi}\text{\text{\text{\texi}\text{\text{\t | | × | 1X | а | h | а | h |

Note: When one or both output controls are high, the eight input/output terminals are in the high-impedance state; however sequential or clearing of the register is not affected.

Z: High impedance

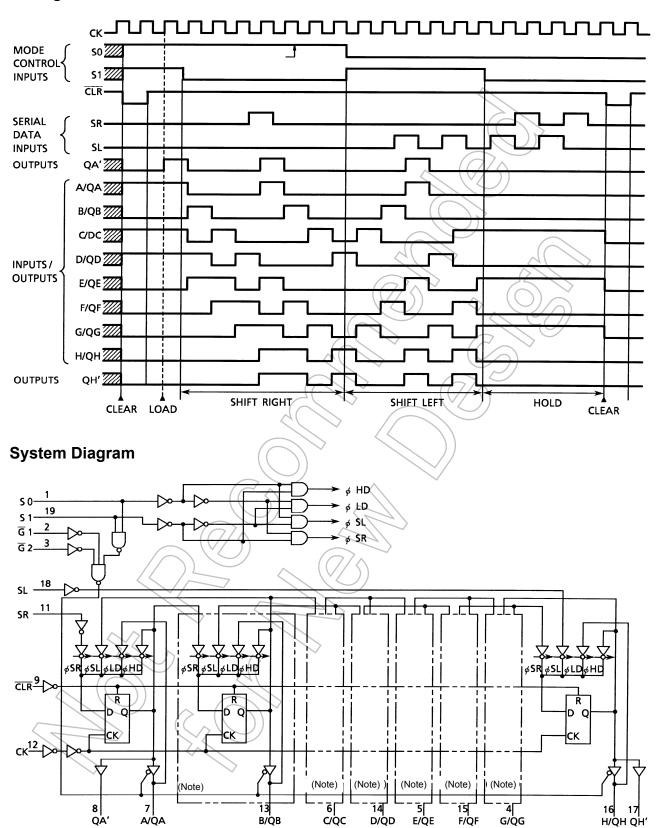
Qn0: The level of Qn before the indicated steady-state input conditions were established.

Qnn: The level of Qn before the most recent active transition indicated by \downarrow or \uparrow .

a, h: The level of the steady-state inputs A, H, respectively.

X: Don't care

Timing Chart



Note: Equivalent circuits

Absolute Maximum Ratings (Note 1)

| Characteristics | Symbol | Rating | Unit |
|------------------------------------|------------------|-------------------------------|-------|
| Supply voltage range | V _{CC} | −0.5 to 7.0 | V |
| DC input voltage | V _{IN} | -0.5 to V _{CC} + 0.5 | V |
| DC output voltage | V _{OUT} | -0.5 to V _{CC} + 0.5 | V |
| Input diode current | I _{IK} | ±20 | mA |
| Output diode current | lok | ±50 | mA |
| DC output current | lout | ±50 | mA |
| DC V _{CC} /ground current | I _{CC} | ±250 |)) mA |
| Power dissipation | PD | 500 (DIP) (Note 2)/180 (SOP) | mW |
| Storage temperature | T _{stg} | -65 to 150 | °C |

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 2: 500 mW in the range of Ta = -40 to 65°C. From Ta = 65 to 85°C a derating factor of -10 mW/°C should be applied up to 300 mW.

Operating Ranges (Note)

| Characteristics | Symbol | Rating | Unit |
|--------------------------|--------------------|---|----------|
| Supply voltage | VCC | 2:0 to 5.5 | V |
| Input voltage | // ŷ _{IN} | 0 to V _{CC} | V |
| Output voltage | Vout | 0 to V _{CC} | V |
| Operating temperature | Topr | -40 to 85 | °C |
| Input rise and fall time | dt/dV | 0 to 100 ($V_{CC} = 3.3 \pm 0.3 \text{ V}$) 0 to 20 ($V_{CC} = 5 \pm 0.5 \text{ V}$) | ns/V |

Note: The operating ranges must be maintained to ensure the normal operation of the device. Unused inputs must be tied to either V_{CC} or GND.



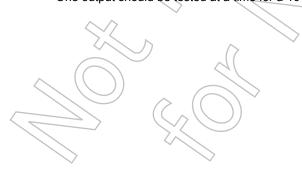
Electrical Characteristics

DC Characteristics

| Characteristics | Symbol | Test Condition V _{CC} | | 7 | Га = 25°(| | Ta = -40 to 85°C | | Unit | | |
|--------------------------|-----------------|---|----------------------------------|-----|-----------|----------|---------------------|------|---------------|-----|--|
| Ondracteristics | Cymbol | | | | Min | Тур. | Max | Min | Max | J | |
| | | | | 2.0 | 1.50 | _ ` | 1 | 1.50 | _ | | |
| High-level input voltage | V_{IH} | | _ | 3.0 | 2.10 | _ | (=) | 2.10 | _ | V | |
| 3 | | | | 5.5 | 3.85 | | | 3.85 | _ | | |
| | | | | 2.0 | _ | +0 | 0.50 | _ | 0.50 | | |
| Low-level input voltage | V_{IL} | | _ | 3.0 | | \times | 0.90 | _ | 0.90 | V | |
| | | | | 5.5 | -(| 7 | 1.65 | _ | 1.65 | | |
| | | | | 2.0 | 1.9 | 2.0 | _ | 1.9 | _ | | |
| | Voн | V _{IN} = V _{IH} or V _{IL} | $I_{OH} = -50~\mu A$ | 3.0 | 2.9 | 3.0 | _ | 2.9 | _ | | |
| High-level output | | | | 4.5 | 4.4 | 4.5 | _ | 4.4 | \rightarrow | V | |
| voltage | | | $I_{OH} = -4 \text{ mA}$ | 3.0 | 2.58 | _ | -6 | 2.48 | > — | • | |
| | | | I _{OH} = -24 mA | 4.5 | 3.94 | _\ | (| 3.80 |) — | | |
| | | | $I_{OH} = -75 \text{ mA}$ (Note) | 5.5 | _ | _ | 1 | 3.85 | _ | | |
| | | V _{IN} = V _{IH} or | | 2.0 | _ | 0.0 | 0.1 | >_ | 0.1 | - V | |
| | V _{OL} | | I _{OL} = 50 μA | 3.0 | _ | 0.0 | 0,1 | _ | 0.1 | | |
| Low-level output | | | | 4.5 | _ | 0.0 | 0.1 | _ | 0.1 | | |
| voltage | VOL | V _{IL} | $I_{OL} = 12 \text{ mA}$ | 3.0 | | | 0.36 | _ | 0.44 | | |
| | | | $I_{OL} = 24 \text{ mA}$ | 4.5 | - | /- | 0.36 | _ | 0.44 | | |
| | | | $I_{OL} = 75 \text{ mA}$ (Note) | 5.5 | _ |))— | _ | _ | 1.65 | | |
| 3-state output | I _{OZ} | $V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} \neq V_{CC}$ or GND | | 5.5 | | | .0.5 | | | ^ | |
| off-state current | | | | 5.5 | _ ~ | _ | ±0.5 | _ | ±5.0 | μА | |
| Input leakage current | I _{IN} | V _{IN} = V _{CC} or GND | | 5.5 | <u> </u> | _ | ±0.1 | _ | ±1.0 | μА | |
| Quiescent supply current | lcc | V _{IN} = V _{CC} or GND | | 5.5 | | | 8.0 | | 80.0 | μА | |

Note: This spec indicates the capability of driving 50 Ω transmission lines.

One output should be tested at a time for a 10 ms maximum duration.





Timing Recommended Operating Conditions (input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition | Ta = 25°C | Ta = -40 to 85°C | Unit | |
|----------------------|--------------------|----------------|---------------------|------------------------|-------|----|
| | | | V _{CC} (V) | Limit | Limit | |
| Minimum pulse width | t _{W (L)} | | 3.3 ± 0.3 | 8.0 | 8.0 | 20 |
| (CK) | t _{W (H)} | _ | 5.0 ± 0.5 | 5.0 | 5.0 | ns |
| Minimum pulse width | | | 3.3 ± 0.3 | 7.0 | 7.0 | |
| (CLR) | t _{W (L)} | _ | 5.0 ± 0.5 | 5.0 | 5.0 | ns |
| Minimum set-up time | | | 3.3 ± 0.3 | 6.0 | 6.0 | |
| (SL, SR, A~H) | t _s | _ (| 5.0 ± 0.5 | 4.0 | 4.0 | ns |
| Minimum set-up time | | | 3.3 ± 0.3 | 11.9 | 13.6 | |
| (S0, S1) | t _s | _ ((` | 5.0 ± 0.5 | 7.0 | 7.0 | ns |
| Minimum hold time | | | 3.3 ± 0.3 | 1.0 | 1.0 | |
| (SL, SR, A~H) | t _h | - 4(>> | 5.0 ± 0.5 | 10 | 1.0 | ns |
| Minimum hold time | | | 3.3 ± 0.3 | 0.0 | 0.0 | |
| (S0, S1) | t _h | ((// 5)) | 5.0 ± 0.5 | 0.0 | 0.0 | ns |
| Minimum removal time | | | 3.3 ± 0.3 | 5.0 | 5.0 | |
| (CLR) | t _{rem} | | 5.0 ± 0.5 | 3.0 | 3.0 | ns |

AC Characteristics (C_L = 50 pF, R_L = 500 Ω_s input: $t_r = t_f = 3$ ns)

| Characteristics | Symbol | Test Condition V _{CC} (V) | | | a = 25°0 | | Ta = - 85 | Unit | |
|-------------------------------|------------------------|------------------------------------|---------------|-----|----------|------|--------------|------|---------|
| | - J | | | Min | Тур. | Max | Min | Max | |
| Propagation delay time | t _{pLH} | | 3.3 ± 0.3 | | 10.6 | 18.4 | 1.0 | 21.0 | ns |
| (CK-QA', QH') | t_{pHL} | | 5.0 ± 0.5 | | 6.8 | 10.5 | 1.0 | 12.0 | |
| Propagation delay time | t _{pLH} | | 3.3 ± 0.3 | \ - | 8.1 | 14.0 | 1.0 | 16.0 | ns |
| (CLR -QA', QH') | t _{pHL} | 7/6 | 5.0 ± 0.5 | _ | 6.1 | 9.2 | 1.0 | 10.5 | |
| Propagation delay time | tpLH | | 3.3\± 0.3 | _ | 10.9 | 19.3 | 1.0 | 22.0 | ns |
| (CK-QA~QH) | tpHL | | 5.0 ± 0.5 | _ | 7.3 | 10.5 | 1.0 | 12.0 | |
| Propagation delay time | t _{pLH} | | 3.3 ± 0.3 | _ | 9.8 | 16.7 | 1.0 | 19.0 | ns |
| (CLR -QA~QH) | t _{pHL} | | 5.0 ± 0.5 | _ | 6.7 | 10.9 | 1.0 | 12.4 | 110 |
| Output enable time | tpZL | | 3.3 ± 0.3 | _ | 9.9 | 17.5 | 1.0 | 20.0 | ns |
| Output enable line | t _{pZH} | | 5.0 ± 0.5 | _ | 6.6 | 9.6 | 1.0 | 11.0 | 115 |
| Output disable time | t _{pLZ} | | 3.3 ± 0.3 | _ | 8.1 | 14.0 | 1.0 | 16.0 | ns |
| Catput discusse time | tpHZ | | 5.0 ± 0.5 | _ | 6.4 | 9.6 | 1.0 | 11.0 | 110 |
| Maximum clock | f _{max} | | 3.3 ± 0.3 | 45 | 90 | _ | 45 | _ | MHz |
| frequency | ımax | <u> </u> | 5.0 ± 0.5 | 80 | 140 | | 80 | _ | IVII IZ |
| Input capacitance | C _{IN} | _ | | | 5 | 10 | | 10 | pF |
| Bus input capacitance | C _{I/O} | | | _ | 13 | | _ | | pF |
| Power dissipation capacitance | C _{PD} (Note) | _ | | _ | 137 | _ | _ | _ | pF |

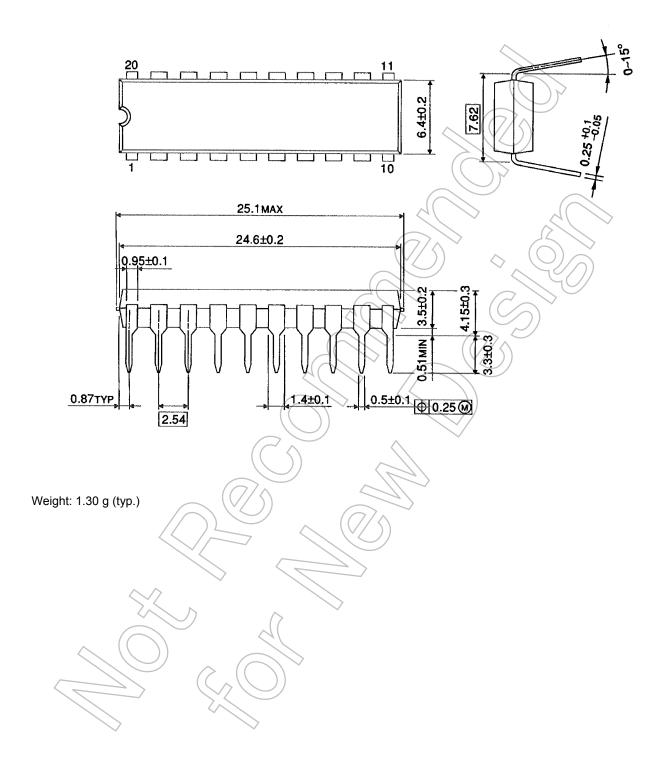
Note: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

 I_{CC} (opr) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$

Package Dimensions

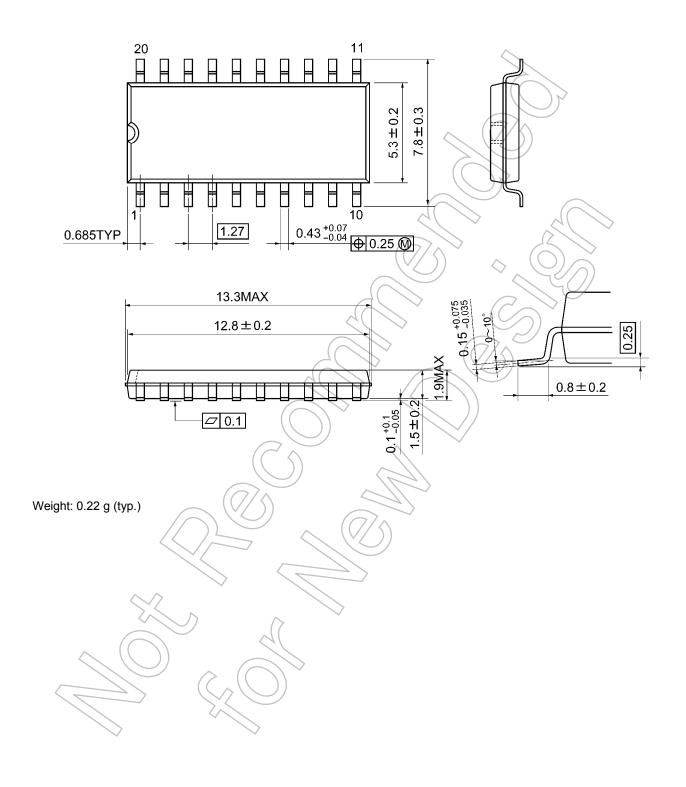
DIP20-P-300-2.54A Unit: mm





Package Dimensions

SOP20-P-300-1.27A Unit: mm



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