MOSFET – Power, Single N-Channel

40 V, 342 A, 0.81 mΩ

NTMJS0D9N04C

V$_{(BR)DSS}$	R$_{DS(ON)}$ MAX	I$_D$ MAX
40 V	0.81 mΩ @ 10 V	342 A

Features

- Small Footprint (5x6 mm) for Compact Design
- Low R$_{DS(on)}$ to Minimize Conduction Losses
- Low Q$_G$ and Capacitance to Minimize Driver Losses
- LFPAK8 Package, Industry Standard
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

LFPAK8
CASE 760AA

D (5,8)

G (4)

S (1,2,3)

N−CHANNEL MOSFET

MARKING DIAGRAM

D D D D

0D9N04
C
AWLYW

1
S S S G
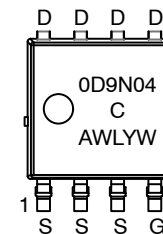
0D9N04C = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

MAXIMUM RATINGS (T$_J$ = 25°C unless otherwise noted)

Symbol	Parameter			Value	Unit
V$_{DSS}$	Drain−to−Source Voltage			40	V
V$_{GS}$	Gate−to−Source Voltage			20	V
I$_D$	Continuous Drain Current R$_{\theta JC}$ (Notes 1, 3)	Steady State	T$_C$ = 25°C	342	A
			T$_C$ = 100°C	242	
P$_D$	Power Dissipation R$_{\theta JC}$ (Note 1)		T$_C$ = 25°C	180	W
			T$_C$ = 100°C	90	
I$_D$	Continuous Drain Current R$_{\theta JA}$ (Notes 1, 2, 3)	Steady State	T$_A$ = 25°C	52	A
			T$_A$ = 100°C	37	
P$_D$	Power Dissipation R$_{\theta JA}$ (Notes 1, 2)		T$_A$ = 25°C	4.2	W
			T$_A$ = 100°C	2.1	
I$_{DM}$	Pulsed Drain Current	T$_A$ = 25°C, t$_p$ = 10 μs		900	A
T$_J$, T$_{stg}$	Operating Junction and Storage Temperature Range			−55 to +175	°C
I$_S$	Source Current (Body Diode)			150	A
E$_{AS}$	Single Pulse Drain−to−Source Avalanche Energy (I$_{L(pk)}$ = 33 A)			1945	mJ
T$_L$	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
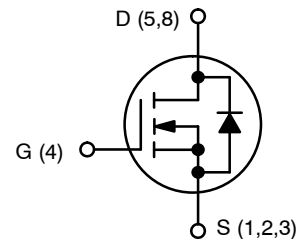
THERMAL RESISTANCE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
R$_{\theta JC}$	Junction−to−Case – Steady State	0.83	°C/W
R$_{\theta JA}$	Junction−to−Ambient – Steady State (Note 2)	35.9	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface−mounted on FR4 board using a 650 mm^2, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

Publication Order Number:
NTMJS0D9N04C/D

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain–to–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA		40			V
$V_{(BR)DSS}$/T_J	Drain–to–Source Breakdown Voltage Temperature Coefficient				14		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25 °C			10	μA
			T_J = 125°C			250	
I_{GSS}	Gate–to–Source Leakage Current	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 6)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		2.0		4.0	V
$V_{GS(TH)}$/T_J	Threshold Temperature Coefficient				7.4		mV/°C
$R_{DS(on)}$	Drain–to–Source On Resistance	V_{GS} = 10 V	I_D = 50 A		0.68	0.81	mΩ
g_{FS}	Forward Transconductance	V_{DS} =15 V, I_D = 50 A			400		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V			7400		pF
C_{OSS}	Output Capacitance				4600		
C_{RSS}	Reverse Transfer Capacitance				127		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = 10 V, V_{DS} = 32 V; I_D = 50 A			117		nC
$Q_{G(TH)}$	Threshold Gate Charge	V_{GS} = 10 V, V_{DS} = 32 V; I_D = 50 A			18		
Q_{GS}	Gate–to–Source Charge				29		
Q_{GD}	Gate–to–Drain Charge				28		
V_{GP}	Plateau Voltage				4.3		V
SWITCHING CHARACTERISTICS (Note 7)							
$t_{d(ON)}$	Turn–On Delay Time	V_{GS} = 10 V, V_{DS} = 32 V, I_D = 50 A, R_G = 2.5 Ω			20		ns
t_r	Rise Time				14		
$t_{d(OFF)}$	Turn–Off Delay Time				71		
t_f	Fall Time				26		
DRAIN–SOURCE DIODE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V, I_S = 50 A	T_J = 25°C		0.8	1.2	V
			T_J = 125°C		0.6		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, dIS/dt = 100 A/μs, I_S = 50 A			82		ns
t_a	Charge Time				54		
t_b	Discharge Time				28		
Q_{RR}	Reverse Recovery Charge				148		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
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7. Switching characteristics are independent of operating junction temperatures.

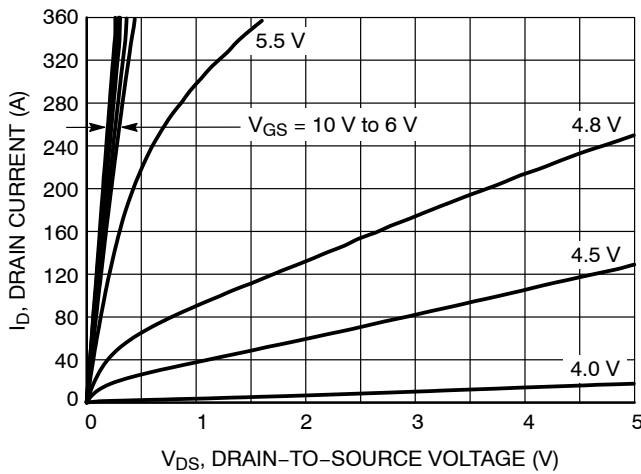## TYPICAL CHARACTERISTICS

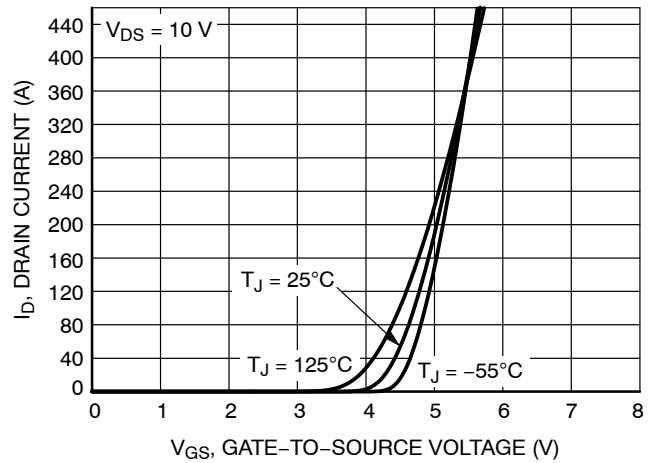Figure 1. On−Region Characteristics
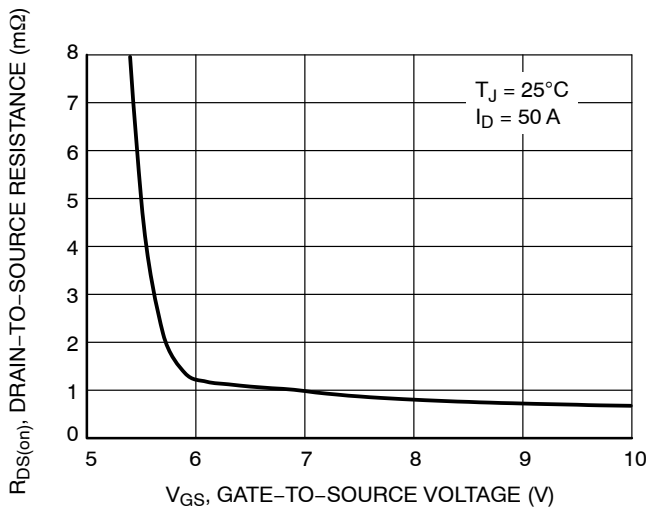

Figure 2. Transfer Characteristics

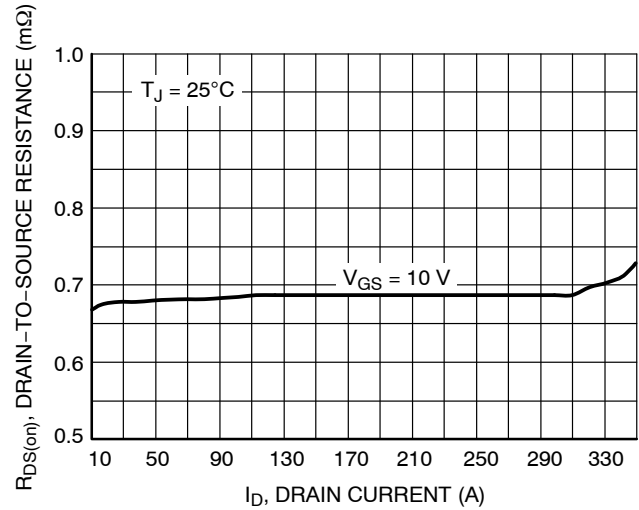Figure 3. On−Resistance vs. Gate−to−Source Voltage

Figure 4. On−Resistance vs. Drain Current and Gate Voltage
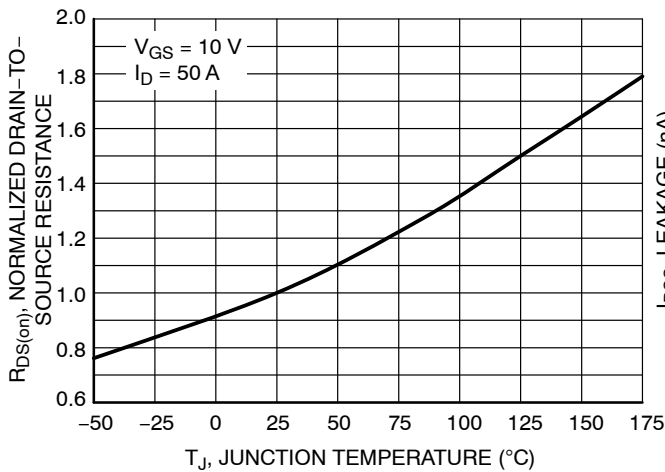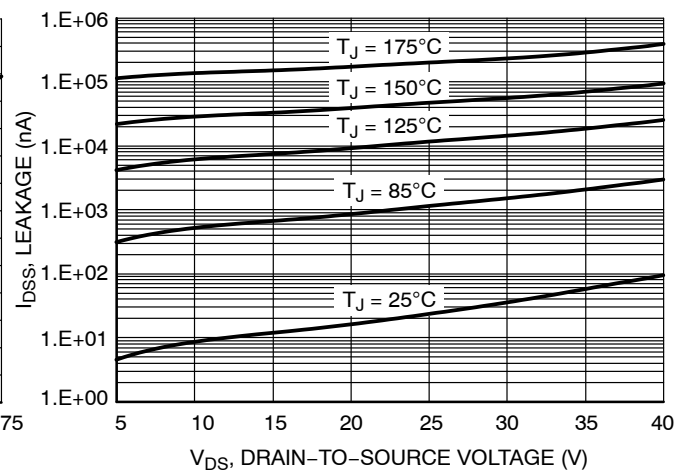

Figure 5. On−Resistance Variation with Temperature
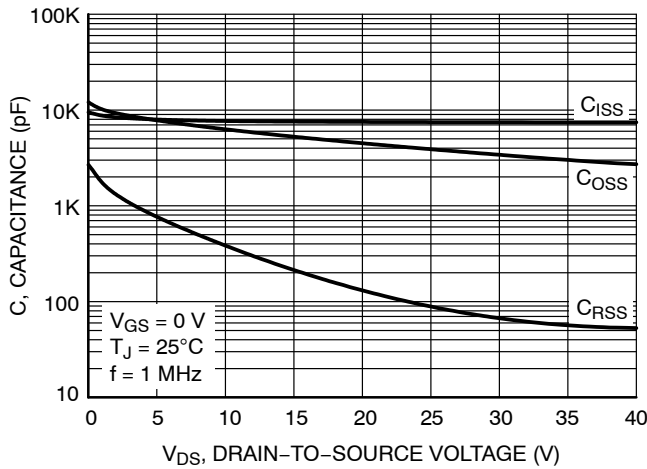

Figure 6. Drain−to−Source Leakage Current vs. Voltage

NTMJS0D9N04C

Figure 7. Capacitance Variation
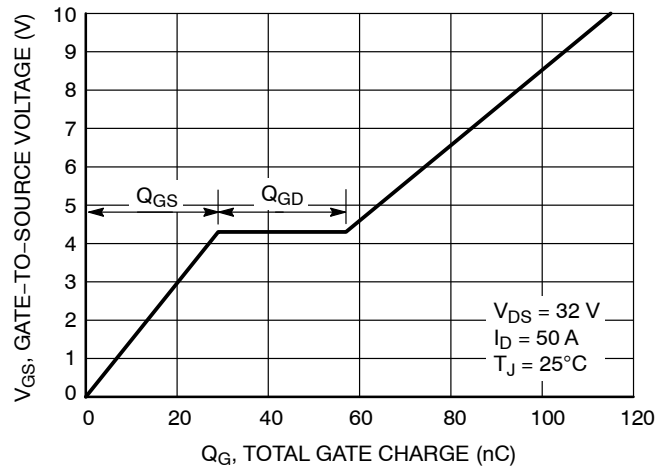
Figure 8. Gate−to−Source Voltage vs. Total Charge
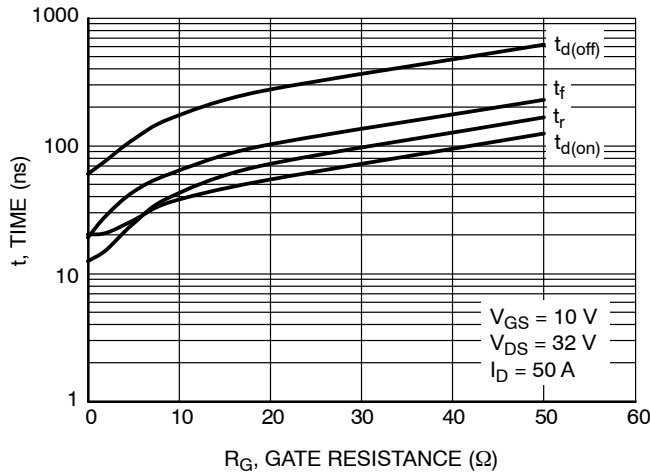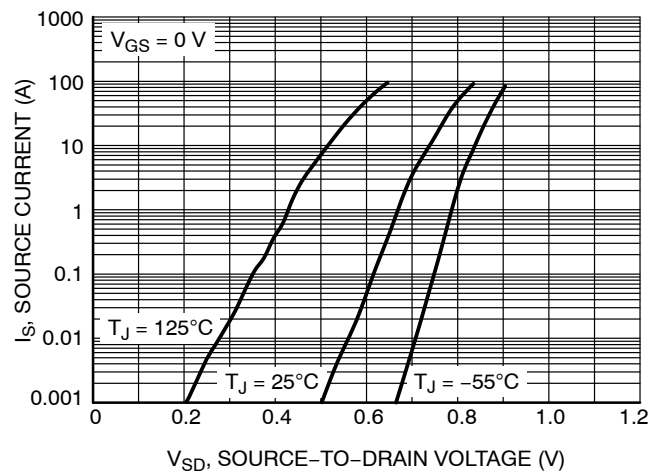

Figure 9. Resistive Switching Time Variation vs. Gate Resistance

Figure 10. Diode Forward Voltage vs. Current
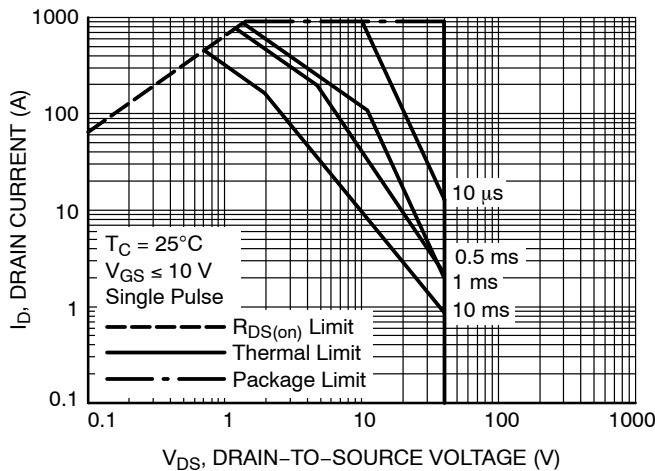
Figure 11. Maximum Rated Forward Biased Safe Operating Area
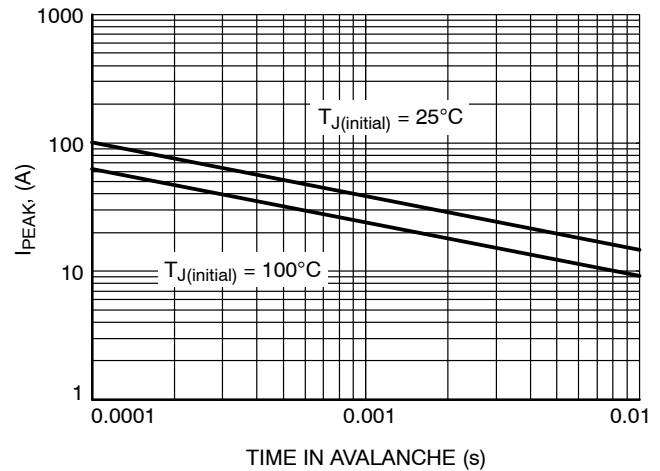
Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)
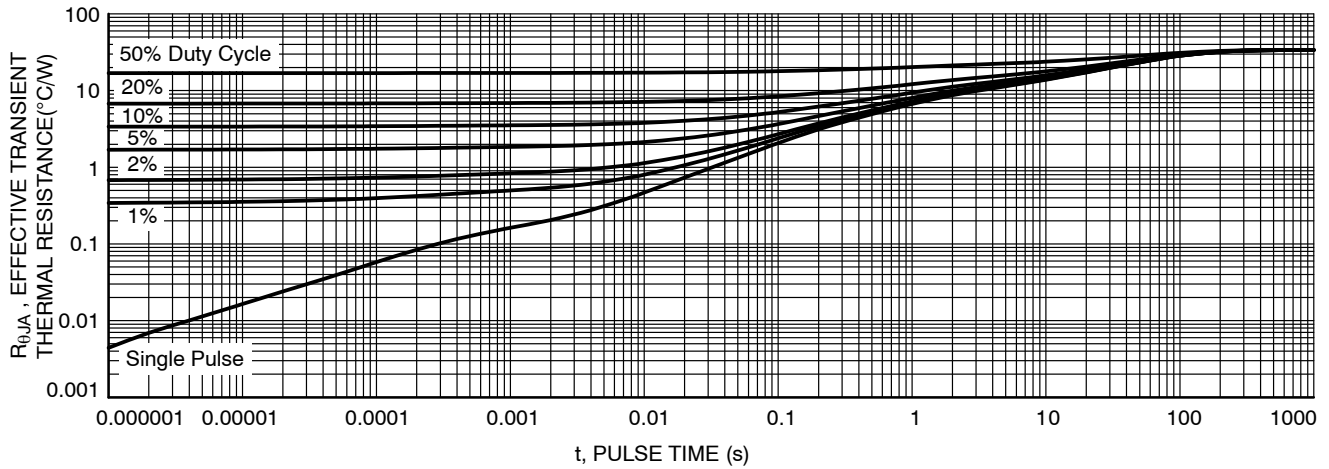
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping[†]
NTMJS0D9N04CTWG	0D9N04C	LFPAK8 (Pb−Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

LFPAK8 4.90x4.80x1.12MM, 1.27P
CASE 760AA
ISSUE D

DATE 22 APR 2024
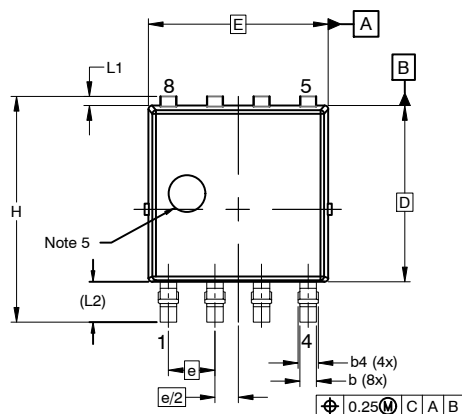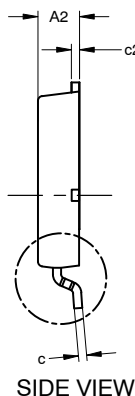
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.150mm PER SIDE.
4. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
5. OPTIONAL MOLD FEATURE.

TOP VIEW

SIDE VIEW
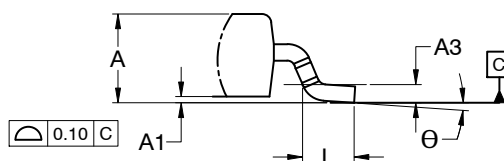
DETAIL 'A'
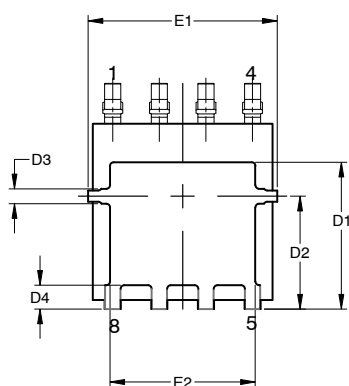
BOTTOM VIEW
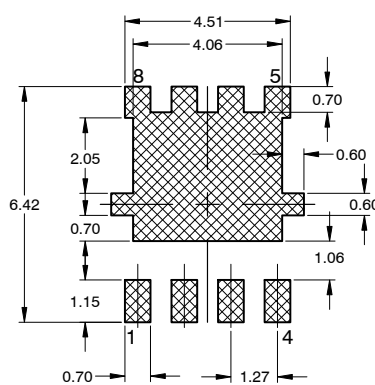
RECOMMENDED LAND PAD

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	1.10	1.20	1.30
A1	0.00	0.08	0.15
A2	1.10	1.15	1.20
A3	0.25 BSC		
b	0.40	0.45	0.50
b4	0.45	0.55	0.65
c	0.19	0.22	0.25
c2	0.19	0.22	0.25
D	4.70	4.80	4.90
D1	3.80	4.00	4.20
D2	2.98	3.08	3.18
D3	0.30	0.40	0.50
D4	0.55	0.65	0.75
E	4.80	4.90	5.00
E1	5.05	5.15	5.25
E2	3.91	3.96	4.01
e	1.27 BSC		
e/2	0.635 BSC		
H	6.00	6.15	6.30
L	0.50	0.70	0.90
L1	0.15	0.25	0.35
L2	1.10 REF		
Θ	0°	4°	8°

*FOR ADDITIONAL INFORMATION ON OUR PB–FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*
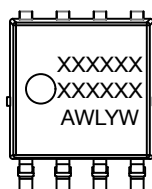
XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98AON82475G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	LFPAK8 4.90x4.80x1.12MM, 1.27P		PAGE 1 OF 1

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical–documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
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