XENSIV™ Battery pack current, voltage and temperature sensor

Key benefits & features

The benefits and features of XENSIV™ AS8512 are listed below:

Table 1 Added value of using AS8512

Benefits	Features
Low supply voltage	3.3 V supply voltage
Redundant measurement possibility	Two high resolution 16-bit Σ - Δ A/D converters
Flexible configuration	Programmable sampling to enable data throughputs from less than 1 Hz to 8 kHz
Unique measurement principle	Zero offset for both channels

- Precision, low noise, programmable gain amplifiers for both channels with gains 5, 25, 40, 100 to support wide dynamic ranges.
- Option for multiplexing either one differential input, or two single ended inputs or the internal temperature sensor on one channel.
- Programmable current source for external temperature sensor connectable to any of the inputs.
- High precision and high stability 1.2 V reference voltage source.
- Digital signal processing with filter options for both channels.
- Four operating modes providing
  - Continuous data acquisition (or)
  - Periodic single-shot acquisition, (or)
  - Continuous acquisition on threshold crossing of programmed current levels (or)
  - A combination of the above
- On chip high-precision 4 MHz RC oscillator or option for external clock.
- –40°C to 105°C ambient operation.
- Chip ID feature
- SSOP-20 pin package.

Applications

The AS8512 is ideal for shunt based batteries sensor - Battery pack current, voltage & temperature measurement.

General description

The AS8512 is a virtually offset free, low noise, two channel measurement device. It is tailored to accurately measure battery current from mA range up to kA range in conjunction with a 100 µΩ shunt resistor in series with the battery rail. Through the second measurement channel it enables capture of, either battery voltage synchronous with the current measurement, or, measure the analog output of an internal or external temperature sensor. Both channels are matched and can either measure small signals up to ±160 mV versus ground, through programmable gain amplifier or larger signals in the 0 to 1 V range without the amplifier.

After analog to digital conversion and filtering, the resulting 16-bit data is accessible via 4-wire standard serial interface (SPI).

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1 Block diagram

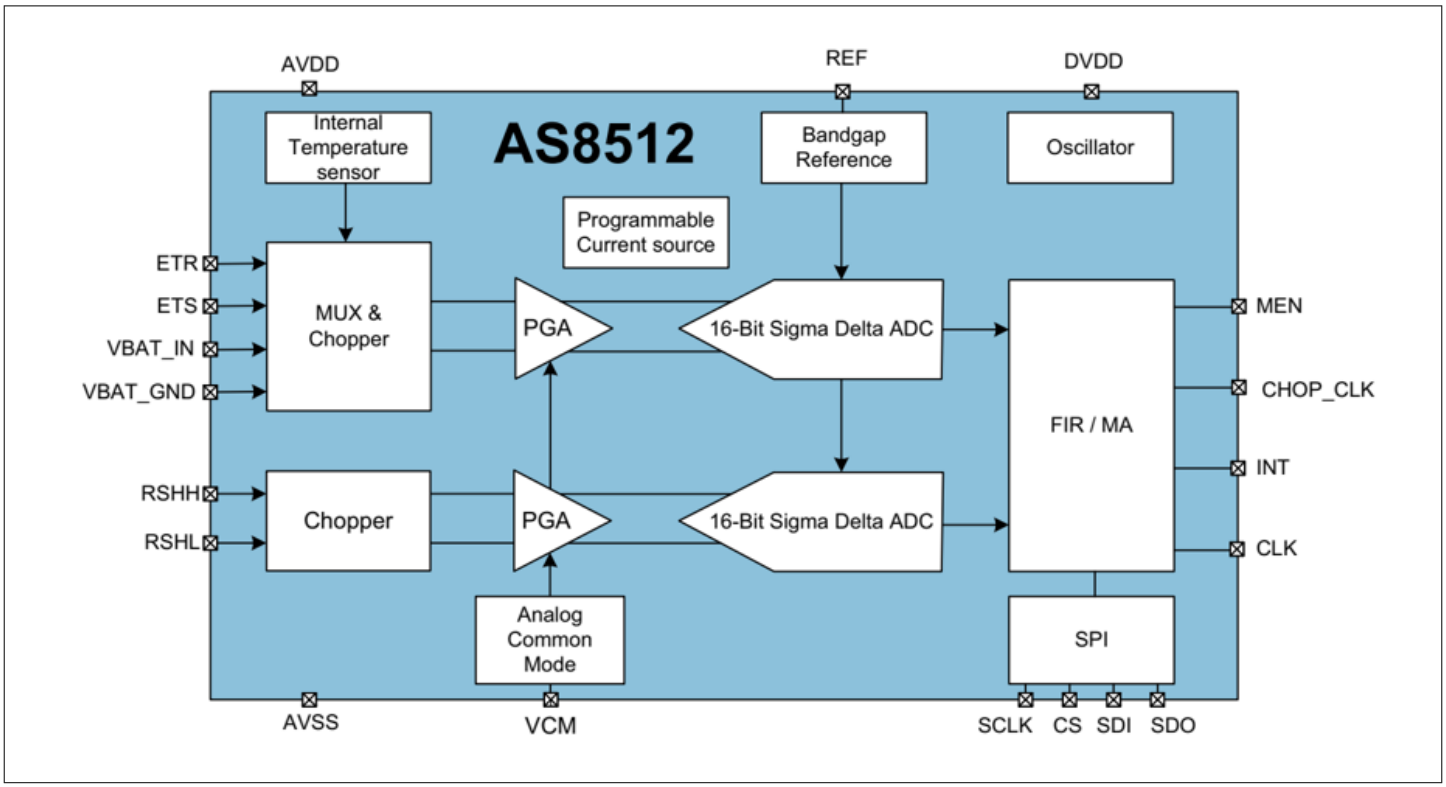


Figure 1 AS8512 block diagram

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2 Ordering information

Product type (Infineon)	Product type (ams)	Description	Ordering code	Delivery form	Package
AS8512-ZSSP-SSOP20	AS8512-ZSSP	Data acquisition device for battery sensors	SP006309807	Tape and reel (2000 pcs)	20-pin SSOP
AS8512-ZSSM-SSOP20	AS8512-ZSSM	Data acquisition device for battery sensors	SP006309809	Tape and reel (500 pcs)	20-pin SSOP

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3 Pin assignments

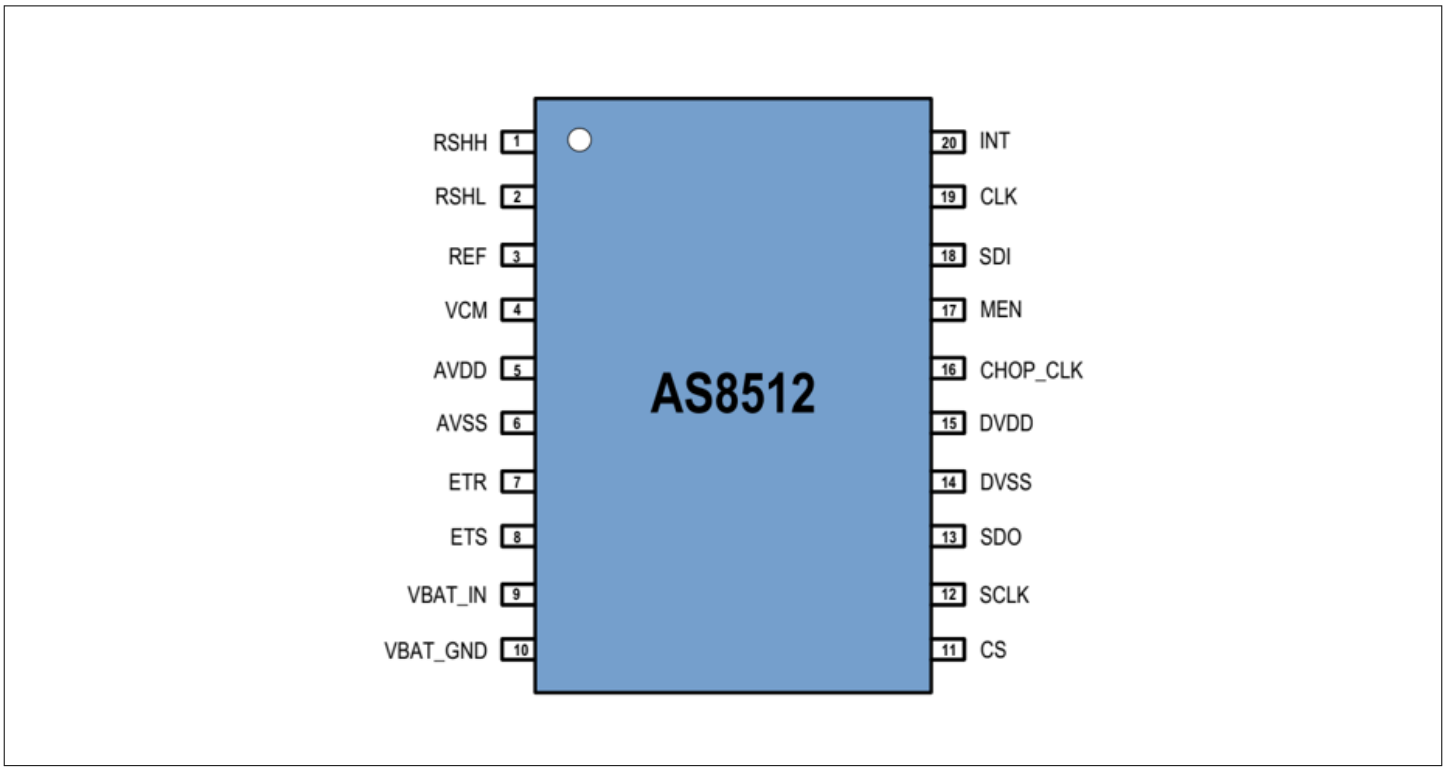


Figure 2 Pin assignment of AS8512 (Top view)

3.1 Pin descriptions

Table 2 Pin description of AS8512

Pin number	Pin name	Pin type	Description
1	RSHH	Analog input	Positive differential input for current channel
2	RSHL		Negative differential input for current channel
3	REF	Analog output	Internal reference voltage to sigma-delta ADC; connect 100 nF to AVSS from this pin.
4	VCM		Common mode voltage to the internal measurement path; connect 100 nF to AVSS from this pin.
5	AVDD	Supply pad	+3.3 V analog power-supply
6	AVSS		0 V power-supply analog
7	ETR	Analog input	Voltage channel single ended input
8	ETS		
9	VBAT_IN		Battery voltage (high) input
10	VBAT_GND		Battery voltage (low) input
11	CS	Digital input with pull-up	Chip select with an internal pull-up resistor (SPI Interface)
12	SCLK	Digital input	Clock signal (SPI Interface)

(table continues...)

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Table 2 (continued) Pin description of AS8512

Pin number	Pin name	Pin type	Description
13	SDO	Digital output	Serial data input (SPI Interface)
14	DVSS	Supply pad	0 V digital ground
15	DVDD		+3.3 V digital supply
16	CHOP_CLK	Digital output	Chop clock used in High side measurements to synchronize external chopper.
17	MEN		Digital output issued during the Standby Mode (SBM) to signal the short duration of data sampling. This signal is useful in the case of a High Side Measurement application.
18	SDI	Digital input	Data signal (SPI Interface)
19	CLK	Digital I/O	By default this pin is the internal clock output which can be used by a microcontroller. The internal clock may also be disabled as an output by programming Register 08. To use an external Clock, Register 08 has to be programmed.
20	INT	Digital output	Active high Interrupt to indicate data is ready

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4 Absolute maximum ratings

Stresses beyond those listed in Table 3 may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in Electrical characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 3 Absolute maximum ratings

Parameter	Min.	Max.	Units	Notes
Electrical parameters				
DC supply voltage (AVDD and DVDD)	–0.3	5	V	
Input voltage (V_{IN})	–0.3	AVDD + 0.3 DVDD + 0.3	V	
Input current (latchup immunity) (I_{SCR})	–100	100	mA	
Electrostatic discharge				
Electrostatic discharge (ESD) all pins	±2		kV	
Continuous power dissipation				
Total power dissipation (all supplies and outputs) (P_t)		50	mW	SSOP20 in still air, soldered on JEDEC standard board @ 105°C ambient, static operation with no time limit
Temperature ranges and storage conditions				
Storage temperature (T_{STRG})	–50	105	°C	
Junction temperature (T_J)		110	°C	
Thermal resistance (R_{th}JC)		80	K/W	JEDEC standard test board, 0 air velocity
Package body temperature (T_{BODY})		260	°C	IPC/JEDEC J-STD-020[1)]
Moisture sensitivity level (MSL)	3			
Humidity non-condensing	5	85	%	

1) The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 “Moisture/Reflow Sensitivity Classification for Non-hermetic Solid State Surface Mount Devices”.

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5 Electrical characteristics

5.1 Operating conditions

Table 4 Operating conditions

Symbol	Parameter	Conditions	Min.	Max.	Units
AVDD	Positive analog supply voltage		3.0	3.6	V
AVSS	0 V ground		0	0	V
A - D	Difference in analog and digital supplies			0.1	V
DVDD	Positive digital supply		2.97	3.63	V
DVSS	0 V digital ground		0	0	V
T_{AMB}	Ambient temperature		–40	105	°C
I_{SUPP}	Supply current			5.5	mA
f_{CLK}	System clock frequency [1)]			4.096	MHz

1) Nominal clock frequency from external or internal oscillator.

5.2 DC/AC characteristics for digital inputs and outputs

All pull-up and pull-down have been implemented with active devices. SDO has been measured with 10 pF load.

Table 5 INT

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{LEAK}	Tri-state leakage current		–1		+1	µA
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				4	mA

Table 6 CS input

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{LEAK}	Input leakage current		–1		+1	µA
I_{pu}	Pull up current	CS pulled to DV_{DD} = 3.3 V	–150		–15	µA

Table 7 SDI

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage		2.0			V
V_{IL}	Low level input voltage				0.8	V
I_{LEAK}	Input leakage current		–1		+1	µA

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Table 8 SDO output

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	High level output voltage	Isource = 8 mA	2.5			V
V_{OL}	Low level output voltage	Isink = 8 mA			0.4	V
I_O	Output current				8	mA

Table 9 CHOP_CLK output

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				4	mA

Table 10 CLK I/O with input schmitt trigger and output buffer

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage	DVDD = 3.3 V	2.4			V
V_{IL}	Low level input voltage	DVDD = 3.3 V			1.0	V
I_{LEAK}	Input leakage current		–1		+1	µA
I_{PD}	Pull down current	CLK pulled to DVSS	10		100	µA
I_O	Output current				4	mA
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V

Table 11 SCLK with input schmitt trigger

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High level input voltage	DVDD = 3.3 V	2.4			V
V_{IL}	Low level input voltage	DVDD = 3.3 V			1.0	V
I_{LEAK}	Input leakage current		–1		+1	µA

Table 12 MEN output

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OH}	High level output voltage		2.5			V
V_{OL}	Low level output voltage				0.4	V
I_O	Output current				2	mA

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5.3 Detailed system and block specifications

5.3.1 Electrical system specifications

Table 13 Electrical system specifications

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
IDD_{NOM}	Current consumption normal mode		3	5.5	mA	
IDD_{SBM}	Current consumption standby mode		40		µA	Average of NORMAL Mode Power consumption over a period of 10s when the device is in STANDBY Mode

5.4 Current measurement ranges (across 100µOhm shunt resistor)

Table 14 Current measurement ranges

Symbol	Parameter	I_{max} [A]	V_{sh} [mV]	PGA gain nominal	Data rate (f_{OUT})	V_{INADC} [1] [mV]	PSR [2] [dB]
I70	Input current range of 70 A in NOM	±77	±8.1	100	@ 1 kHz	890	60
I200	Input current range of 200 A in NOM	±235	±24.7	40	@ 1 kHz	1088	60
I400	Input current range of 400 A in NOM	±400	±42	25	@ 1 kHz	1137	60
I1500	Input current range of 1500 A in NOM	+2076/ –1523	+218/–160	5	@ 1 kHz	1204	60

1) $V_{INADC} = V_{sh} * Gain$, gain deviations to be considered according to Table 15 and Table 16.
2) AVDD, DVDD of 3.3 V with ±5% variation.

The maximum current range can be calculated by the equation:

$$I_{max} = (VREF_{min} - V_{OSDRIFT} * Gn * e)/(Gn * e * R_{SHUNT})$$

Where,

$VREF_{min}$ is minimum ADC reference voltage for the anticipated temperature range e.g. 1220 mV

$V_{OSDRIFT}$ is the maximum input referred PGA offset (e.g. 3 mV)

Gn is the nominal gain as selected (G1 to G4)

e is maximum gain tolerance (1,1)

R_{SHUNT} is the maximum shunt resistance

Exceeding this maximum current range will lead first to non-linearity and finally to clamping.

***Note**: The Data Rate at the output can be calculated according to the formula:*

$$f_{sout} = 2 * fchop/R2$$

(R2 is down sampling ratio taking values 1, 2, 4 up to 32768 as powers of 2)

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Table 15 Valid combinations of the chopper clock, oversampling clock and decimation ratios

Over sampling frequency	Chopper frequency	Decimation ratio
1.024 MHz	2 kHz	64
2.048 MHz	2 kHz	64
2.048 MHz	2 kHz	128
2.048 MHz	4 kHz	64

Table 16 Differential input amplifier for current channel

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN_AMP}	Input voltage range	RSHH and RSHL	–160		+160	mV
I_{IN_AMP}	Input current [1) 2)]	RSHH and RSHL@ + 160 mV input voltage at 105°C with PGA	–50	2	50	nA
ICM	Absolute input voltage range [3)]			–160 +300		mV
G = G1	Gain1 [4) 5) 6)]	I10		100		
G = G2	Gain2 [4) 5) 6)]	I200		40		
G = G3	Gain3 [4) 5) 6)]	I400		25		
G = G4	Gain4 [4) 5) 6)]	I1500		5		
e	Gain deviation	I = 1,2,3,4	0.9*Gi		1.1*Gi	
f_{p_AMP}	Pole frequency [5) 7)]		15			kHz
εT1	Gain drift with temperature [8)]	–20°C to 65°C Gain 5, 25, referenced to room temperature			±0.5	%
V_{os}	Input referred offset [9) 10)]	@ 65°C		350	2700	µV
		After trim at –20°C			420	µV
V_{os_ch}	Measurement path off-set [9) 10)]	Chopping enabled		0		LSB
V_{Ndin}	Noise density [5) 11)]			25		nV / √ Hz
THD	Total harmonic distortion	For 150 Hz input signal		70		dB

1) Leakage test accuracy is limited by tester resource accuracy and tester hardware.
2) For negative input voltages up to –160 mV below ground, Input leakage is typically –20 nA @ 65°C due to forward conductance of protection diode.
3) For gain 100 PGA input common mode is 0V and the minimum supply is 3.15V.
4) The measurement ranges are referred only by the gain of input amplifier, while other parameters such as bandwidth etc. are programmed independently.
5) This parameter is not measured directly in production. It is measured indirectly via gain measurements of the whole path. It is guaranteed by design.
6) Refer to measurement ranges shown in Table 14.
7) Pole frequency of input amplifier changes with GAIN. The number is valid for the gain at G1, while the bandwidth will be higher for other ranges. This parameter is not measured in production.
8) Based on device evaluation. Not tested.
9) These offsets are cancelled if chopping enabled (default).

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10) No impact on the measurement path. If the chopping is enabled, both the offset and offset drift will be eliminated.
11) Noise density calculated by taking system bandwidth as 150 Hz.

5.4.1 Differential input amplifier for voltage channel

Table 17 Differential input amplifier for voltage channel

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN_AMP}	Input voltage range[1) 2)]		–160		+160	mV
I_{IN_AMP}	Input current [3) 2)]	VBAT_IN, ETR, ETS @ +160 mV input voltage at 105°C with PGA	–50	2	50	nA
ICM	Absolute input voltage range[4)]			-160 +300		mV
G = G1	Gain1[5) 6)]			100		
G = G2	Gain2 [5) 6)]			40		
G = G3	Gain3 [5) 6)]			25		
G = G4	Gain4 [5) 6)]			5		
e	Gain deviation	I = 1,2,3,4	0.9*Gi		1.1*Gi	
f_{p_AMP}	Pole frequency [6) 7)]		15			kHz
V_{NDIN}	Noise density[6) 8)]			25		nV / √ Hz
THD	Total harmonic distortion	For 150 Hz input signal		70		dB
εT1	Gain drift with temperature[9)]	–20°C to 65°C Gain 5, 25, referenced to room temperature			±0.5	%
V_{os}	Input referred offset[10)]	After trim at –20°C			420	µV
		@65°C		350	2700	µV
V_{os_ch}	Measurement path off-set[10)]	Chopping enabled		0		LSB

1) Input for the voltage channel can be as high as 1220 mV, in this high input case PGA will be bypassed.
2) For negative input voltages up to -160 mV below ground, Input leakage is typically -20 nA @ 65°C due to forward conductance of protection diode.
3) Leakage test accuracy is limited by tester resource accuracy and tester hardware, especially at low temperatures due to condensing moisture.
4) For gain 100 PGA input common mode is 0V and the minimum supply is 3.15 V.
5) The measurement ranges are referred only by the gain of input amplifier, while other parameters such as bandwidth etc. are programmed independently.
6) This parameter is not measured directly in production. It is measured indirectly via gain measurements of the whole path. It is guaranteed by design.
7) Pole frequency of input amplifier changes with changing the GAIN. The number is valid for the gain at G1, while the bandwidth will be higher for other ranges. This parameter is not measured in production.
8) Noise density calculated by taking system bandwidth as 150 Hz.
9) Based on device evaluation. Not tested.
10) No impact on the measurement path. If the chopping is enabled, both the offset and offset drift will be eliminated.

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5.4.2 Sigma delta analog to digital converter

Table 18 Sigma delta analog to digital converter

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VREF	Reference voltage [1]			1.225		V
V_{INADC}	Input range [2]	At V_{ref} = 1.22V	0		±1.22	V
R1	Oversampling ratio/Decimation ratio [3]		64	128	128	
f_{ovs}	Oversampling frequency [4]			1024/ 2048		kHz
RES	Number of bits				16	bits
BW	Bandwidth [5]		1		500	Hz
S/N	Signal to noise ratio[6]			90		dB

1) Reference voltage might be forced from external.
2) Production test at ±800 mV. Maximum VIN can be 1.22 V with VREF = 1.225 V.
3) Programmable. It is defined with respect to the first decimator in the ΣΔ ADC.
4) Programmable: Internal clock is 1024/2048 kHz; external clock max is 8192 kHz.
5) Dependent on fovs, R1 and R2. The bandwidth is calculated according to the formula:
BW = fovs/(2*R1*R2); the sampling frequency at the output of the A/D converter is 2*BW.
6) Defined at maximum input signal, BW=500 Hz (1Hz to 500 Hz), fovs = 1024 kHz, R1 = 64, fchop = 2 kHz and R2 = 2.

5.4.3 Bandgap reference voltage

Table 19 Bandgap reference voltage

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{REFTRIM}$	Reference voltage after trim [1] [2]	Trim at 65°C		1.225		V
V_{REFACC}	Reference voltage initial accuracy [1] [2]	At 65°C			±3.5	mV
$V_{REFDRIFT}$	Reference voltage temperature drift	Temperature range –40°C to 105°C		+0.4/ –0.6		%
$PSRR_{REF}$	PSR @ dc			80		dB
SUT_{AVDD}	Start up time with supply ramp[3]			5		ms
SUT_{PD}	Start up time from power down[3]				1	ms
R_{NDVREF}	Output resistance of band gap			500	1000	Ω
V_{NDVREF}	Bandgap reference thermal noise density [3]				300	nV/ √ Hz
CL_{VREF}	Output capacitor (ceramic)			100		nF
ESR_{VREF}			0.02		1	Ω

1) Accuracy at 65°C.
2) No DC current is allowed from this pin.
3) This is a design parameter and not production tested.

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5.4.4 Internal (programmable) current source for external temperature measurement

Table 20 External temperature measurement

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I_{CURON}	5-bit current source enabled[1]	5-bit programmable current source	0	270	320	µA
I_{CUROFF}	5-bit current source disabled	Limited by leakage		10		nA
T_{K_CS}	Temperature coefficient of current source [2]			1000		ppm / °K
V_{MAXETR}	Voltage on pin ETR[3]				1000/ G	mV
$V_{MAXETRMOD}$	Max. voltage on pin ETR when PGA is bypassed[4]				1.22	V
V_{MAXETS}	Voltage on pin ETS for resistor sensor [3]				1000/ G	V
$V_{MAXETSMOD}$	Max. voltage on pin ETS when PGA is bypassed[5]				1.22	V

1) Current value can be programmed in steps of 8 µA from 0 to 256 µA with a process error of 30%.
2) Temperature coefficient is not important since external temperature measurement is a 2 step measurement. The value specified is guaranteed by design and will not be tested in production.
3) Maximum voltage on pin ETR (reference) can be calculated by given formula, where G is the gain of PGA (G=100).
4) Maximum voltage on pin ETR, if PGA is bypassed.
5) Maximum voltage on pin ETS, if PGA is bypassed.

5.4.5 CMREF circuit (VCM)

Table 21 CMREF circuit

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{VCM}	Output voltage	1.6	1.7	1.8	V
C_L	Load capacitance		100		nF

5.4.6 Internal AVDD power-on reset

Table 22 Internal AVDD power-on reset

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORHIA}	Power On reset threshold	2.2	2.4	2.6	V
t_{PORA}	POR time - The duration from power ON till the time, internal Power On reset signal goes HIGH[1]	1			µs
I_{PORA}	Current consumption in POR block[2]		1.5		µA

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1) POR pulse is always longer than t_{PORA} whatever the slope of the supply.
2) I_{PORA} can not be switched off.

5.4.7 Internal DVDD power-on reset

Table 23 Internal DVDD power-on reset

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{PORHID}	Power On reset threshold	2.2	2.4	2.7	V
V_{HYST}	Hysteresis[1)]	0.2	0.25	0.4	V
t_{PORD}	POR time - The duration from power ON till the time, internal power On reset signal goes HIGH	1			µs
I_{PORD}	Current[2)]		1.5		µA

1) $V_{PORLO} = V_{PORHI} - V_{HYST}$ where V_{PORLO} is the lower threshold of POR.
2) I_{PORD} can not be switched off.

5.4.8 Low speed oscillator

Table 24 Low speed oscillator

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{LS}	Frequency		262.144		kHz
f_{LS_ACC}	Accuracy		± 7		%
I_{LS}	Supply current		5		µA

5.4.9 High speed oscillator

Table 25 High speed oscillator

Symbol	Parameter	Min.	Typ.	Max.	Units
f_{HS}	Frequency		4.096		MHz
f_{HSACC}	Accuracy [1) 2)]		±4		%
I_{HS}	Supply current		300		µA

1) Accuracy after trimming.
2) Accuracy for limited temperature range of –20°C to 65°C.

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5.4.10 External clock

Table 26 External clock

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_{CLKEXT}	Clock frequency			2048/ 4096/ 8192		kHz
DIV_{CLKEXT}	Clock division factor	To be programmed in Register 08 CLK_REG through the serial bus SPI.		2/4/8		
DC_{CLKEXT}	Duty cycle of external clock		40		60	%

5.4.11 Internal temperature sensor

Table 27 Internal temperature sensor

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
T_{INTRNG}	Temperature sensor range		–40		105	°C
Δ_{TIN}	Temperature measurement accuracy			3		°C
T_{INTSLP}	Temperature sensor slope	Guaranteed by design; at PGA gain 5 which is the recommended gain for internal temperature measurement.		27		Digits/°C
$T_{INT}65_G5$	Temperature sensor output at gain 5		40660	41807	43012	Digits

5.5 System specifications

Table 28 System specifications

Symbol	Parameter	Min.	Typ.	Max.	Units
I_S	Channel to channel isolation[1)]			–90	dB
At	Difference in channel to channel attenuation @600 Hz [1) 2)]			3	dB
Ph	Difference in phase shift between the two channels @600 Hz[1) 2)]			5	deg

1) These specifications are defined by taking one channel as reference and measured on the other channel.
2) Guaranteed by design.

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System measurement error budget for voltage and current channel

Temperature Range: –20°C to 65°C; Output data rate is 1 kHz, VCC = 3.3 V, chopping enabled.

Table 29 System measurement error budget for gains 5 and 25

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
Err	System measurement error [1) 2)]			±0.5	±1.0	%
	Voltage channel signal path measurement error [3)]				±0.5	
	Measurement error due to PGA gain drift				±0.5	%
	Measurement error due to V_{REF} drift				±0.4	%
	Measurement error due to non-linearity of PGA			±0.025		%

1) System measurement error due to noise, individual block parameter drifts and non linearity. Based on evaluation, not tested
2) System error due to offset is neglected because of chopper architecture.
3) PGA is by-passed.

System error compensation function: For battery voltage measurement it is recommended to by-pass the PGA. This eliminates PGA gain drift as an error source, thus error for the VBAT/ VBAT_GND differential signal path is determined by VREF drift with temperature. The typical characteristic of VREF versus temperature extracted from 3 production lots is shown in Figure 3. This function could be used to improve accuracy by an error correction method utilizing the internal temperature sensor. In this case ADC raw data readings need to be corrected with a temperature dependent factor by the software in the external micro controller. This factor is given by a generic compensation function and can be applied to all IC's because VREF is production trimmed to minimize linear coefficient of VREF over temperature.

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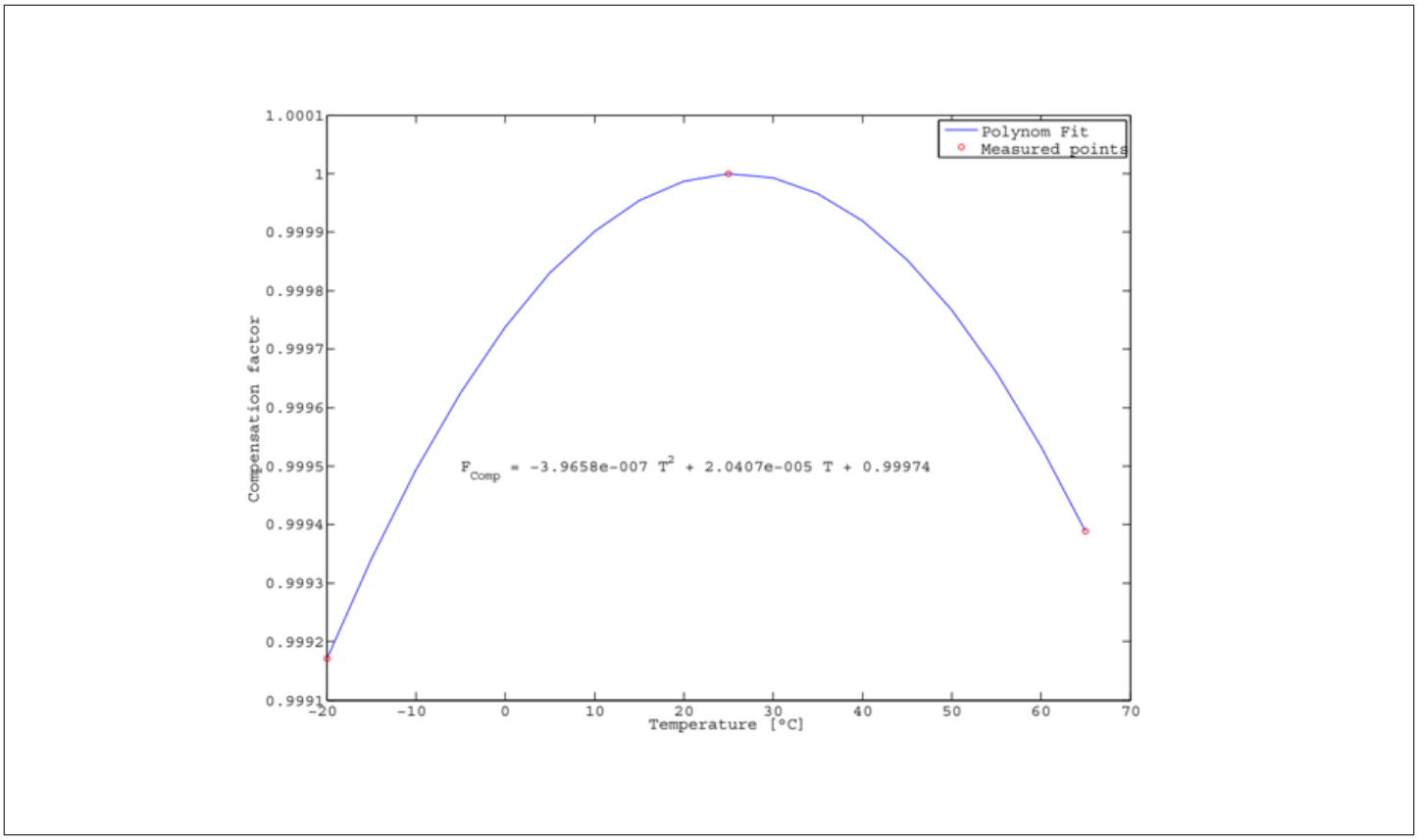


Figure 3 Reference error compensation function

Generic compensation factor the ADC output need to be multiplied with:

F_{comp} = (A*T^2 + B*T + C)

Where:

F_{comp} is the compensation factor for VREF drift over temperature normalized to 1 at 25°C

T is Temperature reading from calibrated internal temperature sensor in [°C]

A: –4E–7

B: 2E–5

C: 0.9997

The compensated ADC value = raw ADC value * F_{comp}

If PGA is by-passed and an external precision reference is applied, the signal path measurement error is basically determined by the drift due to temperature and ageing of the external reference.

Current channel error contributions for a single temperature end of line calibrated system are shunt resistance, PGA gain and VREF changes with temperature. The drift of a shunt resistor made from Manganin alloy and VREF drift with temperature are non-linear and show 2nd order curvature in same direction and similar relative magnitude. Thus shunt error is already reduced by the generic VREF(T) curvature (see Figure 3) if thermally coupled to the AS8512. Over all error can be further reduced by an error correction method in external micro controller by matching typical VREF(T) curvature to R_{shunt} (T) curvature with the help of the internal temperature sensor.

Temperature sensor system considerations: Internal temperature sensor can be used to measure the ambient temperature because there is just 13 mW of AS8512 power dissipation in normal mode. This results in internal self-heating of less than 1°C.

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6 Detailed description

The AS8512 consists of two independent high resolution 16-bit SD analog to digital conversion channels. The measurement path of these two channels integrates a programmable gain amplifier, chopper and de-chopper, sigma-delta modulator, decimator and a digital filter for simultaneous measurement of Current and Voltage/Temperature.

The two measurement channels, namely the Current and Voltage/Temperature measurement channels have identical data path.

The input signal is amplified in the Programmable Gain Amplifier (PGA) with any of the selected gains of 1, 5, 25, 40 and 100 facilitating measurement of a wide range of Current, voltage and temperature levels. Gain Settings for different input ranges and any associated restrictions are explained in the Table 14.

Offset in the measurement path is minimized with the use of a chopper and a de-chopper at appropriate stages in the data path. By default the chopper/de-chopper is ON in the measurement path. It may be disabled by programming the appropriate register.

The amplified input signal is converted into a single-bit pulse-density modulated stream by the Σ -Δ Modulator. A decimator acting as a low-pass filter filters out the quantization noise and generates 16-bit data corresponding to the input signal. The decimation ratios of 64, 128 may be selected in the first filter stage. For reducing data rate further, the second stage decimation can be used.

An optional FIR Filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems.

6.1 Current measurement channel

The voltage across a Shunt Resistor, connected in series with the Battery negative terminal, forms the input signal to the Current Measurement channel. RSHH and RSHL are the Current measurement input pins. Offset in the input signal is nullified with the use of a chopper and a de-chopper at appropriate stages in the data path. The programmable gain amplifier in the data path with programmable settings of 1, 5, 25, 40 and 100 enables measurement of current ranges from ± 1 A to ± 1500 A. The sampled input signal is converted into a single-bit pulse density modulated stream by the Σ - Δ Modulator. A decimator acting as a low-pass filter filters out the quantization noise and generates 16-bit data equivalent to the input current signal. The programmable input sampling rate and the decimation ratio determine the output data rates. The data path can be programmed to provide 1 Hz to 2 kHz rates in the various modes available. An optional FIR filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems.

After enabling the current measurement channel, the delay for the availability of the first sample is two conversion cycles.

6.2 Voltage/temperature measurement channel

The other two parameters of the Battery for measurement are Voltage and its Temperature. The second channel accepts signals from four independent sources through a Multiplexer as listed below:

- An attenuated battery voltage obtained through appropriate external resistor divider, (or)
- A signal from the external temperature sensor, (or)
- A signal from external reference, (or)
- A signal from the internal temperature sensor.

Apart from this difference in the multiplexing of four input signals, the rest of the data path is identical to the Current measurement channel. RSHH and RSHL are the Current measurement input pins.

The Battery Voltage which can go up to 18V is attenuated through a Resistor Divider externally and is applied to the Voltage Channel. The latency for the first result from the voltage measurement channel is two conversion cycles.

A second option on this measurement channel is to measure Temperature. Internally generated constant current is pumped through the Temperature Sensor with positive temperature coefficient, and, a high- precision resistor. The voltages across the sensor and the resistor form the inputs to the measurement channel one at a time. The difference

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between the two voltages which is independent of the magnitude of the current is used to determine the temperature accurately. The Voltage across the sensor is applied between the ETS and VSS pins and, the voltage across the high-precision resistor is applied between ETR and VSS. External Temperature measurement involves the acquisition of two signals one after the other using the same constant current source. The latency for the first result from the temperature measurement channel is two conversion cycles.

A third option on the measurement channel is to measure the internal temperature. Hence, one of the three options for measurement of Battery Voltage, External Temperature and, internal temperature may be carried out by selection of appropriate inputs through the internal multiplexer selection.

6.3 Digital implementation of measurement path

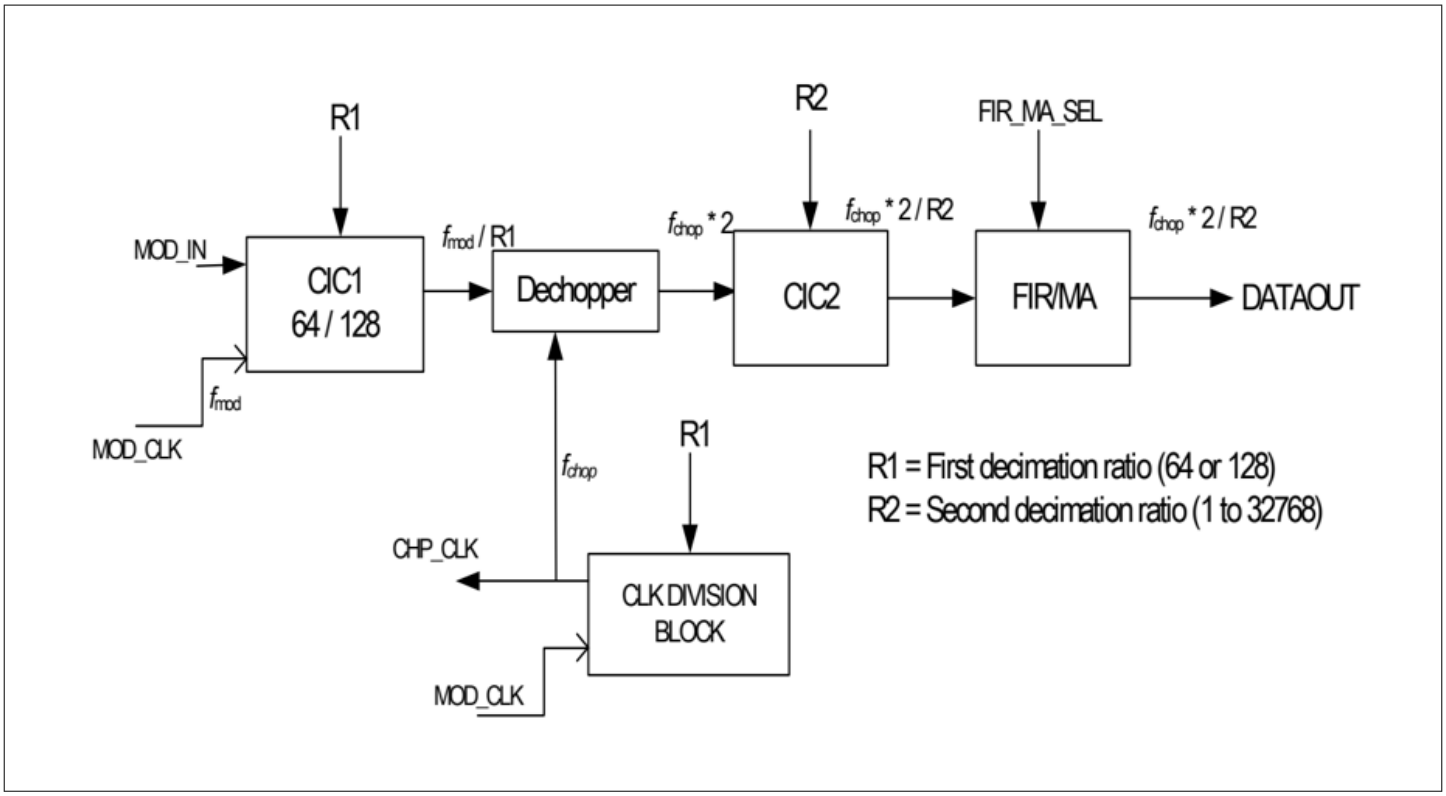


Figure 4 Block diagram of digital implementation

Figure 4, shows the digital implementation of the decimator and filter to process the 1-bit output of the Modulator. This block receives a 1-bit pulse density modulated output (MOD_IN) from the second order sigma delta modulator along with the oversampling frequency clock (MOD_CLK). The MOD_CLK directly goes to a clock division block, which generates chopper clock (CHOP_CLK). The CHOP_CLK can be one of 2 kHz or 4 kHz selected by Register CLK_REG in Table 34. The MOD_CLK can be either 1 MHz or 2 MHz. The Decimation is a two phase process. In the first phase, the R1 down sampling rate can be obtained by selecting either 64 or 128 in Registers DECREG_R1_I, DECREG_R1_V in Table 34. The 16-bit CIC1 output is dechopped with respect to CHOP_CLK. The output of Dechopper is passed through the CIC2 filter with a decimation ratio of 1 to 32768 in steps of power of 2. This output is then processed through a FIR or Moving Average (MA) filter. FIR Filter is provided to offer matched low pass filter response typically required in lead acid battery sensor systems. MA filter is used to provide averaged output and the number of samples for averaging can be any integer value from 1, 3, 7 or 15.

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6.4 Modes of operation

The device operates in four different modes, namely,

- Normal Mode 1 (NOM1),
- Normal Mode 2 (NOM2),
- Standby Mode 1 (SBY1), and,
- Standby Mode 2 (SBY2)

The Normal Modes are full-power modes with the exception that in Normal Mode 2, sampling is normally at a programmed lower frequency and is increased to a higher rate only when a measured input signal level crosses the programmed threshold in the current measurement channel.

The Standby Modes are lower power modes. Sampling is normally at a very low frequency interval. In Standby Mode 2, data sampling can be carried out only when the internal comparator detects the input current to be greater than the programmed threshold and it generates interrupt on the INT pin.

The device enters into the "Stop" state on Power On. This is a state where in the data path is inactive and can be entered into from any of the four Modes. The State transition Diagram involving the state of Stop and the four Modes is illustrated in the Figure 5.

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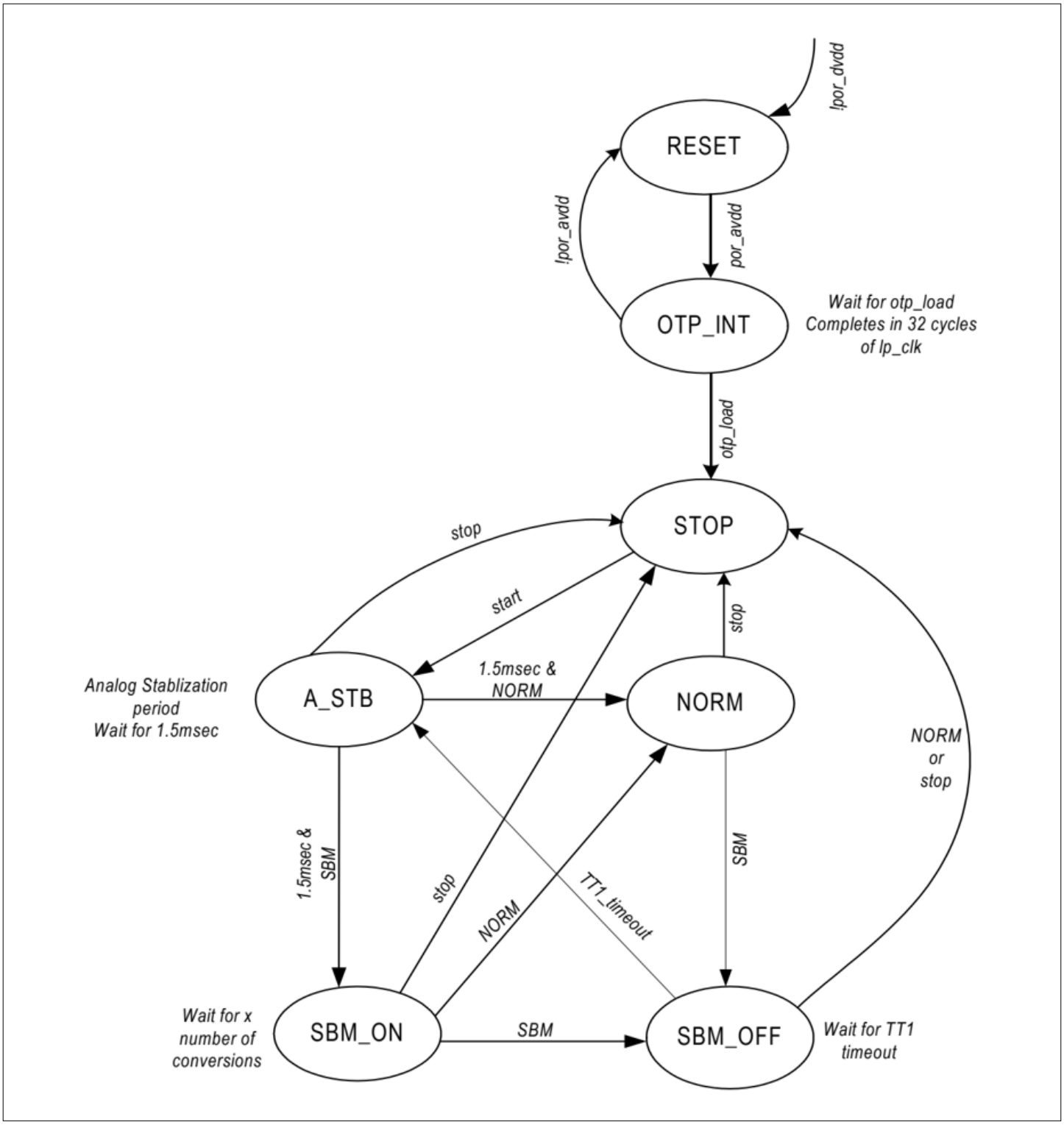


Figure 5 State transition diagram

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***Notes**:*

1. *Device soft reset can be written in any of the following states STOP, A_STB, SBM_ON, SBM_OFF by writing "0" into D[7] of the RESET_REG (Address 0X09).*
2. *Measurement path of soft reset should be written in any the states, STOP, SBM_OFF by writing "0" into D[6] of the RESET_REG (Address 0X09).*
3. *When soft reset is used for the measurement path or for the device, external clock needs to be disabled if the system clock is external clock in the application.*

6.4.1 Normal mode 1 (NOM1)

On Power-on-reset of the device, AS8512 goes into STOP State.

Transition to Normal mode1 (NOM1) occurs when the "START BIT" D0 of Mode Control Register MOD_CTL_REG in Table 34 is set to "1" through the serial port SPI. Data Rate of voltage and current channels can be independently programmed and both the channels generate interrupts for every output available from ADC. The interrupt signal is generated on the INT pin. The width of the interrupt pulse is eight cycles of lp_clk. The data is stable up to the next interrupt. If the data rate is different for the two channels, the interrupt rate would follow the higher rate among the two channels. Data update can be known by reading the status register. The functionality is explained in the waveform shown in Figure 6. When the device is configured to NORMAL Mode1 from any mode the configuration should be through the STOP state only.

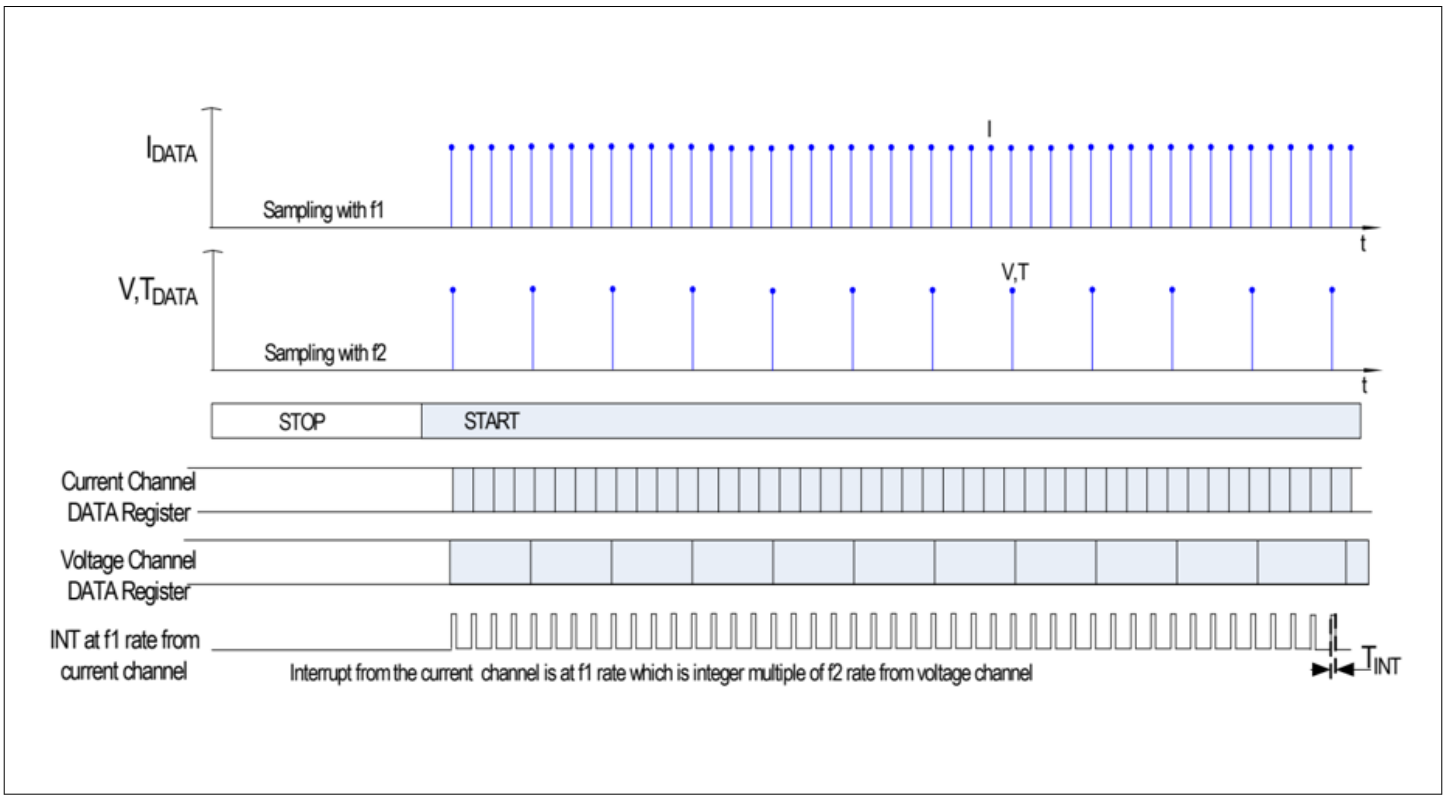


Figure 6 Normal mode 1

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6.4.2 Normal mode 2 (NOM2)

NOM2 differs from NOM1 in such a way that it allows for a relaxed data rate at a period of T_{MC} by programming the corresponding register as long as the amplitude of current is less than a programmed threshold I_{THC} . However, when, the measured input signal exceeds the programmed threshold, the data rate is changed to the rate of NOM1 mode.

Transition to NOM2 occurs when the "START BIT" D0 of Mode Control register MOD_CTL_REG in Table 34 is set to 1 and mode control bits to 01 through SPI. In this mode the data rate should be programmed with the time of T_{MC} . An interrupt signal is generated on INT at the rate of T_{MC} seconds with a pulse width of eight cycles of lp_clk. The data is stable up to the next interrupt. The data sample is compared against the programmed threshold and when it is exceeded, the data sampling rate is changed to provide data at the data rate of NOM1 mode. However, as soon as the data sample amplitude falls below the programmed threshold, the sampling rate is restored to provide data at the rate of T_{MC} . The functionality is illustrated in Figure 7 .

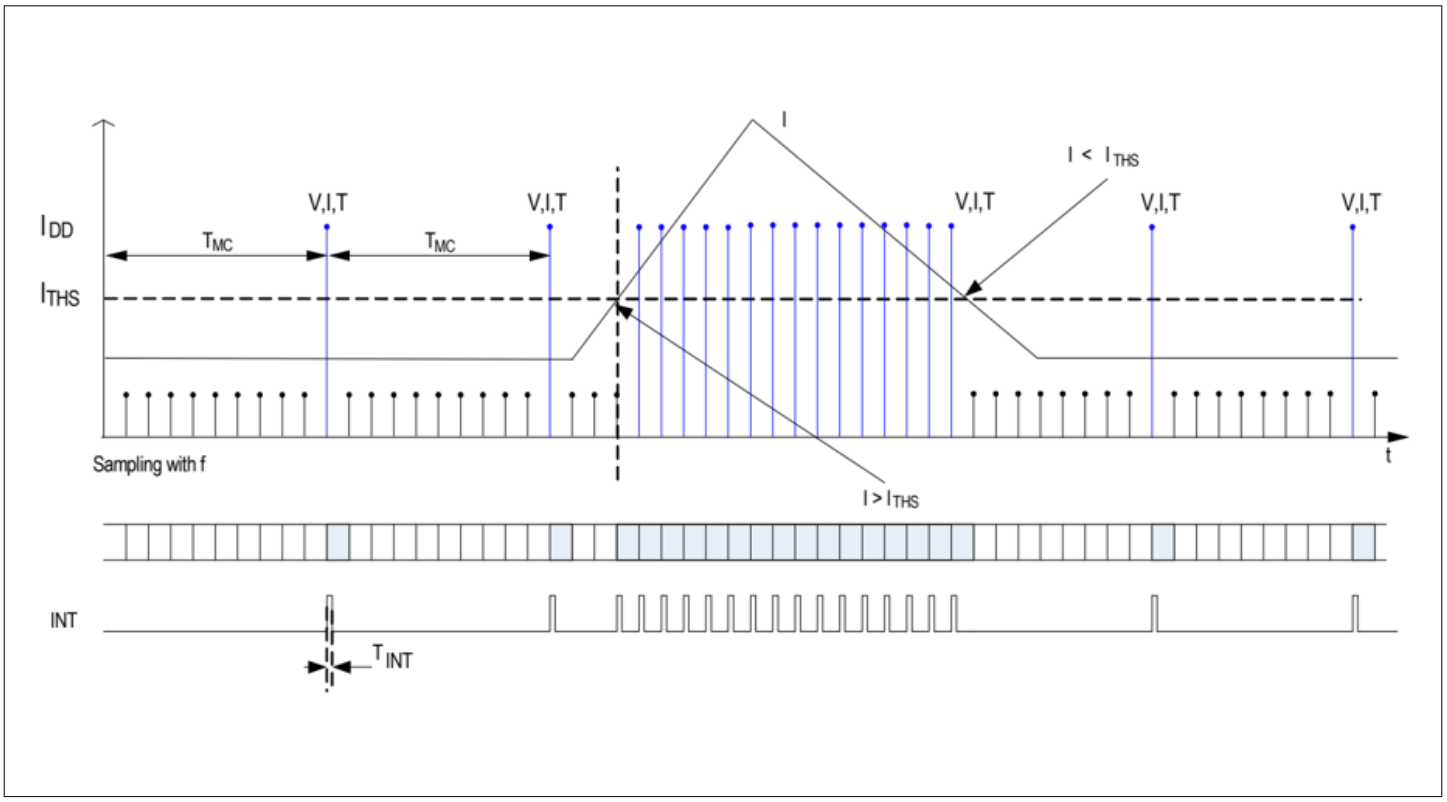


Figure 7 Normal mode 2

6.4.3 Standby mode 1 (SBM1)

The low-power Standby Mode can be entered only through the STOP state. Transition to SBM1 mode occurs when the "START BIT" D0 of Mode Control register MOD_CTL_REG in Table 34 is set to "1" and Mode Control Bits to "10" through SPI. In this mode the date rate is programmable with the time of Ta. An interrupt signal is generated on INT at the rate of Ta seconds., and with a pulse width of eight cycles of lp_clk. The data is stable up to the next interrupt. The functionality is illustrated in Figure 8. During the period of Ta, only one data sample is made available and, during the rest of the period, the device is maintained in STOP state to reduce power consumption. The microcontroller which receives the data on the Interrupt, is also expected to be processing the data for a short time as shown clearly in the Figure 8 to ensure the overall low-power consumption of the data acquisition and processing system.

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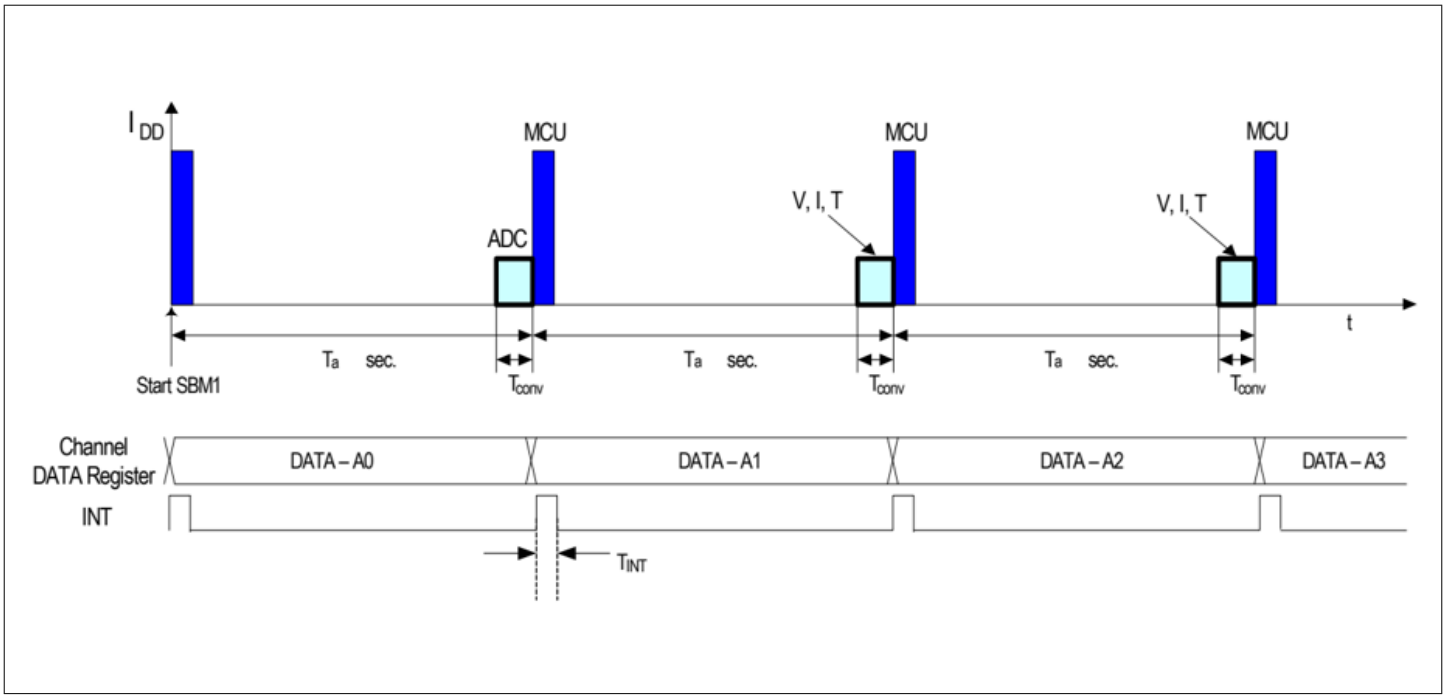


Figure 8 Standby mode 1

6.4.4 Standby mode 2 (SBM2)

Standby mode 2 is an extension of the Standby mode 1 to achieve even a lower power in the data acquisition system by providing interrupt to the microcontroller only when the data sample exceeds the set current threshold. The Standby Mode can be entered only through the STOP state. Transition to SBM2 mode occurs when the "START BIT" D0 of Mode Control register MOD_CTL_REG in Table 34 is set to "1" and Mode Control Bits D7,D6 to "1,1" through SPI. In this mode the date rate is programmable with the time of Ta in the Ta control registers B, C. The data sample is made available and an interrupt signal is generated on INT pin only when the input signal exceeds the threshold set in Current Threshold Registers D,E. It should be noted here that the data is stable for Ta seconds. The functionality is illustrated in Figure 9.

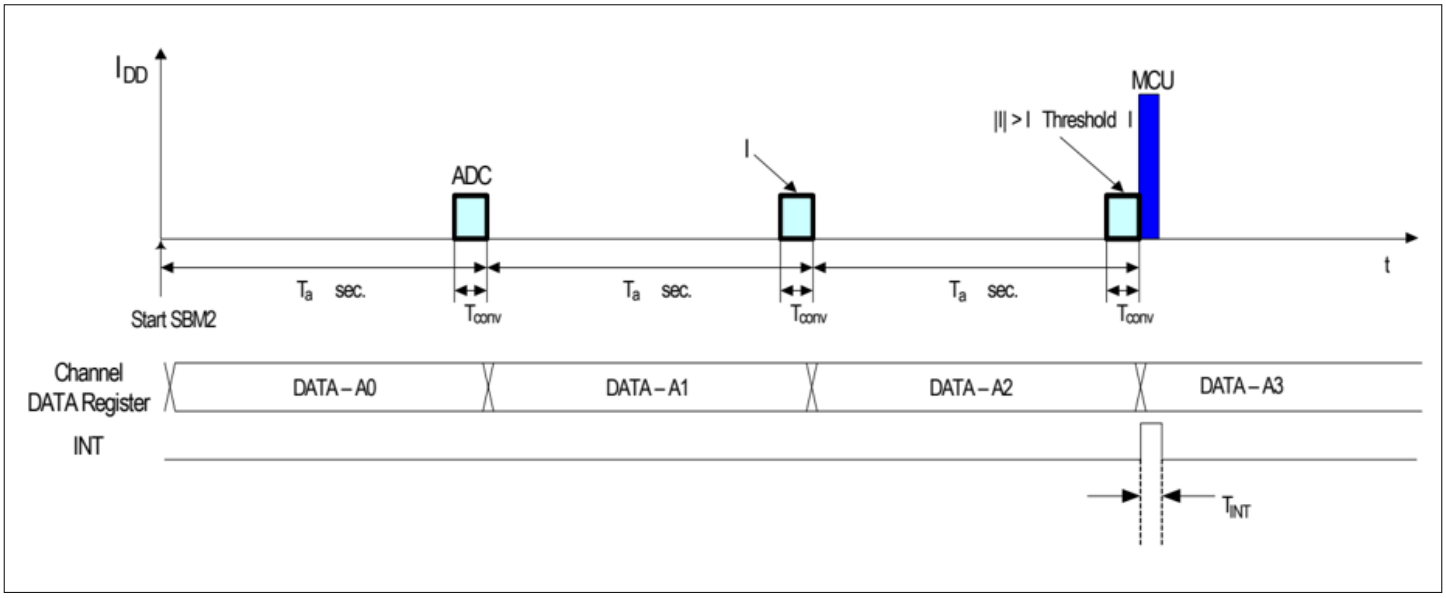


Figure 9 Standby mode2

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6.5 Reference voltage

Band gap-reference voltage is used for the ADC as a reference and for the generation of the current for external temperature measurement.

6.6 Oscillators

A High-speed oscillator (HS) generates the oversampling clock. For internal state machine and Interrupt generation, a low-speed Oscillator (LS) is also available.

6.7 Power-on reset

The AS8512 has PORs, APOR and DPOR on analog and digital power supplies respectively. On PORs of both supplies, initialization sequence happens and the system status is shown in state diagram (see Figure 5).

As shown in the state diagram, the system is in RESET state until DPOR output goes to logic HIGH and subsequently until APOR output goes to logic HIGH. Once analog power supply is available, the system goes into OTP_INT state and loads the default values into the control and data registers and goes into STOP state. If analog POR, APOR goes low at any time, the system goes into RESET state. In the STOP state, the AS8512 can be programmed and by giving start command it starts working following the state machine.

6.8 4-wire serial port interface

The SPI interface is used as interface between the AS8512 and an external micro-controller to configure the device and access the status information. The micro-controller begins communication with the SPI which is configured as a slave. The SPI protocol is simple and the length of each frame is an integer multiple of bytes except when a transmission is started. Each frame has 1 command bit, 7 address/configuration bits, and one or more data bytes. The edge of CS and the level of SCLK during the start of a SPI transaction, determine the edge on which the data is transferred from the SPI and the edge on which the data is sampled by the slave. Table 30 describes the setting of the transfer and sampling edges of SCLK. Figure 10 shows the falling edge and rising edge for data transfer and data sampling respectively, when SCLK is HIGH on the falling edge of CS.

Table 30 CS and SCLK

CS	SCLK	Description
FALL	LOW	Serial data transferred on rising edge of SPI clock. Sampled at falling edge of SPI clock.
FALL	HIGH	Serial data transferred on falling edge of SPI clock. Sampled at rising edge of SPI clock.
ANY	ANY	Serial data transfer edge is unchanged.

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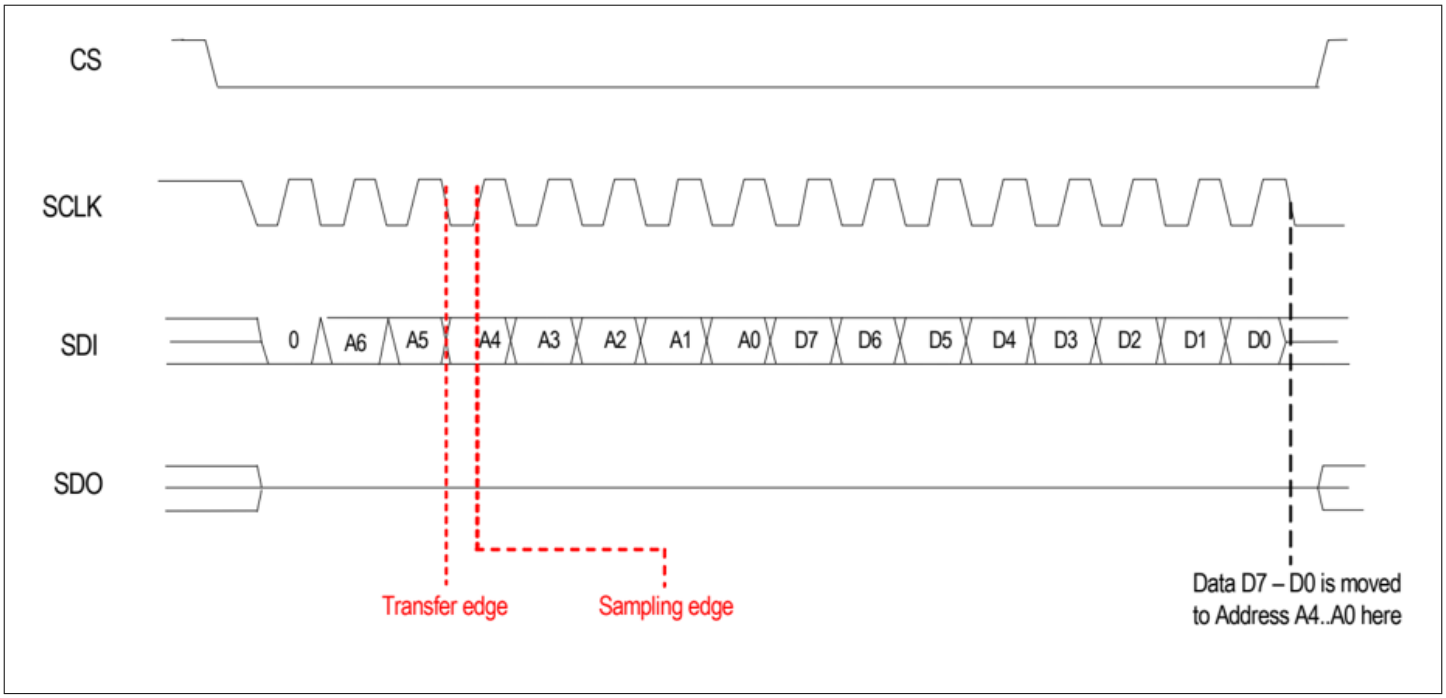


Figure 10 Protocol for serial data write with length = 1

6.8.1 SPI frame

A frame is formed by a first byte for command and address/configuration and a following bit stream that can be formed by an integer number of bytes. Command is coded on the 1 first bit, while address is given on LSB 7 bits (see Table 31).

Table 31 Command bits

Command bits	Register address or transmission configuration						
C0	A6	A5	A4	A3	A2	A1	A0

Table 32 Command bits

C0	Command	<A6:A0>	Description
0	WRITE	ADDRESS	Writes data byte on the given starting address.
1	READ	ADDRESS	Read data byte from the given starting address.

If the command is read or write, one or more bytes follow. When the micro-controller sends more bytes (keeping CS LOW and SCLK toggling), the SPI interface increments the address of the previous data byte and writes/reads data to/from consecutive addresses.

6.8.2 Write command

For write command, C0 = 0. After the command code C0 is transferred, the address of register to be written is provided from MSB to LSB.

Subsequently one or more data bytes can be transferred from MSB to LSB. For each data byte following the first one, used address is the incremented value of the previously written address. Each bit of the frame has to be driven by the SPI master on the SPI clock transfer edge. The SPI slave samples it on the next clock edge. These edges are

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determined by the level of SCLK as shown in Table 30. Figure 11 and Figure 12 are examples of write command without and with address self-increment.

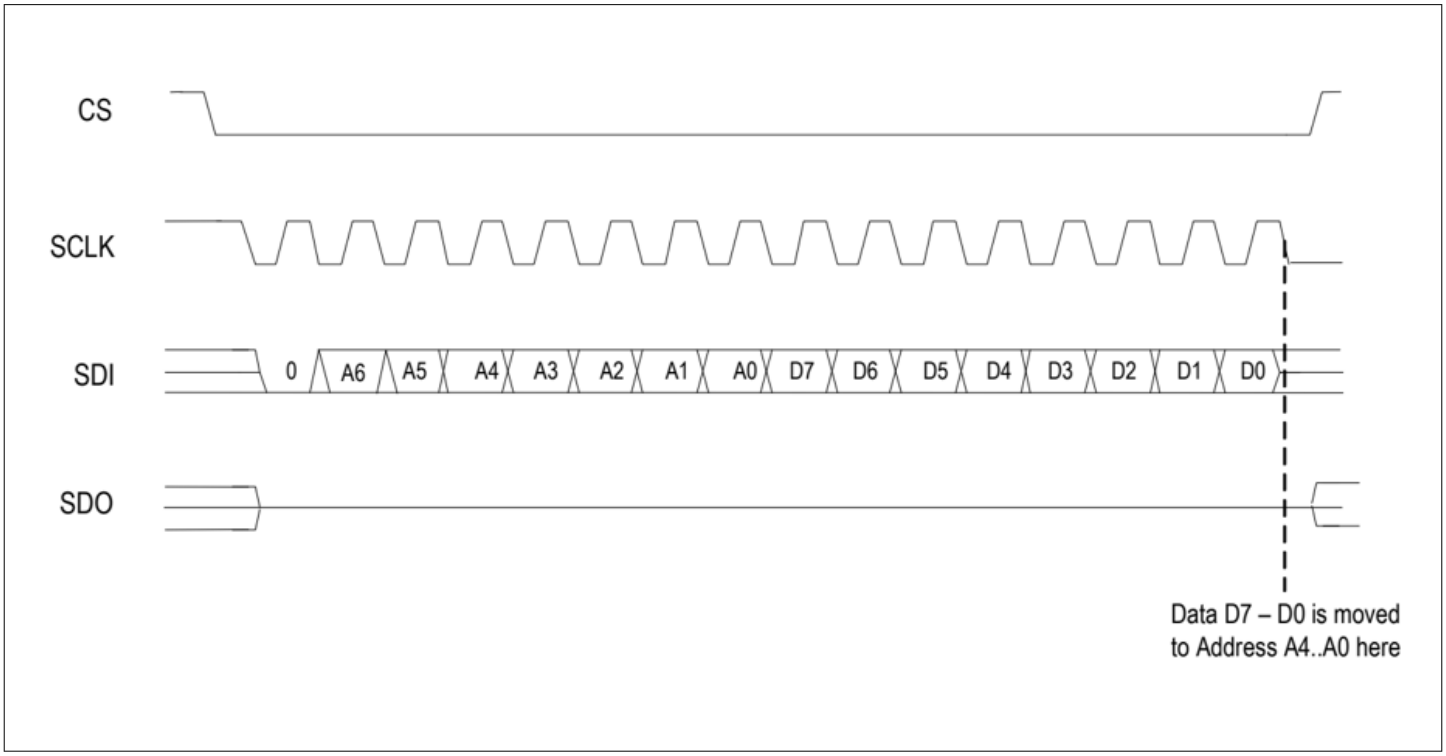


Figure 11 Protocol for serial data write with length = 1

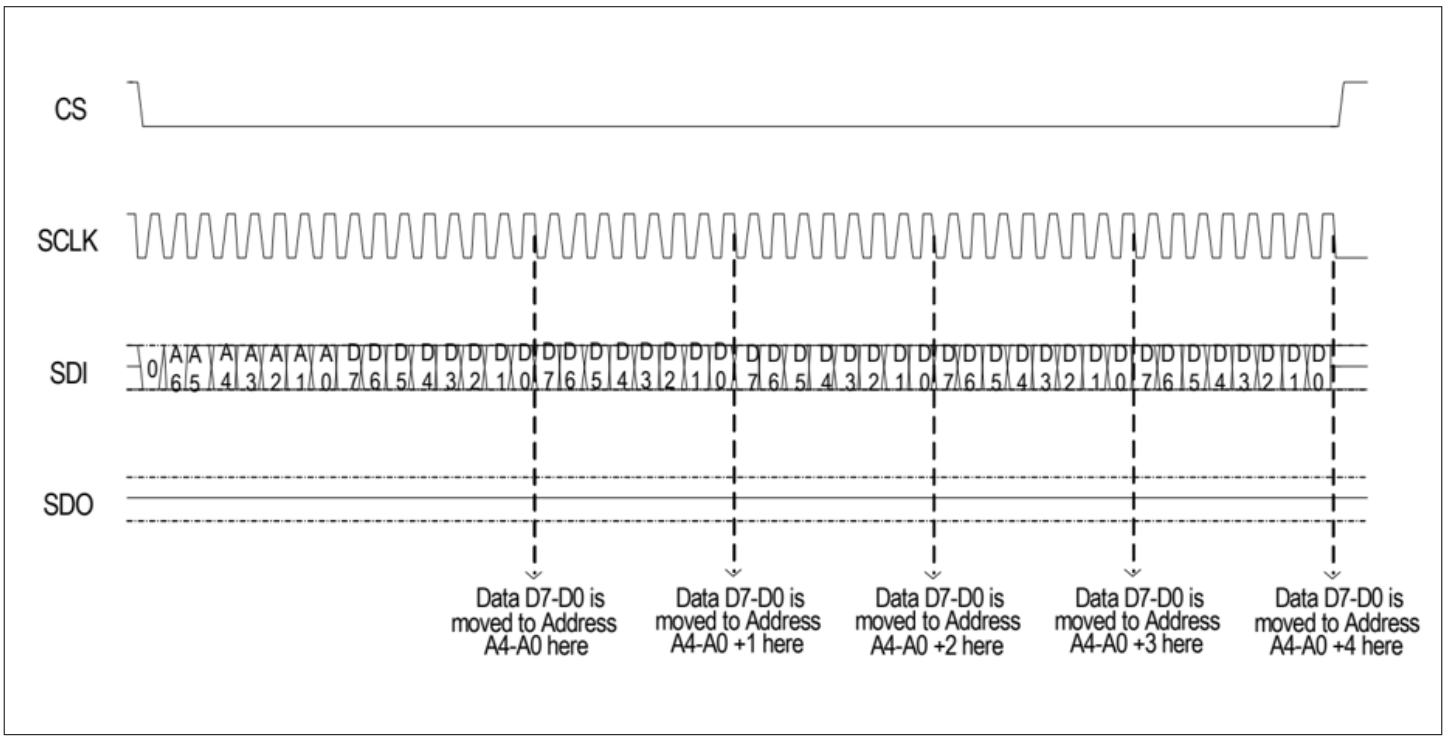


Figure 12 Protocol for serial data write with length = 4

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6.8.3 Read command

For Read command C0 = 1. After the command code C0, the address of register to be read is provided from MSB to LSB. Then one or more data bytes can be transferred from the SPI slave to the master, always from MSB to LSB. To transfer more bytes from consecutive addresses, SPI master keeps CS signal LOW and SPI clock active as long as it desires to read data from the slave. Each bit of the command and address of the frame is to be driven by the SPI master on the SPI clock transfer edge where SPI slave samples it on the next SPI clock edge.

Each bit of the data section of the frame is driven by the SPI slave on the SPI clock transfer edge and SPI master samples it on the next SPI clock edge. These edges are determined as per Table 30 and examples of read command without and with address self-increment.

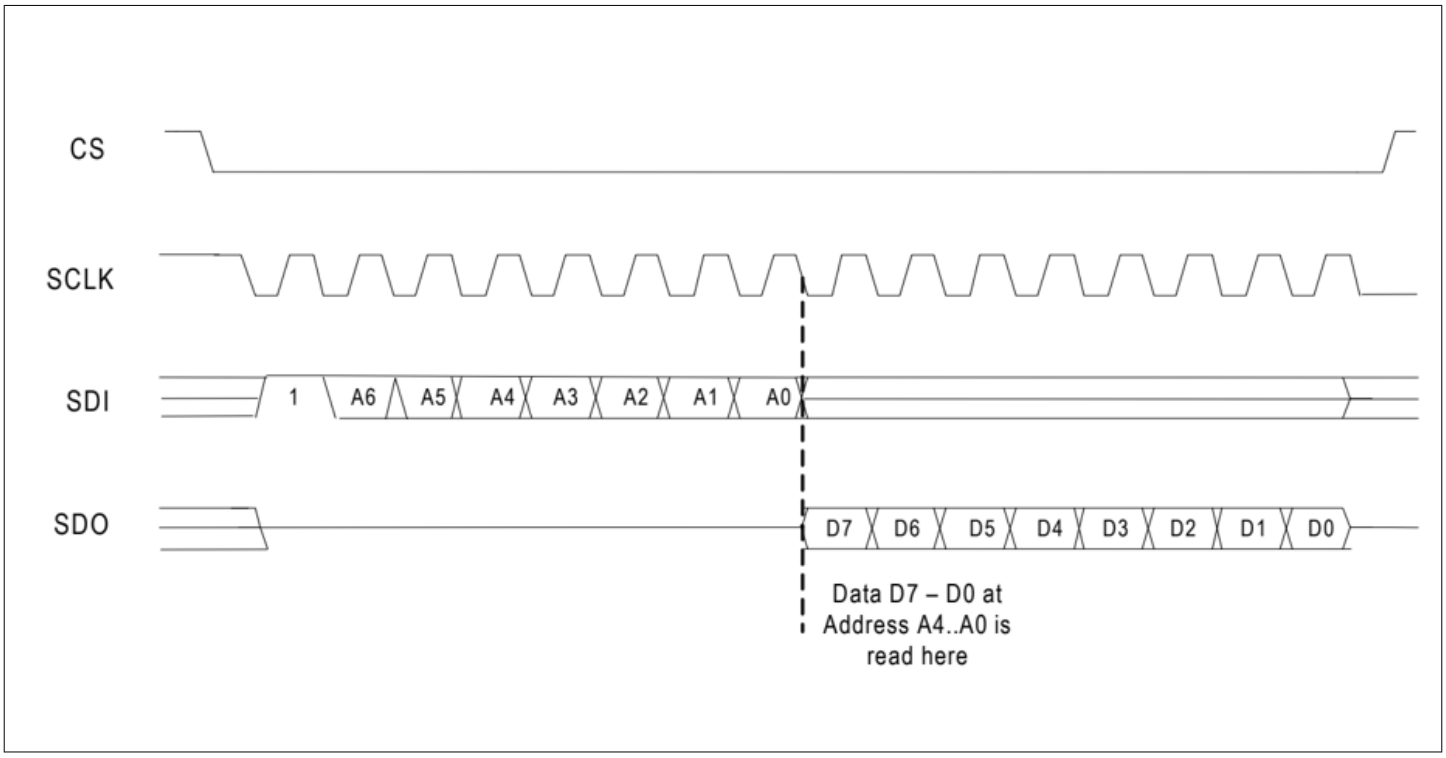


Figure 13 Protocol for serial data read with length = 1

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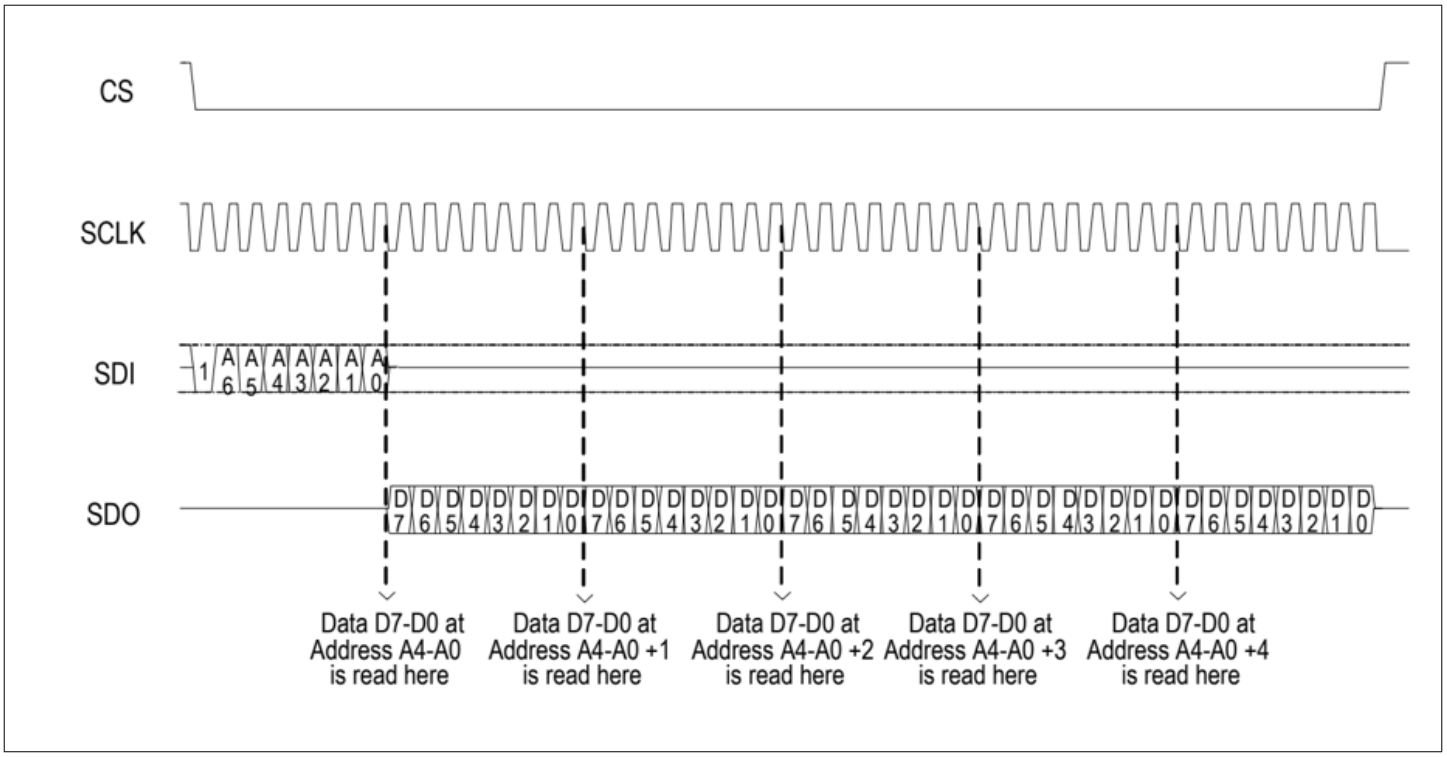


Figure 14 Protocol for serial data read with length = 4

6.8.4 Timings

In the following timing waveforms and parameters are exposed.

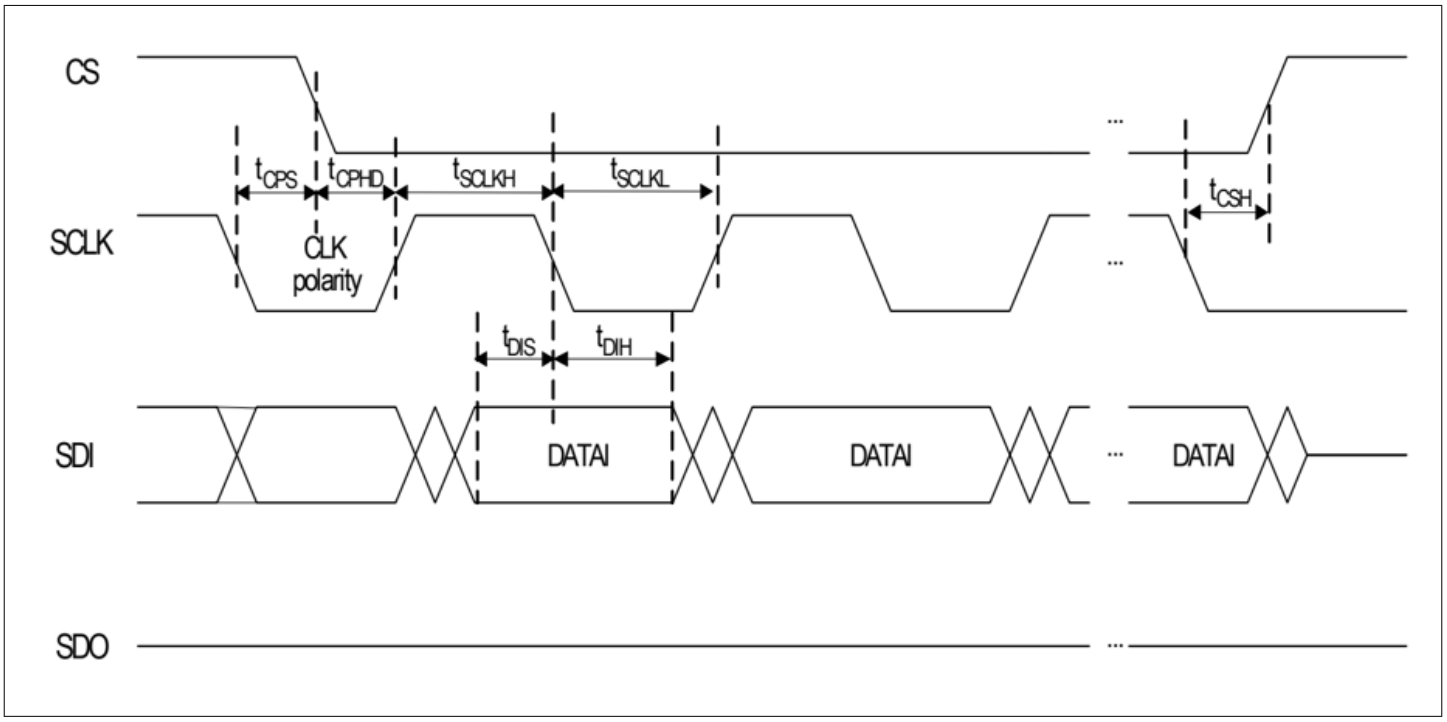


Figure 15 Write timing for writing

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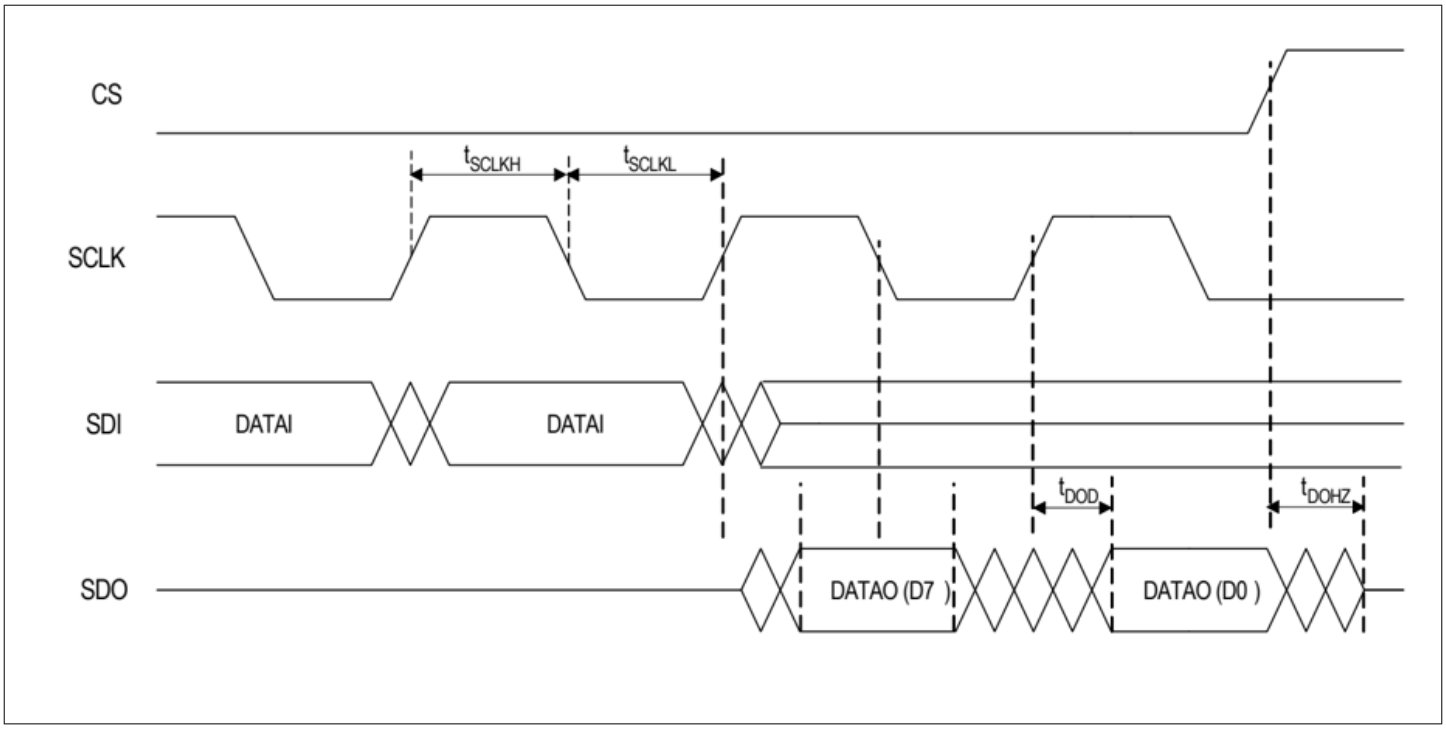


Figure 16 Read timing for reading

6.8.5 SPI interface timing

Table 33 SPI interface timing

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
General						
BR_{SPI}	Bit rate				1	Mbps
T_{SCLKH}	Clock high time		400			ns
T_{SCLKL}	Clock low time		400			ns
Write timing						
t_{DIS}	Data in setup time		20			ns
t_{DIH}	Data in hold time		20			ns
T_{CSH}	CS hold time		20			ns
Read timing						
t_{DOD}	Data out delay				80	ns
t_{DOHZ}	Data out to high impedance delay	Time for the SPI to release the SDO bus			80	ns
Timing parameters when entering 4-wire SPI mode (for determination of CLK polarity)						
t_{CPS}	Clock setup time (CLK polarity)	Setup time of SCLK with respect to CS falling edge	20			ns
t_{CPHD}	Clock hold time (CLK polarity)	Hold time of SCLK with respect to CS falling edge	20			ns

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6.9 Control register

This section describes the control registers used in AS8512. Registers can be broadly classified into the following categories.

- Data access registers
- Status registers
- Digital signal path control registers
- Digital control registers
- Analog control registers

Table 34 Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data
Data access registers					
00	DREG_I1 (ADC data register for current)	0000_0000	R	D[7:0]	Denotes the current ADC MSB Byte (ADC_I[15:8])
01	DREG_I2 (ADC data register for current)	0000_0000	R	D[7:0]	Denotes the current ADC LSB Byte (ADC_I[7:0])
02	DREG_V1 (ADC data register for voltage)	0000_0000	R	D[7:0]	Denotes the voltage ADC MSB Byte (ADC_V[15:8])
03	DREG_V2 (ADC data register for voltage)	0000_0000	R	D[7:0]	Denotes the voltage ADC LSB Byte (ADC_V[7:0])
Status registers					
04	STATUS_REG	0000_0000	R	D[7]	NOM1/NOM2 data ready
				D[6]	NOM2 threshold crossover
				D[5]	SBM1 data ready
				D[4]	SBM2 threshold crossover
				D[3]	APOR status
				D[2]	Data from current channel updated
				D[1]	Data from voltage channel updated
				D[0]	Reserved
Digital signal path control registers for current channel					
05	DEC_REG_R1_I	0100_0101	R/W	D[7]	This bit selects decimation rate is used for current channel. Default is 0 (Down Sampling Rate is 64)
					0: Down sampling rate is 64

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
					1	Down sampling rate is 128
				D[6:5]	These two bits select division ratio of oversampling frequency clock MOD_CLK to be used as chopper clock, CHOP_CLK. Default is “10” (divide by 512)	
					00	Chopper clock always high
					01	Divide by 256
					10	Divide by 512
					11	Divide by 1024
05	DEC_REG_R1_I	0100_0101	R/W	D[4:1]	These four bits select the decimation ratio of second CIC stage. Default is "0010" (equal to 4)	
					0000	1
					0001	2
					0010	4
					0011	8
					0100	16
					0101	32
					0110	64
					0111	128
					1000	256
					1001	512
					1010	1024
					1011	2048
					1100	4096
					1101	8192
					1110	16384
					1111	32768
				D[0]	CIC1 saturation interrupt mask control. Default is 1	
					0	Unmask
					1	Mask

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
06	DEC_REG_R2_I	1100_0101	R/W	D[7]	I-Channel enable, Default 1=Enable	
				D[6]	V-Channel enable, Default 1=Enable	
				D[5]	Interrupt polarity	
					0	Active high
					1	Active low
				D[4]	Interrupt mask control for current channel data ready interrupt on INT pin (Default is 0)	
					0	Unmasked
					1	Masked
				D[3:2]	These two bits select the source of output 16-bit data in normal mode from current channel. Default is 01	
					00	FIR/MA output
					01	CIC2 output
					10	Dechop / Demod output
					11	CIC1 output
				D[1:0]	These two bits select the source of output 16-bit data in SBM mode from current channel. Default is 01	
					00	FIR/MA output
					01	CIC2 output
					10	Dechop/Demod output
					11	CIC1 output
07	FIR CTL_REG_I	0000_0100	R/W	D[7]	This bit selects FIR/MA filter in cur- rent channel. Default is 0 (FIR)	
					0	FIR
					1	MA filter
				D[6:3]	These bits select the number of data samples for averaging in MA filter in current channel. Default is 0000 (bypass)	
					0000	Bypass
					0001	1

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
					0011	3
					0111	7
					1111	15
				D[2:1]	These two bits select the measurement path architecture in both current and voltage channels. Default is 10 (dechopper after CIC)	
					00	Demodulator after CIC1
					01	Demodulator before CIC1
					10	Dechopper after CIC1 (preferred and suggested)
					11	Demodulator before CIC1 with settled sample
				D[0]	Reserved.	Default 0. Do not change
Digital control registers						
08	CLK_REG (Clock control register)	0010_0000	R/W	D[7:6]	Oversampling frequency clock selection. Default is 00 (high speed (HS) internal clock)	
					00	Internal HS clock with no clock output
					01	Internal HS clock with clock output
					10	External clock
				D[5:4]	These two bits select the division ratio for HS clock/external clock. Default is 10 (division by 4)	
					00	No division
					01	Divide by 2
					10	Divide by 4
					11	Divide by 8

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
				D[3:2]	These two bits select the division ratio of HS clock, by which it should be divided before providing it on CLK pin. Default is 00 (no division)	
					00	No division
					01	Divide by 2
					10	Divide by 4
					11	Divide by 8
				D[1]	This bit selects the division ratio of LS clock	
					0	LS_CLK undivided (Low Speed clock)
					1	LS_CLK divide by 2
				D[0]		Reserved
09	RESET_REG (Reset control register)	1100_0000	R/W	D[7]	Entire device can be soft reset by writing "0" into this register bit. This bit will take a default 1 value on coming out of reset	
				D[6]	Measurement path can be soft reset by writing "0" into this register bit. This bit will take a default 1 value after measurement path is reset.	
				D[5:0]	Reserved	
0A	MOD_CTL_REG (Mode control registers)	0000_0000	R/W	D[7:6]	These two bits select the operating mode of the device. Default is 00 (normal mode 1)	
					00	Normal mode 1
					01	Normal mode 2
					10	Standby mode 1
					11	Standby mode 2
				D[5:3]	These three bits select the number of cycles to be ignored before comparison with the set threshold in standby mode. Default is 000 (3 cycles of data)	
					000	3 cycles of data
					001	4 cycles of data
					010	5 cycles of data

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
					011	6 cycles of data
					100	7 cycles of data
					101	8 cycles of data
					110	9 cycles of data
					111	10 cycles of data
				D[2]	This bit controls the CHOP_CLK availability on CHOP_CLK pin. Default is 0.	
					0	Disabled
					1	Enabled
				D[1]	Enabling the MEN pin to indicate transition from standby to normal mode.	
					0	Disabled
					1	Enabled
				D[0]	This bit is used to take the device from STOP state to any of the Modes based on D[7:6] selection of this register.	
					0	Retain in STOP state
					1	Enables transition to normal or standby modes.
0B	MOD_Ta_REG1 (Ta control register)	1000_0000	R/W	D[7]	Unit of Ta in SBM1/SBM2. Default is 1	
					0	Unit is in milliseconds
					1	Unit is in seconds
				D[6:0]	MSB value of Ta	
0C	MOD_Ta_REG2 (Ta control register)	0000_0000	R/W	D[7:0]	Unit of Ta in SBM1/SBM2 LSB value of Ta	
0D	MOD_I_{TH}_REG1 (Current threshold register)	0000_0000	R/W	D[7:0]	MSB bits of 16 bits SBM2 threshold register	
0E	MOD_I_{TH}_REG2 (Current threshold register)	0000_0000	R/W	D[7:0]	LSB bits of 16 bits SBM2 threshold register	
0F	MOD_T_{MC}_REG1 (T_{MC} control registers)	0000_0000	R/W	D[7:0]	MSB value of number of data sam- ples to be dropped from ADC before sending Interrupt in NOM2	

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
10	MOD_T_{MC}_REG2 (T_{MC} control register)	0000_0000	R/W	D[7:0]	LSB value of number of data sam- ples to be dropped from ADC before sending Interrupt in NOM2	
11	NOM_I_{TH}_REG1	0000_0000	R/W	D[7:0]	Eight MSB bits of NOM2 current threshold register	
12	NOM_I_{TH}_REG2	0000_0000	R/W	D[7:0]	Eight LSB bits of NOM2 current threshold register	
Analog control registers						
13	PGA_CTL_REG (PGA control registers)	0101_0000	R/W	D[7:6]	Setting of gain G of current channel PGA. Default is 01 (G = 25)	
					00	5
					01	25
					10	40
					11	100
				D[5:4]	Setting of gain G in voltage chan- nel. Default is 01 (G =25)	
					00	5
					01	25
					10	40
					11	100
				D[3:0]	Reserved	
14	PD_CTL_REG_1 (Power Down Control Register)	1100_1111	R/W	D[7]	0	Disable chopper clock to current channel
					1	Enable chopper clock to Current channel
				D[6]	0	Disable Chopper clock to voltage channel
					1	Enable chopper clock to voltage channel
				D[5]		Reserved
				D[4]		Reserved
				D[3]	0	Disable current channel PGA
					1	Enable current channel PGA

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
				D[2]	0	Disable current channel ΣΔ modulator
					1	Enable current channel ΣΔ modulator
				D[1]	0	Disable voltage channel PGA
					1	Enable voltage channel PGA
				D[0]	0	Disable voltage channel ΣΔ modulator
					1	Enable voltage channel ΣΔ modulator
15	PD_CTL_REG_2 (Power down control register)	1111_0011	R/W	D[7]	0	Disable CIC1 of both channels
					1	Enable CIC1 of both channels
				D[6]	0	Disable CIC2 of both channels
					1	Enable CIC2 of both channels
				D[5]	0	Disable dechopper in both channels
					1	Enable dechopper in both channels
				D[4]	0	Disable FIR in both channels
					1	Enable FIR in both channels
				D[3]	0	Do not bypass PGA in current channel. Default 0
					1	Bypass PGA in current channel
				D[2]	0	Do not bypass PGA in voltage channel. Default 0

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
					1	Bypass PGA in voltage channel
				D[1]	0	Disable current channel chopper
					1	Enable current channel chopper
				D[0]	0	Disable voltage channel chopper
					1	Enable voltage channel chopper
16	PD_CTL_REG_3 (Power down control register)	1111_1000		D[7]	0	Disable common mode reference
					1	Enable common mode reference
				D[6]	0	Disable internal current source
					1	Enable internal current source
				D[5]	0	Disable Internal tempera- ture sensor
					1	Enable Internal tempera- ture sensor
				D[4]		Reserved (Default 1). Do not change
				D[3]		Reserved (Default 1). Do not change
				D[2]	0	Data output in binary numbering system
					1	Data output in 2's comple- ment numbering system
				D[1]		Reserved (Default 0). Do not change
				D[0]		Reserved
17	ACH_CTL_REG (Analog channel selection register)	0000_0000	R/W	D[7:6]	These bits specify the selection of voltage/temperature in voltage channel. Default is 00 (voltage channel).	
					00	Voltage channel

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
					01	External temperature channel ETR
					10	External temperature channel ETS
					11	Internal temperature channel
				D[5]	Reserved (Default 0). Do not change	
				D[4]	Internal current source switch enable. Default is 0. Note: D4 bit is used for enabling current source to the channel selected by bits D[7,6] of this regis- ter.	
					0	Disabled
					1	
						Enabled
				D[3]	Enable/disable Internal current source to RSHH pin of current channel	
					0	Disabled
					1	Enabled
				D[2]	Enable/disable current source switch to RSHL pin of current channel	
					0	Disabled
					1	Enabled
				D[1:0]	Reserved	
18	ISC_CTL_REG (Current source setting register)	0000_0000	R/W	D[7:3]	These three bits specify the selection of magnitude of current from the Internal current source. Default is 00000 (0 µA).	
					00000	0 µA
					00001	8.5 µA
					00010	17 µA
					00100	34.5 µA
					01000	68 µA
					10000	135 µA
					11111	270 µA
				D[2:0]	Reserved	
19	OTP_EN_REG	0000_0000	R/W	D[7]	1	Reserved (default = 1). Do not change

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
				D[6:0]	Reserved	
44	STATUS_REG_2	0000_0000	R	D[7]	Status indicating data saturation in current channel	
				D[6]	Status indicating data saturation in voltage channel	
				D[5:0]	Reserved	
Digital signal path control registers for voltage channel						
45	DEC_REG_R1_V	0100_0101	R/W	D[7]	Selection of decimation ratio for voltage/temperature channel. Default is 0 (down sampling rate is 64)	
					0	Down sampling rate is 64
					1	Down sampling rate is 128
				D[6:5]	Division of oversampling clock, which is used as chopper clock. Default is 10 (divide by 512)	
					00	Chopper clock always high
					01	Divide by 256
					10	Divide by 512
					11	Divide by 1024
				D[4:1]	Decimation ratio of CIC2. Default is 0010 (4)	
					0000	1
					0001	2
					0010	4
					0011	8
					0100	16
					0101	32
					0110	64
					0111	128
					1000	256
					1001	512
					1010	1024
					1011	2048

(table continues...)

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Table 34 (continued) Control registers[1)]

Addr in HEX	Register name	POR value in BIN	R/W		8-bit control/status data	
					1100	4096
					1101	8192
					1110	16384
					1111	32768
				D[0]	CIC1 saturation interrupt mask control. Default is 1	
					0	Unmasked
					1	Masked
46	DEC_REG_R2_V	0000_0100	R/W	D[7:5]	Reserved	
				D[4]	Interrupt mask control for voltage channel data ready. Interrupt on INT pin (Default is 0)	
					0	Unmasked
					1	Masked
				D[3:2]	These two bits select the source of output 16-bit data in normal mode from voltage channel. Default is 01	
					00	FIR / MA output
					01	CIC2 output
					10	Dechop / Demod output
					11	CIC output
				D[1:0]	Reserved	
47	FIR CTL_REG_V	0000_0000	R/W		These bits select the number of data samples for averaging in MA filter in voltage channel. Default is 0000 (bypass)	
				D[6:3]	0000	Bypass
					0001	1
					0011	3
					0111	7
					1111	15
				D[2:0]	Reserved	

1) All the registers from address 0x19 to 0x2C are read-only.

There is an OTP test lock bit set by factory which locks the write access to all the test registers from 0x1A to 0x2C.

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6.9.1 Standby mode - power consumption

In standby mode 1 there is a timer based accurate measurement every Ta seconds. The device itself stays in idle-mode as long as it does not get a different command from the SPI interface. Internal oscillator frequency is typically foscint=262 kHz to reduce power consumption as long as the timer runs. After every time out of Ta seconds, it performs accurate measurement of current, voltage/temperature. Data ready is signaled to microcontroller through an interrupt signal on INT and goes into STOP state.

In the SBM the following equations hold:

- $T_{sbm1} = T_a = 10s$ (default value is 10s); the power consumption is valid for this setting. This is the period of the repetition rate in SBM 1 and SBM2.
- $T_{sett} \approx 2$ ms (depending on external capacitors). This is the time required by the analog part to settle when the new measuring period is started. Any measurements performed during T_{sett} produce invalid results.
- T1 = 3ms (by default setting, every third measurement is sent to microcontroller in the SBM mode 1) is the time needed to perform the first measurement.
- $T_{meas} = T_{sett} + T1$ is the total active time needed to get a valid result.
- DRSBM = $T_{meas}/T_{sbm} \approx 5ms/10s$. This is the ratio of repetition time versus the active time (Device in NOM mode).

Power consumption = (DR_{SBM} *NOM mode power consumption) + ((10s-5 ms)/10s)*Stop mode power consumption)

6.9.2 Initialization sequence at power ON

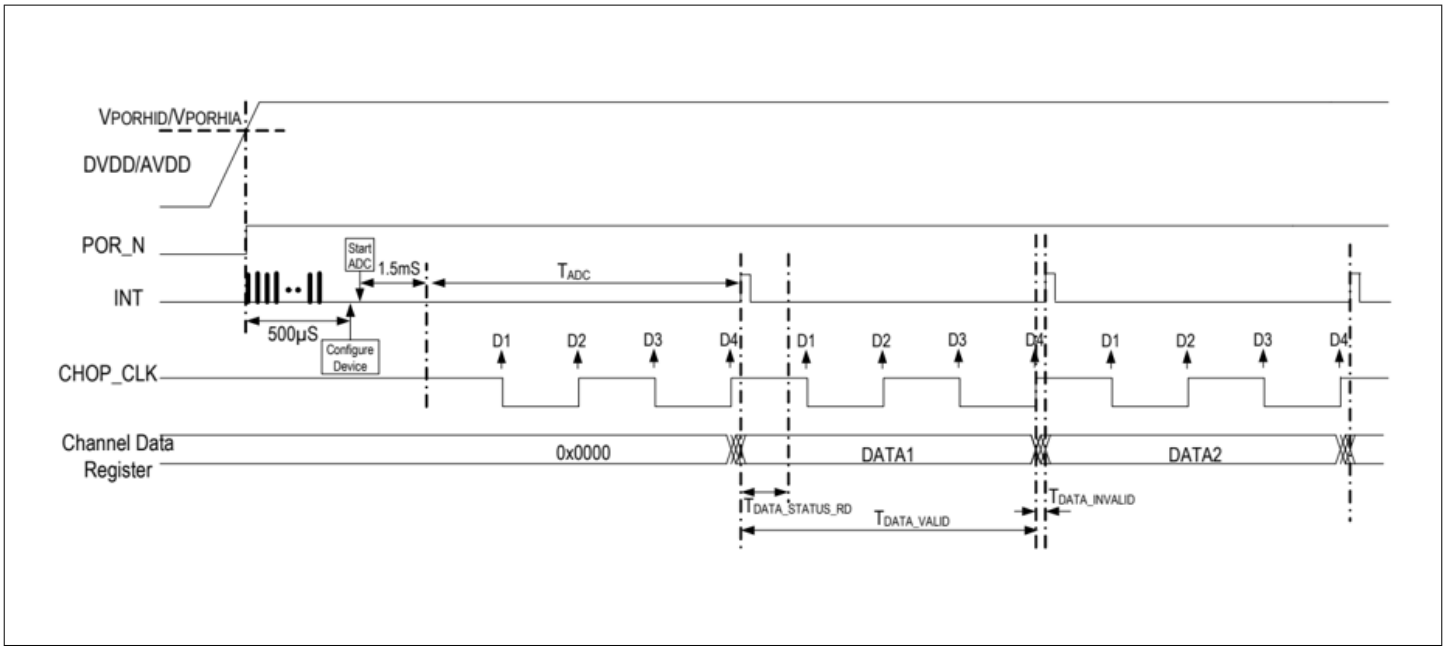


Figure 17 AS8512 device initialization sequence at power ON

Device initialization starts if the DVDD and AVDD supplies are switched ON and DVDD > V_{PORHID} . The duration period of initialization is 500 µ s and during this period, INT pin toggles at the rate of internal low power oscillator. Toggling on INT during the period of initialization should be ignored in the system. Device configuration and activation should be carried out only after the initialization period.

On ADC start, device enters into analog stabilization state and takes 1.5ms for oscillator and reference to settle. After this 1.5ms period, the first interrupt will occur after a time period of T_{ADC} .

$T_{DATA_STATUS_RD}$ is the time period during which the micro-controller should complete reading of data and status from the device. If reading is carried out beyond this time period, then, ADC performance will degrade for next sample generation. Status register gets cleared automatically only when micro-controller reads this register. Data in the

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channel registers is changed after T_{DATA_VALID} duration. Ensure that data channel registers and status registers are not read during the $T_{DATA_INVALID}$ duration.

Example:

Configuration registers are set as follows:

CLK_REG = 8'b0010_0000

DEC_REG_R1_I = 0100_0101

DEC_REG_R2_I = 1100_0101

FIR_CTL_REG_I = 0000_0100

ADC is configured to a data rate of 1 KHz, CHOP_CLK to 2KHz, and modulator clock to 1 MHz, decimation ratio of CIC1 = 64, and decimation ratio of CIC2 = 4. With these settings the various time periods as shown in the Figure 17 are as follows:

$T_{DATA_STATUS_RD}$ = 100 µs

($T_{DATA_STATUS_RD}$ = (1/mod_clk) * R1 * [((mod_clk/(2*chop_clk))*(1/R1)) - 2.5)]

$T_{DATA_INVALID}$ = 8 µs

T_{ADC} = 1 ms

T_{DATA_VALID} = T_{ADC} - $T_{DATA_INVALID}$ = 1 ms - 8 µs

CHOP_CLK and POR_N are internal signals of the device.

Table 35 provides valid combinations of modulator clock, chopper clock and decimation R1 and the corresponding values of $T_{DATA_STATUS_RD}$ and T_{ADC} .

Table 35 Valid combinations of modulator clock, chopper clock and decimation ratio R1

Modulator clock	Chopper frequency CHOP_CLK	Decimation ratio R1	$T_{DATA_STATUS_RD}$	TADC R2/ (2*CHOP_CLK) for R2=4
1.024 MHz	2 KHz	64	1 µs * 64 * [4 - 2.5] = 96 µs	1 ms
2.048 MHz	2 KHz	64	0.5 µs * 64 * [8 - 2.5] = 176 µs	1 ms
2.048 MHz	2 KHz	128	0.5 µs * 128 * [4 - 2.5] = 96 µs	1 ms
2.048 MHz	4 KHz	64	0.5 µs * 64 * [4 - 2.5] = 48 µs	0.5 ms

6.9.3 Soft-reset of device using bit D[7] of reset register 0x09

It is possible to soft-reset the device by writing "0" into D[7] bit of reset register at 0x09. On applying soft-reset, the device enters into initialization state and D[6] bit changes back to "1". The duration period of Initialization is 500 µs, and, during this period, INT pin toggles at the rate of internal low power oscillator. Toggling on INT during the period of initialization should be ignored in the system. Device configuration and activation should be carried out only after the initialization period. See Figure 18 for the timing details of the sequence of device initialization on soft-reset.

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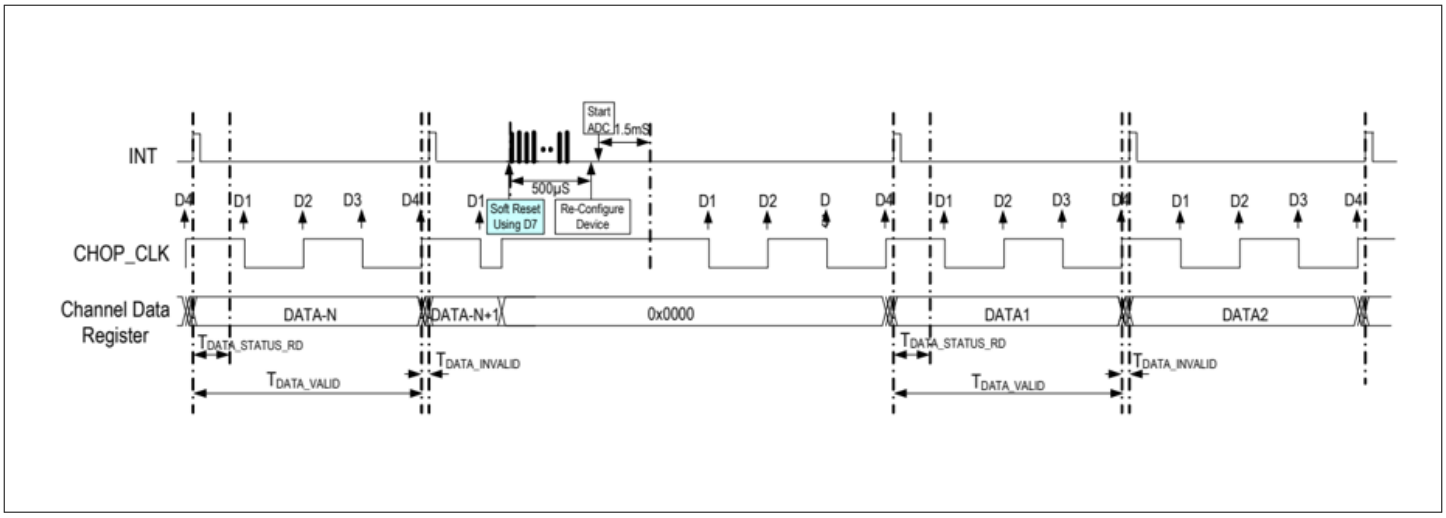


Figure 18 AS8512 device initialization sequence at soft-reset

6.9.4 Reconfiguring gain setting of PGA

Only PGA gain settings can be changed dynamically while ADC conversions are in progress. When PGA gain settings are changed, the first sample from the ADC is invalid. Ignore the first interrupt after the gain re-configuration. Valid data starts from the second interrupt onwards.

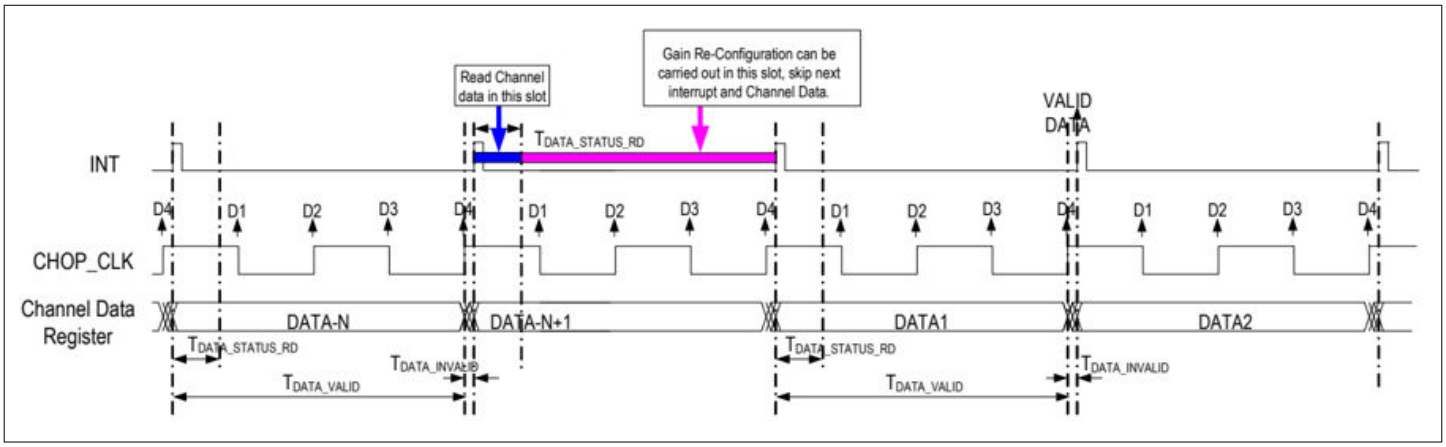


Figure 19 AS8512 - Re-configuration of gain setting of PGA

6.9.5 Configuring the device during normal mode

Following registers can be programmed dynamically when the device is in operational mode (normal mode).

- ACH_CTL_REG address is 0x17 for channel selection on the voltage measurement path.
- PGA_CTL_REG address is 0x13 for gain setting.
- PD_CTL_REG2 address is 0x15 for PGA bypass.
- ISC_CTL_REG address is 0x18 for current source programmability.

During the operation (normal mode) of the device, if any of the registers need to be programmed or changed other than the above mentioned registers, then it is required to STOP the device by writing into MOD_CTL_REG "STOP" bit and configure the device as per the requirements and start the device.

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6.10 Low side current measurement application

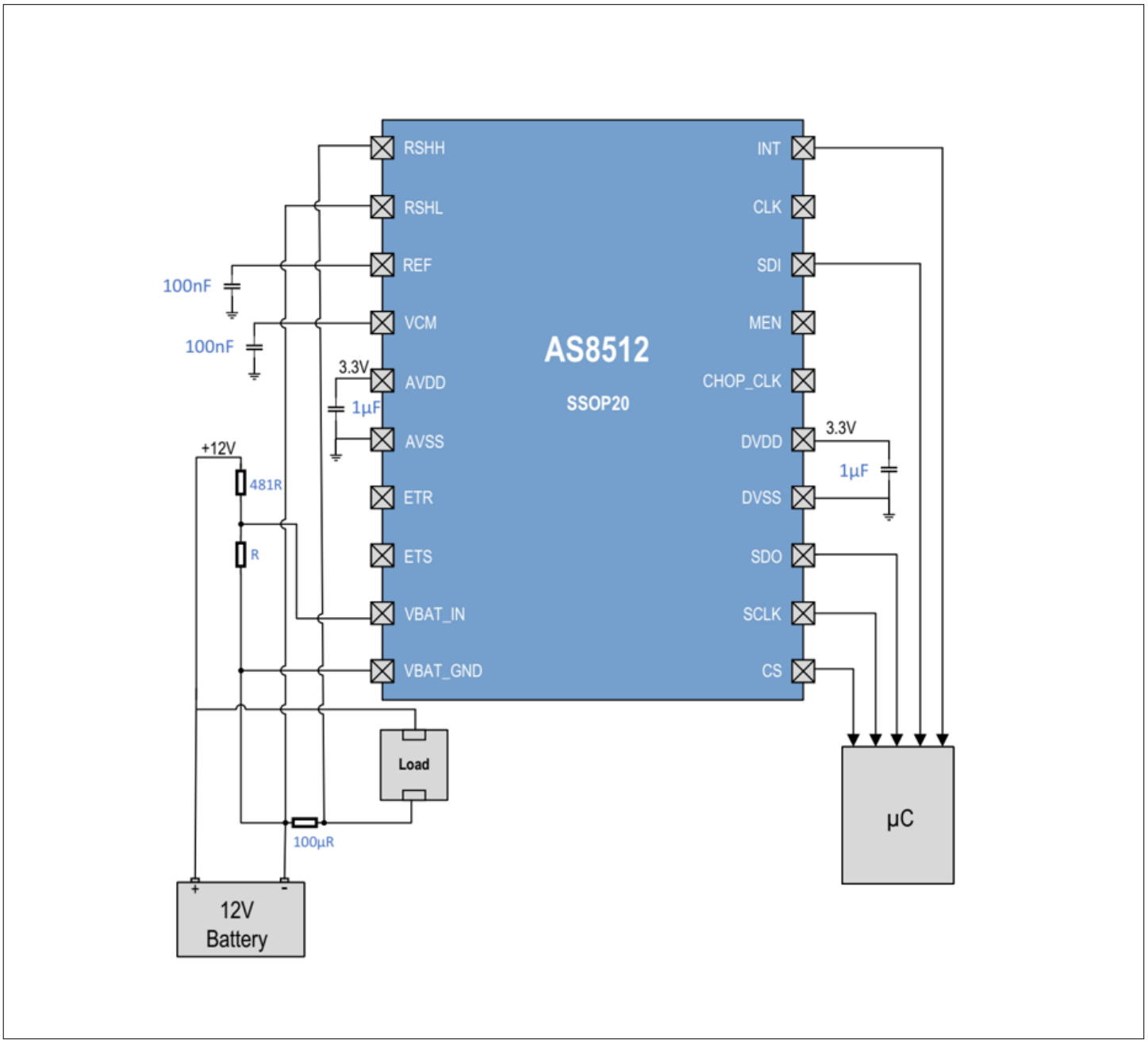
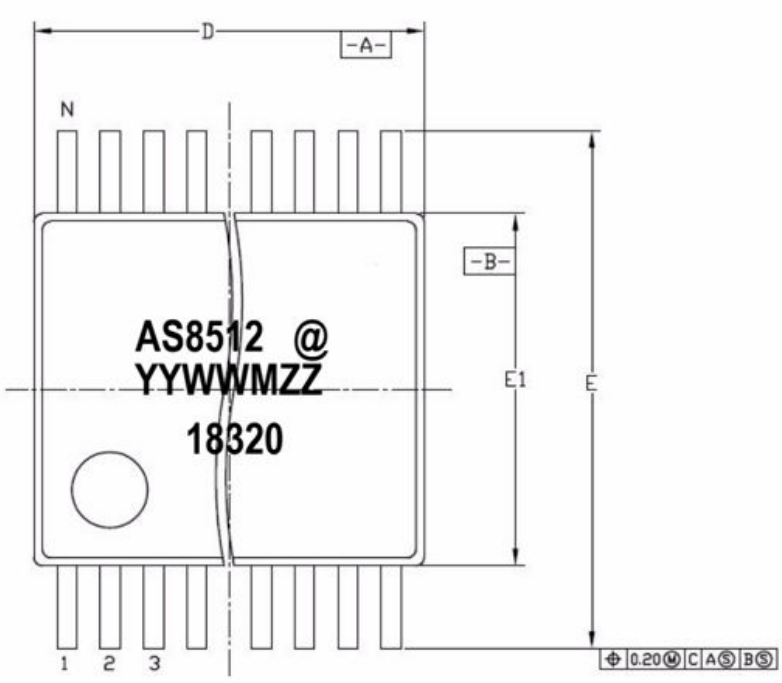


Figure 20 Application diagram

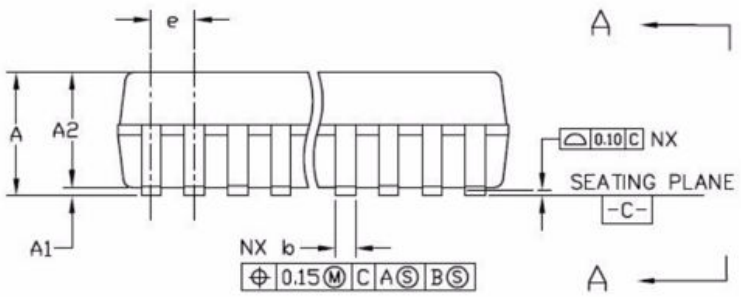
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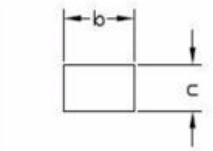
7 Package drawings & markings

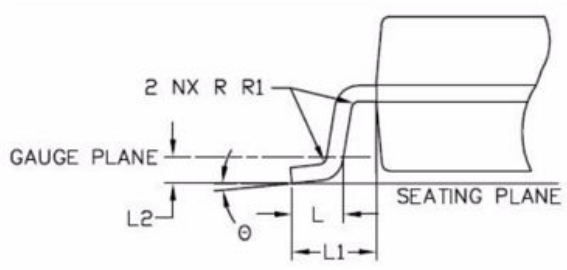
The product is available in a 20-pin SSOP package.



Symbol	Min	Nom	Max
A	-	-	2.00
A1	0.05	-	-
A2	1.65	1.75	1.85
b	0.22	-	0.38
c	0.09	-	0.25
D	6.90	7.20	7.50
E	7.40	7.80	8.20
E1	5.00	5.30	5.60
e	-	0.65 BSC	-
L	0.55	0.75	0.95
L1	-	1.25 REF	-
L2	-	0.25 BSC	-
R	0.09	-	-
θ	0°	4°	8°
N		20	







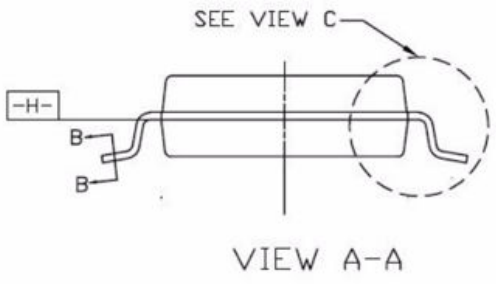


Figure 21 Drawings and dimensions

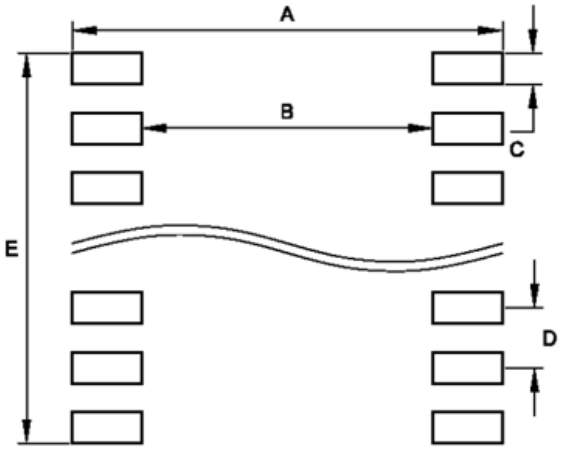
Note:
- *Dimensions & tolerancing conform to ASME Y14.5M-1994.*
- *All dimensions are in millimeters. Angles are in degrees.*

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Table 36 Marking: @YYWWMZZ

@	YY	WW	M	ZZ
Sublot identifier	Last two digits of the current year	Manufacturing week	Assembly plant identifier	Letters of free choice

7.1 Recommended PCB footprint



Recommended footprint data	
Symbol	mm
A	9.02
B	6.16
C	0.46
D	0.65
E	6.31

Figure 22 PCB footprint

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Revision history

Document revision	Date	Description of changes
1.00	2026-09-17	Document rebranded from ams-OSRAM to Infineon; technical specifications remain unchanged. **Legacy ams changes from previous revision to revision V1.00:** • Document security class is updated to "PUBLIC" in the footer

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