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**2.6A, 55V, 0.090 Ohm, N-Channel UltraFET Power MOSFET**



This N-Channel power MOSFET is manufactured using the innovative UltraFET® process. This advanced process technology achieves the

lowest possible on-resistance per silicon area, resulting in outstanding performance. This device is capable of withstanding high energy in the avalanche mode and the diode exhibits very low reverse recovery time and stored charge. It was designed for use in applications where power efficiency is important, such as switching regulators, switching converters, motor drivers, relay drivers, low-voltage bus switches, and power management in portable and battery-operated products.

Formerly developmental type TA75307.

**Ordering Information**

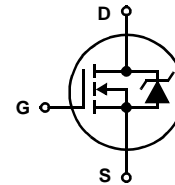
PART NUMBER	PACKAGE	BRAND
HUFA75307T3ST	SOT-223	5307

NOTE: HUFA75307T3ST is available only in tape and reel.

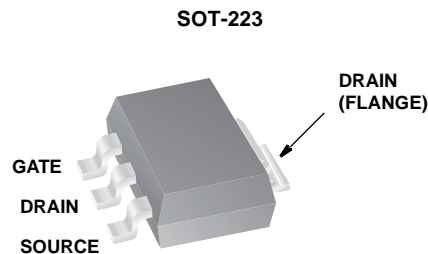
**Features**

- 2.6A, 55V
- Ultra Low On-Resistance,  $r_{DS(ON)} = 0.090\Omega$
- Diode Exhibits Both High Speed and Soft Recovery
- Temperature Compensating PSpice® Model
- Thermal Impedance SPICE Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Related Literature
  - TB334, "Guidelines for Soldering Surface Mount Components to PC Boards"

**Symbol**



**Packaging**



This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>  
Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.  
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

# HUFA75307T3ST

## Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

			UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$	55	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$	55	V
Gate to Source Voltage . . . . .	$V_{GS}$	$\pm 20V$	V
Drain Current			
Continuous (Figure 2) (Note 2) . . . . .	$I_D$	2.6	A
Pulsed Drain Current . . . . .	$I_{DM}$	Figure 5	
Pulsed Avalanche Rating . . . . .	$E_{AS}$	Figures 6, 14, 15	
Power Dissipation (Note 2) . . . . .	$P_D$	1.1	W
Derate Above $25^\circ\text{C}$ . . . . .		9.09	mW/ $^\circ\text{C}$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$	-55 to 150	$^\circ\text{C}$
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s. . . . .	$T_L$	300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334. . . . .	$T_{pkg}$	260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1.  $T_J = 25^\circ\text{C}$  to  $125^\circ\text{C}$ .

## Electrical Specifications $T_A = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	$BV_{DSS}$	$I_D = 250\mu\text{A}$ , $V_{GS} = 0V$ (Figure 11)	55	-	-	V
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250\mu\text{A}$ (Figure 10)	2	-	4	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 50V$ , $V_{GS} = 0V$	-	-	1	$\mu\text{A}$
		$V_{DS} = 45V$ , $V_{GS} = 0V$ , $T_A = 150^\circ\text{C}$	-	-	250	$\mu\text{A}$
Gate to Source Leakage Current	$I_{GSS}$	$V_{GS} = \pm 20V$	-	-	100	nA
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 2.6A$ , $V_{GS} = 10V$ (Figure 9)	-	0.070	0.090	$\Omega$
Turn-On Time	$t_{ON}$	$V_{DD} = 30V$ , $I_D \cong 2.6A$ , $R_L = 11.5\Omega$ , $V_{GS} = 10V$ , $R_{GS} = 25\Omega$	-	-	55	ns
Turn-On Delay Time	$t_{d(ON)}$		-	5	-	ns
Rise Time	$t_r$		-	30	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$		-	35	-	ns
Fall Time	$t_f$		-	25	-	ns
Turn-Off Time	$t_{OFF}$		-	-	90	ns
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $20V$	-	14	17	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0V$ to $10V$	-	8.3	10	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $2V$	-	0.6	0.8	nC
Gate to Source Gate Charge	$Q_{gs}$		-	1.00	-	nC
Gate to Drain "Miller" Charge	$Q_{gd}$		-	4.00	-	nC
Input Capacitance	$C_{ISS}$	$V_{DS} = 25V$ , $V_{GS} = 0V$ , $f = 1\text{MHz}$ (Figure 12)	-	250	-	pF
Output Capacitance	$C_{OSS}$		-	115	-	pF
Reverse Transfer Capacitance	$C_{RSS}$		-	30	-	pF
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Pad Area = $0.171\text{ in}^2$ (see note 2)	-	-	110	$^\circ\text{C/W}$
		Pad Area = $0.068\text{ in}^2$	-	-	128	$^\circ\text{C/W}$
		Pad Area = $0.026\text{ in}^2$	-	-	147	$^\circ\text{C/W}$

## Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	$V_{SD}$	$I_{SD} = 2.6A$	-	-	1.25	V
Reverse Recovery Time	$t_{rr}$	$I_{SD} = 2.6A$ , $dI_{SD}/dt = 100A/\mu\text{s}$	-	-	40	ns
Reverse Recovered Charge	$Q_{RR}$	$I_{SD} = 2.6A$ , $dI_{SD}/dt = 100A/\mu\text{s}$	-	-	50	nC

### NOTE:

2.  $110^\circ\text{C/W}$  measured using FR-4 board with  $0.171\text{ in}^2$  footprint for 1000s.

## Typical Performance Curves

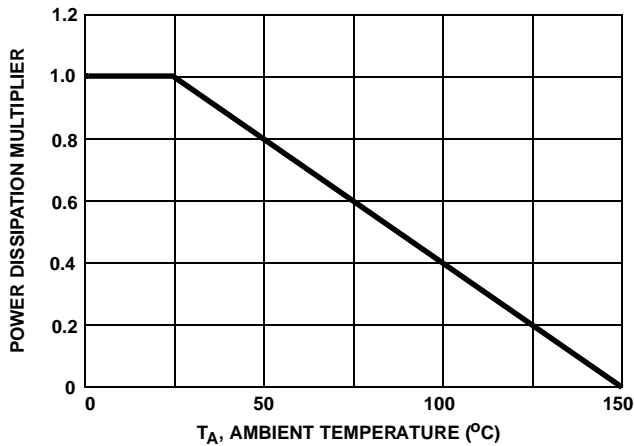


FIGURE 1. NORMALIZED POWER DISSIPATION vs AMBIENT TEMPERATURE

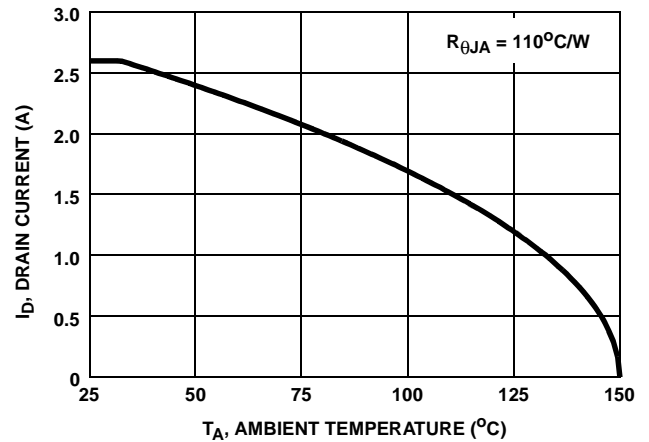


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs AMBIENT TEMPERATURE

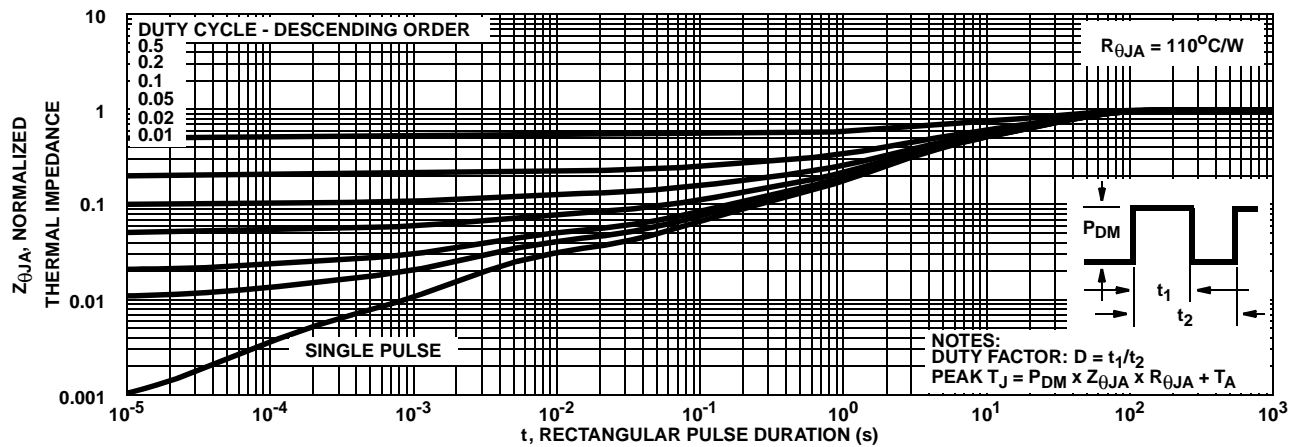


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

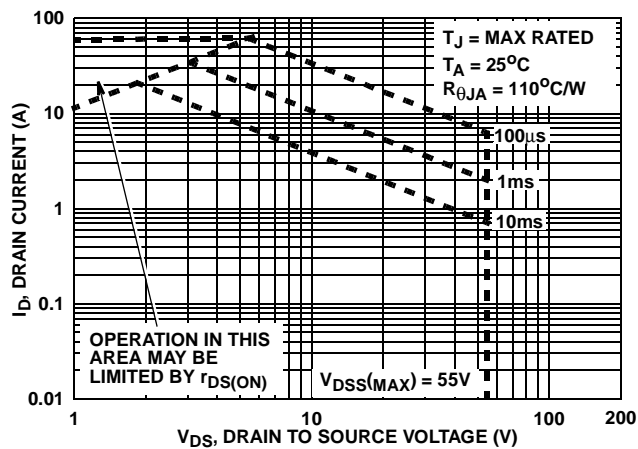


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

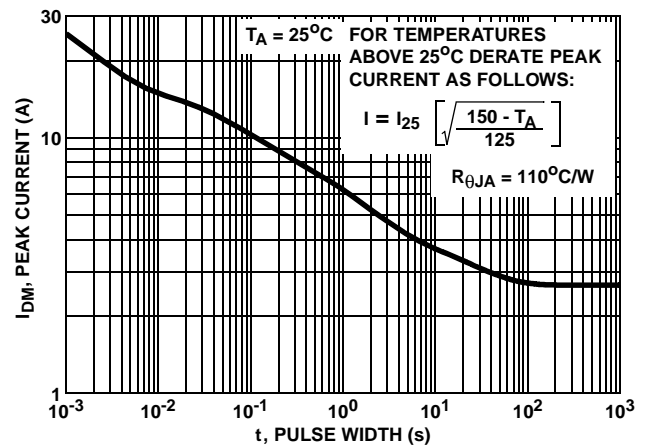
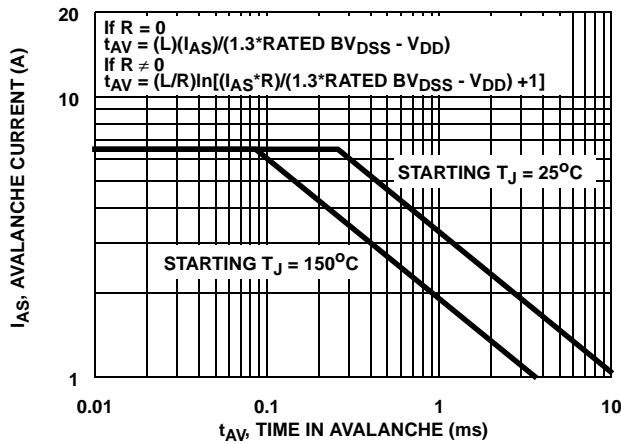
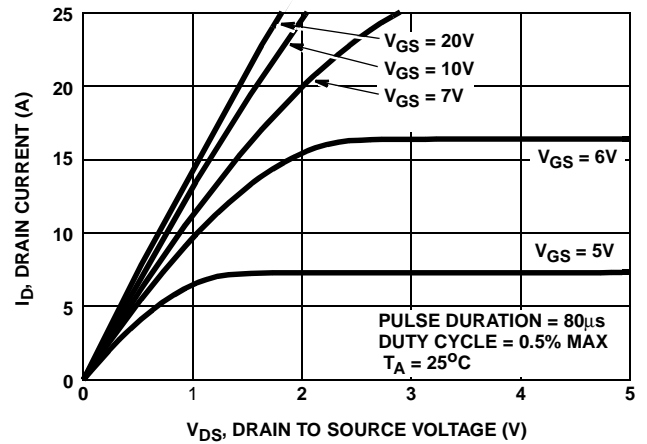


FIGURE 5. PEAK CURRENT CAPABILITY

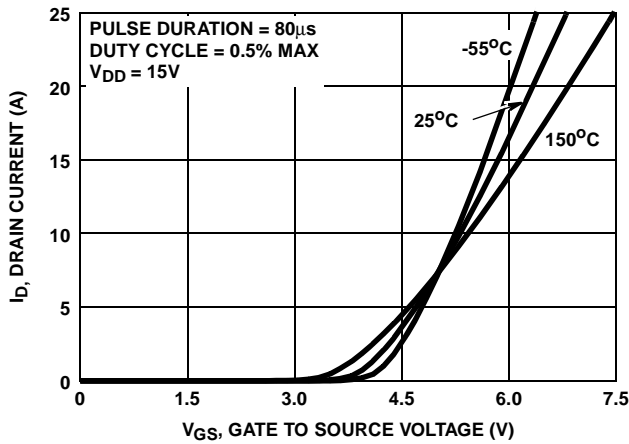
# Typical Performance Curves (Continued)



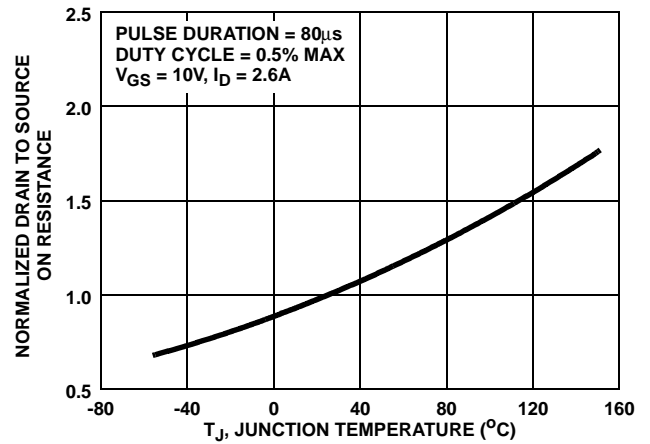
NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.  
**FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY**



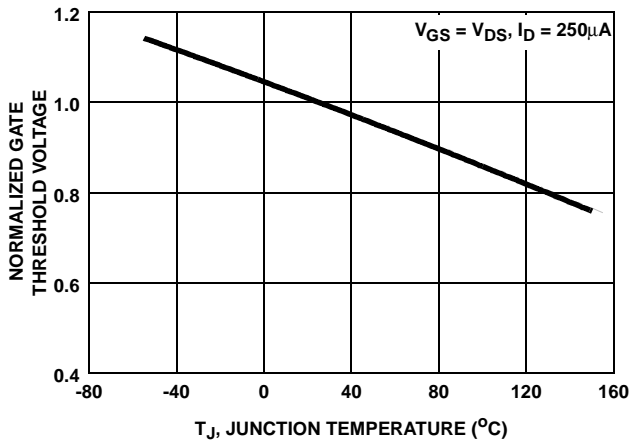
**FIGURE 7. SATURATION CHARACTERISTICS**



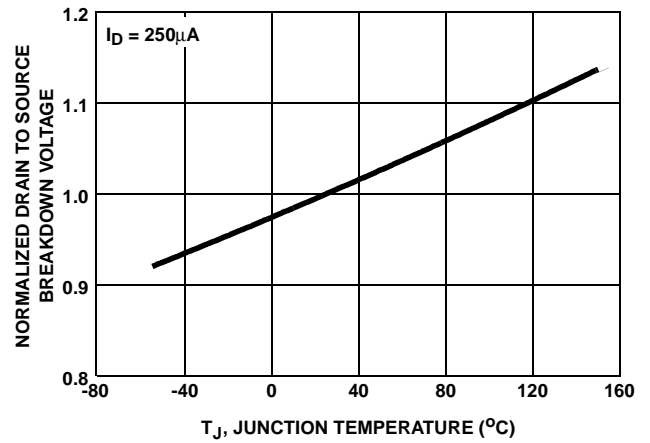
**FIGURE 8. TRANSFER CHARACTERISTICS**



**FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE**



**FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE**



**FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE**

## Typical Performance Curves (Continued)

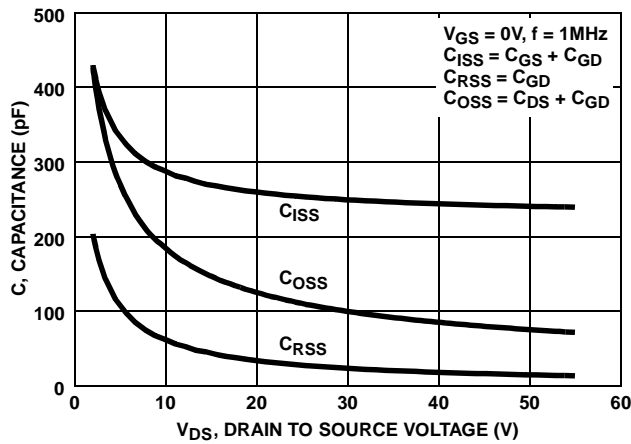
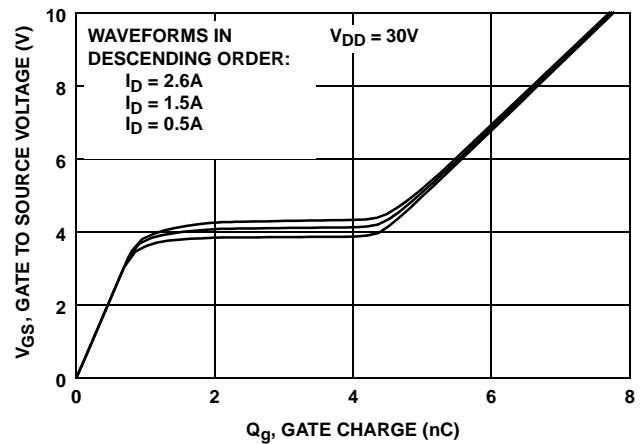


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms

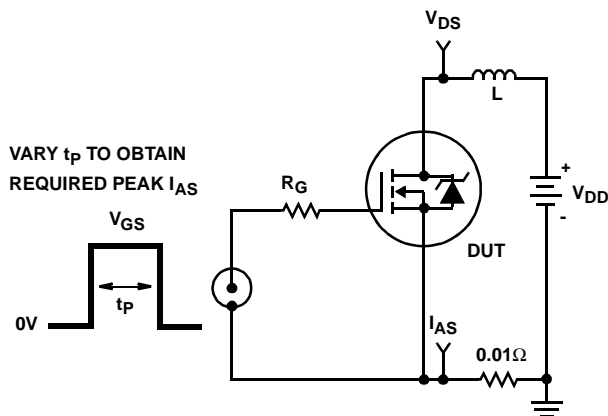


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

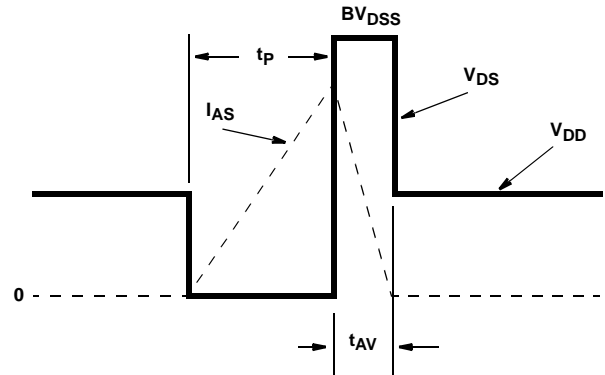


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

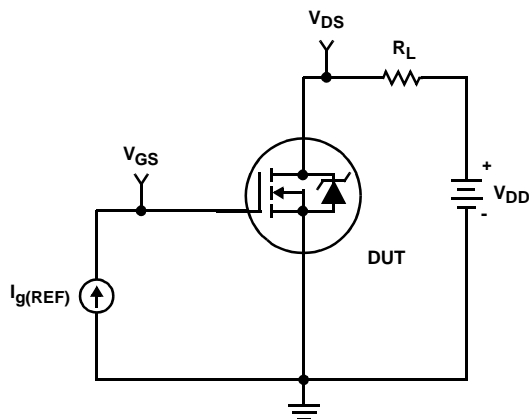


FIGURE 16. GATE CHARGE TEST CIRCUIT

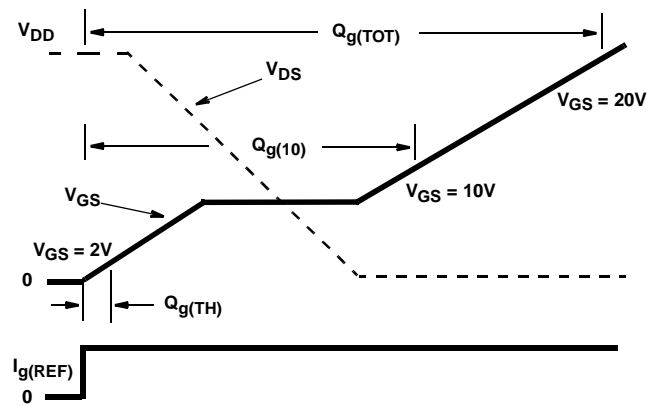


FIGURE 17. GATE CHARGE WAVEFORM

## Test Circuits and Waveforms (Continued)

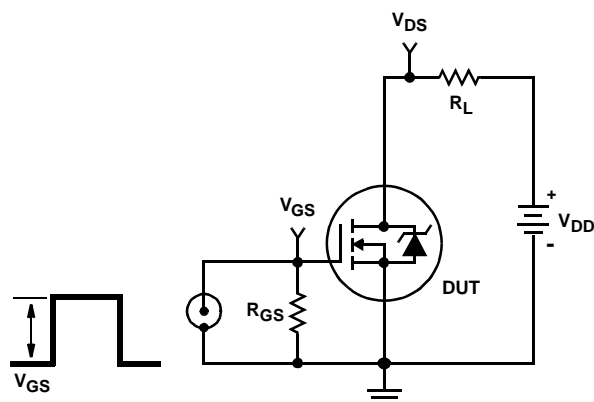


FIGURE 18. SWITCHING TIME TEST CIRCUIT

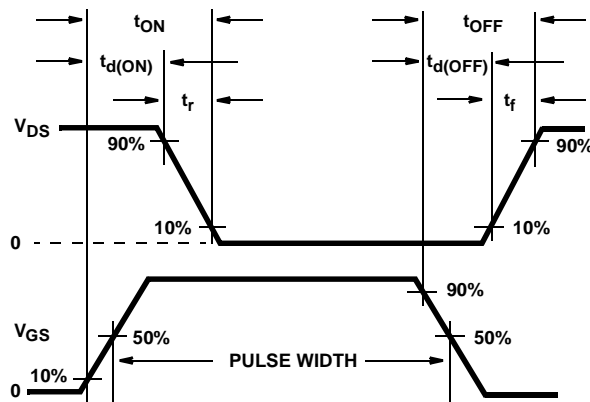


FIGURE 19. RESISTIVE SWITCHING WAVEFORMS

## Thermal Resistance vs. Mounting Pad Area

The maximum rated junction temperature,  $T_{J(MAX)}$ , and the thermal resistance of the heat dissipating path determines the maximum allowable device power dissipation,  $P_{D(MAX)}$ , in an application. Therefore the application's ambient temperature,  $T_A$  ( $^{\circ}C$ ), and thermal resistance  $R_{\theta JA}$  ( $^{\circ}C/W$ ) must be reviewed to ensure that  $T_{J(MAX)}$  is never exceeded. Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{D(MAX)} = \frac{(T_{J(MAX)} - T_A)}{R_{\theta JA}} \quad (EQ. 1)$$

In using surface mount devices such as the SOT-223 package, the environment in which it is applied will have a significant influence on the part's current and maximum power dissipation ratings. Precise determination of the  $P_{D(MAX)}$  is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

Fairchild provides thermal information to assist the designer's preliminary application evaluation. Figure 20 defines the  $R_{\theta JA}$  for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds

of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the Fairchild device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

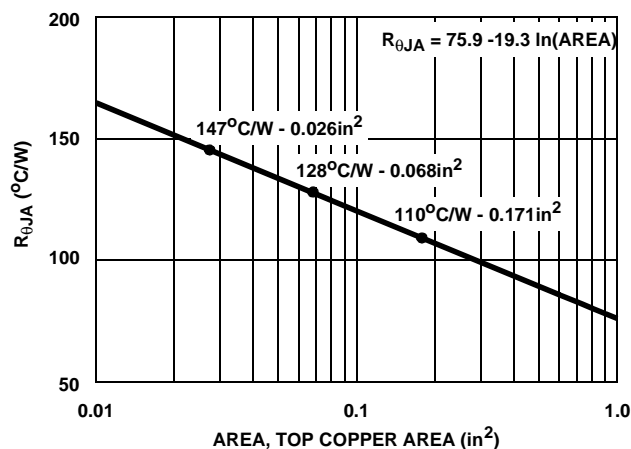


FIGURE 20. THERMAL RESISTANCE vs MOUNTING PAD AREA

Displayed on the curve are the three  $R_{\theta JA}$  values listed in the Electrical Specifications table. The three points were chosen to depict the compromise between the copper board area, the thermal resistance and ultimately the power dissipation,  $P_{D(MAX)}$ . Thermal resistances corresponding to other component side copper areas can be obtained from Figure 20 or by calculation using Equation 2. The area, in square inches is the top copper area including the gate and source pads.

$$R_{\theta JA} = 75.9 - 19.3 \times \ln(\text{Area}) \quad (EQ. 2)$$

# PSPICE Electrical Model

.SUBCKT HUFA75307T3ST 2 1 3 ; rev 7/25/97

CA 12 8 3.5e-10  
CB 15 14 3.7e-10  
CIN 6 8 2.26e-10

DBODY 7 5 DBODYMOD  
DBREAK 5 11 DBREAKMOD  
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 57.4  
EDS 14 8 5 8 1  
EGS 13 8 6 8 1  
ESG 6 10 6 8 1  
EVTHRES 6 21 19 8 1  
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
LGATE 1 9 1.4e-9  
LSOURCE 3 7 3.1e-10  
K1 LGATE LSOURCE 0.131

MMED 16 6 8 8 MMEDMOD  
MSTRO 16 6 8 8 MSTROMOD  
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
RDRAIN 50 16 RDRAINMOD 7.0e-3  
RGATE 9 20 1.9  
RLDRAIN 2 5 10  
RLGATE 1 9 14  
RLSOURCE 3 7 3  
RSLC1 5 51 RSLCMOD 1e-6  
RSLC2 5 50 1e3  
RSOURCE 8 7 RSOURCEMOD 5.6e-2  
RVTHRES 22 8 RVTHRESMOD 1  
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
S1B 13 12 13 8 S1BMOD  
S2A 6 15 14 13 S2AMOD  
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={{(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51)/(1e-6\*50),3))}}

.MODEL DBODYMOD D (IS = 2.6e-13 RS = 2.34e-2 IKF = 5.5 N = 0.995 TRS1 = 2.8e-3 TRS2 = 1.1e-5 CJO = 3.7e-10 TT = 3.5e-8 M = 0.46 + XTI = 5.5)

.MODEL DBREAKMOD D (RS = 0. 5IKF = 0.1 N = 1 TRS1 = 3e-3 TRS2 = -5e-5)

.MODEL DPLCAPMOD D (CJO = 5.6e-1 OIS = 1e-3 ON = 10 M = 0.92)

.MODEL MMEDMOD NMOS (VTO = 3.25 KP = 1.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1.9)

.MODEL MSTROMOD NMOS (VTO = 3.68 KP = 13.5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)

.MODEL MWEAKMOD NMOS (VTO = 2.83 KP = 0.03 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 19 RS = 0.1)

.MODEL RBREAKMOD RES (TC1 = 1.08e-3 TC2 = 5e-7)

.MODEL RDRAINMOD RES (TC1 = 1.7e-2 TC2 = 1e-4)

.MODEL RSLCMOD RES (TC1 = 1e-9 TC2 = 1e-4)

.MODEL RSOURCEMOD RES (TC1 = 3.3e-3 TC2 = 1e-9)

.MODEL RVTHRESMOD RES (TC1 = -1.9e-3 TC2 = -4e-6)

.MODEL RVTEMPMOD RES (TC1 = -2.9e-3 TC2 = 2.2e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -7.1 VOFF = -4)

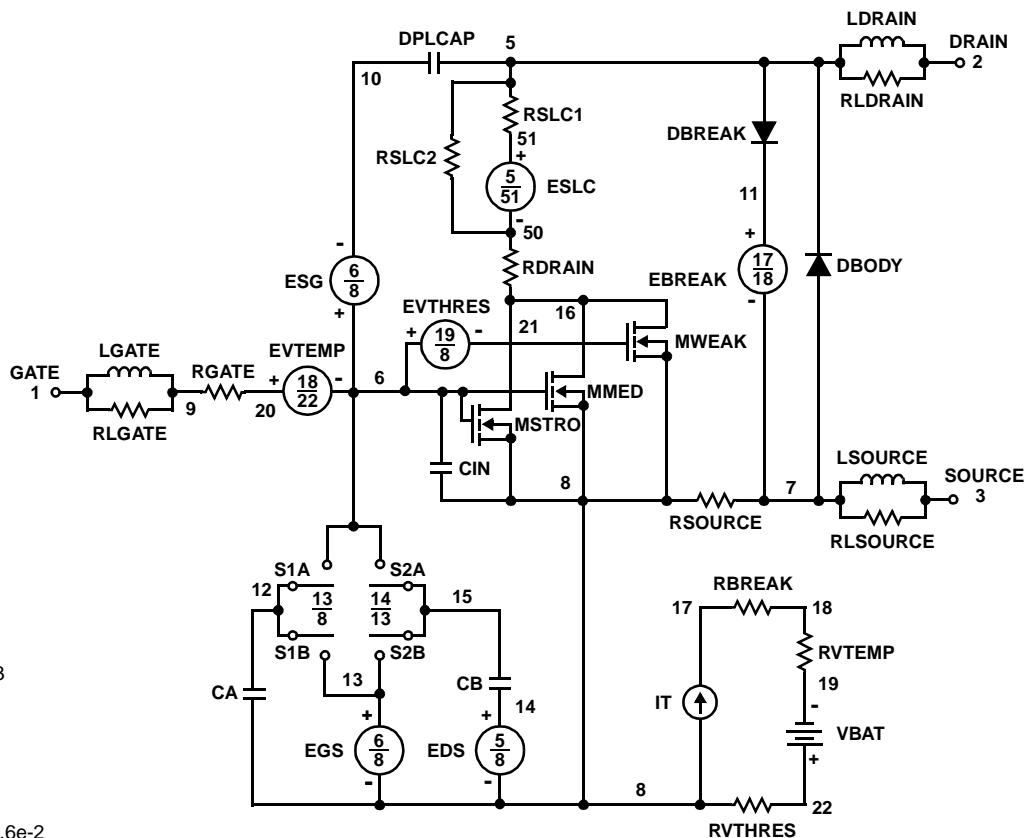
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4 VOFF = -7.1)

.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.01 VOFF = 1.9)

.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 1.9 VOFF = 0.01)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





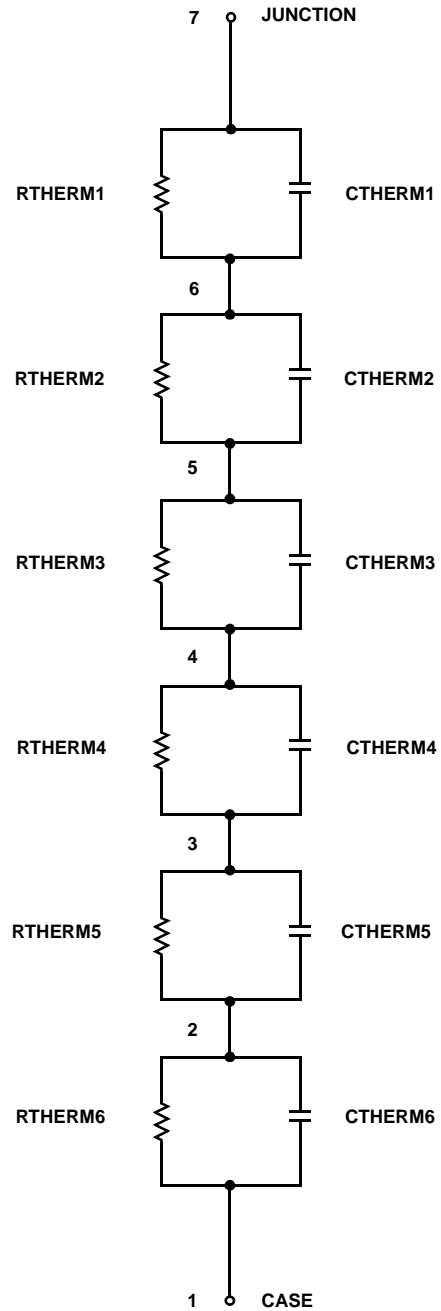
## SPICE Thermal Model

REV 15 Nov 97

HUFA75307T3ST

CTHERM1 7 6 7.5e-5  
 CHERM2 6 5 3.5e-4  
 CHERM3 5 4 1.2e-3  
 CHERM4 4 3 1.5e-2  
 CHERM5 3 2 6.9e-2  
 CHERM6 2 1 4.5e-1

RHERM1 7 6 7.5e-2  
 RHERM2 6 5 2.0e-1  
 RHERM3 5 4 1.2  
 RHERM4 4 3 3.3  
 RHERM5 3 2 28  
 RHERM6 2 1 90



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DenseTrench™	GTO™	Power247™	SuperSOT™-6	
DOMETM	HiSeC™	PowerTrench®	SuperSOT™-8	
EcoSPARK™	ISOPPLANAR™	QFET™	SyncFET™	
E <sup>2</sup> CMOS™	LittleFET™	QST™	TinyLogic™	
EnSigna™	MicroFET™	QT Optoelectronics™	TruTranslation™	
FACT™	MicroPak™	Quiet Series™	UHC™	
FACT Quiet Series™	MICROWIRE™	SILENT SWITCHER®	UltraFET®	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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Datasheet Identification	Product Status	Definition
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No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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Rev. H4

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