LP2995 DDR Termination Regulator

Check for Samples: LP2995

FEATURES

- **Low Output Voltage Offset**
- **Works with +5v, +3.3v and 2.5v Rails**
- **Source and Sink Current**
- **Low External Component Count**
- **No External Resistors Required**
- **Linear Topology**
- **Available in SOIC-8, SO PowerPAD-8 or WQFN-16 Packages**
- **Low Cost and Easy to Use**

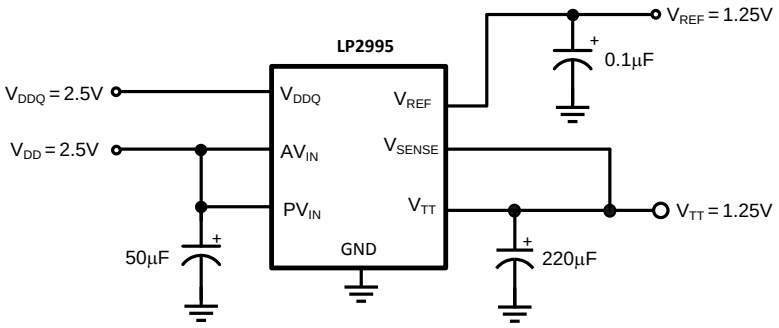
APPLICATIONS

- **DDR Termination Voltage**
- **SSTL-2**
- **SSTL-3**

DESCRIPTION

The LP2995 linear regulator is designed to meet the JEDEC SSTL-2 and SSTL-3 specifications for termination of DDR-SDRAM. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 1.5A continuous current and transient peaks up to 3A in the application as required for DDR-SDRAM termination. The LP2995 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DDR DIMMS.

Typical Application Circuit



Connection Diagram

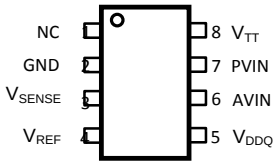


Figure 1. SOIC-8 (D0008A) Package Top View

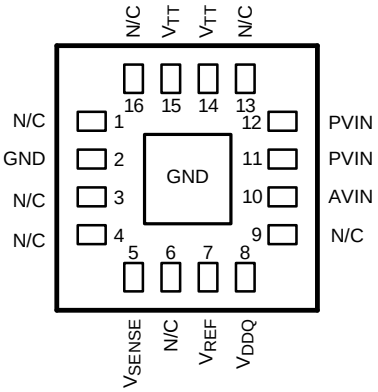


Figure 2. NHP- 16 Package Top View

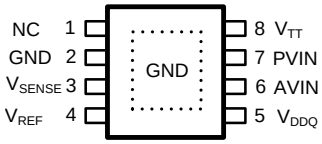


Figure 3. SO PowerPAD-8 (DDA0008A) Package Top View

PIN DESCRIPTIONS

SOIC-8 Pin or SO PowerPAD-8 Pin	WQFN Pin	Name	Function
1	1,3,4,6,9, 13,16	NC	No internal connection. Can be used for vias.
2	2	GND	Ground.
3	5	VSENSE	Feedback pin for regulating VTT.
4	7	VREF	Buffered internal reference voltage of VDDQ/2.
5	8	VDDQ	Input for internal reference equal to VDDQ/2.
6	10	AVIN	Analog input pin.
7	11, 12	PVIN	Power input pin.
8	14, 15	VTT	Output voltage for connection to termination resistors.
	EP	EP	Exposed pad thermal connection. Connect to Ground.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

AVIN to GND	−0.3V to +6V
PVIN to GND	-0.3V to AVIN
VDDQ (3)	−0.3V to +6V
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
SO PowerPAD-8 Thermal Resistance (θ_{JA})	43°C/W
SOIC-8 Thermal Resistance (θ_{JA})	151°C/W
WQFN-16 Thermal Resistance (θ_{JA})	51°C/W
Lead Temperature (Soldering, 10 sec)	260°C
ESD Rating (4)	1kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For ensured specifications and test conditions see Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) VDDQ voltage must be less than 2 x (AVIN - 1) or 6V, whichever is smaller.
(4) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Range

Junction Temp. Range (1)	0°C to +125°C
AVIN to GND	2.2V to 5.5V
PVIN to GND	2.2V to AVIN

(1) At elevated temperatures, devices must be derated based on thermal resistance. The device in the SOIC-8 package must be derated at θ_{JA} = 151° C/W junction to ambient with no heat sink. The device in the WQFN-16 must be derated at θ_{JA} = 51° C/W junction to ambient.

Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = 0°C to +125°C). Unless otherwise specified, AVIN = PVIN = 2.5V, VDDQ = 2.5V(1).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	V_{REF} Voltage	I_{REF_OUT} = 0mA	**1.21**	1.235	**1.26**	V
VOS_{VTT}	V_{TT} Output Voltage Offset	I_{OUT} = 0A (2)	−15 **−20**	0	15 **20**	mV
$\Delta V_{TT}/V_{TT}$	Load Regulation (3)	I_{OUT} = 0 to 1.5A		0.5		%
		I_{OUT} = 0 to −1.5A		−0.5		
Z_{VREF}	V_{REF} Output Impedance	I_{REF} = −5µA to +5µA		5		kΩ
Z_{VDDQ}	VDDQ Input Impedance			100		kΩ
I_q	Quiescent Current	I_{OUT} = 0A (4)		250	**400**	µA

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate TI's Average Outgoing Quality Level (AOQL).
(2) V_{TT} offset is the voltage measurement defined as V_{TT} subtracted from V_{REF}.
(3) Load regulation is tested by using a 10ms current pulse and measuring V_{TT}.
(4) Quiescent current defined as the current flow into AVIN.

Typical Performance Characteristics

Iq vs V_{IN} (25°C)

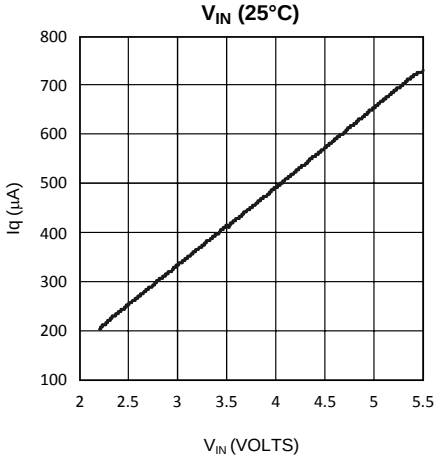


Figure 4.

Iq vs Temperature (V_{IN} = 2.5V)

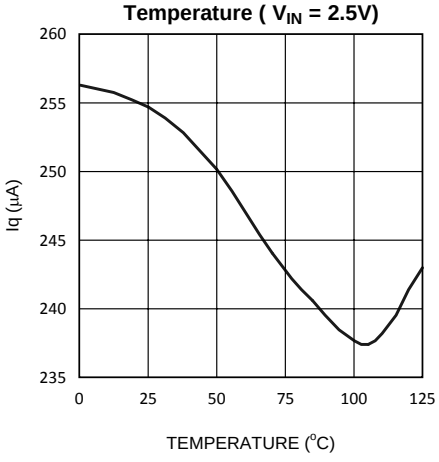


Figure 5.

Iq vs V_{IN} (0, 25, 85, and 125°C)

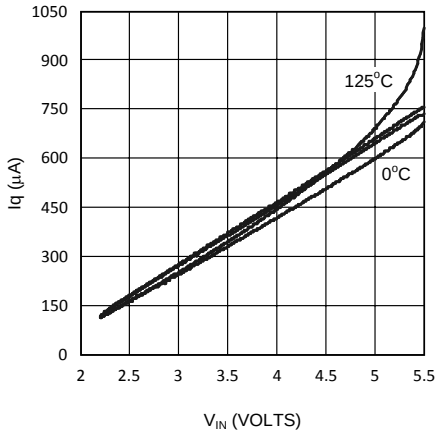


Figure 6.

V_{REF} vs I_{REF}

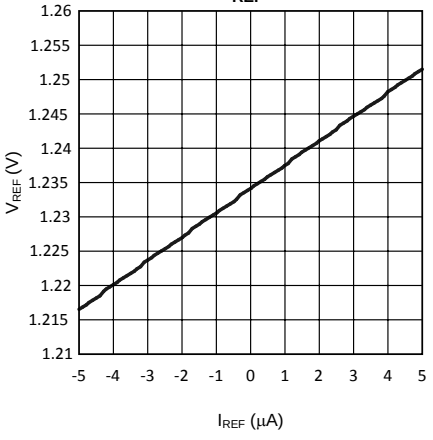


Figure 7.

V_{REF} vs Temperature (No Load)

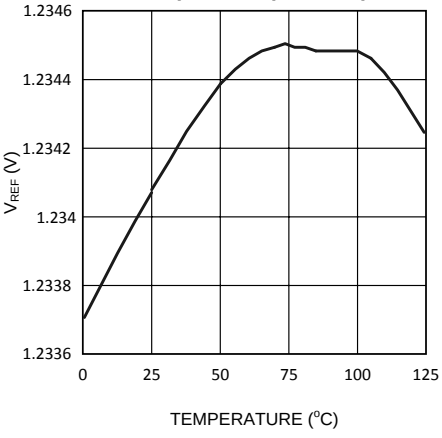


Figure 8.

V_{TT} vs I_{OUT} (0, 25, 85, and 125°C)

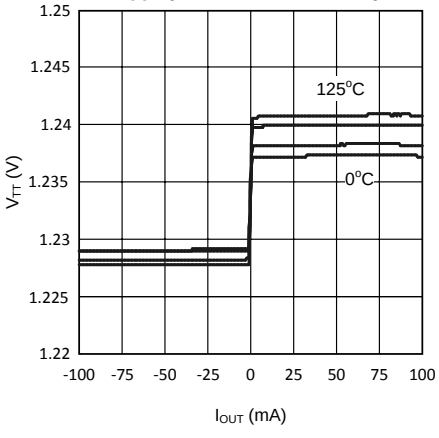


Figure 9.

Typical Performance Characteristics (continued)

V_{TT} vs I_{OUT}

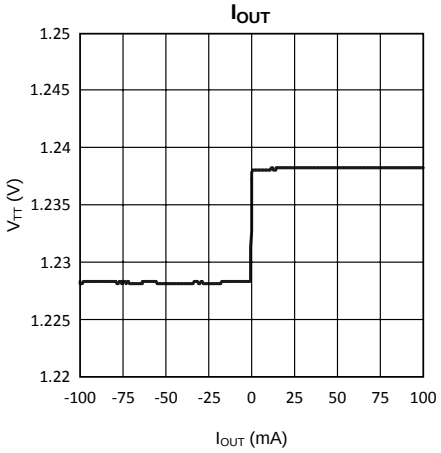


Figure 10.

Maximum Output Current (Sourcing) vs V_{IN} (VDDQ = 2.5)

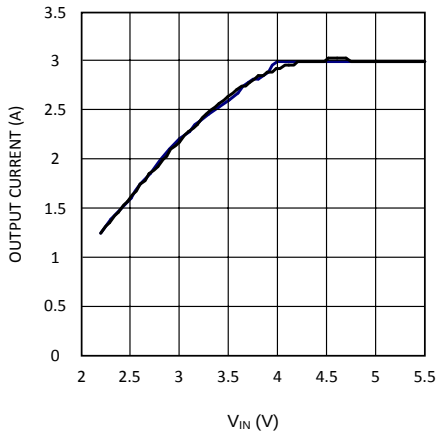


Figure 11.

Maximum Output Current (Sinking) vs V_{IN} (VDDQ = 2.5)

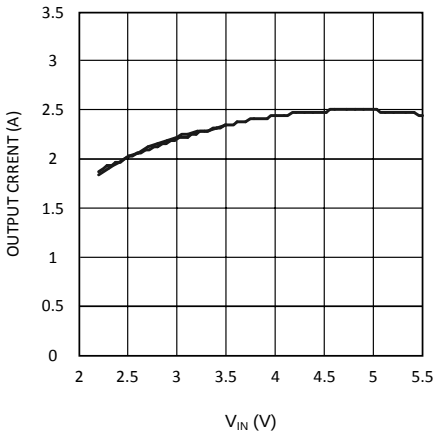
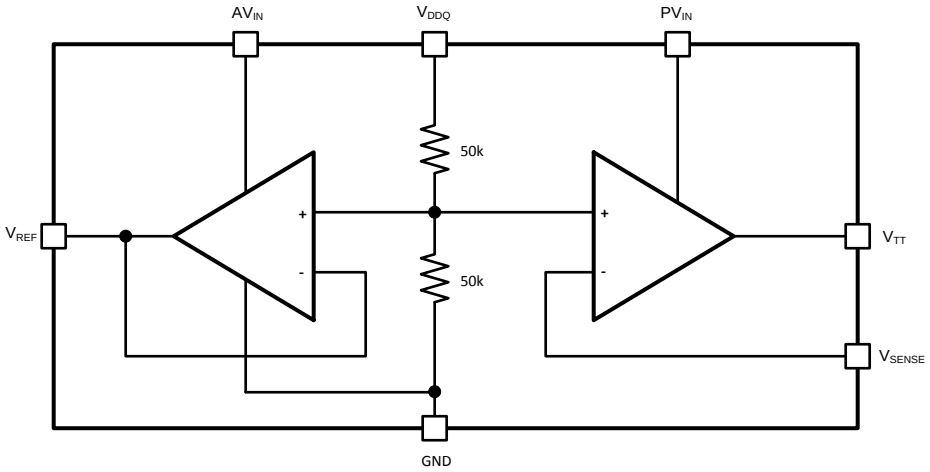


Figure 12.

Block Diagram



DETAILED DESCRIPTION

The LP2995 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-2 and SSTL-3. The LP2995 is capable of sinking and sourcing current at the output V_{TT}, regulating the voltage to equal VDDQ / 2. A buffered reference voltage that also tracks VDDQ / 2 is generated on the V_{REF} pin for providing a global reference to the DDR-SDRAM and Northbridge Chipset. V_{TT} is designed to track the V_{REF} voltage with a tight tolerance over the entire current range while preventing shoot through on the output stage.

Series Stub Termination Logic (SSTL) was created to improve signal integrity of the data transmission across the memory bus. This termination scheme is essential to prevent data error from signal reflections while transmitting at high frequencies encountered with DDR RAM. The most common form of termination is Class II single parallel termination. This involves using one Rs series resistor from the chipset to the memory and one Rt termination resistor. This implementation can be seen below in Figure 13.

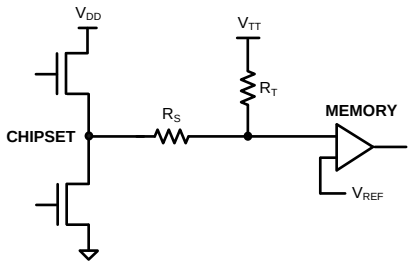


Figure 13.

Typical values for R_S and R_T are 25 Ohms although these can be changed to scale the current requirements from the LP2995. For determination of the current requirements of DDR-SDRAM termination please refer to the accompanying application notes.

Pin Descriptions

AVIN AND PVIN

AVIN and PVIN are the input supply pins for the LP2995. AVIN is used to supply all the internal control circuitry for the two op-amps and the output stage of V_{REF}. PVIN is used exclusively to provide the rail voltage for the output stage on the power operational amplifier used to create V_{TT}. For SSTL-2 applications AVIN and PVIN pins should be connected directly and tied to the 2.5V rail for optimal performance. This eliminates the need for bypassing the two supply pins separately.

VDDQ

VDDQ is the input that is used to create the internal reference voltage for regulating V_{TT} and V_{REF}. This voltage is generated by two internal 50kΩ resistors. This specifies that V_{TT} and V_{REF} will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense for the reference input. This can be achieved by connecting VDDQ directly to the 2.5V rail at the DIMM. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-2 applications VDDQ will be a 2.5V signal, which will create a 1.25V reference voltage on V_{REF} and a 1.25V termination voltage at V_{TT}. For SSTL-3 applications it may be desirable to have a different scaling factor for creating the internal reference voltage besides 0.5. For instance a typical value that is commonly used is to have the reference voltage equal VDDQ*0.45. This can be achieved by placing a resistor in series with the VDDQ pin to effectively change the resistor divider.

V_{SENSE}

The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the LP2995, then the long trace will cause a significant IR drop, resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus.

NOTE

If remote load regulation is not used, then the V_{SENSE} pin must still be connected to V_{TT}.

V_{REF}

V_{REF} provides the buffered output of the internal reference voltage VDDQ / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from V_{REF}. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 µF to 0.01 µF is recommended.

V_{TT}

V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The LP2995 is designed to handle peak transient currents of up to ± 3A with a fast transient response. The maximum continuous current is a function of V_{IN} and can be viewed in the Typical Performance Characteristics section. If a transient is expected to last above the maximum continuous current rating for a significant amount of time then the output capacitor should be sized large enough to prevent an excessive voltage drop. Despite the fact that the LP2995 is designed to handle large transient output currents it is not capable of handling these for long durations, under all conditions. The reason for this is the standard packages are not able to thermally dissipate the heat as a result of the internal power loss. If large currents are required for longer durations, then care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal derating should always be used (please refer to the Thermal Dissipation section).

Component Selection

INPUT CAPACITOR

The LP2995 does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 50 µF. Ceramic capacitors can also be used, a value in the range of 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2995 is placed close to the bulk capacitance from the output of the 2.5V DC-DC converter.

OUTPUT CAPACITOR

The LP2995 has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of V_{TT}. As a general recommendation the output capacitor should be sized above 100 µF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

- AL - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP2995. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.
- Ceramic - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100 µF range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.
- Hybrid - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and

performance are critical, although their cost is typically higher than any other capacitor.

Capacitor recommendations for different application circuits can be seen in the accompanying application notes with supporting evaluation boards.

Thermal Dissipation

Since the LP2995 is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise (T_{Rmax}) can be calculated given the maximum ambient temperature (T_{Amax}) of the application and the maximum allowable junction temperature (T_{Jmax}).

$$T_{Rmax} = T_{Jmax} - T_{Amax}$$

From this equation, the maximum power dissipation (P_{Dmax}) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA}$$

The θ_{JA} of the LP2995 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the θ_{JA} of the SOIC-8 is 163°C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 151.2°C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard. Figure 14 shows how the θ_{JA} varies with airflow for the two boards mentioned.

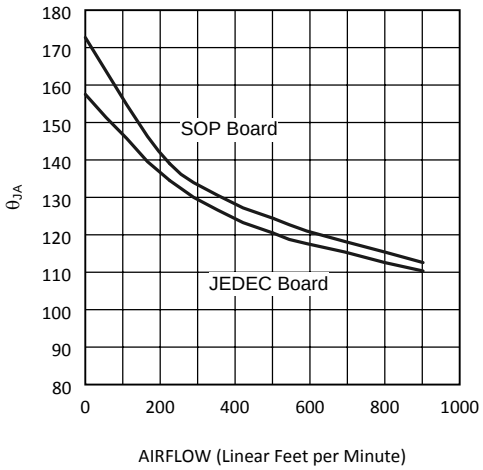


Figure 14. θ_{JA} vs Airflow (SOIC-8)

Layout is also extremely critical to maximize the output current with the WQFN package. By simply placing vias under the DAP the θ_{JA} can be lowered significantly. Figure 15 shows the WQFN thermal data when placed on a 4-layer JEDEC board with copper thickness of 0.5/1/1/0.5 oz. The number of vias, with a pitch of 1.27 mm, has been increased to the maximum of 4 where a θ_{JA} of 50.41°C/W can be obtained. Via wall thickness for this calculation is 0.036 mm for 1oz. Copper.

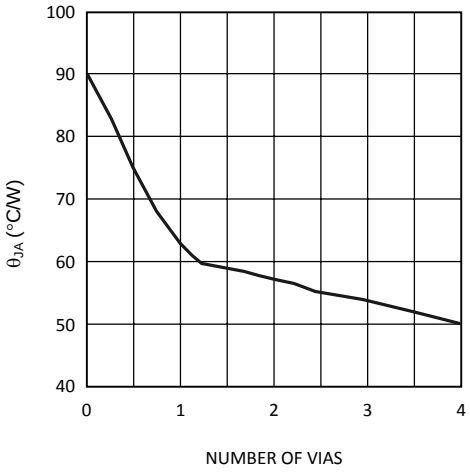


Figure 15. WQFN-16 θ_{JA} vs # of Vias (4 Layer JEDEC Board))

Additional improvements in lowering the θ_{JA} can also be achieved with a constant airflow across the package. Maintaining the same conditions as above and utilizing the 2x2 via array, Figure 16 shows how the θ_{JA} varies with airflow.

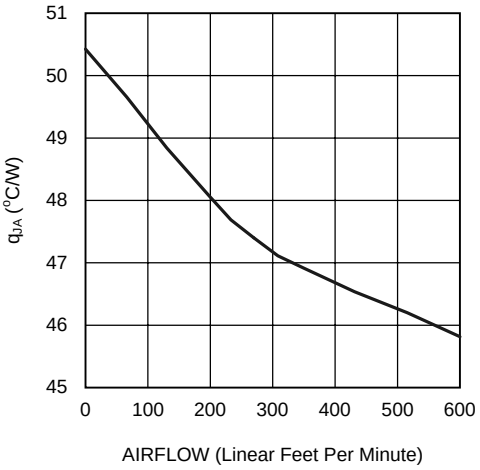


Figure 16. θ_{JA} vs Airflow Speed (JEDEC Board with 4 Vias)

Typical Application Circuits

The typical application circuit used for SSTL-2 termination schemes with DDR-SDRAM can be seen in Figure 17.

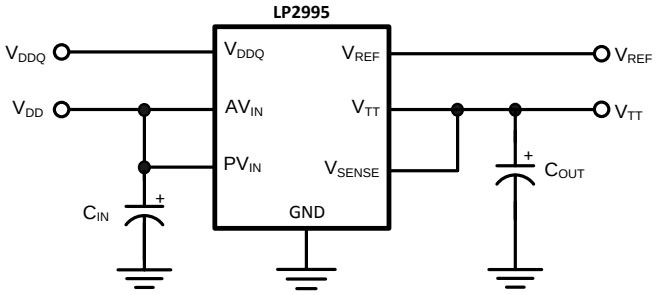


Figure 17. SSTL-2 Implementation

For SSTL-3 and other applications it may be desirable to change internal reference voltage scaling from VDDQ * 0.5. An external resistor in series with the VDDQ pin can be used to lower the reference voltage. Internally two 50 kΩ resistors set the output V_{TT} to be equal to VDDQ * 0.5. The addition of a 11.1 kΩ external resistor will change the internal reference voltage causing the two outputs to track VDDQ * 0.45. An implementation of this circuit can be seen in Figure 18.

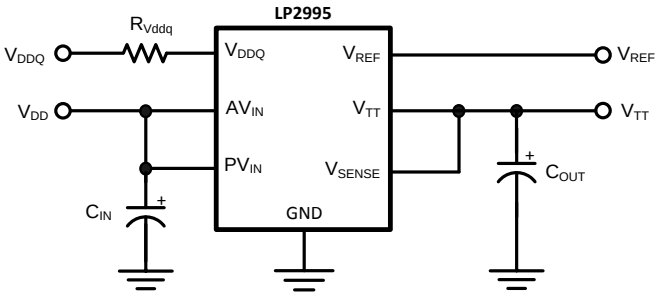


Figure 18. SSTL-3 Implementation

Another application that is sometimes required is to increase the V_{TT} output voltage from the scaling factor of VDDQ * 0.5. This can be accomplished independently of V_{REF} by using a resistor divider network between V_{TT}, V_{SENSE} and Ground. An example of this circuit can be seen in Figure 19.

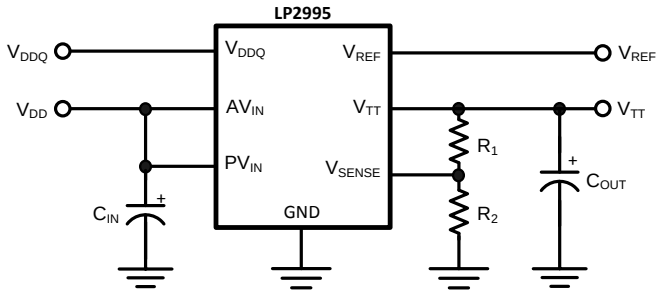


Figure 19.

PCB Layout Considerations

1. AVIN and PVIN should be tied together for optimal performance. A local bypass capacitor should be placed as close as possible to the PVIN pin.
2. GND should be connected to a ground plane with multiple vias for improved thermal performance.
3. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
4. VDDQ can be connected remotely to the VDDQ rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
5. V_{REF} should be bypassed with a 0.01 µF or 0.1 µF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the V_{REF} pin.

REVISION HISTORY

Changes from Revision L (March 2013) to Revision M	Page
• Changed layout of National Data Sheet to TI format	11

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2995LQ/NOPB	ACTIVE	WQFN	NHP	16	1000	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	L00005B	Samples
LP2995M/NOPB	ACTIVE	SOIC	D	8	95	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	2995M	Samples
LP2995MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	LP2995	Samples
LP2995MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	RoHS & Green	SN	Level-3-260C-168 HR	0 to 125	LP2995	Samples
LP2995MX/NOPB	ACTIVE	SOIC	D	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM	0 to 125	2995M	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

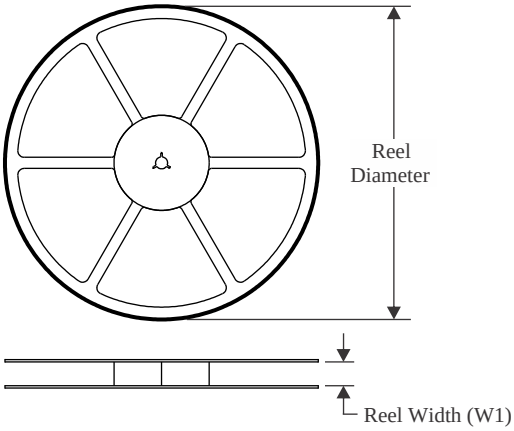
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

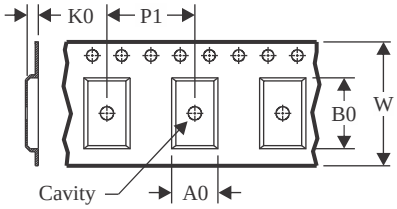
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

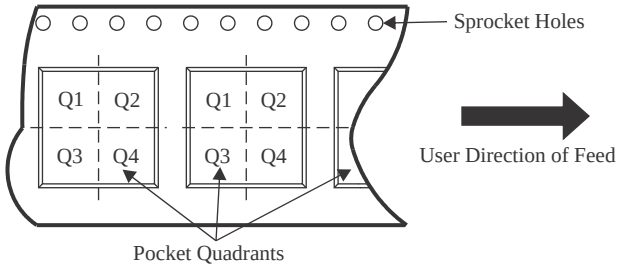


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

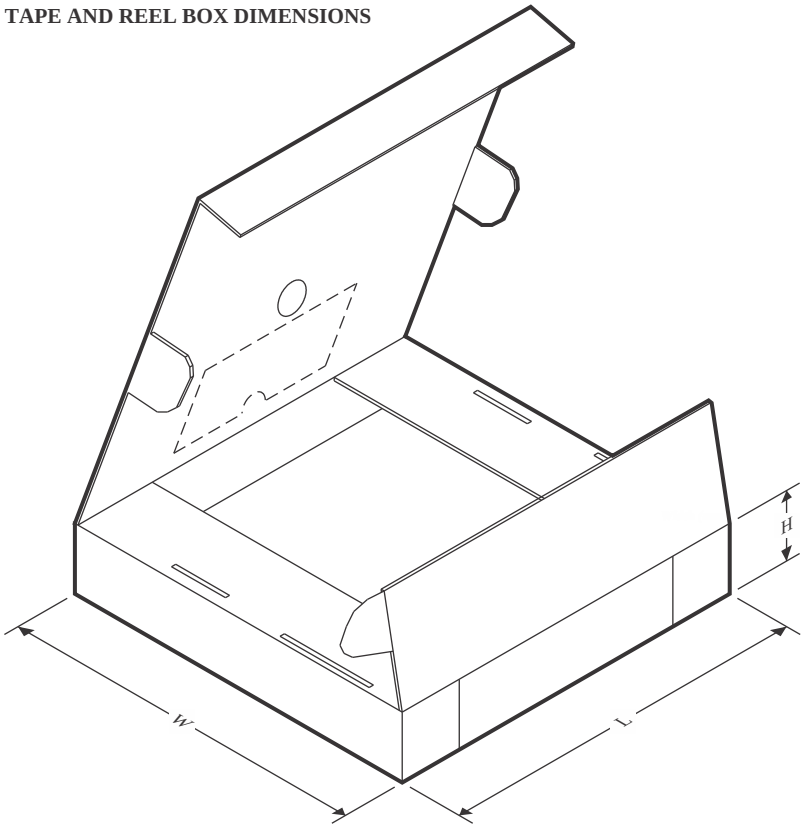
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2995LQ/NOPB	WQFN	NHP	16	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1
LP2995MRX/NOPB	SO PowerPAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2995MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

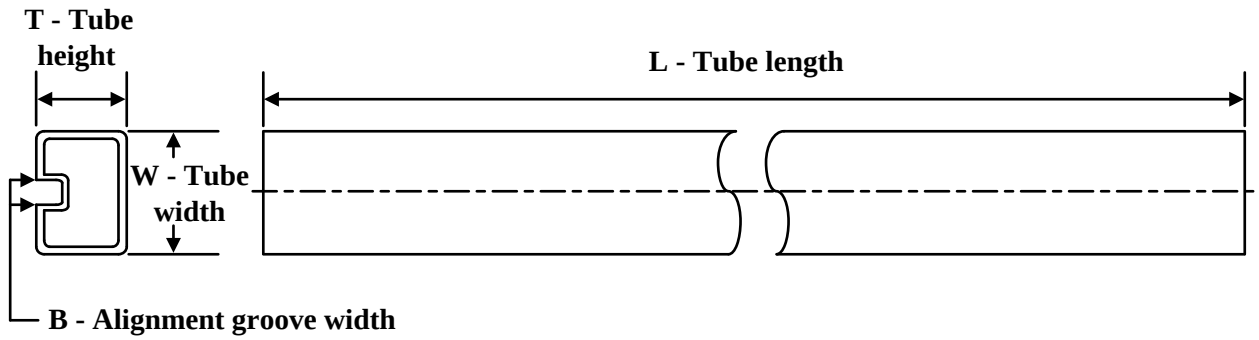
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2995LQ/NOPB	WQFN	NHP	16	1000	208.0	191.0	35.0
LP2995MRX/NOPB	SO PowerPAD	DDA	8	2500	356.0	356.0	35.0
LP2995MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

TUBE



*All dimensions are nominal

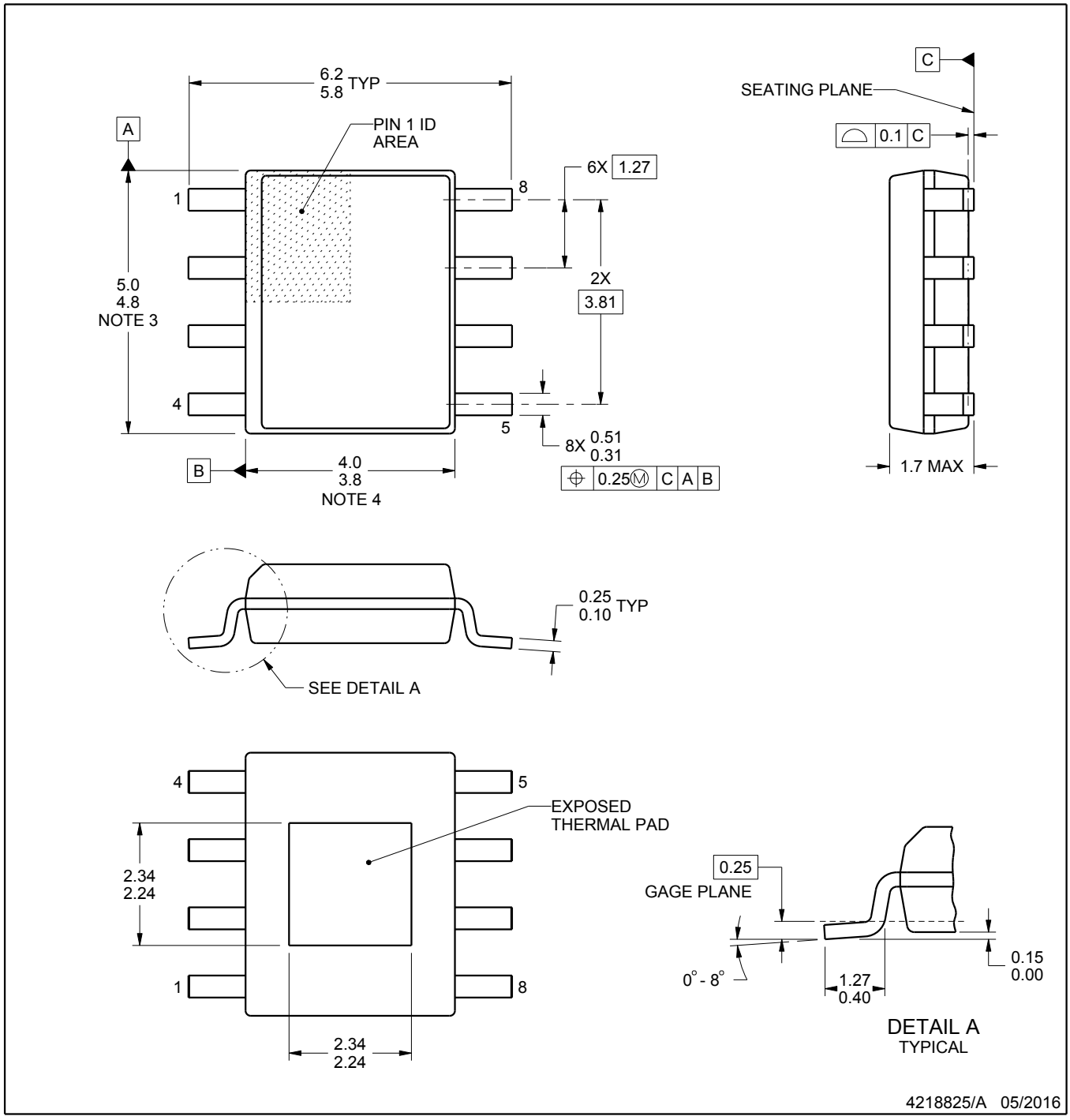
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
LP2995M/NOPB	D	SOIC	8	95	495	8	4064	3.05
LP2995MR/NOPB	DDA	HSOIC	8	95	495	8	4064	3.05

PACKAGE OUTLINE

DDA0008A

PowerPAD™ SOIC - 1.7 mm max height

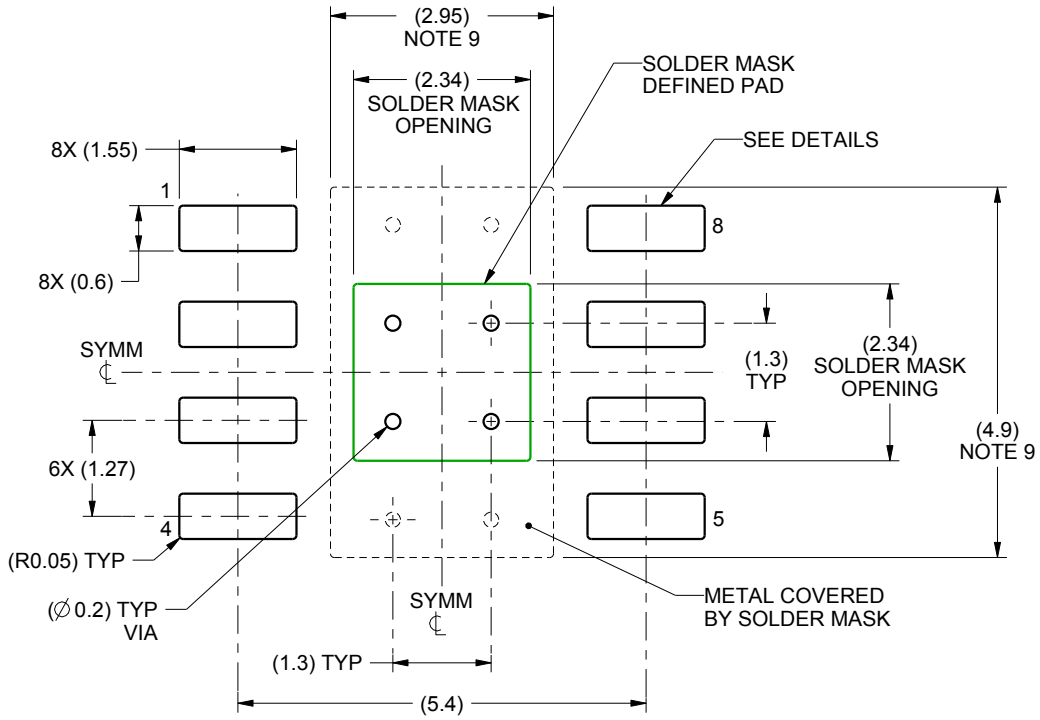
PLASTIC SMALL OUTLINE



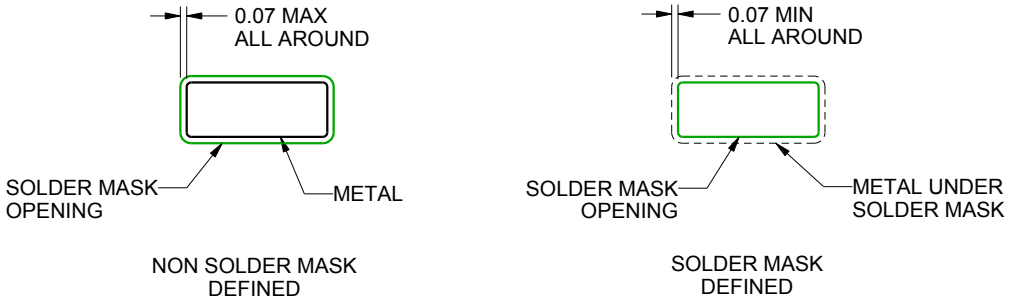
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X

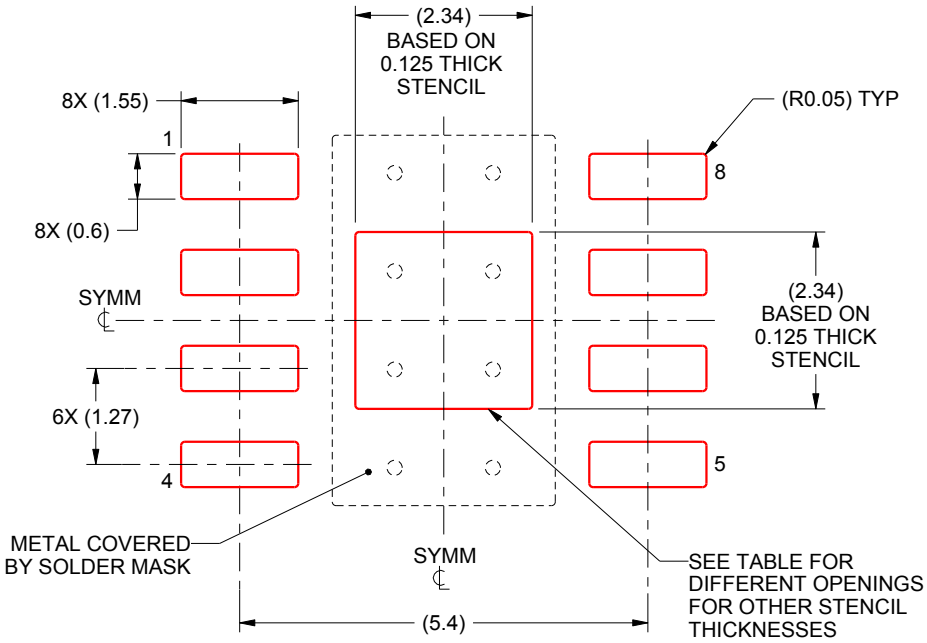


SOLDER MASK DETAILS

4218825/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

4218825/A 05/2016

NOTES: (continued)

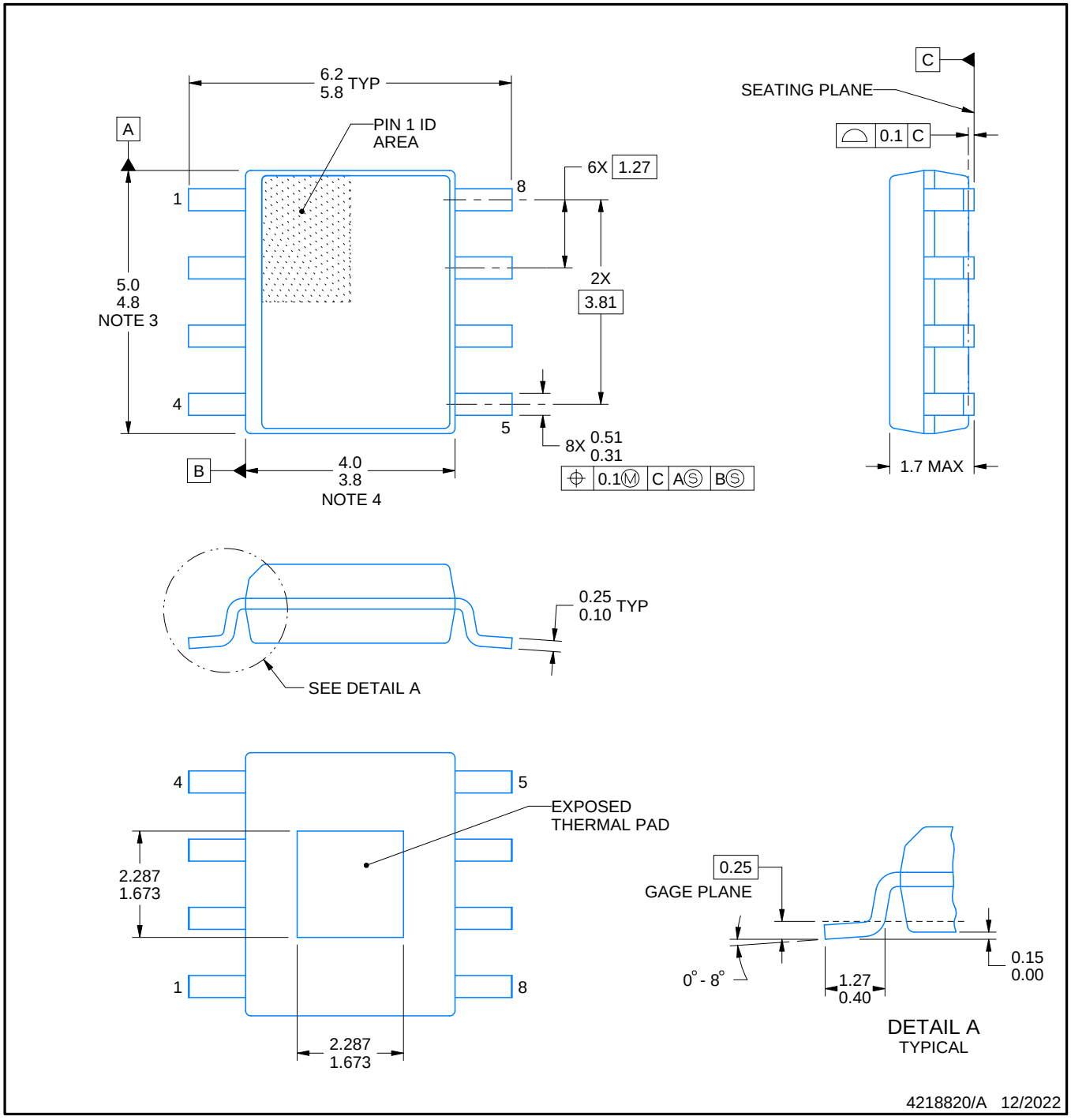
11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DDA0008D

PowerPAD™ SOIC - 1.7 mm max height

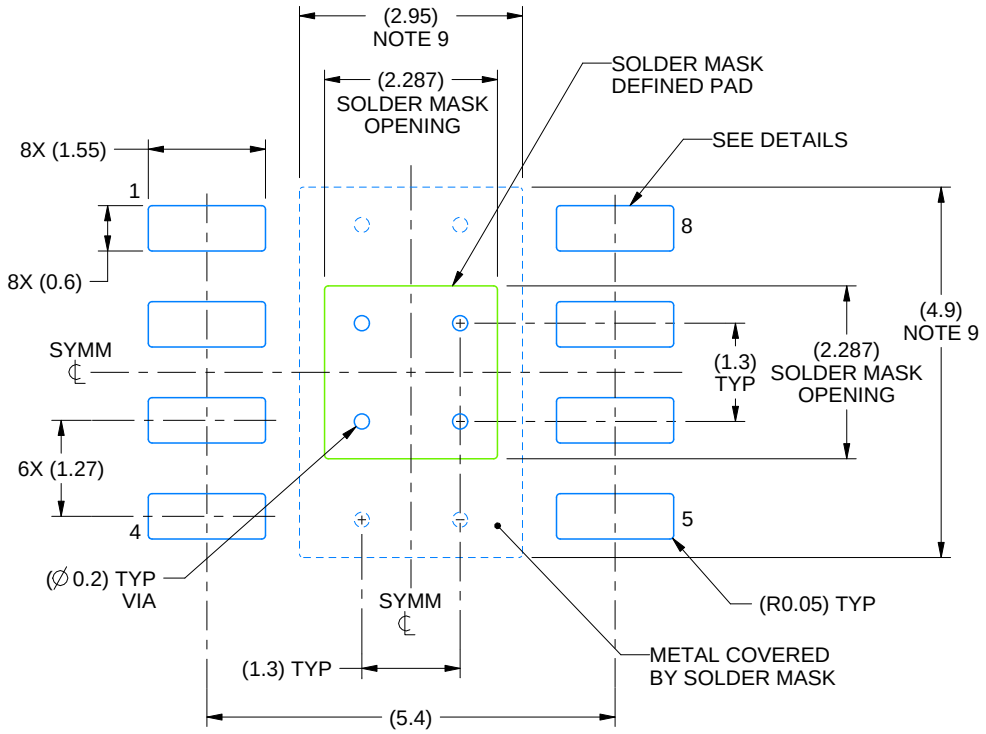
PLASTIC SMALL OUTLINE



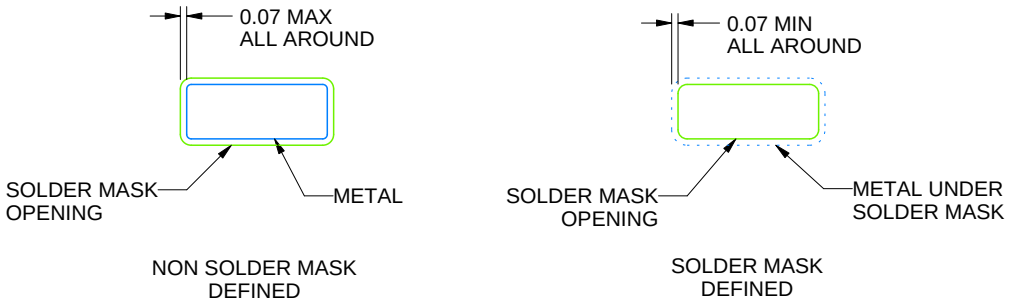
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

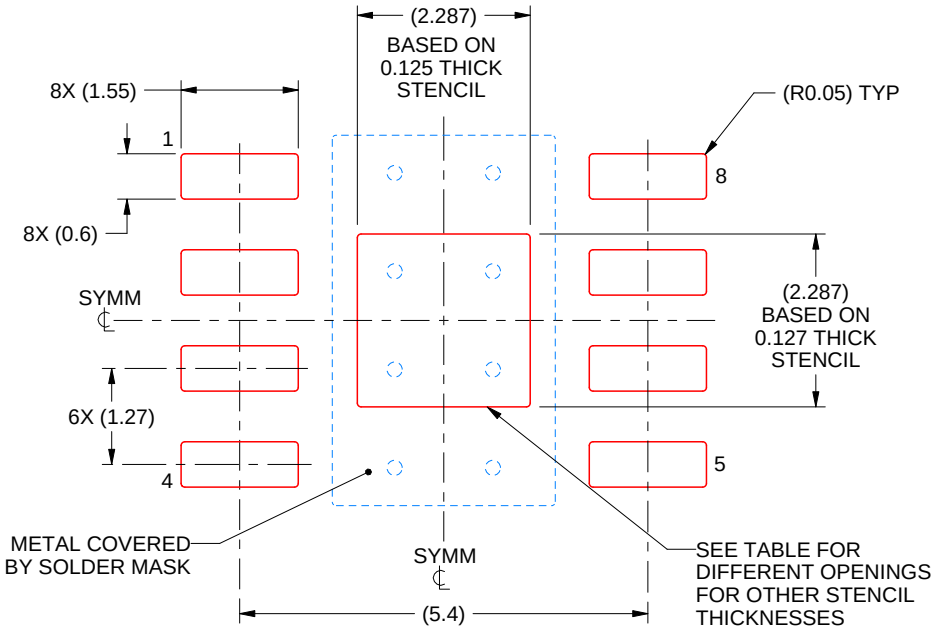


SOLDER MASK DETAILS

4218820/A 12/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

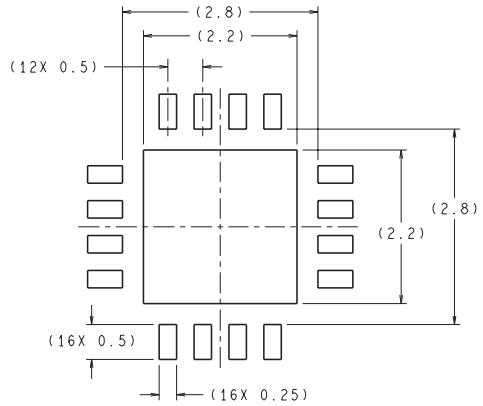
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.557 X 2.557
0.125	2.287 X 2.287 (SHOWN)
0.150	2.088 X 2.088
0.175	1.933 X 1.933

4218820/A 12/2022

NOTES: (continued)

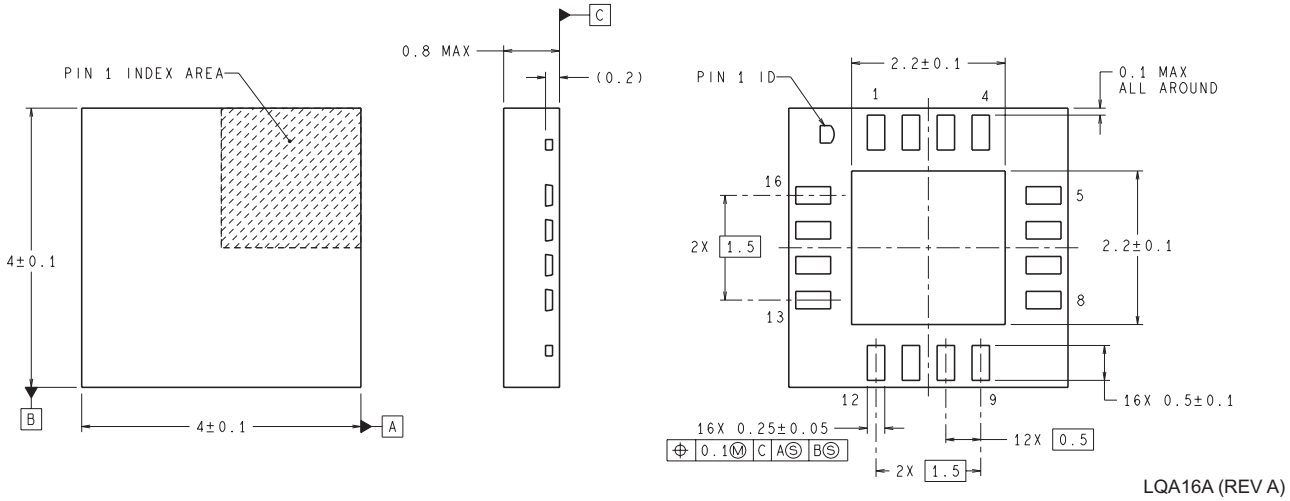
10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

NHP0016A



RECOMMENDED LAND PATTERN
1:1 RATION WITH PKG SOLDER PADS

DIMENSIONS ARE IN MILLIMETERS



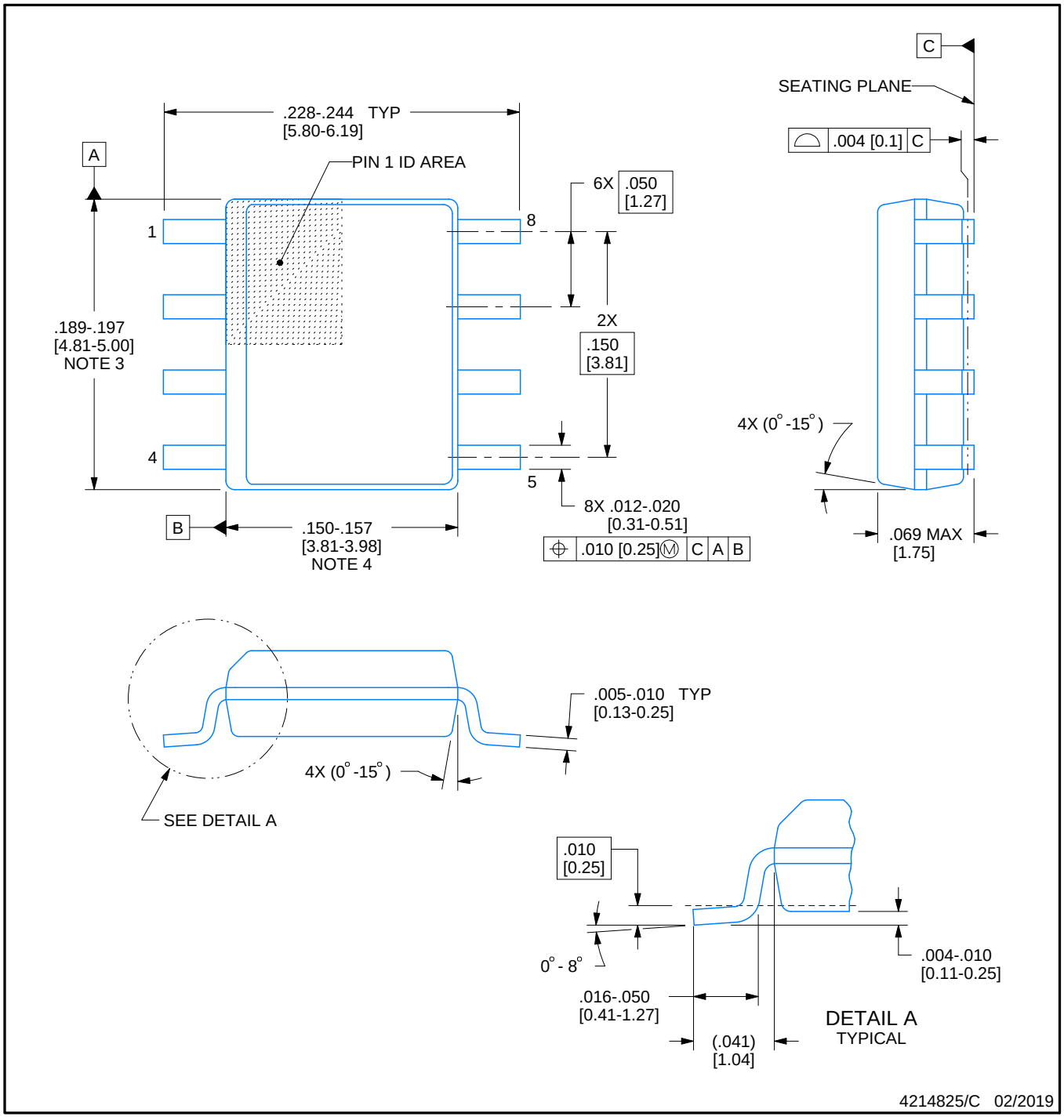
LQA16A (REV A)

PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



NOTES:

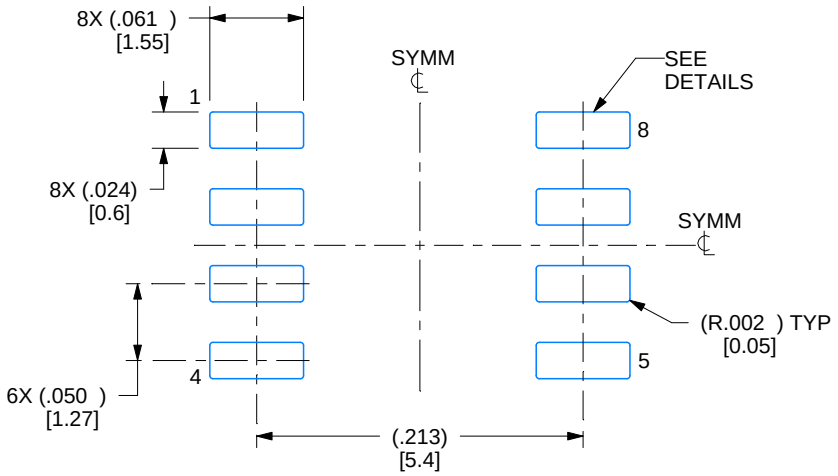
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

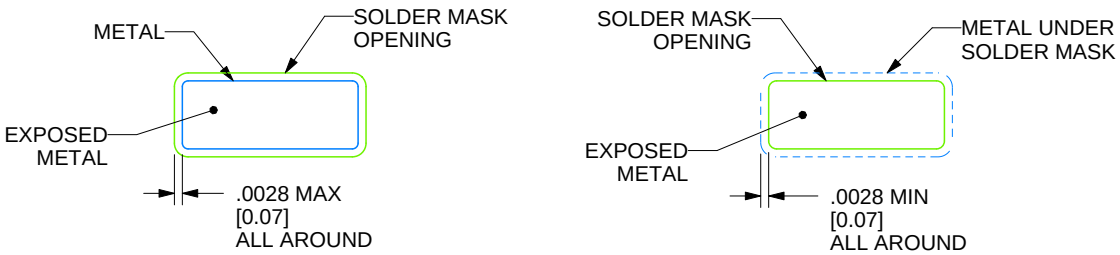
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

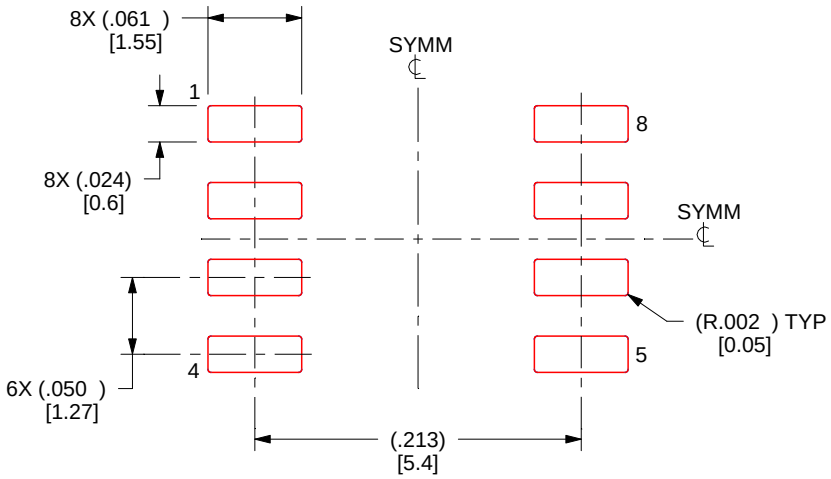
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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