

CoolGaN™ Gen2
650 V CoolGaN™ enhancement-mode Power Transistor

Infineon’s CoolGaN™ is a highly efficient GaN (gallium nitride) transistor technology for power conversion in the voltage range up to 650 V. With extensive experience on the semiconductor market, Infineon’s GaN technology brought the e-mode concept to maturity with end-to-end production in high volumes. The pioneering quality ensures the highest standards and offers the most reliable and performing solution among all GaN HEMTs on the market.

Features

- Enhancement mode transistor - Normally OFF switch
- Ultra fast switching
- No reverse-recovery charge
- Capable of reverse conduction
- Low gate charge, low output charge
- Superior commutation ruggedness
- ESD (HBM/CDM) JEDEC standards

Benefits

- Improves system efficiency
- Improves power density
- Enables highest operating frequency
- System cost reduction savings
- Reduces EMI

Potential applications

Industrial, telecom, datacenter SMPS, charger and adapter based on half-bridge topologies (half-bridge topologies for hard and soft switching such as Totem pole PFC, high frequency LLC).

Product validation

Fully qualified according to JEDEC for Industrial Applications
Please note: Target Datasheet to change without further notice

Table 1 Key Performance Parameters

Parameter	Value	Unit
$V_{DS,max}$	650	V
$R_{DS(on),max}$	30	mΩ
$Q_{g,typ}$	16.0	nC
$I_{D,pulse}$	130	A
$Q_{oss} @ 400 V$	83	nC
Q_{rr}	0	nC

Type/Ordering Code	Package	Marking	Related Links
IGLT65R025D2	PG-HDSOP-16	65R025D2	see Appendix A

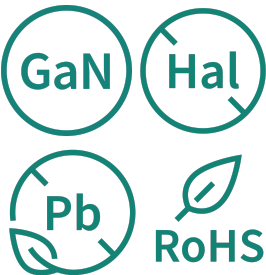
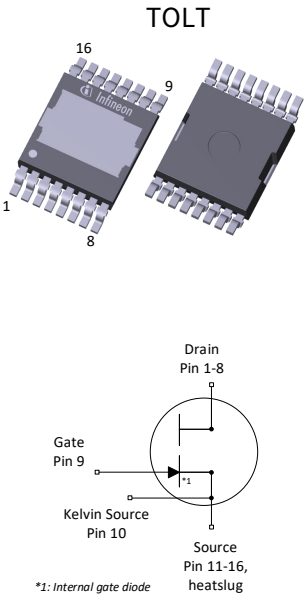




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Datasheet

1 Maximum ratings

at $T_j = 25\text{ °C}$, unless otherwise specified. Stresses beyond max ratings may cause permanent damage to the device. For optimum lifetime and reliability, Infineon recommends operating conditions that do not continuously exceed 80 % of the maximum ratings stated (unless otherwise explicitly stated). For further information, contact your local Infineon sales office.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Drain source voltage, continuous	$V_{DS,max}$	-	-	650	V	$V_{GS} = 0\text{ V}$, derating recommendation acc. JEDEC JEP198
Leakage current at drain source transient voltage	$I_{DS,trans}$	-	-	28	mA	$V_{GS} = 0\text{ V}$, $V_{DS,trans} = 900\text{ V}$
Drain source voltage transient	$V_{DS,trans}$	-	-	900	V	<1 % duty cycle, <1 μs , 1 M pulses
Drain source voltage, pulsed	$V_{DS,pulse}$	-	-	750	V	$T_j = 25\text{ °C}$; $V_{GS} \leq 0\text{ V}$; cumulated stress time $\leq 1\text{ h}$
	$V_{DS,pulsed}$	-	-	650		$T_j = 125\text{ °C}$; $V_{GS} \leq 0\text{ V}$; cumulated stress time $\leq 1\text{ h}$
Switching surge voltage, pulsed	$V_{DS,surge}$	-	-	750	V	DC bus voltage = 700 V; turn off $V_{DS,pulse} = 750\text{ V}$; turn on $I_{D,pulse} = 63\text{ A}$; $T_j = 105\text{ °C}$; $f \leq 100\text{ kHz}$, $t \leq 100\text{ sec.}$ (10 million pulses)
Continuous current, drain source ¹⁾	I_D	-	-	67	A	$T_c = 25\text{ °C}$; $T_j = T_{j,max}$
Pulsed current, drain source	$I_{D,pulse}$	-130 -70	-	130 70	A	$T_j = 25\text{ °C}$; $I_G = 60\text{ mA}$; See Diagram 3, 5 $T_j = 125\text{ °C}$; $I_G = 60\text{ mA}$; See Diagram 4, 6
Gate current, continuous ²⁾	$I_{G,avg}$	-	-	46	mA	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$; See Table 9
Gate current, pulsed ²⁾	$I_{G,pulsed}$	-4.6	-	4.6	A	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$; See Table 9
Gate source voltage, continuous ²⁾	V_{GS}	-10	-	-	V	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$; See Diagram 12
Gate source voltage, pulsed ²⁾	$V_{GS,pulse}$	-25	-	-	V	$T_j = -55\text{ °C}$ to $T_j = 150\text{ °C}$; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	-	-	219	W	$T_c = 25\text{ °C}$
Operating junction temperature	T_j	-55	-	150	°C	-
Storage temperature	T_{stg}	-55	-	150	°C	Max shelf life depends on storage conditions
Drain-source voltage slew-rate	dv/dt	-	-	200	V/ns	-

¹⁾ Limited by $T_{j,max}$. Maximum Duty Cycle $D = 0.75$

²⁾ We recommend using an advanced driving technique to optimize the device performance. Please see gate drive application note for more details.

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	0.57	°C/W	-
Thermal resistance, junction - ambient	R_{thJA}	-	-	68	°C/W	Device on PCB, minimum footprint
Thermal resistance, junction - ambient for SMD version	R_{thJA}	-	-	92	°C/W	Device on 40 mm*40 mm*1.5 mm epoxy PCB FR4 with 6 cm ² (one layer, 70 µm thickness) copper area. PCB is vertical without air stream cooling.
Reflow soldering temperature	T_{sold}	-	-	260	°C	reflow MSL1

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless specified otherwise

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	0.9 -	1.2 1	1.6 -	V	$I_{DS}=6.1\text{ mA}$; $V_{DS}=10\text{ V}$; $T_j=25\text{ °C}$ $I_{DS}=6.1\text{ mA}$; $V_{DS}=10\text{ V}$; $T_j=150\text{ °C}$
Gate-Source reverse clamping voltage	$V_{GS, clamp}$	-	-	-8	V	$I_{GS}=-1\text{ mA}$
Drain-Source leakage current	I_{DSS}	-	2.3 46	230 -	μA	$V_{DS}=650\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ $V_{DS}=650\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=150\text{ °C}$
Drain-Source on-state resistance	$R_{DS(on)}$	-	0.025 0.053	0.030 -	Ω	$I_G=60\text{ mA}$; $I_D=18\text{ A}$; $T_j=25\text{ °C}$ $I_G=60\text{ mA}$; $I_D=18\text{ A}$; $T_j=150\text{ °C}$
Gate resistance	$R_{G,int}$	-	-	-	Ω	LCR impedance measurement; $f=f_{res}$, open drain;

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	770	-	pF	$V_{GS}=0\text{ V}$; $V_{DS}=400\text{ V}$, $f=1\text{ MHz}$
Output capacitance	C_{oss}	-	122	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=400\text{ V}$, $f=1\text{ MHz}$
Reverse Transfer capacitance	C_{rss}	-	1.47	-	pF	$V_{GS}=0\text{ V}$, $V_{DS}=400\text{ V}$, $f=1\text{ MHz}$
Effective output capacitance, energy related ³⁾	$C_{o(er)}$	-	tbd	-	pF	$V_{DS}=0\text{ to }400\text{ V}$
Effective output capacitance, time related ⁴⁾	$C_{o(tr)}$	-	tbd	-	pF	$V_{GS}=0\text{ V}$; $V_{DS}=0\text{ to }400\text{ V}$; $I_D=\text{const}$
Output charge	Q_{oss}	-	83	-	nC	$V_{DS}=0\text{ to }400\text{ V}$
Turn-on delay time	$t_{d(on)}$	-	tbd	-	ns	$I_D=18\text{ A}$; $R_{ON}=2.2\text{ Ohm}$; $R_{OFF}=2.2\text{ Ohm}$; $R_{SS}=150\text{ Ohm}$; $C_C=6.8\text{ nF}$; $V_{DRV}=12\text{ V}$; see Table 8
Turn-off delay time	$t_{d(off)}$	-	tbd	-	ns	$I_D=18\text{ A}$; $R_{ON}=2.2\text{ Ohm}$; $R_{OFF}=2.2\text{ Ohm}$; $R_{SS}=150\text{ Ohm}$; $C_C=6.8\text{ nF}$; $V_{DRV}=12\text{ V}$; see Table 8
Rise time	t_r	-	tbd	-	ns	$I_D=18\text{ A}$; $R_{ON}=2.2\text{ Ohm}$; $R_{OFF}=2.2\text{ Ohm}$; $R_{SS}=150\text{ Ohm}$; $C_C=6.8\text{ nF}$; $V_{DRV}=12\text{ V}$; see Table 8
Fall time	t_f	-	tbd	-	ns	$I_D=18\text{ A}$; $R_{ON}=2.2\text{ Ohm}$; $R_{OFF}=2.2\text{ Ohm}$; $R_{SS}=150\text{ Ohm}$; $C_C=6.8\text{ nF}$; $V_{DRV}=12\text{ V}$; see Table 8

³⁾ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V

⁴⁾ $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 6 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	16	-	nC	$V_{GS}=0$ to 3 V; $V_{DS}=400$ V, $I_D=18$ A

Table 7 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.2	2.5	V	$V_{GS}=0$ V; $I_{SD}=18$ A
Pulsed current, reverse	$I_{SD,pulse}$	-	-	130	A	$I_G=60$ mA
Reverse recovery charge ⁵⁾	Q_{rr}	-	0	-	nC	$I_{SD}=18$ A; $V_{DS}=400$ V

⁵⁾ Excluding Q_{oss}

4 Test Circuits

Table 8 Reverse Channel Characteristics Test

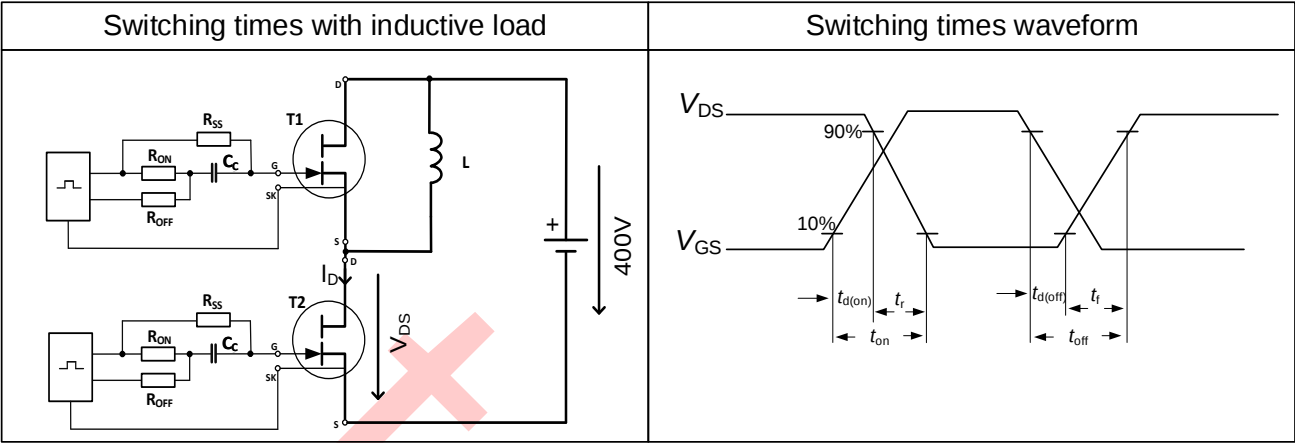
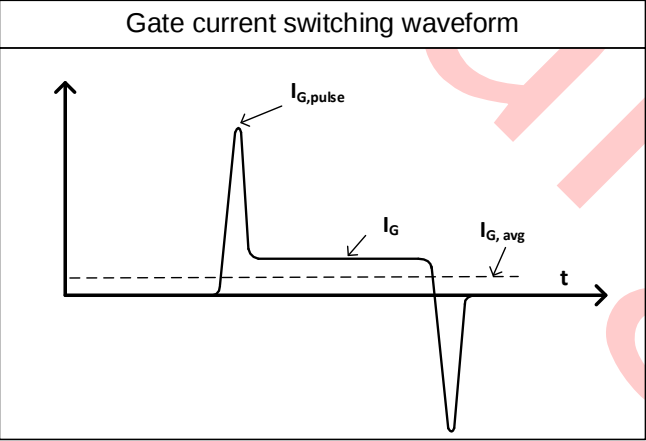


Table 9 Gate current switching waveform



5 Package Outlines

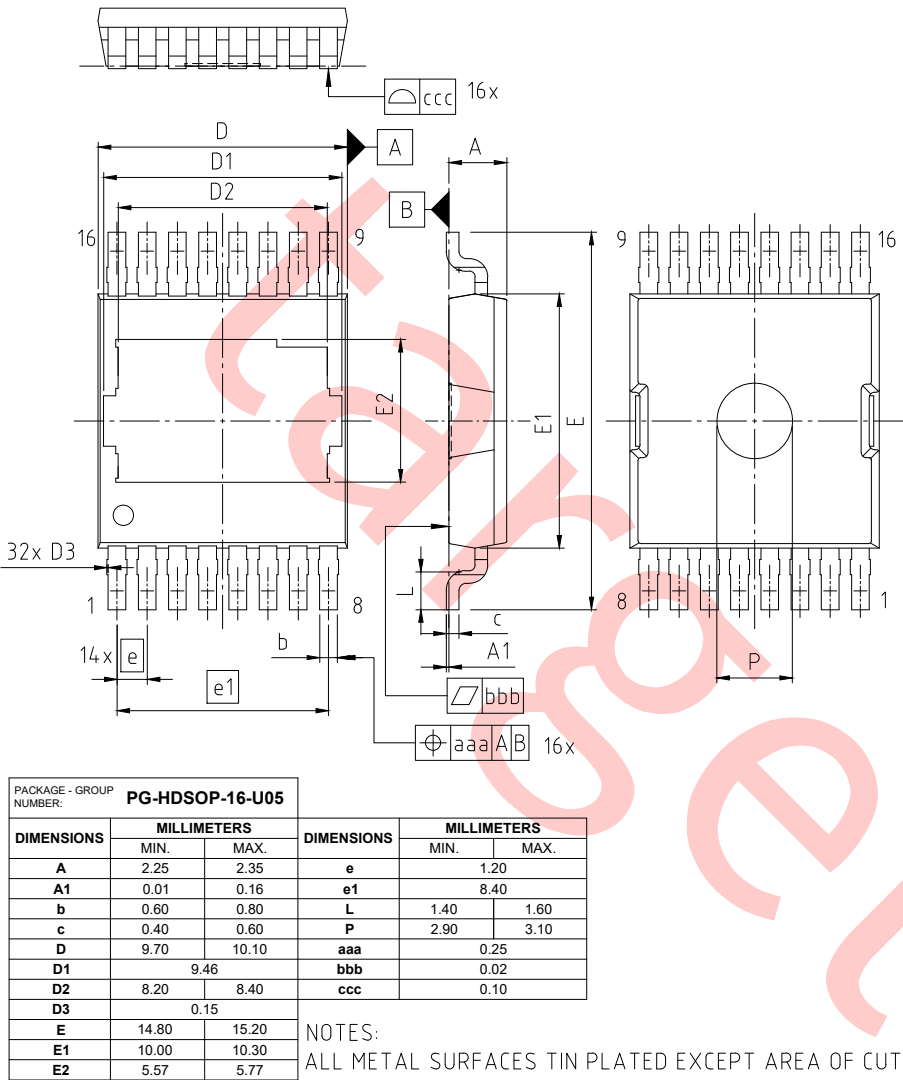
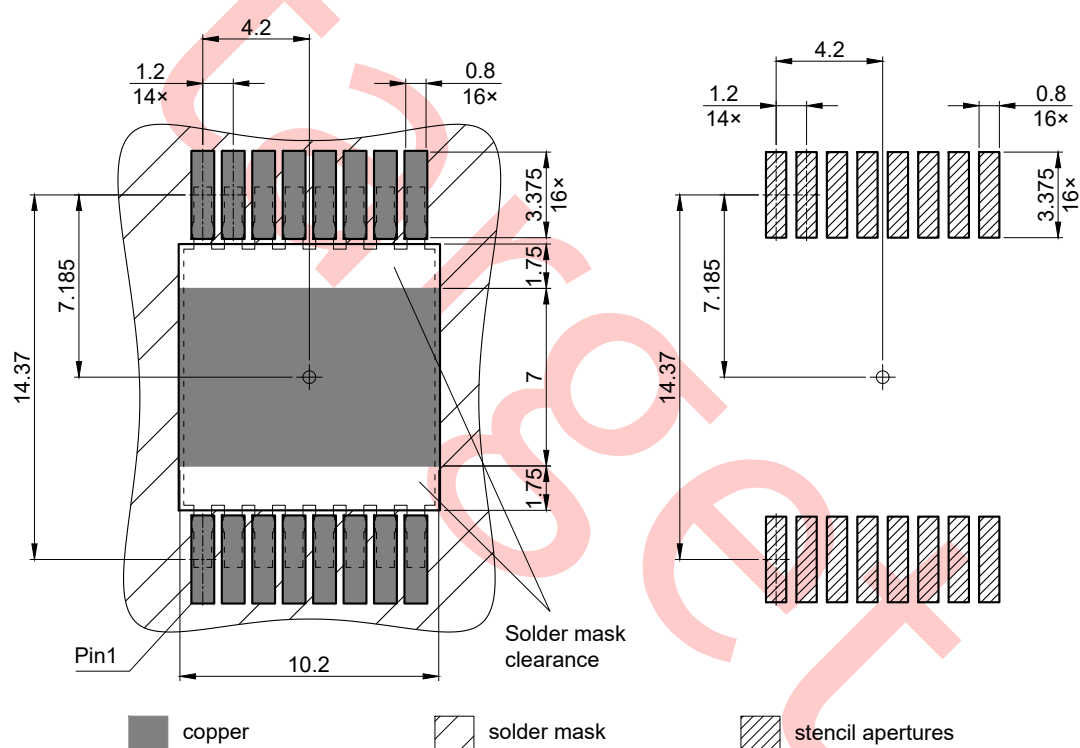
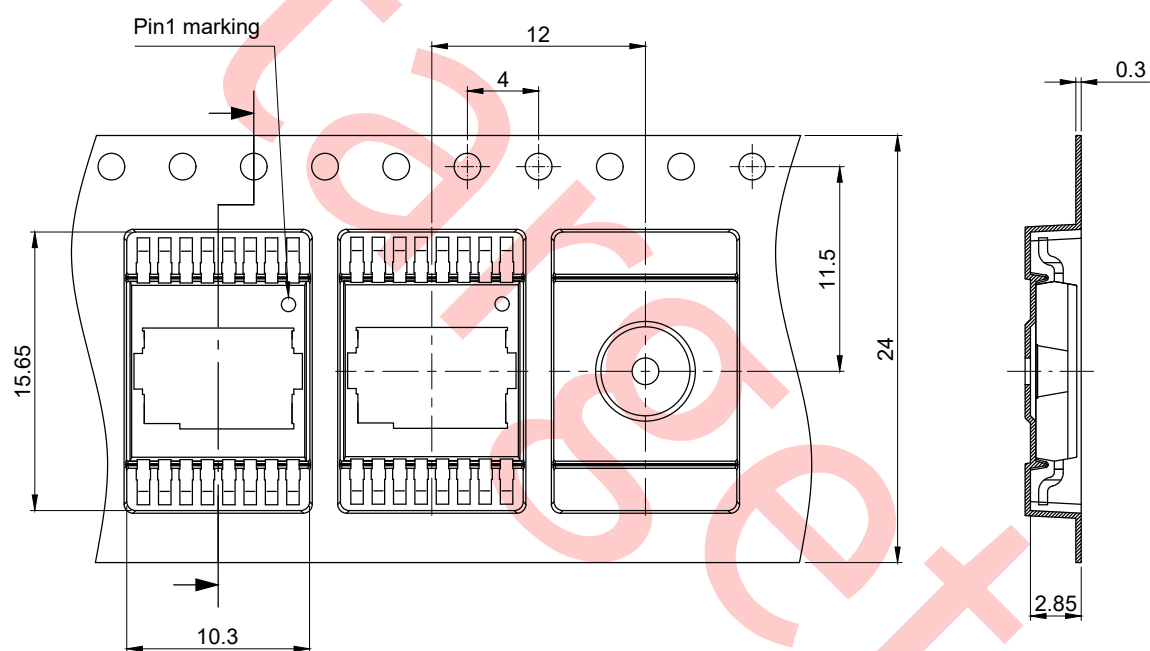


Figure 1 Outline PG-HDSOP-16, dimensions in mm



All dimensions are in units mm
 Based on stencil thickness 0.2 mm
 All pads are non-solder mask defined

Figure 2 Outline PG-HDSOP-16, dimensions in mm



All dimensions are in units mm

The drawing is in compliance with ISO 128-30, Projection Method 1 []

Figure 3 Outline PG-HDSOP-16, dimensions in mm

6 Appendix A

Table 10 **Related Links**

- [IFX CoolGaN™ GaN 650 V webpage](#)
- [IFX CoolGaN™ GaN 650 V reliability white paper](#)
- [IFX CoolGaN™ GaN 650 V gate driver application note](#)
- [IFX CoolGaN™ GaN 650 V applications information](#)

datasheet

Revision History

IGLT65R025D2

Revision 2024-04-15, Rev. 0.1

Previous Revision

Revision	Date	Subjects (major changes since last revision)
0.1	2024-04-15	Release of target

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