DATA SHEET
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ecoSwitch™ Advanced Load Management

Controlled Load Switch with Reverse Current Protection and Low R_{ON}

NCP45780

The NCP45780 load management device provides a component and area−reducing solution for efficient power domain switching with inrush current limit via soft start. These devices are designed to integrate control and driver functionality with back−to−back high performance low on−resistance power MOSFETs in a single package. This cost effective solution is ideal for reverse current applications and the specific power management and disconnect functions used in USB Type−C and Type−C Power Delivery ports.

Features

- Advanced Controller with Charge Pump
- Integrated N−Channel MOSFET with Low R_{ON}
- Soft−Start via Controlled Slew Rate
- Adjustable Slew Rate Control
- Fault Detection with Power Good Output
- Thermal Shutdown and Under Voltage Lockout
- Short−Circuit and Adjustable Over−Current Protections
- Reverse−current Protection
- Input Voltage Range 3 V to 24 V
- Extremely Low Standby Current
- This is a Pb−free Device

Typical Applications

- USB Type C Power Delivery
- Reverse Current Load Switching Applications
- Notebook and Tablet Computers
- Telecom, Networking, Medical and Industrial Equipment
- Set−Top Boxes, Servers and Gateways
- Hot−Swap Devices and Peripheral Ports

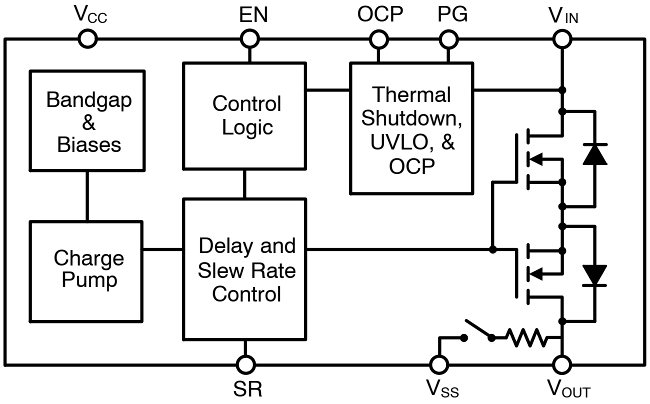
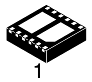


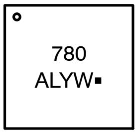
Figure 1. Block Diagram

R_{ON} TYP	V_{CC}	V_{IN}	I_{MAX}
13.5 mΩ	4.5 V	3 V	7 A



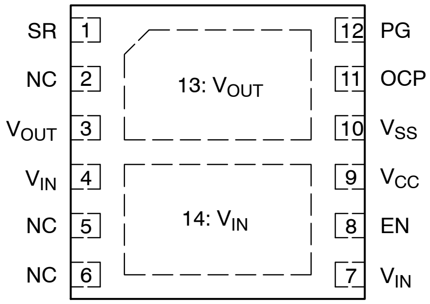
DFN12, 3x3
CASE 506EN

MARKING DIAGRAM



780 = Specific Device Code
A = Assembly Location
L = Wafer Lot
YW = Year / Week
▪ = Pb−Free Package

PIN CONFIGURATION



(Top View)

ORDERING INFORMATION

Device	Package	Shipping
NCP45780IMN24RTWG	DFN12	3000 / Tape & Reel

April, 2022 − Rev. 1

Table 1. PIN DESCRIPTION

Pin	Name	Function
1	SR	Slew Rate control pin. Slew rate adjustment made with an external capacitor to GND; float if not used.
3,13	V_{OUT}	Source of MOSFET connected to load. – **Pin 16 should be used for high current (>0.5 A)**
4,7,14	V_{IN}	Input voltage (3 V – 24 V) – **Pin 13 should be used for high current (>0.5 A)**
8	EN	Active−high digital input used to turn on the MOSFET driver, pin has an internal pull down resistor to GND.
9	V_{CC}	Driver supply voltage (3.0 V – 5.5 V)
10	V_{SS}	Driver ground
11	OCP	Over−current protection trip point adjustment made with a voltage applied (0 V – 1.2 V), pin has an internal pull up resistor to EN; short to ground if over−current protection is not needed.
12	PG	Active−high, open−drain output that indicates when the gate of the MOSFET is fully charged, external pull up resistor ≥ 100 kΩ to an external voltage source required; tie to GND if not used.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	−0.3 to 6	V
Input Voltage Range	V_{IN}	−0.3 to 30	V
Output Voltage Range	V_{OUT}	−0.3 to 30	V
EN Input Voltage Range	V_{EN}	−0.3 to (V_{CC} + 0.3)	V
PG Output Voltage Range (Note 1)	V_{PG}	−0.3 to 6	V
OCP Input Voltage Range	V_{OCP}	−0.3 to 6	V
Thermal Resistance, Junction−to−Ambient, Steady State (Note 2)	$R_{\theta JA}$	176.16	°C/W
Thermal Resistance, Junction−to−Case (V_{IN} Paddle)	$R_{\theta JC}$	2.5	°C/W
Continuous MOSFET Current @ T_A = 25°C (Note 2)	I_{MAX}	20	A
Total Power Dissipation @ T_A = 25°C (Note 2) Derate above T_A = 25°C	P_D	3.49 34.9	W mW/°C
Storage Temperature Range	T_{STG}	−55 to 150	°C
Lead Temperature, Soldering (10 sec.)	T_{SLD}	260	°C
ESD Capability, Human Body Model (Notes 3, 4)	ESD_{HBM}	2	kV
ESD Capability, Charged Device Model (Notes 3, 4)	ESD_{CDM}	1	kV
Latch−up Current Immunity (Note 3)	LU	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. PG is an open drain output that requires an external pull−up resistor > 100 kΩ to an external voltage source.
2. Surface−mounted on FR4 board using the minimum recommended pad size, 1 oz Cu. Over current protection will limit maximum realized current to 12.5 A at highest setting.
3. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78
4. Rating is for all pins except for V_{IN} and V_{OUT} which are tied to the internal MOSFET's Drain and Source. Typical MOSFET ESD performance for V_{IN} and V_{OUT} should be expected and these devices should be treated as ESD sensitive.

Table 3. OPERATING RANGES

Rating	Symbol	Min	Max	Unit
V_{CC} – (V_{IN} > 4.5 V)	V_{CC}	3	5.5	V
V_{CC} – (V_{IN} < 4.5 V)	V_{CC}	4.5	5.5	V
V_{IN} – (V_{CC} > 4.5 V)	V_{IN}	3	24	V
V_{IN} – (V_{CC} < 4.5 V)	V_{IN}	4.5	24	V
OFF to ON Transition Energy Dissipation Limit (See application section)	E_{TRANS}	0	100	mJ
OCP External Resistor to VSS	R_{OCP}	short	open	kΩ
VSS	V_{SS}		0	V
Ambient Temperature	T_A	−40	85	°C
Junction Temperature	T_J	−40	125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS (T_J = 25°C, V_{CC} = 3 V − 5.5 V, unless otherwise specified)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
On−Resistance	V_{CC} = 4.5 V, V_{IN} = 3 V	R_{ON}		13.5	16	mΩ
Leakage Current − V_{IN} to V_{OUT} (Note 5)	V_{EN} = 0 V, V_{IN} = 24 V, V_{CC} = 5.5 V	I_{LEAK}		35	100	nA
Leakage Current − V_{OUT} to V_{IN} (Notes 5, 6)	V_{EN} = 0 V, V_{IN} = 24 V, V_{CC} = 5.5 V	I_{LEAK}		35	100	nA
V_{IN} Control Current − V_{IN} to V_{SS}	V_{EN} = 0 V, V_{IN} = 24 V, V_{CC} = 5.5 V	I_{INCTL}		0.8	1.5	μA
	V_{EN} = V_{CC}, V_{IN} = 24 V, V_{CC} = 5.5 V	I_{INCTL_EN}		150	300	
Supply Standby Current (Note 7)	V_{EN} = 0 V, V_{CC} = 5.5 V	I_{STBY}		1.6	5	μA
Supply Dynamic Current (Notes 8, 14)	V_{EN} = V_{CC}, V_{CC} = 5.5 V	I_{DYN}		350	500	μA
EN Input High Voltage (Note 14)		V_{IH}	2			V
EN Input Low Voltage		V_{IL}			0.8	V
EN Input Leakage Current	V_{EN} = 0 V	I_{IL}	−1.0	0.06	1	μA
EN Pull Down Resistance		R_{PD}	76	100	124	kΩ
PG Output Low Voltage	I_{SINK} = 100 μA	V_{OL}		20	100	mV
PG Output Leakage Current	V_{TERM} = 3.3 V	I_{OH}		5	100	nA
Slew Rate Control Constant (Notes 9, 11)		K_{SR}	70	110	130	μA

FAULT PROTECTIONS

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Thermal Shutdown Threshold (Note 10)		T_{SDT}		145		°C
Thermal Shutdown Hysteresis (Note 10)		T_{HYS}		20		°C
V_{IN} Under Voltage Lockout Threshold	V_{IN} rising	V_{UVLO}		2		V
V_{IN} Under Voltage Lockout Hysteresis		V_{HYS}		200		mV
Over−Current Protection Trip	R_{OCP} = open	I_{TRIP}	0.5	0.75	1.1	A
	R_{OCP} = 100 kΩ			3.1		
	R_{OCP} = 20 kΩ			5.7		
	R_{OCP} = short to GND			7.7		
Over−Current Protection Blanking Time		t_{OCP}		2.25		ms
Short−Circuit Protection Trip Current	(Notes 12, 13)	I_{SC}		12.5		A

5. Average current from V_{IN} to V_{OUT} with MOSFET turned off.
6. Reverse current protection prevents current flow from V_{OUT} to V_{IN} when the EN pin is low. When EN is asserted, current is allowed to travel in either direction.
7. Average current from V_{CC} to GND with MOSFET turned off.
8. Average current from V_{CC} to GND after charge up time of MOSFET.
9. See Applications Information section for details on how to adjust the gate slew rate.
10. Operation above T_J = 125°C is not implied.
11. Loads with changing impedance may cause inconsistent slew rate.
12. Transient currents exceeding the short−circuit protection trip current will cause the device to fault. For OCP setting less than 20 kΩ, high steady state currents may cause an over temperature lockout before the OCP threshold is reached due to self−heating.
13. Short Circuit Protection protects the device against hard shorts ($R_{SHORT} \leq 250$ mΩ V_{OUT} to Ground) for V_{IN} < 18 V, and against soft shorts (R_{SHORT} > 250 mΩ) for V_{IN} < 24 V. Short circuit protection testing assumed a 100 W supply capability limit on V_{IN}.
14. The voltage on EN be < 0.8 V or within ±0.7 V of V_{CC} to prevent leakage from V_{CC} to EN exceeding the specified maximum dynamic current.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 5. SWITCHING CHARACTERISTICS (T_J = 25°C unless otherwise specified) (Notes 15, 16)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Output Slew Rate − Default (Note 17)	V_{CC} = 4.5 V; V_{IN} = 3 V	SR	13	20.5	29	V/ms
	V_{CC} = 5.0 V; V_{IN} = 3 V		13	20.5	29	
	V_{CC} = 3.3 V; V_{IN} = 24 V		13	22.5	29	
	V_{CC} = 5.0 V; V_{IN} = 24 V		13	22.5	29	
Output Turn−on Delay	V_{CC} = 4.5 V; V_{IN} = 3 V	T_{ON}	100	175	700	μs
	V_{CC} = 5.0 V; V_{IN} = 3 V		100	175	700	
	V_{CC} = 3.3 V; V_{IN} = 24 V		100	475	700	
	V_{CC} = 5.0 V; V_{IN} = 24 V		100	475	700	
Output Turn−off Delay	V_{CC} = 3.0 V; V_{IN} = 3 V	T_{OFF}		83		μs
	V_{CC} = 5.5 V; V_{IN} = 3 V			56		
	V_{CC} = 3.0 V; V_{IN} = 24 V			50		
	V_{CC} = 5.5 V; V_{IN} = 24 V			42		
Power Good Turn−on Time	V_{CC} = 4.5 V; V_{IN} = 3 V	$T_{PG,ON}$	0.25	0.575	2.5	ms
	V_{CC} = 5.0 V; V_{IN} = 3 V		0.25	0.535	2.5	
	V_{CC} = 3.3 V; V_{IN} = 24 V		0.25	1.8	2.5	
	V_{CC} = 5.0 V; V_{IN} = 24 V		0.25	1.6	2.5	
Power Good Turn−off Time	V_{CC} = 4.5 V; V_{IN} = 3 V	$T_{PG,OFF}$		10		ns
	V_{CC} = 5.0 V; V_{IN} = 3 V			10		
	V_{CC} = 3.3 V; V_{IN} = 24 V			10		
	V_{CC} = 5.0 V; V_{IN} = 24 V			10		

15. See below figure for Test Circuit and Timing Diagram.
16. Tested with the following conditions: $V_{TERM} = V_{CC}$; R_{PG} = 100 kΩ; R_L = 10 Ω; C_L = 0.1 μF.
17. Loads with changing impedance may cause inconsistent slew rate.

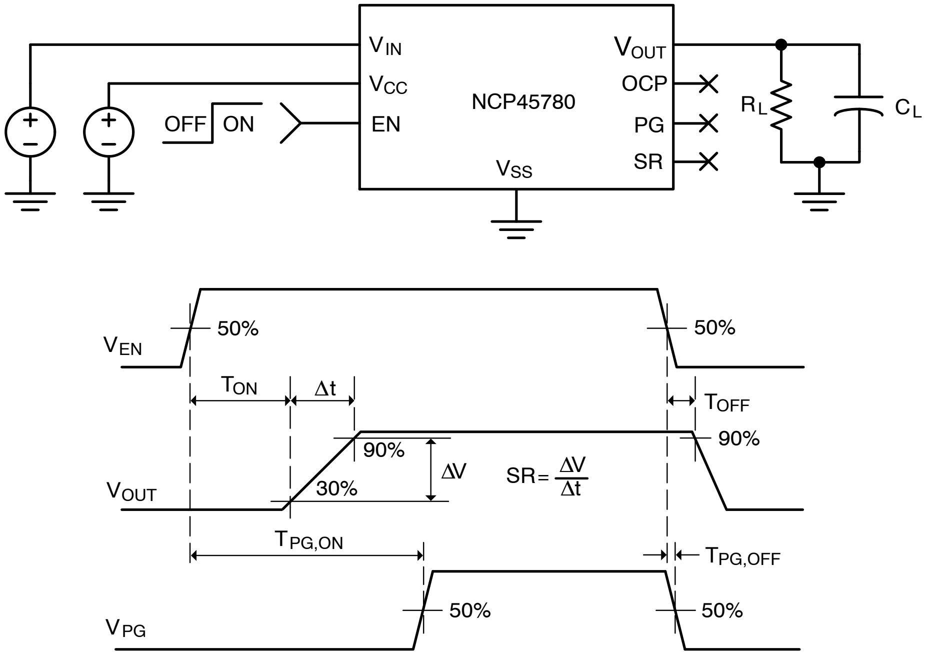


Figure 2. Switching Characteristics Test Circuit and Timing Diagrams

TYPICAL CHARACTERISTICS

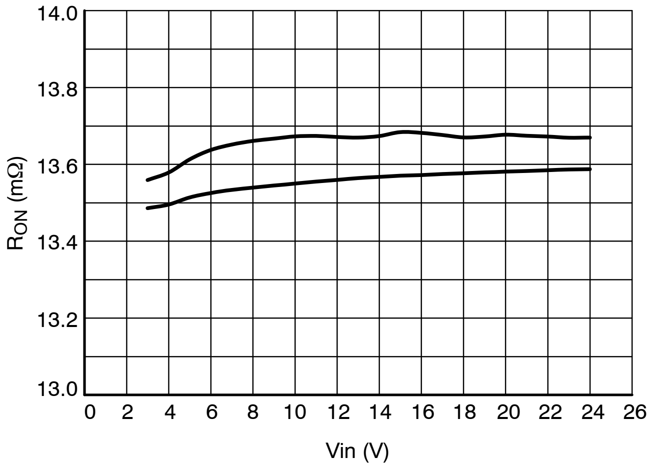


Figure 3. On−Resistance vs. Input Voltage

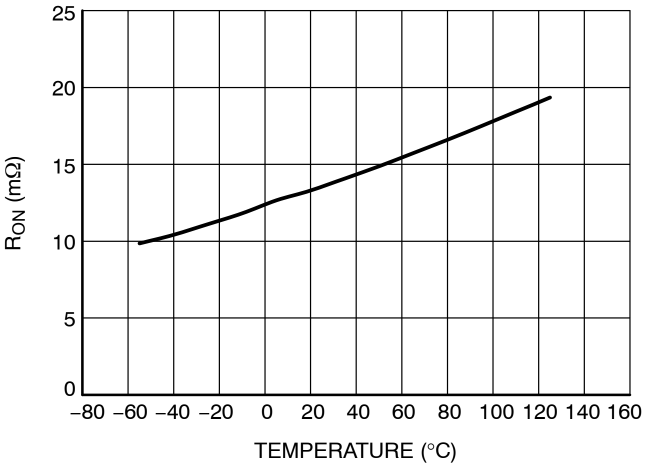


Figure 4. On−Resistance vs. Temperature

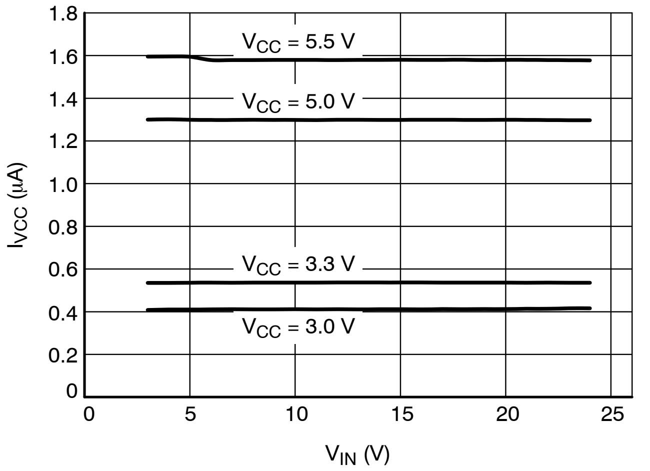


Figure 5. Supply Standby Current vs. Input Voltage

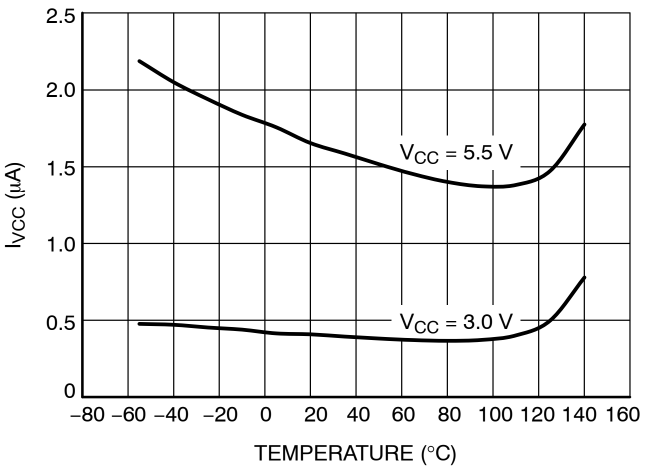


Figure 6. Supply Standby Current vs. Temperature

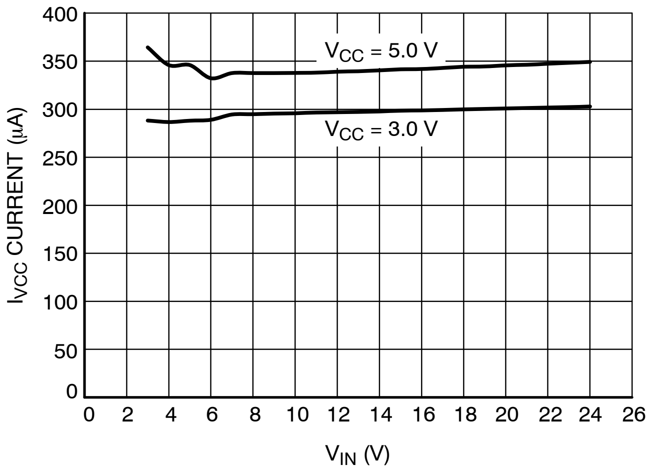


Figure 7. Dynamic Current vs. Input Voltage

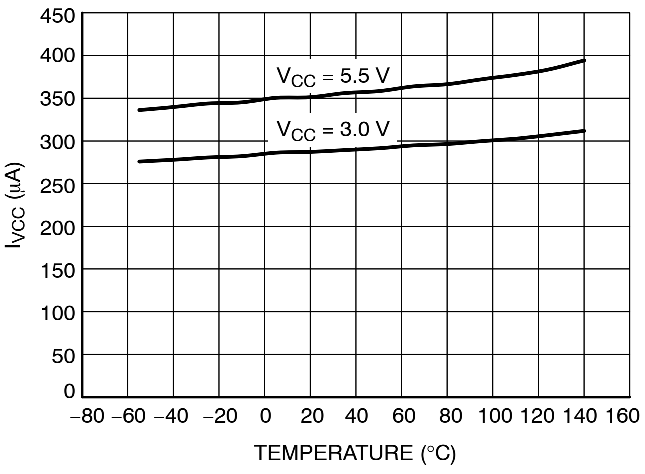


Figure 8. Supply Dynamic Current vs. Temperature

TYPICAL CHARACTERISTICS

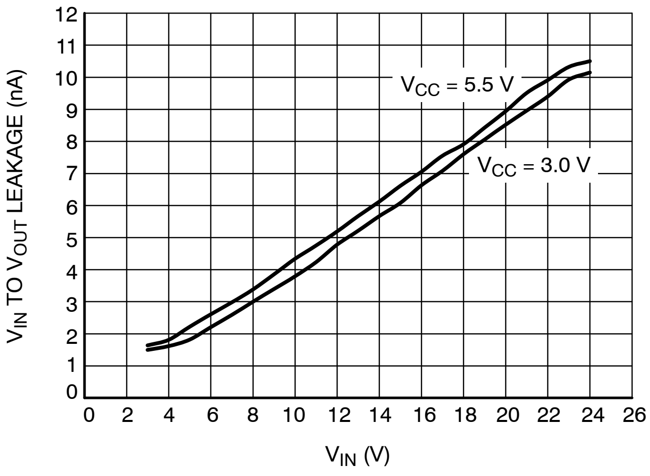


Figure 9. Vin to Vout Leakage with EN = 0 V

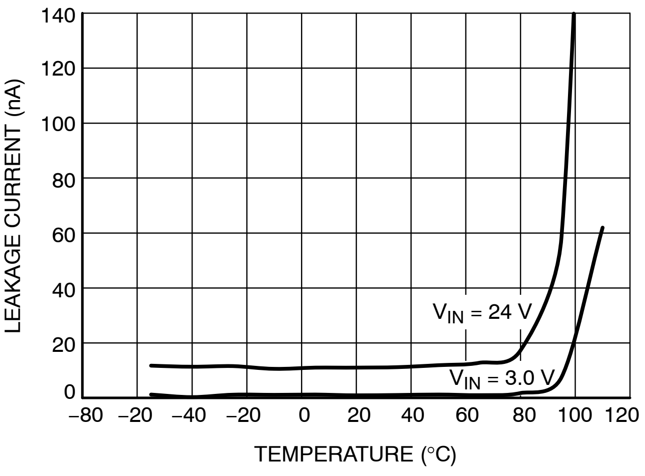


Figure 10. Input to Output Leakage vs. Temperature

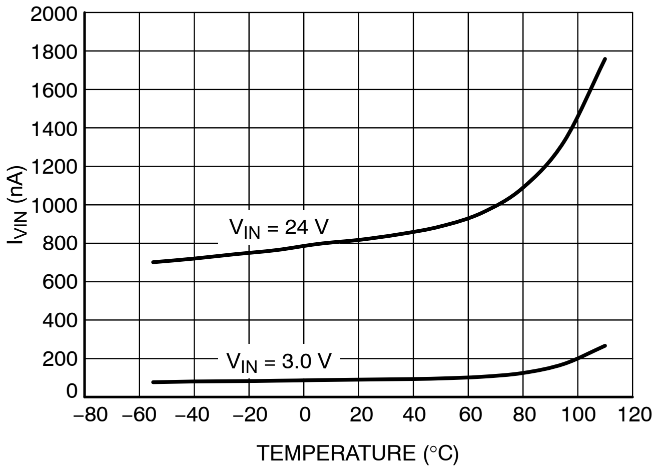


Figure 11. Vin Controller Current vs. Temperature (EN = 0)

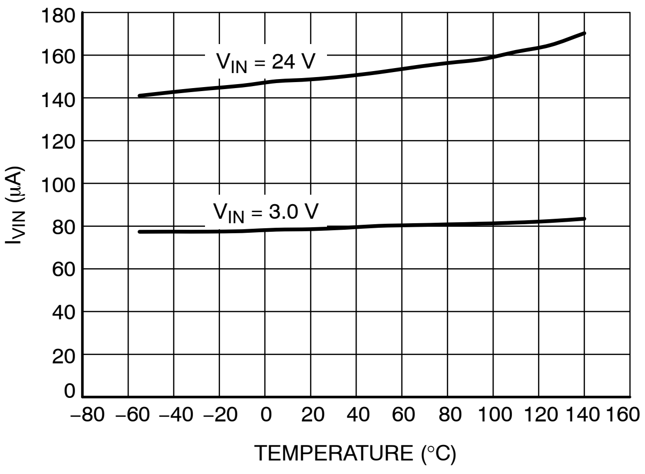


Figure 12. Vin Controller Current vs. Temperature (EN = VCC)

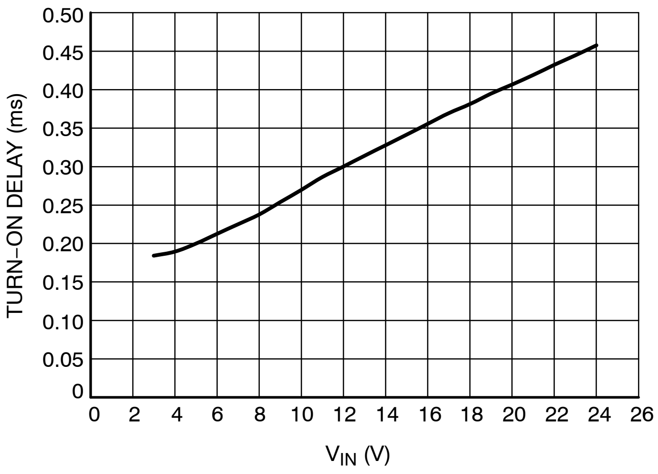


Figure 13. Output Turn−On Delay vs. Input Voltage

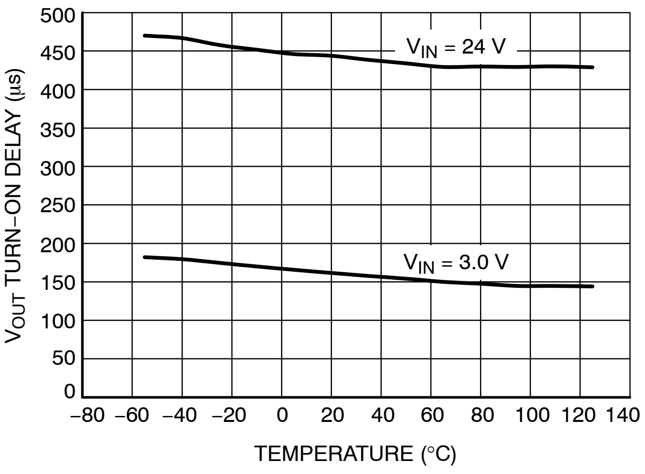


Figure 14. Output Turn−On Delay vs. Temperature

TYPICAL CHARACTERISTICS

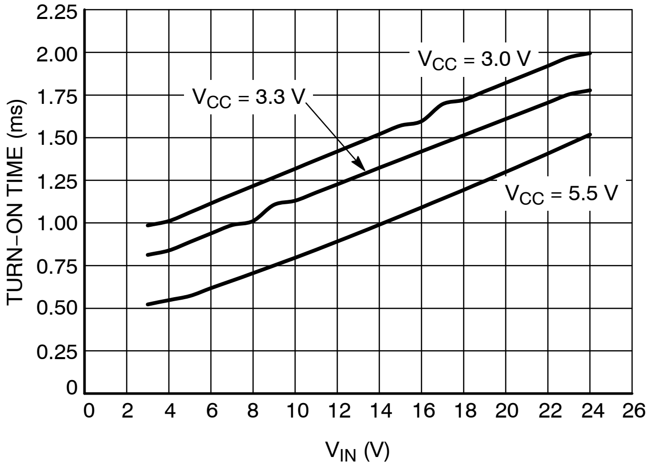


Figure 15. Power Good Turn−On Time vs. Input Voltage

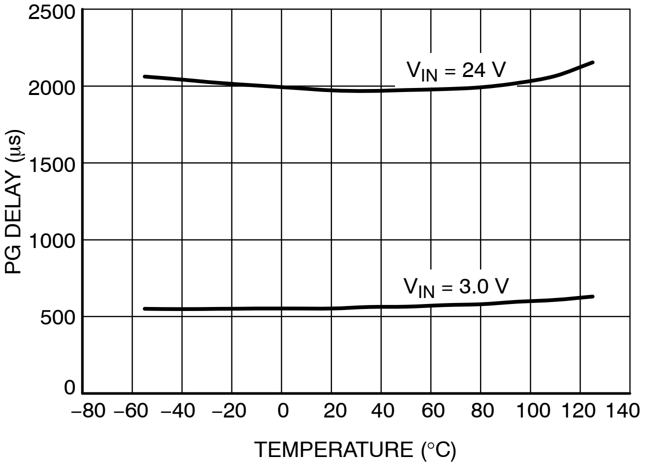


Figure 16. Power Good Turn−On Delay vs. Temperature

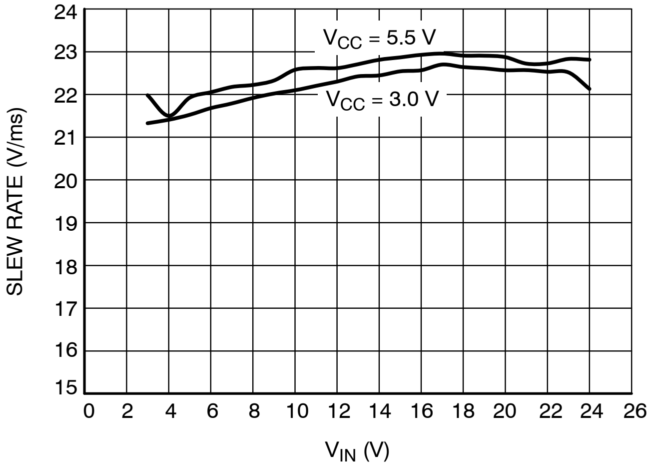


Figure 17. Default Slew Rate vs. Input Voltage (SR pin = floating)

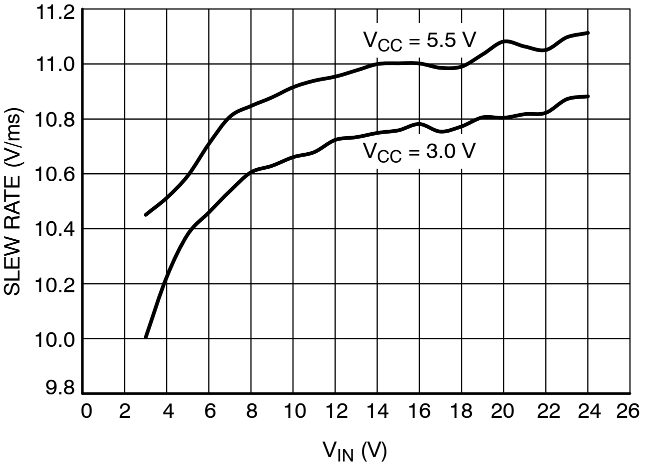


Figure 18. Slew Rate vs. Input Voltage (SR pin = 10 nF to GND)

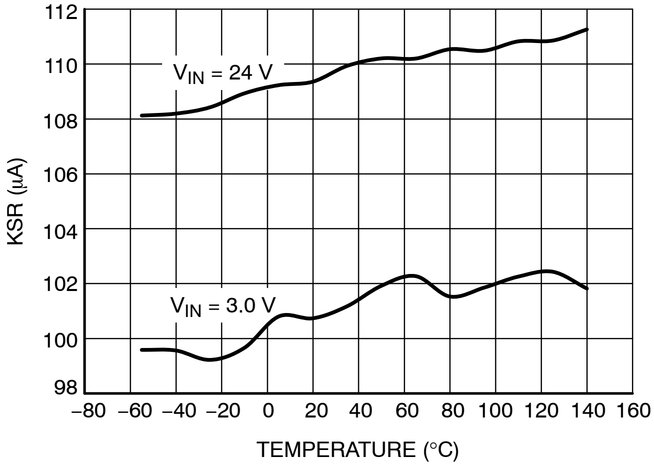


Figure 19. KSR vs. Temperature

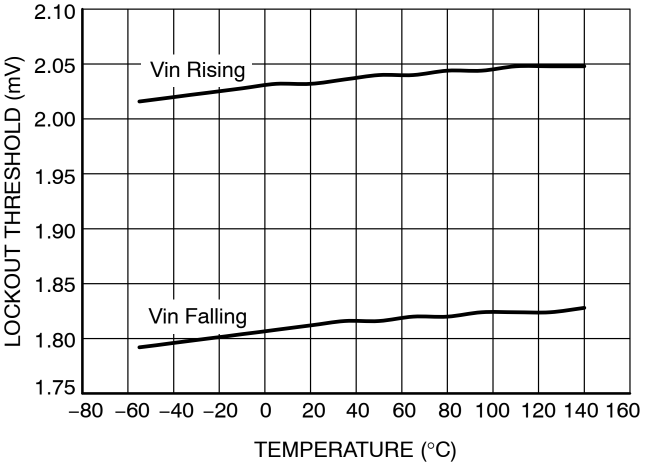


Figure 20. UVLO Trip Voltage vs. Temperature

TYPICAL CHARACTERISTICS

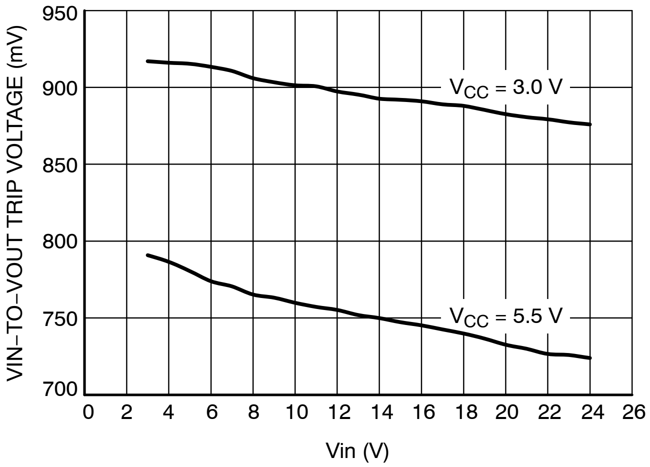


Figure 21. OCP Trip Voltage vs. Input Voltage (OCP = Open)

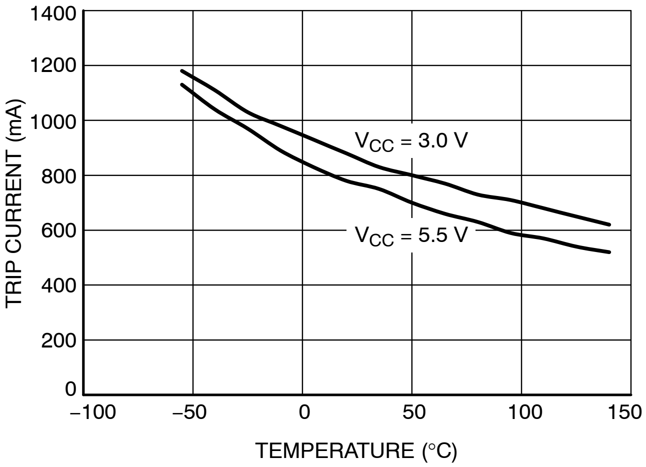


Figure 22. OCP Trip Current vs. Temperature (OCP = Open)

APPLICATIONS INFORMATION

Enable Control

The NCP45780 part enables the MOSFET in an active−high configuration. When the EN pin is at a logic high level and the V_{CC} supply pin has an adequate voltage applied, the MOSFET will be enabled. When the EN pin is at a logic low level, the MOSFET will be disabled. An internal pull down resistor to ground on the EN pin ensures that the MOSFET will be disabled when not driven.

Short−Circuit Protection (Hard short)

The NCP45780 device is equipped with short−circuit protection that helps protect the part and the system from a sudden high−current event, such as the output, V_{OUT}, being hard−shorted to ground.

Once active, the circuitry monitors the voltage difference between the V_{IN} pin and the V_{OUT} pin. When the difference is equal to the short−circuit protection threshold voltage, the MOSFET is turned off. The part remains off and is latched in the Fault state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Over−Current Protection (Soft short)

The NCP45780 device is equipped with an over−current protection (OCP) that helps protect the part and the system from a high current event which exceeds the expected operational current (e.g., a soft short).

In the event that the current from the V_{IN} pin to the V_{OUT} pin exceeds the OCP threshold for longer than the blanking time, the MOSFET will shut down and the PG pin is driven low. Like the short−circuit protection, the part remains latched in the Fault state until EN is toggled or V_{CC} supply voltage is cycled, at which point the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

The over−current trip point is determined by the resistance between the OCP pin and ground. If no over−current protection is needed, then the OCP pin should be tied to GND; if the OCP protection is disabled in this way, the short−circuit protection will still remain active.

Thermal Shutdown

The thermal shutdown of the NCP45780 device protects the part from internally or externally generated excessive temperatures. When an over−temperature condition is detected, the MOSFET is turned off.

The part comes out of thermal shutdown when the junction temperature decreases to a safe operating temperature as dictated by the thermal hysteresis. Upon exiting a thermal shutdown state, and if EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Under Voltage Lockout

The under voltage lockout of the NCP45780 device turns the MOSFET off when the input voltage, V_{IN}, drops below the under voltage lockout threshold.

If the V_{IN} voltage rises above the under voltage lockout threshold, and EN remains active, the MOSFET will be turned on in a controlled fashion with the normal output turn−on delay and slew rate.

Power Good

The NCP45780 device has a power good output (PG) that can be used to indicate when the gate of the MOSFET is fully charged. The PG pin is an active−high, open−drain output that requires an external pull up resistor, R_{PG}, greater than or equal to 100 kΩ to an external voltage source, VTERM, that is compatible with input levels of all devices connected to this pin.

The power good output can be used as the enable signal for other active−high devices in the system. This allows for guaranteed by design power sequencing and reduces the number of enable signals needed from the system controller. If the power good feature is not used in the application, the PG pin should be tied to GND.

Slew Rate Control

The NCP45780 device is equipped with controlled output slew rate, which provides soft start functionality. This limits the inrush current caused by capacitor charging and enables these devices to be used in hot swapping applications.

The slew rate can be decreased with an external capacitor added between the SR pin and ground. With an external capacitor present, the slew rate can be determined by the following equation:

$$\text{Slew Rate} = \frac{K_{SR}}{C_{SR}} \text{ [V/s]} \qquad \text{(eq. 1)}$$

where K_{SR} is the specified slew rate control constant, found on page 3, and C_{SR} is the capacitor added between the SR pin and ground. Note that the slew rate of the device will always be the lower of the default slew rate and the adjusted slew rate. Therefore, if the C_{SR} is not large enough to decrease the slew rate more than the specified default value, the slew rate of the device will be the default value.

Capacitive Load

The peak in−rush current associated with the initial charging of the application load capacitance needs to stay below the specified I_{max}. C_L (capacitive load) should be less than C_{max} as defined by the following equation:

$$C_{max} = \frac{I_{max}}{SR_{typ}} \qquad \text{(eq. 2)}$$

where I_{max} is the maximum load current, and SR_{typ} is the typical default slew rate when no external load capacitor is added to the SR pin.

OFF to ON Transition Energy Dissipation

The energy dissipation due to load current traveling from V_{IN} to V_{OUT} is very low during steady state operation due to the low R_{ON}. When the EN signal is asserted high, the load switch transitions from an OFF state to an ON state. During this time, the resistance from V_{IN} to V_{OUT} transitions from high impedance to R_{ON}, and additional energy is dissipated in the device for a short period of time. The worst case energy dissipated during the OFF to ON transition can be approximated by the following equation:

$$E = 0.5 \cdot V_{IN} \cdot \left(I_{INRUSH} + 0.8 \cdot I_{LOAD}\right) \cdot dt \qquad \text{(eq. 3)}$$

where V_{IN} is the voltage on the V_{IN} pin, I_{INRUSH} is the inrush current caused by capacitive loading on V_{OUT}, and dt is the time it takes V_{OUT} to rise from 0 V to V_{IN}. I_{INRUSH} can be calculated using the following equation:

$$I_{INRUSH} = \frac{dv}{dt} \cdot C_L \qquad \text{(eq. 4)}$$

where dv/dt is the programmed slew rate, and C_L is the capacitive loading on V_{OUT}. To prevent thermal lockout or damage to the device, the energy dissipated during the OFF to ON transition should be limited to E_{TRANS} listed in operating ranges table.

ecoSwitch LAYOUT GUIDELINES

Electrical Layout Considerations

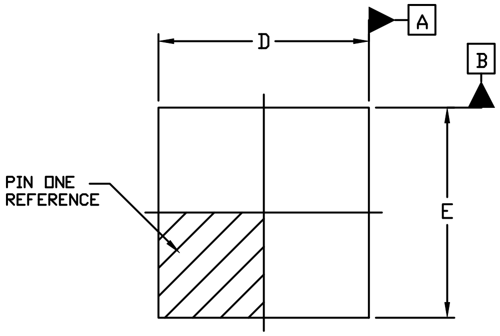
Correct physical PCB layout is important for proper low noise accurate operation of all ecoSwitch products.

Power Planes: The ecoSwitch is optimized for extremely low R_{ON} resistance, however, improper PCB layout can substantially increase source to load series resistance by adding PCB board parasitic resistance. Solid connections to the V_{IN} and V_{OUT} pins of the ecoSwitch to copper planes should be used to achieve low series resistance and good thermal dissipation. The ecoSwitch requires ample heat dissipation for correct thermal lockout operation. The internal FET dissipates load condition dependent amounts of power in the milliseconds following the rising edge of enable, and providing good thermal conduction from the packaging to the board is critical. The amount of heat spreading available to the part affects the maximum OCP threshold. Higher self−heating will cause the OCP trip point to decrease. Capacitive coupling of V_{IN} to V_{OUT} should be avoided, as this will adversely affect slew rates.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

DFN12 3x3, 0.5P
CASE 506EN
ISSUE O

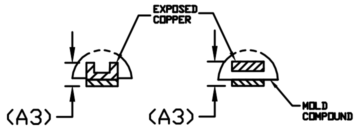
DATE 27 SEP 2018



TOP VIEW

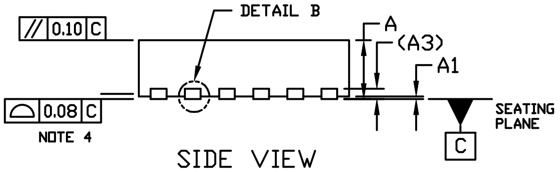
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	—	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	2.90	3.00	3.10
D2	1.03	1.13	1.23
E	2.90	3.00	3.10
E2	1.80	1.90	2.00
e	0.50 BSC		
k	0.20	—	—
L	0.20	0.30	0.40
L1	—	—	0.15

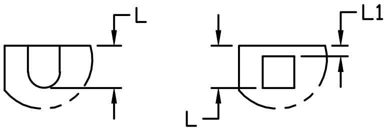


DETAIL B

ALTERNATE CONSTRUCTIONS

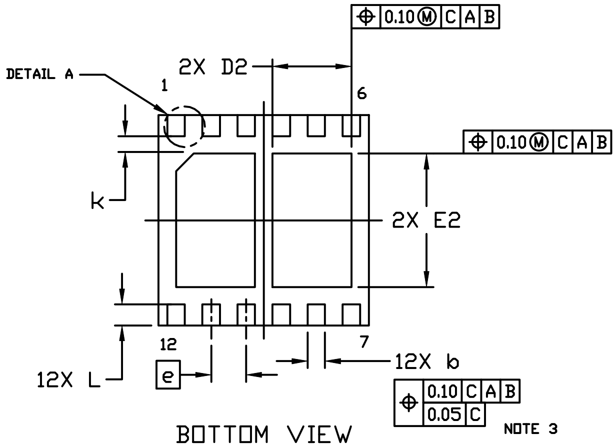


SIDE VIEW

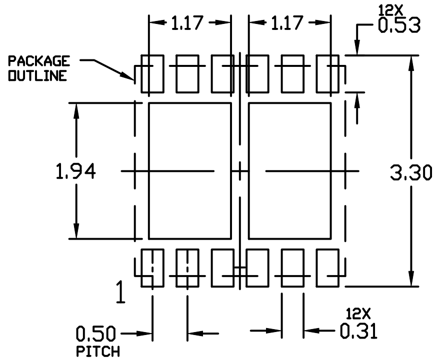


DETAIL A

ALTERNATE TERMINAL CONSTRUCTIONS

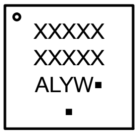


BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

GENERIC MARKING DIAGRAM*



XXXXX
XXXXX
ALYW▪
▪

XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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