

1. General description

Planar passivated AC Thyristor Triac power switch in a SOT186A (TO-220F) "full pack" plastic package with self-protective capabilities against low and high energy transients. This "series CTN" triac will commutate the full RMS current at the maximum rated junction temperature ($T_{j(max)} = 150\text{ °C}$) without the aid of a snubber. It is used in applications where "high junction operating temperature capability" is required.

2. Features and benefits

- Clamping structure ensuring safe high over-voltage withstand capability
- High junction operating temperature capability ($T_{j(max)} = 150\text{ °C}$)
- High minimum I_{GT} for guaranteed immunity to gate noise
- Full cycle AC conduction
- Over-voltage withstand capability to IEC 61000-4-5
- Pin compatible with standard triacs
- Planar passivated for voltage ruggedness and reliability
- Protective self turn-on capability for high energy transients
- Safe clamping capability for low energy over-voltage transients
- Less sensitive gate for high noise immunity
- Triggering in three quadrants only
- Very high immunity to false turn-on by dV/dt and IEC 61000-4-4 fast transient
- Package meets UL94V0 flammability requirement
- Package is RoHS compliant
- Package meets UL1557 isolation test requirement rated at 2500V RMS

3. Applications

- AC fan, pump and compressor controls
- Highly inductive, resistive and safety loads
- Large and small appliances (White Goods)
- Reversing induction motor controls
- Applications subject to high temperature ($T_{j(max)} = 150\text{ °C}$)

4. Quick reference data

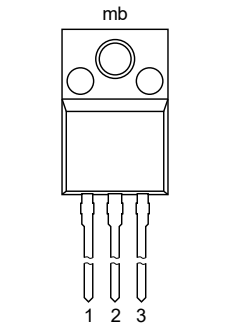
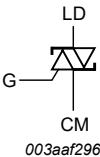
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_h \leq 70\text{ °C}$; Fig. 1 ; Fig. 2 ; Fig. 3	-	-	16	A

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 20\text{ ms}$; Fig. 4 ; Fig. 5		-	-	140	A
		full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 16.7\text{ ms}$		-	-	150	A
T_j	junction temperature			-	-	150	$^{\circ}\text{C}$
V_{PP}	peak pulse voltage	$T_j = 25\text{ }^{\circ}\text{C}$; non-repetitive, off-state; Fig. 6		-	-	2	kV
Static characteristics							
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7		5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7		5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 7		5	-	35	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 9		-	-	30	mA
V_T	on-state voltage	$I_T = 20\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; Fig. 10		-	-	1.5	V
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ }^{\circ}\text{C}$		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ }^{\circ}\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit		1500	-	-	V/ μs
		$V_{DM} = 536\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; exponential waveform; gate open circuit		1000	-	-	V/ μs
di_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; gate open circuit; snubberless condition		12	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit		15	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit		20	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	CM	common	 TO-220F (SOT186A)	 003aaf296
2	LD	load		
3	G	gate		
mb	n.c.	mounting base; isolated		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACTT16X-800CTN	TO-220F	plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3-lead TO-220 "full pack"	SOT186A

7. Limiting values

Table 4. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DRM}	repetitive peak off-state voltage		-	800	V
I _{T(RMS)}	RMS on-state current	full sine wave; T _h ≤ 70 °C; Fig. 1; Fig. 2; Fig. 3	-	16	A
I _{TSM}	non-repetitive peak on-state current	full sine wave; T _{j(init)} = 25 °C; t _p = 20 ms; Fig. 4; Fig. 5	-	140	A
		full sine wave; T _{j(init)} = 25 °C; t _p = 16.7 ms	-	150	A
I ² t	I ² t for fusing	t _p = 10 ms; sine-wave pulse	-	98	A ² s
di _T /dt	rate of rise of on-state current	I _G = 70 mA	-	100	A/μs
I _{GM}	peak gate current		-	2	A
P _{GM}	peak gate power		-	5	W
P _{G(AV)}	average gate power	over any 20 ms period	-	0.5	W
T _{stg}	storage temperature		-40	150	°C
T _j	junction temperature		-	150	°C
V _{PP}	peak pulse voltage	T _j = 25 °C; non-repetitive, off-state; Fig. 6	-	2	kV

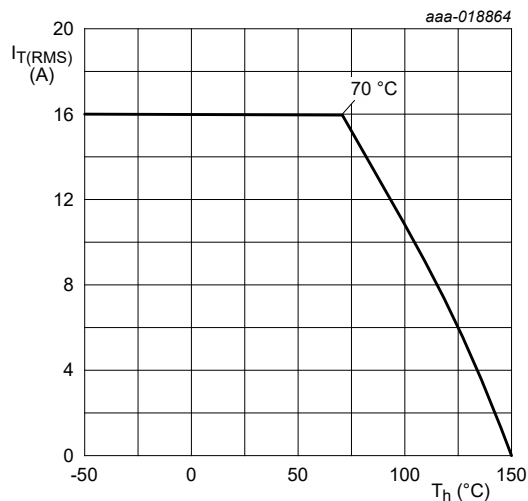


Fig. 1. RMS on-state current as a function of heatsink temperature; maximum values

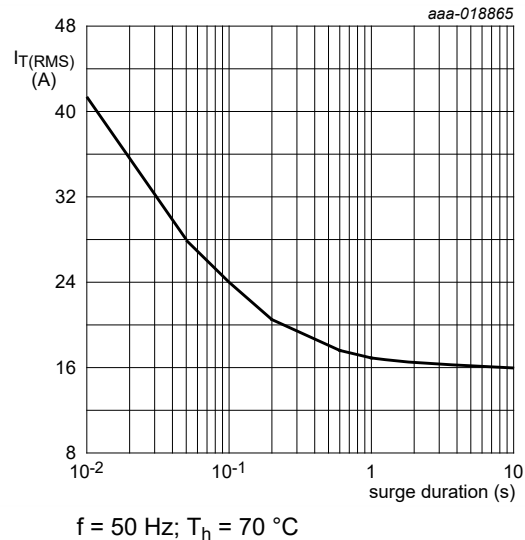


Fig. 2. RMS on-state current as a function of surge duration; maximum values
f = 50 Hz; T_h = 70 °C

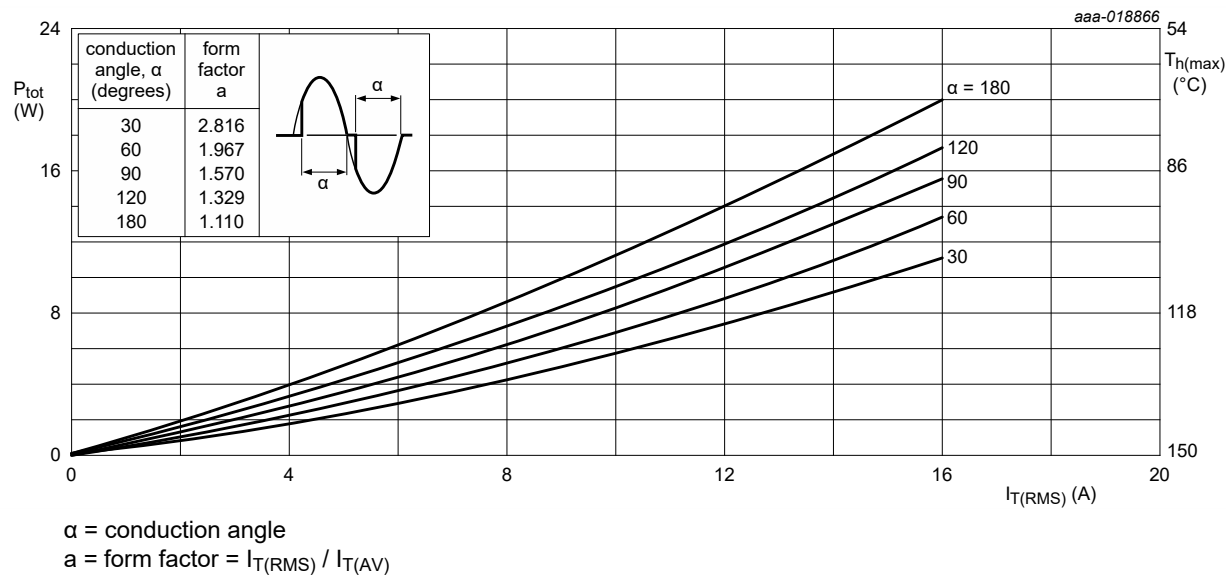


Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

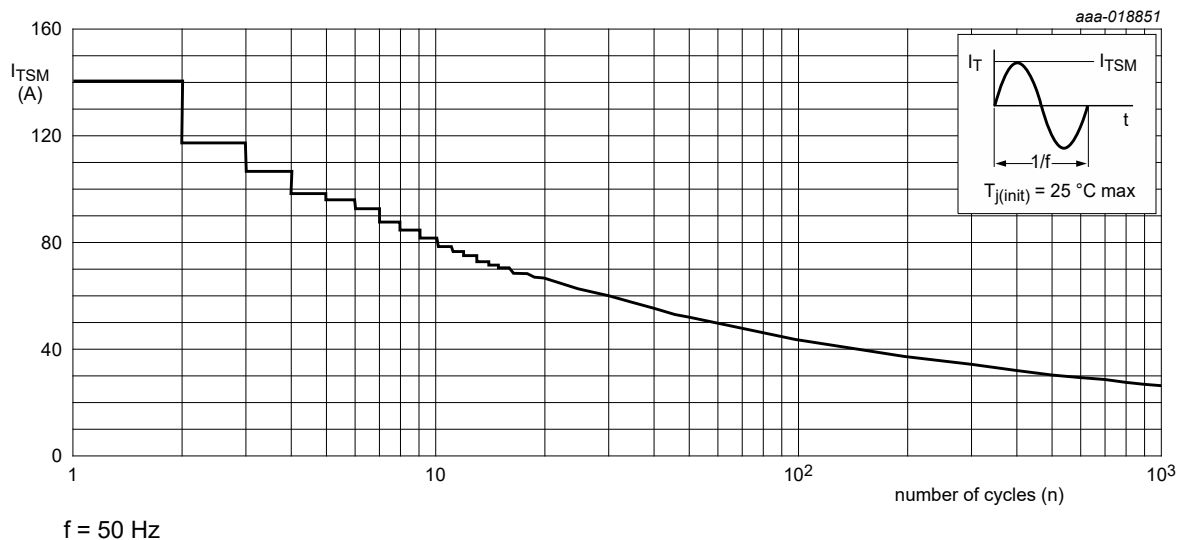


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

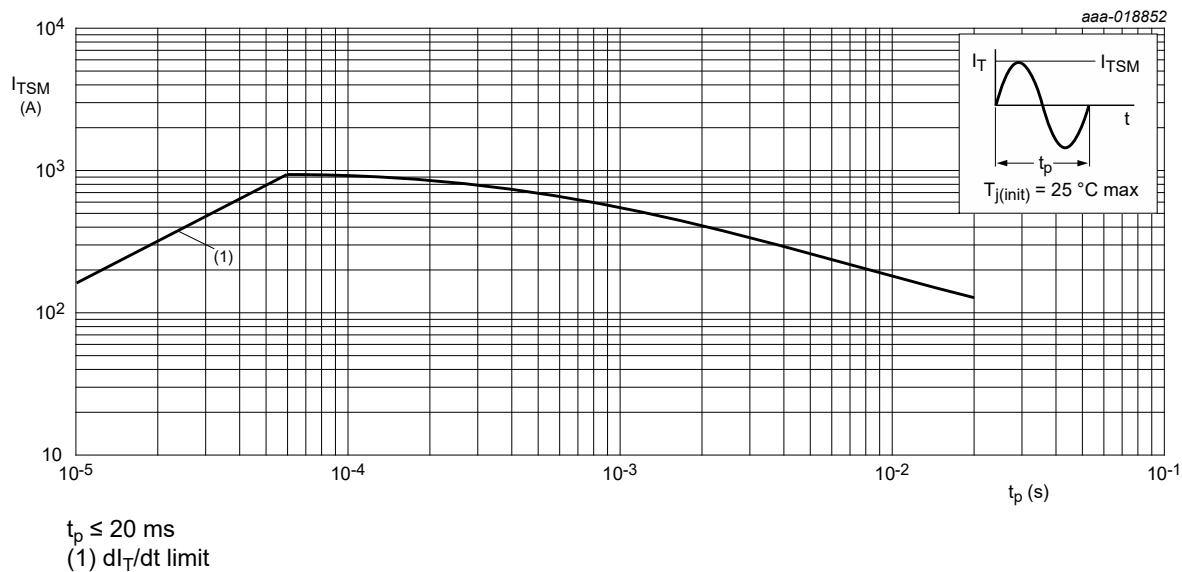


Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

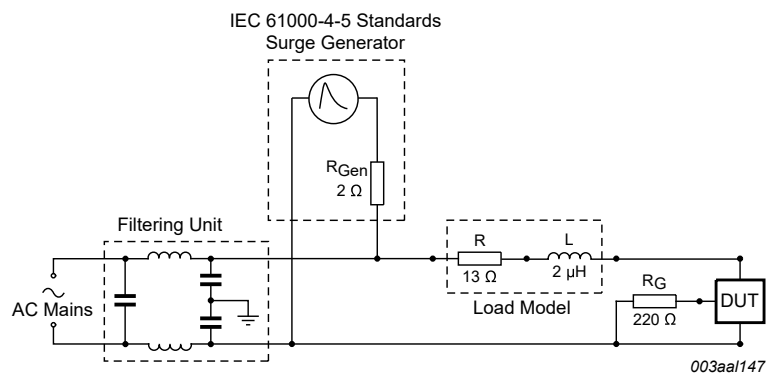


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-h)}$	thermal resistance from junction to heatsink	full or half cycle; with heatsink compound		-	-	4	K/W
		full or half cycle; without heatsink compound		-	-	5.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	in free air		-	55	-	K/W

9. Isolation characteristics

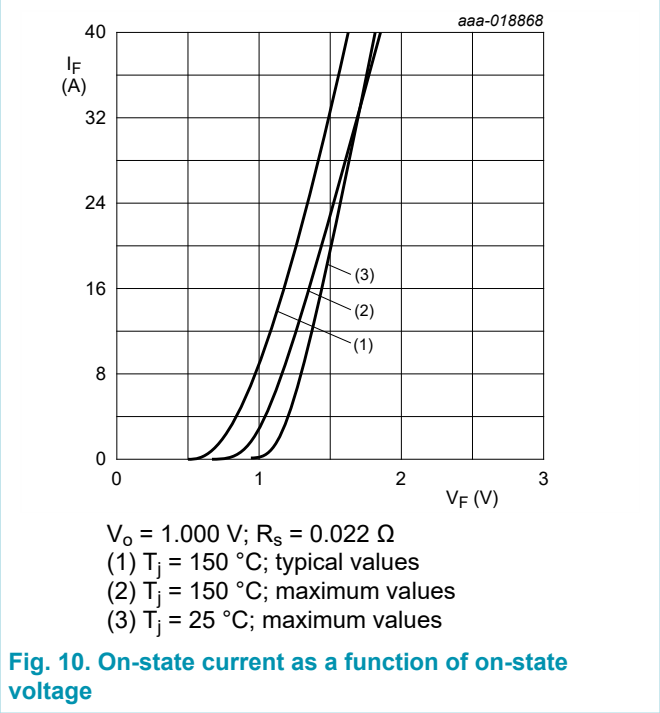
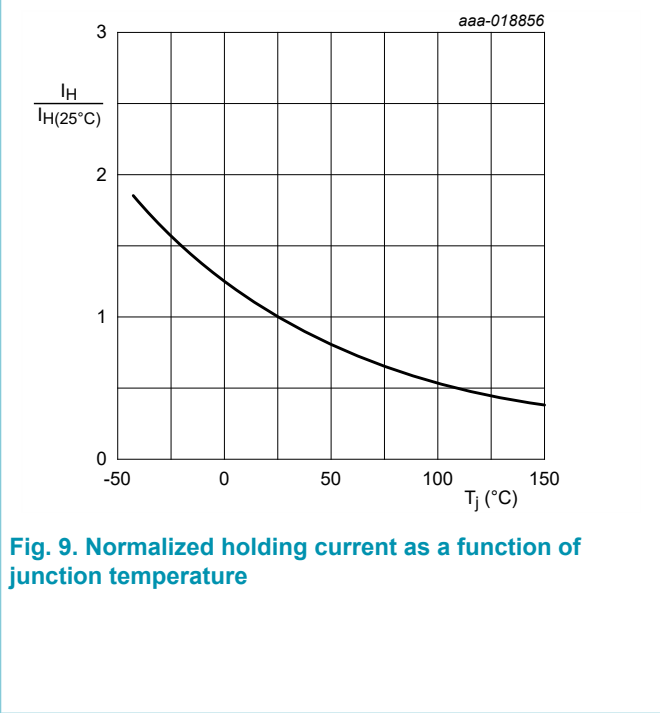
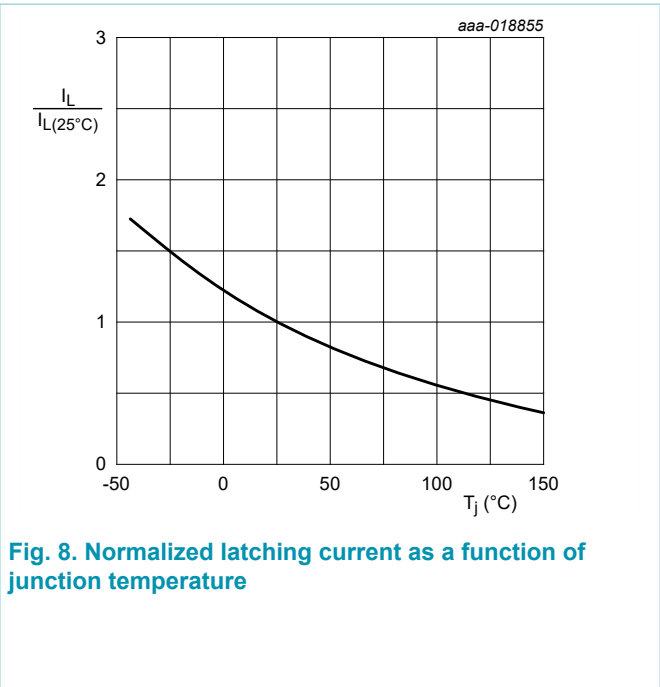
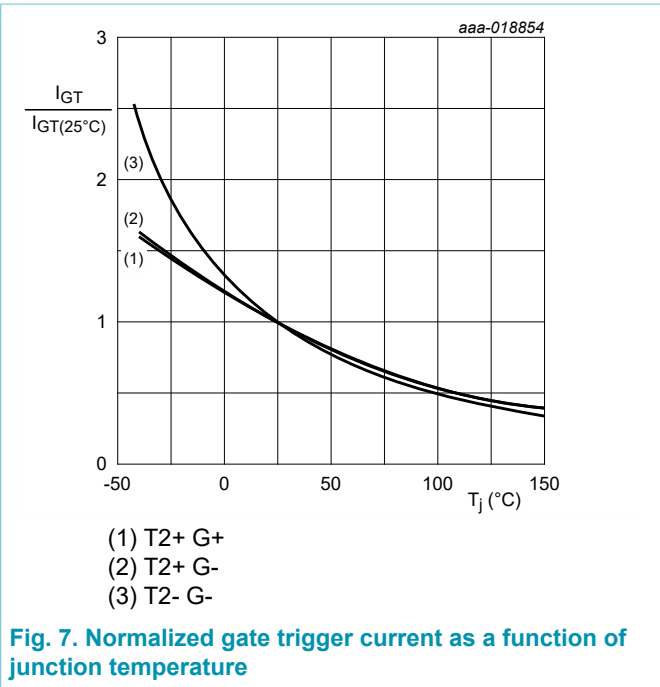
Table 6. Isolation characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{isol(RMS)}$	RMS isolation voltage	from all terminals to external heatsink; sinusoidal waveform; clean and dust free; $50\text{ Hz} \leq f \leq 60\text{ Hz}$; $T_h = 25\text{ }^{\circ}\text{C}$		-	-	2500	V
C_{isol}	isolation capacitance	from main terminal 2 to external heatsink; $f = 1\text{ MHz}$; $T_h = 25\text{ }^{\circ}\text{C}$		-	10	-	pF

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 7	5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 7	5	-	35	mA
		$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 7	5	-	35	mA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G+; $T_j = 25\text{ °C}$; Fig. 8	-	-	40	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD+ G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	50	mA
		$V_D = 12\text{ V}$; $I_G = 100\text{ mA}$; LD- G-; $T_j = 25\text{ °C}$; Fig. 8	-	-	40	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ °C}$; Fig. 9	-	-	30	mA
V_T	on-state voltage	$I_T = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 10	-	-	1.5	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 11	-	0.8	1	V
		$V_D = 400\text{ V}$; $I_T = 100\text{ mA}$; $T_j = 150\text{ °C}$; Fig. 11	0.2	0.45	-	V
I_D	off-state current	$V_D = 800\text{ V}$; $T_j = 25\text{ °C}$	-	-	10	μA
		$V_D = 800\text{ V}$; $T_j = 150\text{ °C}$	-	-	2	mA
V_{CL}	clamping voltage	$I_{CL} = 0.1\text{ mA}$; $t_p = 1\text{ ms}$; $T_j = 25\text{ °C}$	850	-	-	V
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 536\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	1500	-	-	V/ μs
		$V_{DM} = 536\text{ V}$; $T_j = 150\text{ °C}$; exponential waveform; gate open circuit	1000	-	-	V/ μs
dI_{com}/dt	rate of change of commutating current	$V_D = 400\text{ V}$; $T_j = 150\text{ °C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 20\text{ V}/\mu\text{s}$; gate open circuit; snubberless condition	12	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 150\text{ °C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 10\text{ V}/\mu\text{s}$; gate open circuit	15	-	-	A/ms
		$V_D = 400\text{ V}$; $T_j = 150\text{ °C}$; $I_{T(RMS)} = 16\text{ A}$; $dV_{com}/dt = 1\text{ V}/\mu\text{s}$; gate open circuit	20	-	-	A/ms



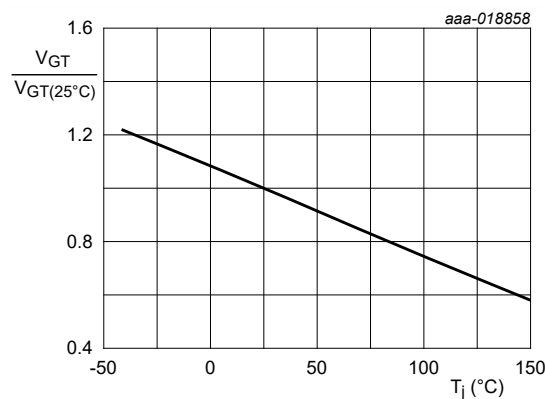
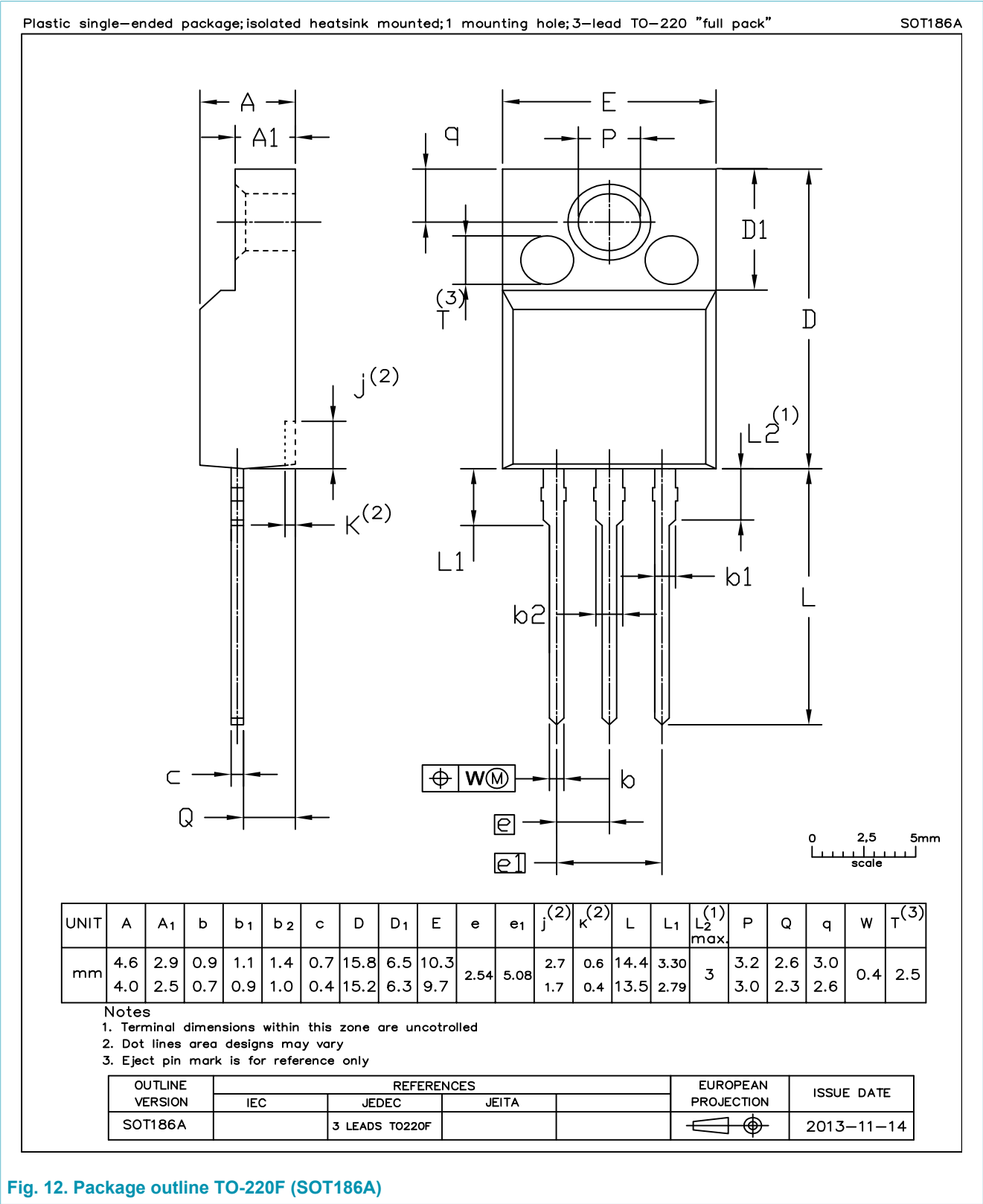


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline



12. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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