1. Overview

1.1 Features

The M16C/5LD and M16C/56D Group's microcomputers (MCUs) are single-chip control units that utilize high-performance silicon gate CMOS technology with the M16C/60 Series CPU core. The M16C/5LD and M16C/56D Groups are available in 64-pin and 80-pin plastic molded LQFP packages. These MCUs employ sophisticated instructions for a high level of efficiency and they are capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier and DMAC for high-speed operation processing which make it adequate for controlling office equipment, home appliances, and industrial equipment.
The M16C/5LD Group has one CAN module, which makes it suitable for factory automation LAN system.

1.1.1 Applications

Factory automation LAN system, audio components, cameras, televisions, household appliances, office equipment, communication devices, mobile devices, industrial equipment, and other applications.

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1.2 Specifications

Table 1.1 to Table 1.4 list specifications of the M16C/5LD Group, M16C/56D Group.

Table 1.1 Specifications (80-pin Version) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits) • Basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC = 3.0 to 5.5 V) 40ns (f(BCLK) = 25MHz, VCC = 2.7 to 5.5V) • Operating mode: Single-chip mode
Memory	ROM, RAM, data flash	See Table 1.5. and Table 1.6.
Voltage Detection	Voltage detector	• 2 voltage detect points
Clock	Clock generator	• 4 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable • Low-power consumption modes: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• 71 CMOS inputs/outputs, a pull-up resistor selectable
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{\text{NMI}}$, $\overline{\text{INT}}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		• 15 bits × 1 (with prescaler) • Automatic reset start function selectable • Dedicated 125 kHz on-chip oscillator for the watchdog timer contained
DMA	DMAC	• 4 channels, Cycle-steal transfer mode • Trigger sources: 42 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 3 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/ output compare)	• 16-bit timer × 1 (base timer) • I/O: 8 channels
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART4	4 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I^2C-bus, IEBus)
A/D Converter		10-bit resolution × 27 channels (A/D circuit) 10-bit resolution × 4 channels (A/D1 circuit)

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Table 1.2 Specifications (80-pin Version) (2/2)

Item	Function	Specification
CRC Calculator		• 1 circuit • CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant • MSB/LSB selectable
Multi-master I^2C-bus Interface		1 channel
CAN Module		32-slot message buffer × 1 channel (M16C/5LD Group only)
Flash Memory		• Programming and erasure supply voltage: 2.7 to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V 25 MHz / 2.7 to 5.5 V
Current Consumption		Described in 5. “Electrical Characteristics”
Operating Temperature		-40°C to 85°C (1)
Package		80-pin plastic mold LQFP: PLQP0080KB-A (Previous package code: 80P6Q-A)

Note:
1. Refer to Table 1.5 “Product List of M16C/5LD Group” and Table 1.6 “Product List of M16C/56D Group” for the Operating Temperature.

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Table 1.3 Specifications (64-pin Version) (1/2)

Item	Function	Specification
CPU	Central processing unit	M16C/60 Series CPU Core (Multiplier: 16 × 16 → 32 bits, Multiply-accumulate unit: 16 × 16 + 32 → 32 bits) • Basic instructions: 91 • Minimum instruction execution time: 31.25 ns (f(BCLK) = 32 MHz, VCC = 3.0 to 5.5 V) 40ns (f(BCLK) = 25MHz, VCC = 2.7 to 5.5V) • Operating mode: Single-chip mode
Memory	ROM, RAM, data flash	See Table 1.5. and Table 1.6.
Voltage Detection	Voltage detector	2 voltage detect points
Clock	Clock generator	• 4 circuits (Main clock, sub clock, PLL frequency synthesizer, 125 kHz on-chip oscillator) • Oscillation stop detector: Main clock oscillator stop/restart detection • Frequency divide circuit: Divide-by-1, 2, 4, 8, or 16 selectable • Low-power consumption modes: Wait mode, stop mode • Real-time clock
I/O Ports	Programmable I/O ports	• 55 CMOS inputs/outputs, a pull-up resistor selectable
Interrupts		• Interrupt vectors: 70 • External interrupt inputs: 11 ($\overline{NMI}$, $\overline{INT}$ × 6, key input × 4) • Interrupt priority levels: 7
Watchdog Timer		• 15 bits × 1 (with prescaler) • Automatic reset start function selectable • Dedicated 125 kHz on-chip oscillator for the watchdog timer contained
DMA	DMAC	• 4 channels, Cycle-steal transfer mode • Trigger sources: 40 • Transfer modes: 2 (single transfer, repeat transfer)
Timers	Timer A	16-bit timer × 5 Timer mode, event counter mode, one-shot timer mode, pulse-width modulation (PWM) mode Two-phase pulse signal processing in event counter mode (two-phase encoder input) × 3 Programmable output mode × 3
	Timer B	16-bit timer × 3 Timer mode, event counter mode, pulse frequency measurement mode, pulse-width measurement mode
	Timer function for three-phase motor control	Three-phase motor control timer × 1 (timers A1, A2, A4, and B2 used) On-chip dead time timer
	Timer S (Input capture/output compare)	• 16-bit timer × 1 (base timer) • I/O: 8 channels
	Task monitoring timer	16-bit timer × 1 channel
	Real-time clock	Count: seconds, minutes, hours, weeks
Serial Interface	UART0 to UART3	3 channels (UART, clock synchronous serial interface) 1 channels (UART, clock synchronous serial interface, I^2C-bus, IEBus)
A/D Converter		10-bit resolution × 16 channels (A/D circuit) 10-bit resolution × 4 channels (A/D1 circuit)

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Table 1.4 Specifications (64-pin Version) (2/2)

Item	Function	Specification
CRC Calculator		• 1 circuit • CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant • MSB/LSB selectable
Multi-master I^2C-bus Interface		1 channel
CAN Module		32-slot message buffer × 1 channel (M16C/5LD Group only)
Flash Memory		• Programming and erasure supply voltage: 2.7 to 5.5 V • Programming and erasure endurance: 1,000 times (program ROM 1, program ROM 2)/10,000 times (data flash) • Program security: ROM code protect, ID code check
Debug Functions		On-board flash rewrite function, address match × 4
Operating Frequency/Power Supply Voltage		32 MHz / 3.0 to 5.5 V 25 MHz / 2.7 to 5.5 V
Current Consumption		Described in 5. “Electrical Characteristics”
Operating Temperature		-40°C to 85°C (1)
Package		64-pin plastic mold LQFP: PLQP0064KB-A (Previous package code: 64P6Q-A)

Note:
1. Refer to Table 1.5 “Product List of M16C/5LD Group” and Table 1.6 “Product List of M16C/56D Group” for the Operating Temperature.

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1.3 Product List

Table 1.5 shows product information on the M16C/5LD Group, M16C/56D Group. Figure 1.1 shows part numbers, memory sizes, and packages. Figure 1.2 shows marking drawing (top view).

Table 1.5 Product List of M16C/5LD Group As of November 2011

Part Number	ROM Capacity			RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash				
R5F35L30DFF	64 KB	16 KB	4 KB x 2 blocks	4 KB	1 channel	PLQP0064KB-A	
R5F35L23DFE	96 KB	16 KB	4 KB x 2 blocks	8 KB		PLQP0080KB-A	
R5F35L33DFF						PLQP0064KB-A	
R5F35L26DFE	128 KB	16 KB	4 KB x 2 blocks	12 KB		PLQP0080KB-A	
R5F35L36DFF						PLQP0064KB-A	
R5F35L2EDFE	256 KB	16 KB	4 KB x 2 blocks	20 KB		PLQP0080KB-A	
R5F35L3EDFF						PLQP0064KB-A	

(D): Under development
(P): Under planning

The old package names are as follows:
PLQP0080KB-A: 80P6Q-A
PLQP0064KB-A: 64P6Q-A

Table 1.6 Product List of M16C/56D Group As of November 2011

Part Number	ROM Capacity			RAM Capacity	CAN	Package Name	Remarks
	Program ROM 1	Program ROM 2	Data flash				
R5F35630DFF	64 KB	16 KB	4 KB x 2 blocks	4 KB	N/A	PLQP0064KB-A	
R5F35623DFE	96 KB	16 KB	4 KB x 2 blocks	8 KB		PLQP0080KB-A	
R5F35633DFF						PLQP0064KB-A	
R5F35626DFE	128 KB	16 KB	4 KB x 2 blocks	12 KB		PLQP0080KB-A	
R5F35636DFF						PLQP0064KB-A	
R5F3562EDFE	256 KB	16 KB	4 KB x 2 blocks	20 KB		PLQP0080KB-A	
R5F3563EDFF						PLQP0064KB-A	

(D): Under development
(P): Under planning

The old package names are as follows:
PLQP0080KB-A: 80P6Q-A
PLQP0064KB-A: 64P6Q-A

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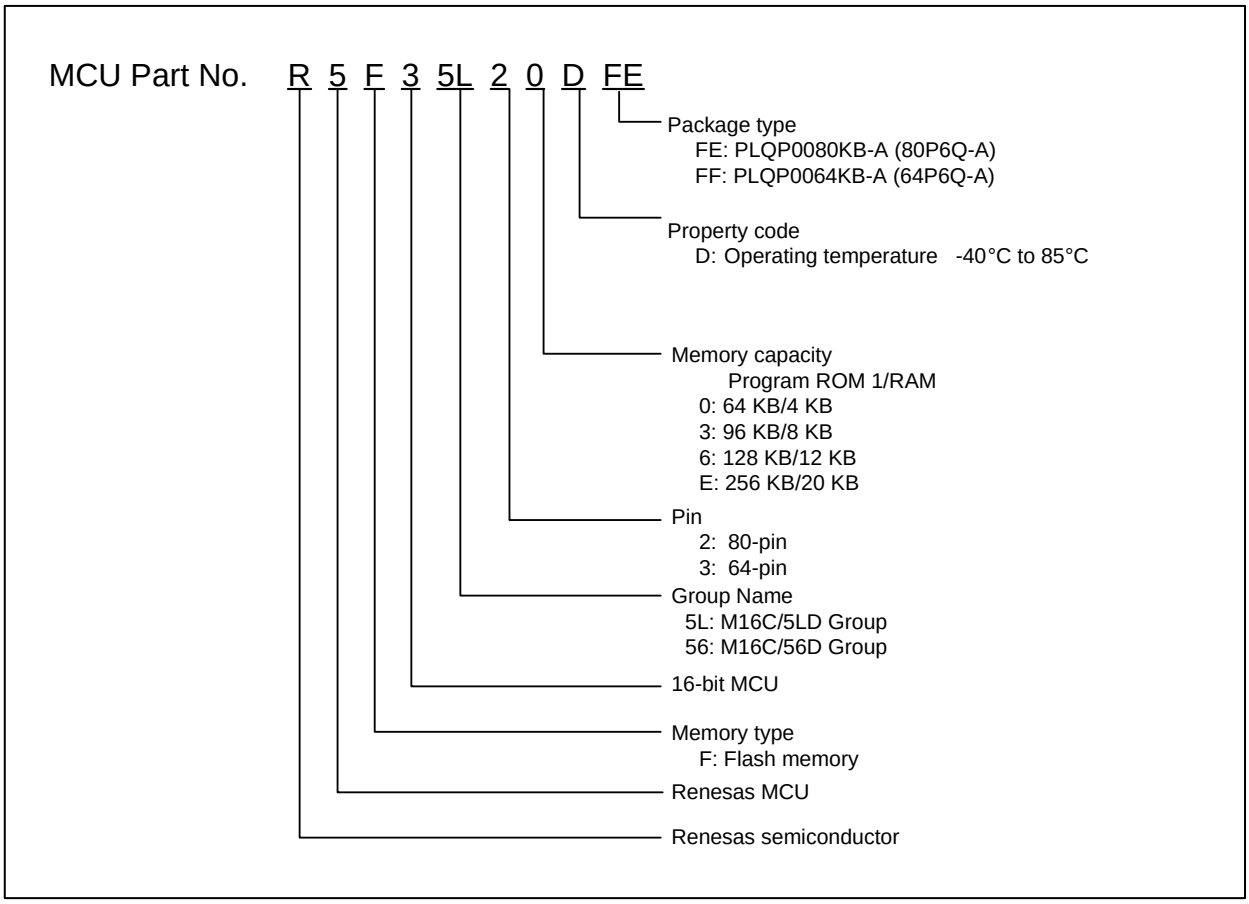


Figure 1.1 Correspondence of Part Number, Memory Size, and Package

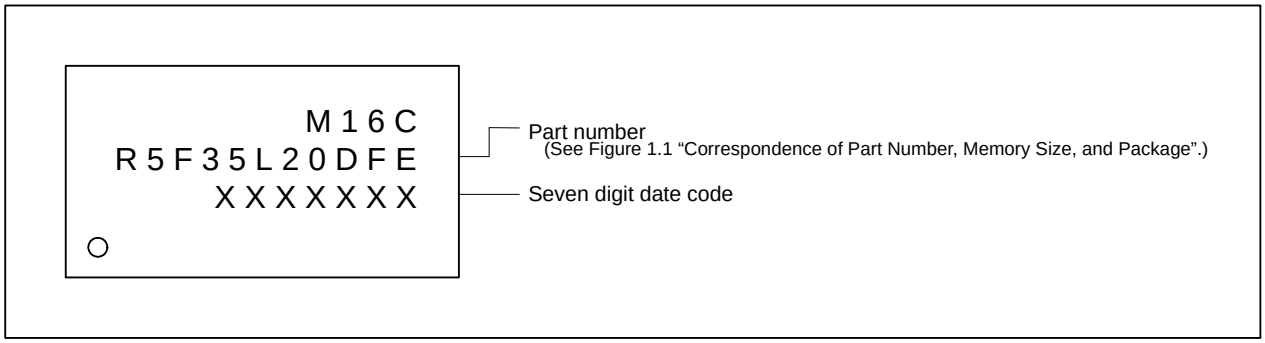
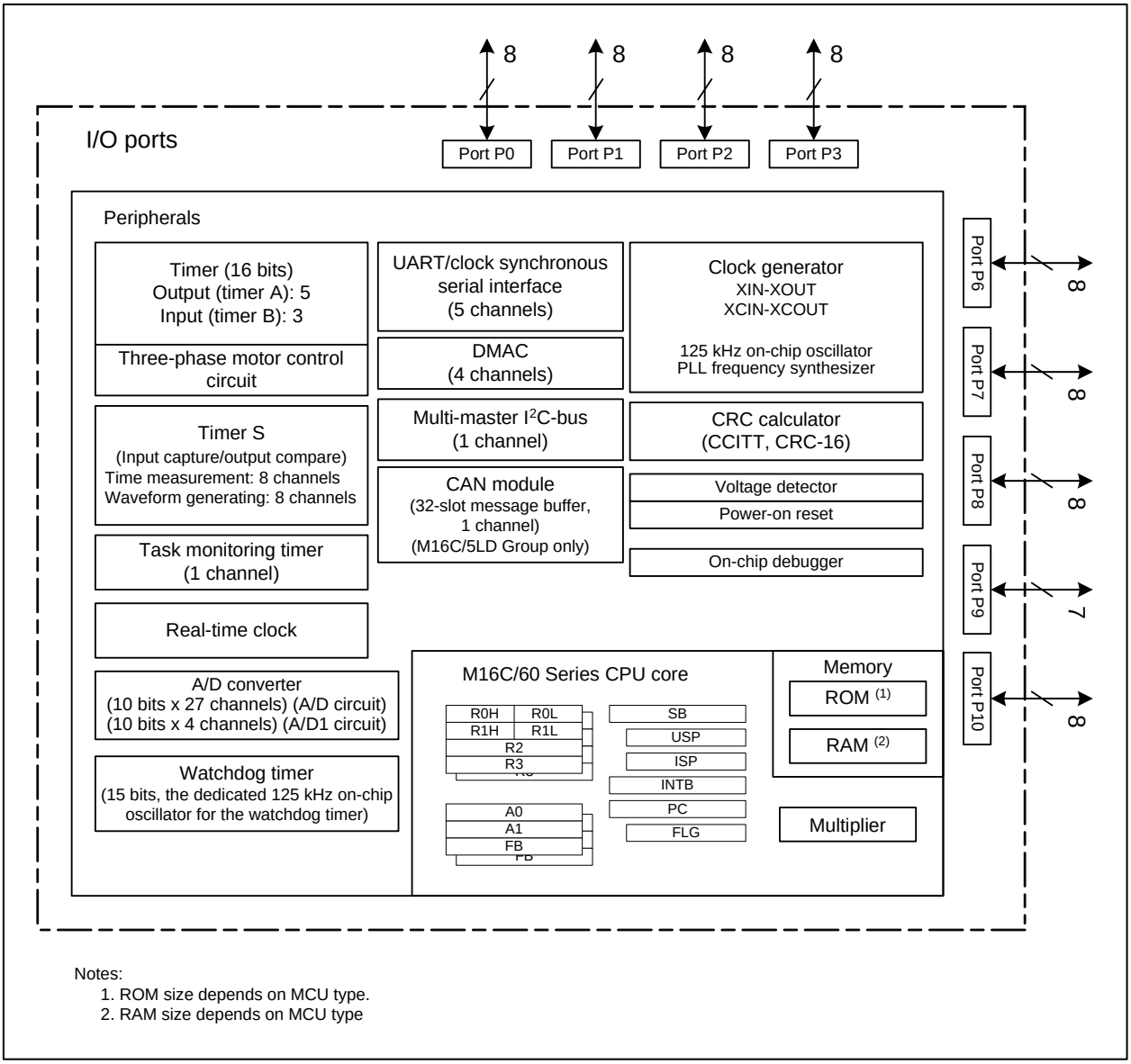


Figure 1.2 Marking Diagram of Flash Memory Version (Top View)

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1.4 Block Diagram

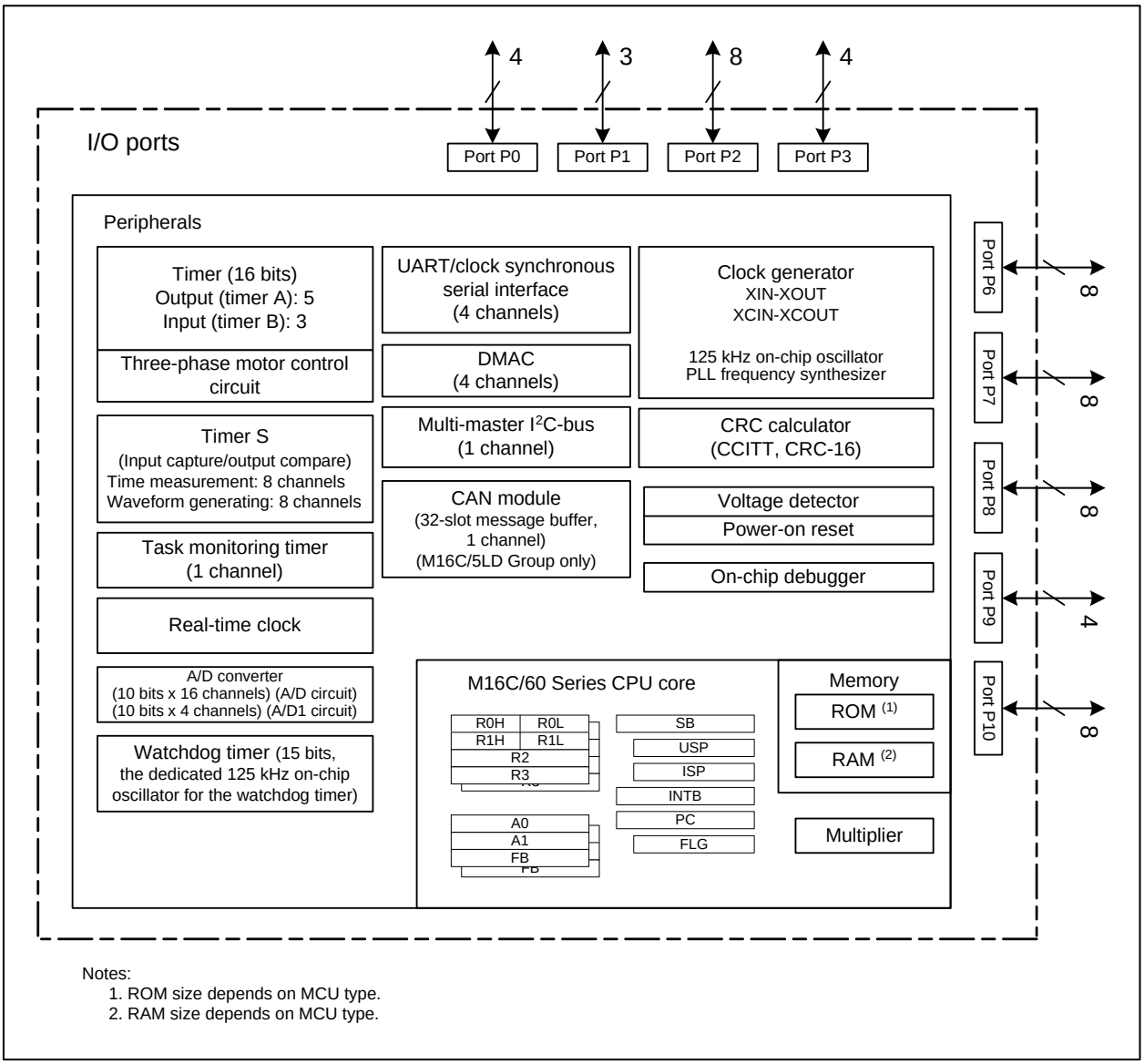
Figure 1.3 shows a block diagram of M16C/5LD Group, M16C/56D Group 80-pin package. Figure 1.4 shows a block diagram of the M16C/5LD Group, M16C/56D Group 64-pin package.



Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type

Figure 1.3 80-Pin Block Diagram

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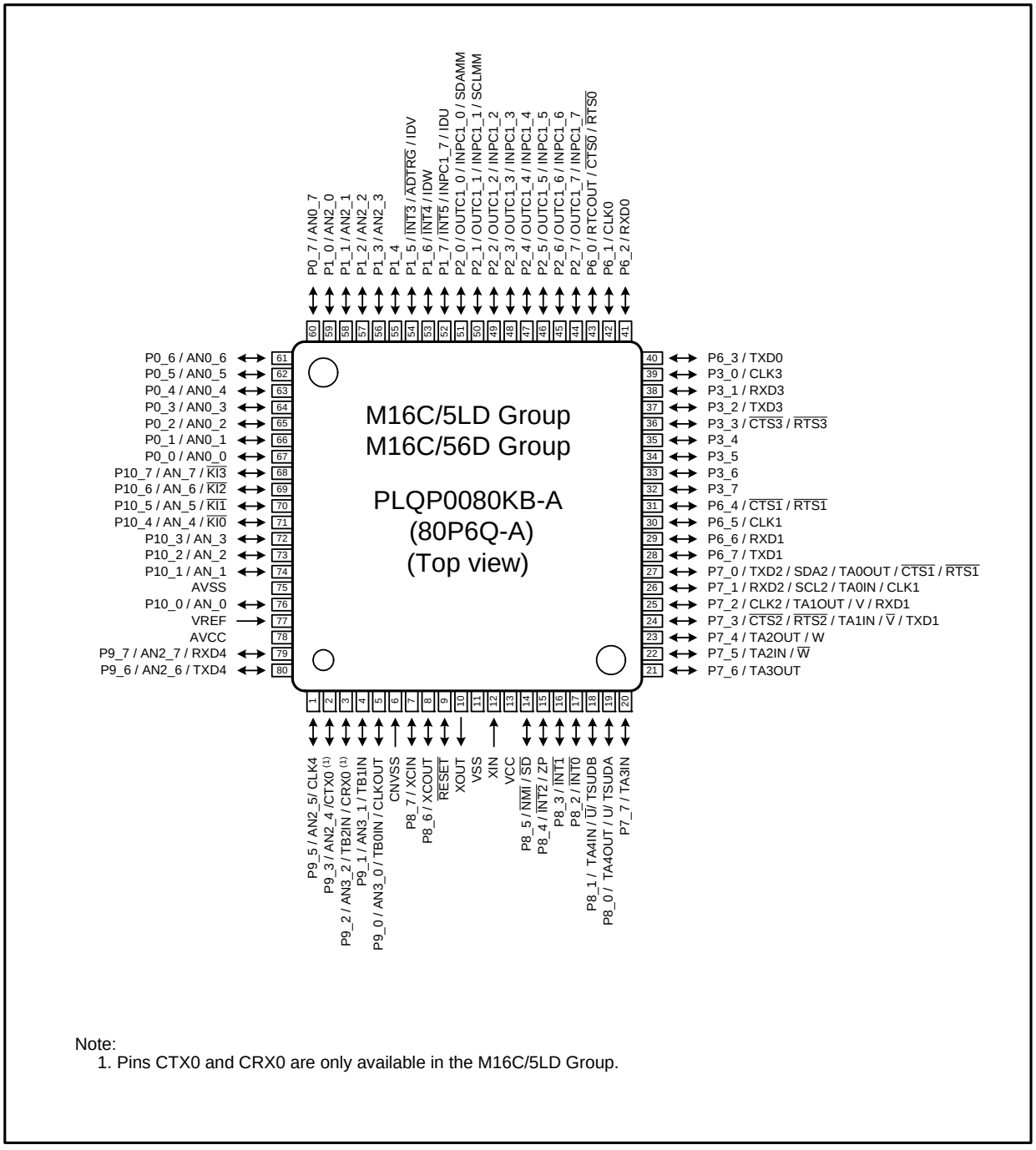
Notes:
1. ROM size depends on MCU type.
2. RAM size depends on MCU type.

Figure 1.4 64-Pin Block Diagram

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1.5 Pin Assignments

Figure 1.5 shows the pin assignments for 80-pin package, and Table 1.7 and Table 1.8 list pin names for 80-pin package.



Note:
1. Pins CTX0 and CRX0 are only available in the M16C/5LD Group.

Figure 1.5 Pin Assignment for 80-Pin Package (Top View)

Set bits PACR2 to PACR0 in the PACR register to 010b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

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Table 1.7 Pin Names, 80-Pin Package (1/2)

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I2C-bus pin	Analog Pin
1		P9_5				CLK4		AN2_5
2		P9_3				CTX0 (1)		AN2_4
3		P9_2		TB2IN		CRX0 (1)		AN3_2
4		P9_1		TB1IN				AN3_1
5	CLKOUT	P9_0		TB0IN				AN3_0
6	CNVSS							
7	XCIN	P8_7						
8	XCOUT	P8_6						
9	$\overline{\text{RESET}}$							
10	XOUT							
11	VSS							
12	XIN							
13	VCC							
14		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
15		P8_4	$\overline{\text{INT2}}$	ZP				
16		P8_3	$\overline{\text{INT1}}$					
17		P8_2	$\overline{\text{INT0}}$					
18		P8_1		TA4IN/$\overline{\text{U}}$	TSUDB			
19		P8_0		TA4OUT/U	TSUDA			
20		P7_7		TA3IN				
21		P7_6		TA3OUT				
22		P7_5		TA2IN/$\overline{\text{W}}$				
23		P7_4		TA2OUT/W				
24		P7_3		TA1IN/$\overline{\text{V}}$		$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1		
25		P7_2		TA1OUT/V		CLK2/RXD1		
26		P7_1		TA0IN		RXD2/SCL2/CLK1		
27		P7_0		TA0OUT		TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
28		P6_7				TXD1		
29		P6_6				RXD1		
30		P6_5				CLK1		
31		P6_4				$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
32		P3_7						
33		P3_6						
34		P3_5						
35		P3_4						
36		P3_3				$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$		
37		P3_2				TXD3		
38		P3_1				RXD3		
39		P3_0				CLK3		
40		P6_3				TXD0		

Note 1. There are pins CTX0 and CRX0 only in the M16C/5LD Group.

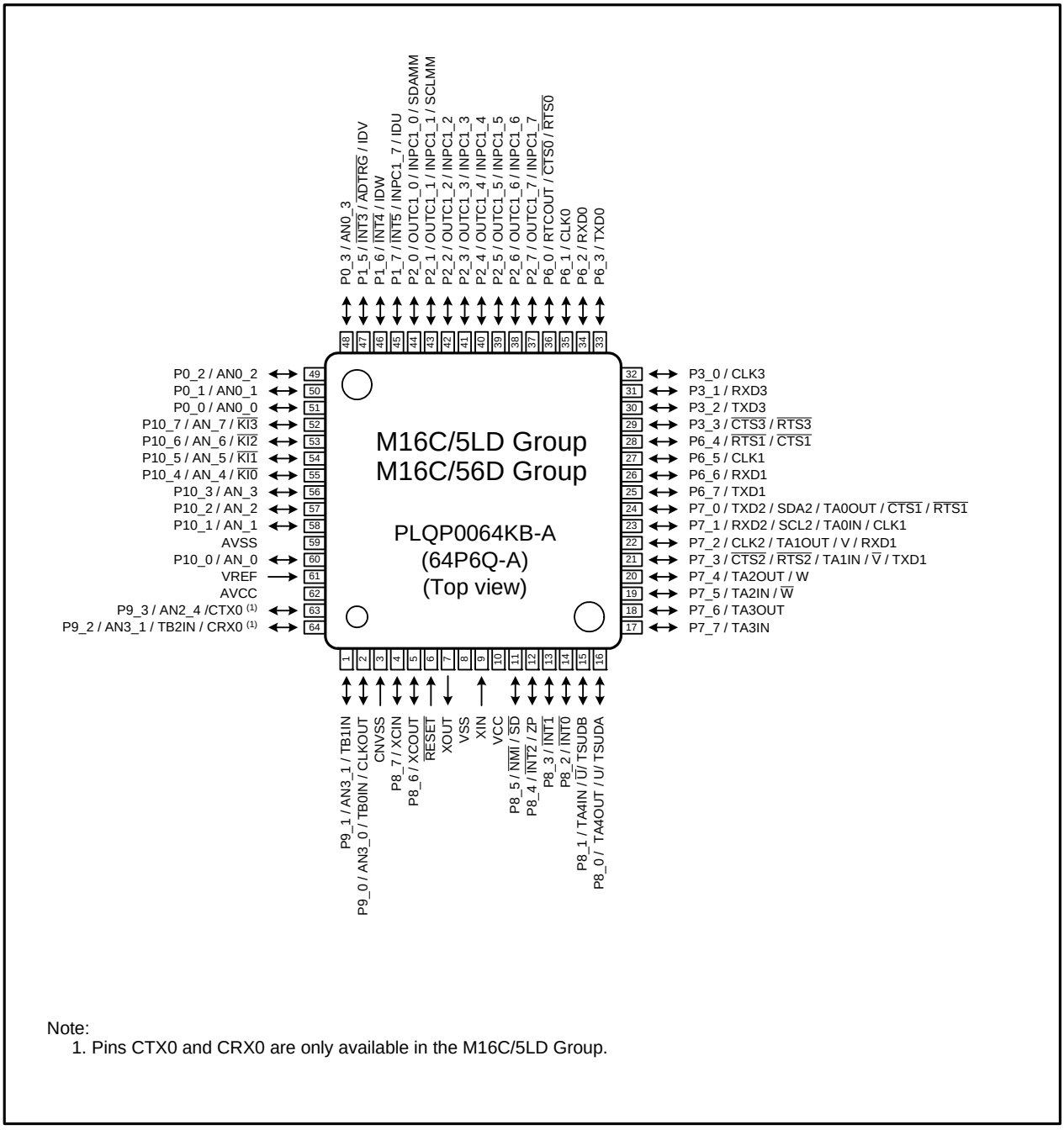
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Table 1.8 Pin Names, 80-Pin Package (2/2)

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I2C-bus pin	Analog Pin
41		P6_2				RXD0		
42		P6_1				CLK0		
43		P6_0		RTCOUT		$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
44		P2_7			OUTC1_7/INPC1_7			
45		P2_6			OUTC1_6/INPC1_6			
46		P2_5			OUTC1_5/INPC1_5			
47		P2_4			OUTC1_4/INPC1_4			
48		P2_3			OUTC1_3/INPC1_3			
49		P2_2			OUTC1_2/INPC1_2			
50		P2_1			OUTC1_1/INPC1_1		SCLMM	
51		P2_0			OUTC1_0/INPC1_0		SDAMM	
52		P1_7	$\overline{\text{INT5}}$	IDU	INPC1_7			
53		P1_6	$\overline{\text{INT4}}$	IDW				
54		P1_5	$\overline{\text{INT3}}$	IDV				$\overline{\text{ADTRG}}$
55		P1_4						
56		P1_3						AN2_3
57		P1_2						AN2_2
58		P1_1						AN2_1
59		P1_0						AN2_0
60		P0_7						AN0_7
61		P0_6						AN0_6
62		P0_5						AN0_5
63		P0_4						AN0_4
64		P0_3						AN0_3
65		P0_2						AN0_2
66		P0_1						AN0_1
67		P0_0						AN0_0
68		P10_7	$\overline{\text{KI3}}$					AN_7
69		P10_6	$\overline{\text{KI2}}$					AN_6
70		P10_5	$\overline{\text{KI1}}$					AN_5
71		P10_4	$\overline{\text{KI0}}$					AN_4
72		P10_3						AN_3
73		P10_2						AN_2
74		P10_1						AN_1
75	AVSS							
76		P10_0						AN_0
77	VREF							
78	AVCC							
79		P9_7				RXD4		AN2_7
80		P9_6				TXD4		AN2_6

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Figure 1.6 shows the pin assignments for 64-pin package and Table 1.9 and Table 1.10 list pin names for 64-pin package.



Note:
1. Pins CTX0 and CRX0 are only available in the M16C/5LD Group.

Figure 1.6 Pin Assignment for 64-Pin Package (Top View)

Set bits PACR2 to PACR0 in the PACR register to 010b before signals are input or output to individual pins after reset. When the PACR register is not set, signals are not input or output for some of the pins.

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Table 1.9 Pin Names, 64-Pin Package (1/2)

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I2C-bus pin	Analog Pin
1		P9_1		TB1IN				AN3_1
2	CLKOUT	P9_0		TB0IN				AN3_0
3	CNVSS							
4	XCIN	P8_7						
5	XCOUT	P8_6						
6	$\overline{\text{RESET}}$							
7	XOUT							
8	VSS							
9	XIN							
10	VCC							
11		P8_5	$\overline{\text{NMI}}$	$\overline{\text{SD}}$				
12		P8_4	$\overline{\text{INT2}}$	ZP				
13		P8_3	$\overline{\text{INT1}}$					
14		P8_2	$\overline{\text{INT0}}$					
15		P8_1		TA4IN/$\overline{\text{U}}$	TSUDB			
16		P8_0		TA4OUT/U	TSUDA			
17		P7_7		TA3IN				
18		P7_6		TA3OUT				
19		P7_5		TA2IN/$\overline{\text{W}}$				
20		P7_4		TA2OUT/W				
21		P7_3		TA1IN/$\overline{\text{V}}$		$\overline{\text{CTS2}}$/$\overline{\text{RTS2}}$/TXD1		
22		P7_2		TA1OUT/V		CLK2/RXD1		
23		P7_1		TA0IN		RXD2/SCL2/CLK1		
24		P7_0		TA0OUT		TXD2/SDA2/$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
25		P6_7				TXD1		
26		P6_6				RXD1		
27		P6_5				CLK1		
28		P6_4				$\overline{\text{CTS1}}$/$\overline{\text{RTS1}}$		
29		P3_3				$\overline{\text{CTS3}}$/$\overline{\text{RTS3}}$		
30		P3_2				TXD3		
31		P3_1				RXD3		
32		P3_0				CLK3		
33		P6_3				TXD0		
34		P6_2				RXD0		
35		P6_1				CLK0		
36		P6_0		RTCOUT		$\overline{\text{CTS0}}$/$\overline{\text{RTS0}}$		
37		P2_7			OUTC1_7/INPC1_7			
38		P2_6			OUTC1_6/INPC1_6			
39		P2_5			OUTC1_5/INPC1_5			
40		P2_4			OUTC1_4/INPC1_4			

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Table 1.10 Pin Names, 64-Pin Package (2/2)

Pin No.	Control pin	Port	Inter-rupt Pin	Timer Pin	Timer S Pin	UART/CAN Pin	Multi-master I^2C-bus pin	Analog Pin
41		P2_3			OUTC1_3/INPC1_3			
42		P2_2			OUTC1_2/INPC1_2			
43		P2_1			OUTC1_1/INPC1_1		SCLMM	
44		P2_0			OUTC1_0/INPC1_0		SDAMM	
45		P1_7	$\overline{INT5}$	IDU	INPC1_7			
46		P1_6	$\overline{INT4}$	IDW				
47		P1_5	$\overline{INT3}$	IDV				$\overline{ADTRG}$
48		P0_3						AN0_3
49		P0_2						AN0_2
50		P0_1						AN0_1
51		P0_0						AN0_0
52		P10_7	$\overline{KI3}$					AN_7
53		P10_6	$\overline{KI2}$					AN_6
54		P10_5	$\overline{KI1}$					AN_5
55		P10_4	$\overline{KI0}$					AN_4
56		P10_3						AN_3
57		P10_2						AN_2
58		P10_1						AN_1
59	AVSS							
60		P10_0						AN_0
61	VREF							
62	AVCC							
63		P9_3				CTX0 (1)		AN2_4
64		P9_2		TB2IN		CRX0 (1)		AN3_2

Note 1. There are pins CTX0 and CRX0 only in the M16C/5LD Group.

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1.6 Pin Functions

Table 1.11 Pin Functions (64-Pin and 80-Pin Packages) (1/2)

Signal Name	Pin Name	I/O	Description
Power supply	VCC, VSS	I	Apply 2.7 to 5.5 V to VCC pin and 0 V to VSS pin.
Analog power supply	AVCC, AVSS	I	Power supply for the A/D converter. Pins AVCC and AVSS should be connected to VCC and VSS, respectively.
Reset input	$\overline{\text{RESET}}$	I	Driving this pin low resets the MCU.
CNVSS	CNVSS	I	Connect to VSS via a resistor.
Main clock input	XIN	I	Input/output for the main clock oscillator. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. (1) To apply an external clock, connect it to XIN and leave XOUT open. When XIN is not used, connect XIN to VCC pin and leave XOUT open.
Main clock output	XOUT	O	
Sub clock input	XCIN	I	Input/output for the sub clock oscillator. Connect a crystal oscillator between XCIN and XCOUT. (1)
Sub clock output	XCOUT	O	
Clock output	CLKOUT	O	This pin outputs the clock having the same frequency as f1, f8, f32, or fC.
$\overline{\text{INT}}$ interrupt input	$\overline{\text{INT0}}$ to $\overline{\text{INT5}}$	I	Input for $\overline{\text{INT}}$ interrupt.
$\overline{\text{NMI}}$ input	$\overline{\text{NMI}}$	I	Input for $\overline{\text{NMI}}$ interrupt.
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Input for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	Timers A0 to A4 input/output
	TA0IN to TA4IN	I	Timers A0 to A4 input
	ZP	I	Input for Z-phase
Timer B	TB0IN to TB2IN	I	Timers B0 to B2 input
Three-phase motor control timer	U,$\overline{\text{U}}$,V,$\overline{\text{V}}$,W,$\overline{\text{W}}$	O	Output for three-phase motor control timers
	IDU, IDW, IDV, $\overline{\text{SD}}$	I	Input for three-phase motor control timers
Real-time clock	RTCOUT	O	Output for real-time clock
Serial interface UART0 to UART3	$\overline{\text{CTS0}}$ to $\overline{\text{CTS3}}$	I	Input to control data transmission
	$\overline{\text{RTS0}}$ to $\overline{\text{RTS3}}$	O	Output to control data reception
	CLK0 to CLK3	I/O	Transfer clock input/output
	RXD0 to RXD3	I	Serial data input
	TXD0 to TXD3	O	Serial data output
UART2 I^2C mode	SDA2	I/O	Serial data input/output
	SCL2	I/O	Transfer clock input/output
Multi-master I^2C-bus	SDAMM	I/O	Serial data input/output
	SCLMM		Transfer clock input/output

Note:
1. Please contact the manufacturer of crystal/ceramic resonator for oscillation characteristic.

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Table 1.12 Pin Functions (64-Pin and 80-Pin Packages) (2/2)

Signal Name	Pin Name	I/O	Description
Reference voltage input	VREF	I	Reference voltage input pin for the A/D converter.
A/D converter	AN_0 to AN_7	I	Analog input
	AN0_0 to AN0_3 AN2_4 AN3_0 to AN3_2	I	
	$\overline{\text{ADTRG}}$	I	Input for an external trigger
Timer S	INPC1_0 to INPC1_7	I	Input for time measurement function
	OUTC1_0 to OUTC1_7	O	Output for waveform generating function
	TSUDA, TSUDB	I	Two-phase pulse input
CAN Module (1)	CRX0	I	Receive data input for CAN communication
	CTX0	O	Transmit data output for CAN communication
I/O port	P0_0 to P0_3 P1_5 to P1_7 P2_0 to P2_7 P3_0 to P3_3 P6_0 to P6_7 P7_0 to P7_7 P8_0 to P8_7 P9_0 to P9_3 P10_0 to P10_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, pull-up resistor is selectable for every unit of 4 bits.

Note:
1. The CAN module is only in the M16C/5LD Group.

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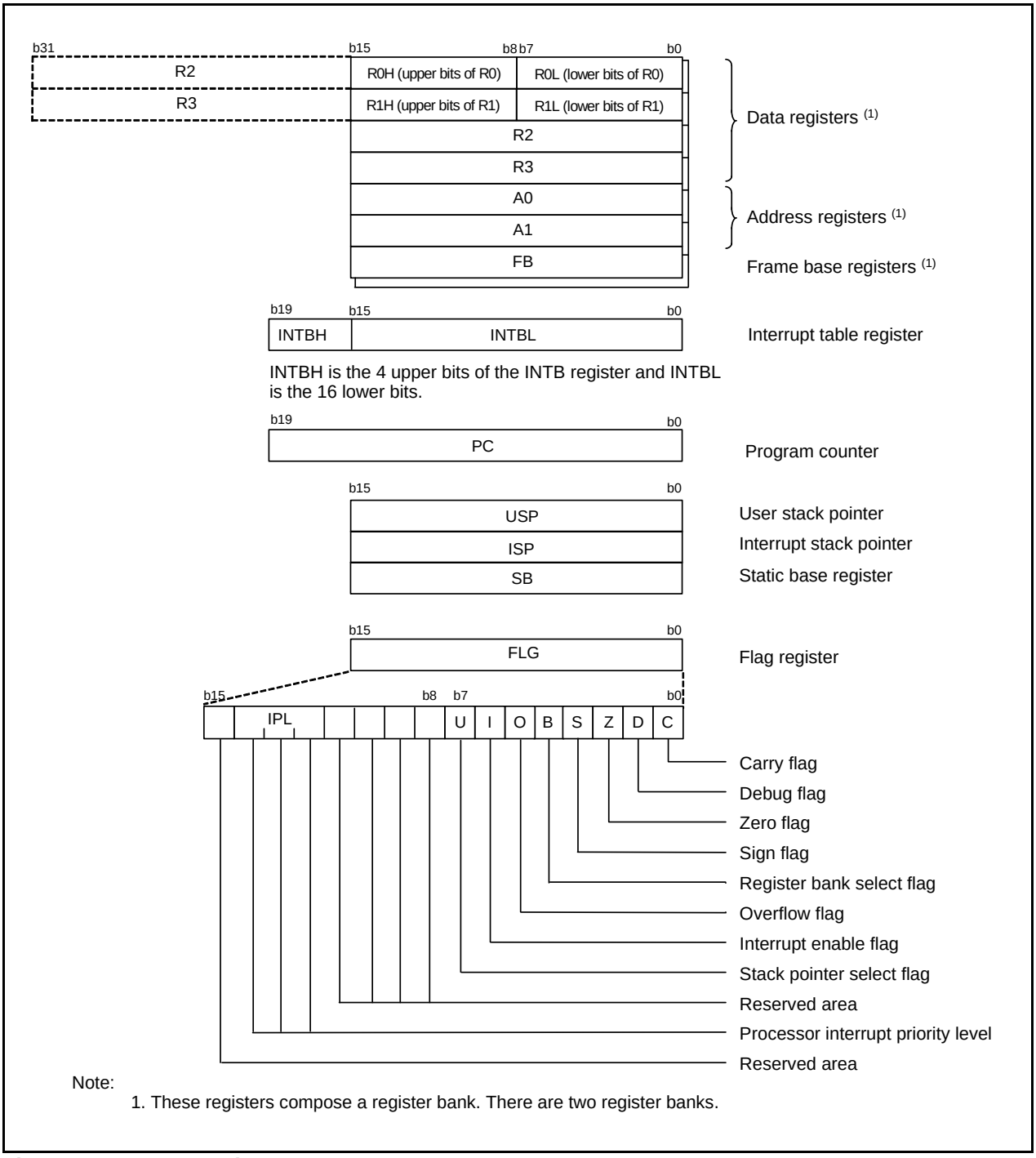
Table 1.13 Pin Functions (80-Pin Package Only)

Signal Name	Pin Name	I/O	Description
Serial Interface UART4	CLK4	I/O	Transfer clock input/output
	RXD4	I	Serial data input
	TXD4	O	Serial data output
A/D converter	AN0_4 to AN0_7 AN2_0 to AN2_3 AN2_5 to AN2_7	I	Analog input for the A/D converter
I/O port	P0_4 to P0_7 P1_0 to P1_4 P3_4 to P3_7 P9_5 to P9_7	I/O	CMOS I/O ports. Each port has a corresponding direction register with which each pin can be set to input or output. For input ports, pull-up resistor is selectable for every unit of 4 bits.

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2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. Seven registers (R0, R1, R2, R3, A0, A1, and FB) out of 13 compose a register bank, and there are two register banks.



Note:
1. These registers compose a register bank. There are two register banks.

Figure 2.1 CPU Registers

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2.1 Data Registers (R0, R1, R2, and R3)

R0, R1, R2, and R3 are 16-bit registers used for transfer, arithmetic, and logic operations. R0 and R1 can be split into upper (R0H/R1H) and lower (R0L/R1L) bits to be used separately as 8-bit data registers. R0 can be combined with R2, and R3 can be combined with R1 and be used as 32-bit data registers R2R0 and R3R1, respectively.

2.2 Address Registers (A0 and A1)

A0 and A1 are 16-bit registers used for indirect addressing, relative addressing, transfer, arithmetic, and logic operations. A0 can be combined with A1 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register that is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

The PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The USP and ISP stack pointers (SP) are each comprised of 16 bits. The U flag is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C Flag)

The C flag retains a carry, borrow, or shift-out bit generated by the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z Flag)

The Z flag becomes 1 when an arithmetic operation results in 0. Otherwise, it becomes 0.

2.8.4 Sign Flag (S Flag)

The S flag becomes 1 when an arithmetic operation results in a negative value. Otherwise, it becomes 0.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O Flag)

The O flag becomes 1 when an arithmetic operation results in an overflow. Otherwise, it becomes 0.

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2.8.7 Interrupt Enable Flag (I Flag)

The I flag enables maskable interrupts.
Maskable interrupts are disabled when the I flag is 0, and enabled when it is 1. The I flag becomes 0 when an interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1.
The U flag becomes 0 when a hardware interrupt request is accepted, or the INT instruction of software interrupt number 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from 0 to 7.
If a requested interrupt has higher priority than IPL, the interrupt request is enabled.

2.8.10 Reserved Areas

Only set these bits to 0. The read value is undefined.

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3. Memory

Special function registers (SFRs) are allocated from address 00000h to 003FFh and from 0D000h to 0D7FFh. Peripheral function control registers are located here. All blank spaces within SFRs are reserved, so do not access any blank spaces.

The internal RAM is allocated from address 00400h to superior direction. For example, a 8 KB internal RAM is addressed from 00400h to 023FFh. The internal RAM is used not only for data storage but also for stack area when subroutines are called or when interrupt request are acknowledged.

The internal ROM is flash memory. Three internal ROM areas are available: data flash, program ROM 1, and program ROM 2.

The data flash is addressed from 0E000h to 0FFFFh. This data flash space is used not only for data storage but also for program storage.

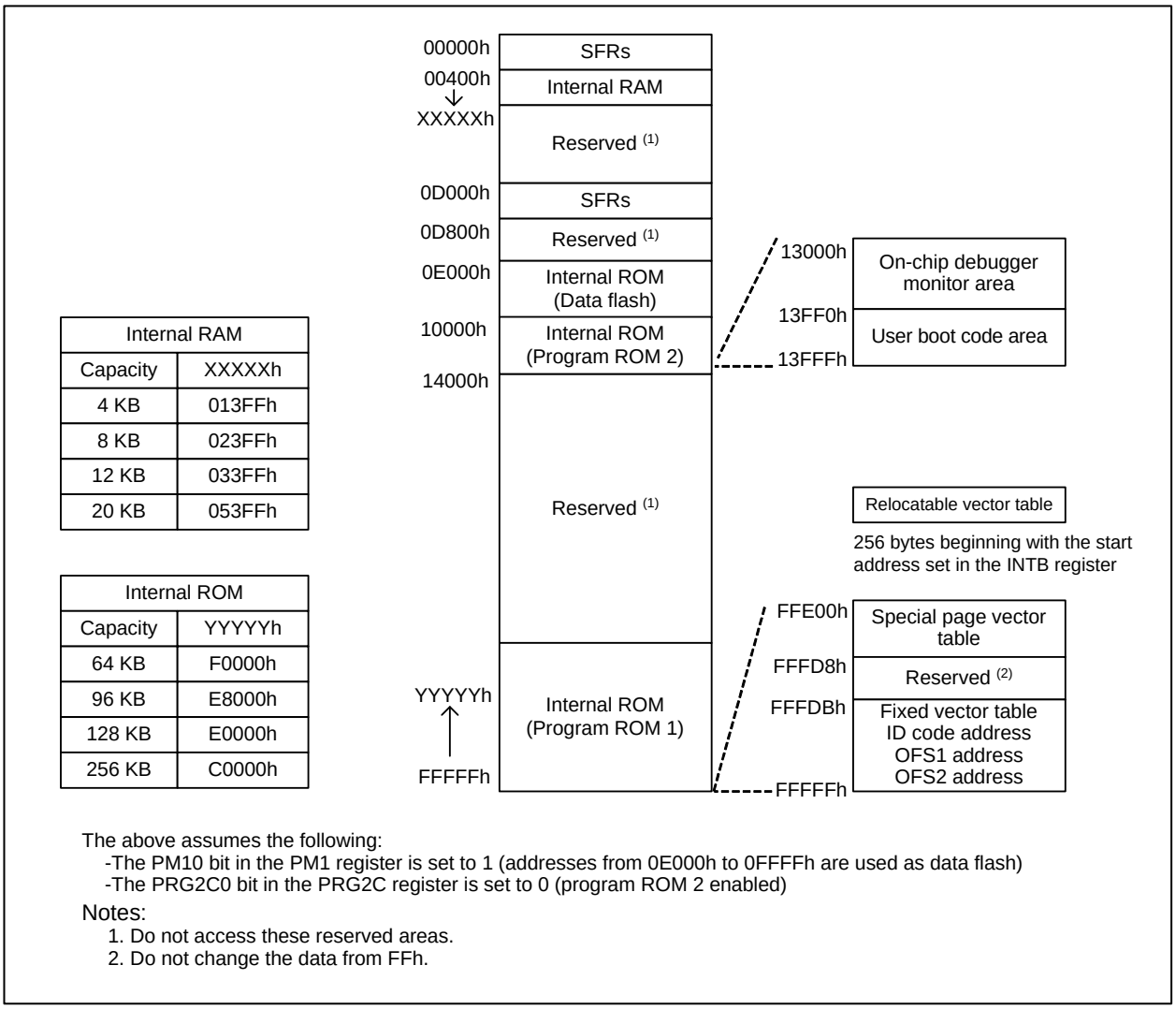
Program ROM 2 is assigned addresses 10000h to 13FFFh. Program ROM 1 is assigned addresses FFFFFh to inferior direction. For example, the 64 KB program ROM 1 space has addresses F0000h to FFFFFh.

The special page vectors are assigned addresses FFE00h to FFFD7h. They are used for the JMPS instruction and JSRS instruction. Refer to the M16C/60, M16C/20, M16C/Tiny Series Software Manual for details.

The fixed vector table for interrupts, ID code write address, OFS1 address and OSF2 address are assigned addresses FFFDBh to FFFFFh.

The 256 bytes beginning with the start address set in the INTB register compose the relocatable vector table for interrupts.

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Internal RAM	
Capacity	XXXXXh
4 KB	013FFh
8 KB	023FFh
12 KB	033FFh
20 KB	053FFh

Internal ROM	
Capacity	YYYYYh
64 KB	F0000h
96 KB	E8000h
128 KB	E0000h
256 KB	C0000h

The above assumes the following:
-The PM10 bit in the PM1 register is set to 1 (addresses from 0E000h to 0FFFFh are used as data flash)
-The PRG2C0 bit in the PRG2C register is set to 0 (program ROM 2 enabled)

Notes:
1. Do not access these reserved areas.
2. Do not change the data from FFh.

Figure 3.1 Memory Map

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4. Special Function Registers (SFRs)

4.1 SFRs

An SFR is a control register for a peripheral function.

Table 4.1 SFR Information (1) (1)

Address	Register	Symbol	Reset Value
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	0000 1000b
0006h	System Clock Control Register 0	CM0	0100 1000b
0007h	System Clock Control Register 1	CM1	0010 0000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	CM2	0X00 0010b (3)
000Dh			
000Eh			
000Fh			
0010h	Program 2 Area Control Register	PRG2C	XXXX XX00b
0011h			
0012h	Peripheral Clock Select Register	PCLKR	0000 0011b
0013h			
0014h			
0015h	Clock Prescaler Reset Flag	CPSRF	0XXX XXXXb
0016h			
0017h			
0018h	Reset Source Determine Register	RSTFR	XX0X 001Xb (hardware reset) (4)
0019h	Voltage Detector 2 Flag Register	VCR1	0000 1000b (2)
001Ah	Voltage Detector Operation Enable Register	VCR2	000X 0000b (2, 5) 001X 0000b (2, 6)
001Bh			
001Ch	PLL Control Register 0	PLC0	0X01 X010b
001Dh			
001Eh	Processor Mode Register 2	PM2	XX00 0X01b
001Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Software reset, watchdog timer reset, oscillator stop detect reset, and voltage monitor 2 reset do not affect the following registers: registers VCR1 and VCR2.
3. Oscillator stop detect reset does not affect bits CM20, CM21, and CM27.
4. The state of bits in the RSTFR register depends on the reset type.
5. This is the reset value when the LVDAS bit of the OFS1 address is 1 during hardware reset.
6. This is the reset value after voltage monitor 0 reset, power-on reset, or when the LVDAS bit of the OFS1 address is 0 during hardware reset.

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Table 4.2 SFR Information (2) (1)

Address	Register	Symbol	Reset Value
0020h			
0021h			
0022h			
0023h			
0024h			
0025h			
0026h	Voltage Monitor Function Select Register	VWCE	00h
0027h			
0028h	Voltage Detector 2 Level Select Register	VD2LS	0000 0100b(2)
0029h			
002Ah	Voltage Monitor 0 Control Register	VW0C	1100 1X10b(3, 4) 1100 1X11b(3, 5)
002Bh			
002Ch	Voltage Monitor 2 Control Register	VW2C	1000 0X10b(3, 6)
002Dh			
002Eh			
002Fh			
0030h			
0031h			
0032h			
0033h			
0034h			
0035h			
0036h			
0037h			
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. Hardware reset, power-on reset, voltage monitor 0 reset, or voltage monitor 2 reset.
3. Software reset, watchdog timer reset, oscillator stop detect reset, voltage monitor 0 reset, and voltage monitor 2 reset do not affect the following registers or bit: the VW0C register, and bits VW2C2 and VW2C3 in the VW2C register.
4. This is the reset value when the LVDAS bit of the OFS1 address is 1 during hardware reset
5. This is the reset value after voltage monitor 0 reset, power-on reset, or when the LVDAS bit of the OFS1 address is 0 during hardware reset.
6. This is the reset value after hardware reset, power-on reset, or voltage monitor 0 reset

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Table 4.3 SFR Information (3) (1)

Address	Register	Symbol	Reset Value
0040h			
0041h			
0042h			
0043h			
0044h	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XX00 X000b
0045h			
0046h			
0047h			
0048h	$\overline{\text{INT5}}$ Interrupt Control Register	INT5IC	XX00 X000b
0049h	$\overline{\text{INT4}}$ Interrupt Control Register	INT4IC	XX00 X000b
004Ah	UART2 Bus Collision Detection Interrupt Control Register Task Monitoring Timer Interrupt Control Register	BCNIC TMOSIC	XXXX X000b
004Bh	DMA0 Interrupt Control Register	DM0IC	XXXX X000b
004Ch	DMA1 Interrupt Control Register	DM1IC	XXXX X000b
004Dh	Key Input Interrupt Control Register A/D 1 Conversion Interrupt Control Register	KUPIC ADEIC	XXXX X000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXX X000b
004Fh	UART2 Transmit Interrupt Control Register	S2TIC	XXXX X000b
0050h	UART2 Receive Interrupt Control Register	S2RIC	XXXX X000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXX X000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXX X000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXX X000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXX X000b
0055h	Timer A0 Interrupt Control Register	TA0IC	XXXX X000b
0056h	Timer A1 Interrupt Control Register	TA1IC	XXXX X000b
0057h	Timer A2 Interrupt Control Register	TA2IC	XXXX X000b
0058h	Timer A3 Interrupt Control Register	TA3IC	XXXX X000b
0059h	Timer A4 Interrupt Control Register	TA4IC	XXXX X000b
005Ah	Timer B0 Interrupt Control Register	TB0IC	XXXX X000b
005Bh	Timer B1 Interrupt Control Register	TB1IC	XXXX X000b
005Ch	Timer B2 Interrupt Control Register	TB2IC	XXXX X000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00 X000b
005Eh	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XX00 X000b
005Fh	$\overline{\text{INT2}}$ Interrupt Control Register	INT2IC	XX00 X000b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.4 SFR Information (4) (1)

Address	Register	Symbol	Reset Value
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h	DMA2 Interrupt Control Register	DM2IC	XXXX X000b
006Ah	DMA3 Interrupt Control Register	DM3IC	XXXX X000b
006Bh			
006Ch			
006Dh			
006Eh			
006Fh	UART4 Transmit Interrupt Control Register Real-Time Clock Compare Interrupt Control Register	S4TIC RTCCIC	XXXX X000b
0070h	UART4 Receive Interrupt Control Register	S4RIC	XXXX X000b
0071h	CAN0 Wake-up Interrupt Control Register	C0WIC	XXXX X000b
0072h	UART3 Transmit Interrupt Control Register CAN0 Error Interrupt Control Register	S3TIC C0EIC	XXXX X000b
0073h	UART3 Receive Interrupt Control Register	S3RIC	XXXX X000b
0074h	Real-Time Clock Cycle Interrupt Control Register	RTCTIC	XXXX X000b
0075h	CAN0 Reception Complete Interrupt Control Register	C0RIC	XXXX X000b
0076h	CAN0 Transmission Complete Interrupt Control Register	C0TIC	XXXX X000b
0077h	CAN0 Receive FIFO Interrupt Control Register	C0FRIC	XXXX X000b
0078h	CAN0 Transmit FIFO Interrupt Control Register	C0FTIC	XXXX X000b
0079h	IC/OC Interrupt 0 Control Register	ICOC0IC	XXXX X000b
007Ah	IC/OC Channel 0 Interrupt Control Register	ICOCH0IC	XXXX X000b
007Bh	IC/OC Interrupt 1 Control Register I2C-bus Interface Interrupt Control Register	ICOC1IC IICIC	XXXX X000b
007Ch	IC/OC Channel 1 Interrupt Control Register SCL/SDA Interrupt Control Register	ICOCH1IC SCLDAIC	XXXX X000b
007Dh	IC/OC Channel 2 Interrupt Control Register	ICOCH2IC	XXXX X000b
007Eh	IC/OC Channel 3 Interrupt Control Register	ICOCH3IC	XXXX X000b
007Fh	IC/OC Base Timer Interrupt Control Register	BTIC	XXXX X000b
0080h to 012Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.5 SFR Information (5) (1)

Address	Register	Symbol	Reset Value
0130h			
0131h			
0132h			
0133h			
0134h			
0135h			
0136h			
0137h			
0138h			
0139h			
013Ah			
013Bh			
013Ch			
013Dh			
013Eh			
013Fh			
0140h	A/D1 Register 0	AD10	XXXX XXXXb
0141h			0000 00XXb
0142h	A/D1 Register 1	AD11	XXXX XXXXb
0143h			0000 00XXb
0144h	A/D1 Register 2	AD12	XXXX XXXXb
0145h			0000 00XXb
0146h	A/D1 Register 3	AD13	XXXX XXXXb
0147h			0000 00XXb
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h	A/D1 Trigger Control Register	AD1TRGCON	XXXX 00XXb
0153h			
0154h	A/D1 Control Register 2	AD1CON2	0000 X00Xb
0155h			
0156h	A/D1 Control Register 0	AD1CON0	0000 0XXXb
0157h	A/D1 Control Register 1	AD1CON1	0000 X000b
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h to 017Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.6 SFR Information (6) (1)

Address	Register	Symbol	Reset Value
0180h	DMA0 Source Pointer	SAR0	XXh
0181h			XXh
0182h			0Xh
0183h			
0184h	DMA0 Destination Pointer	DAR0	XXh
0185h			XXh
0186h			0Xh
0187h			
0188h	DMA0 Transfer Counter	TCR0	XXh
0189h			XXh
018Ah			
018Bh			
018Ch	DMA0 Control Register	DM0CON	0000 0X00b
018Dh			
018Eh			
018Fh			
0190h	DMA1 Source Pointer	SAR1	XXh
0191h			XXh
0192h			0Xh
0193h			
0194h	DMA1 Destination Pointer	DAR1	XXh
0195h			XXh
0196h			0Xh
0197h			
0198h	DMA1 Transfer Counter	TCR1	XXh
0199h			XXh
019Ah			
019Bh			
019Ch	DMA1 Control Register	DM1CON	0000 0X00b
019Dh			
019Eh			
019Fh			
01A0h	DMA2 Source Pointer	SAR2	XXh
01A1h			XXh
01A2h			0Xh
01A3h			
01A4h	DMA2 Destination Pointer	DAR2	XXh
01A5h			XXh
01A6h			0Xh
01A7h			
01A8h	DMA2 Transfer Counter	TCR2	XXh
01A9h			XXh
01AAh			
01ABh			
01ACh	DMA2 Control Register	DM2CON	0000 0X00b
01ADh			
01AEh			
01AFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	Reset Value
01B0h	DMA3 Source Pointer	SAR3	XXh
01B1h			XXh
01B2h			0Xh
01B3h			
01B4h	DMA3 Destination Pointer	DAR3	XXh
01B5h			XXh
01B6h			0Xh
01B7h			
01B8h	DMA3 Transfer Counter	TCR3	XXh
01B9h			XXh
01BAh			
01BBh			
01BCh	DMA3 Control Register	DM3CON	0000 0X00b
01BDh			
01BEh			
01BFh			
01C0h	Timer B0-1 Register	TB01	XXh
01C1h			XXh
01C2h	Timer B1-1 Register	TB11	XXh
01C3h			XXh
01C4h	Timer B2-1 Register	TB21	XXh
01C5h			XXh
01C6h	Pulse Period/Pulse Width Measurement Mode Function Select Register 1	PPWFS1	XXXX X000b
01C7h			
01C8h	Timer B Count Source Select Register 0	TBCS0	00h
01C9h	Timer B Count Source Select Register 1	TBCS1	X0h
01CAh			
01CBh			
01CCh			
01CDh			
01CEh			
01CFh			
01D0h	Timer A Count Source Select Register 0	TACS0	00h
01D1h	Timer A Count Source Select Register 1	TACS1	00h
01D2h	Timer A Count Source Select Register 2	TACS2	X0h
01D3h			
01D4h	16-bit Pulse Width Modulation Mode Function Select Register	PWMFS	0XX0 X00Xb
01D5h	Timer A Waveform Output Function Select Register	TAPOFS	XXX0 0000b
01D6h			
01D7h			
01D8h	Timer A Output Waveform Change Enable Register	TAOW	XXX0 X00Xb
01D9h			
01DAh	Three-Phase Protect Control Register	TPRC	00h
01DBh			
01DCh			
01DDh			
01DEh			
01DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.8 SFR Information (8) (1)

Address	Register	Symbol	Reset Value
01E0h			
01E1h			
01E2h			
01E3h			
01E4h			
01E5h			
01E6h			
01E7h			
01E8h			
01E9h			
01EAh			
01EBh			
01ECh			
01EDh			
01EEh			
01EFh			
01F0h	Task Monitor Timer Register	TMOS	XXh
01F1h			XXh
01F2h	Task Monitor Timer Count Start Flag	TMOSSR	XXXX XXX0b
01F3h	Task Monitor Timer Count Source Select Register	TMOSCS	XXXX 0000b
01F4h	Task Monitor Timer Protect Register	TMOSPR	00h
01F5h			
01F6h			
01F7h			
01F8h			
01F9h			
01FAh			
01FBh			
01FCh			
01FDh			
01FEh			
01FFh			
0200h			
0201h			
0202h			
0203h			
0204h			
0205h	Interrupt Source Select Register 3	IFSR3A	00h
0206h	Interrupt Source Select Register 2	IFSR2A	00h
0207h	Interrupt Source Select Register	IFSR	00h
0208h			
0209h			
020Ah			
020Bh			
020Ch			
020Dh			
020Eh	Address Match Interrupt Enable Register	AIER	XXXX XX00b
020Fh	Address Match Interrupt Enable Register 2	AIER2	XXXX XX00b

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.9 SFR Information (9) (1)

Address	Register	Symbol	Reset Value
0210h	Address Match Interrupt Register 0	RMAD0	00h
0211h			00h
0212h			X0h
0213h			
0214h	Address Match Interrupt Register 1	RMAD1	00h
0215h			00h
0216h			X0h
0217h			
0218h	Address Match Interrupt Register 2	RMAD2	00h
0219h			00h
021Ah			X0h
021Bh			
021Ch	Address Match Interrupt Register 3	RMAD3	00h
021Dh			00h
021Eh			X0h
021Fh			
0220h	Flash Memory Control Register 0	FMR0	0000 0001b (Other than user boot mode) 0010 0001b (User boot mode)
0221h	Flash Memory Control Register 1	FMR1	00X0 XX0Xb
0222h	Flash Memory Control Register 2	FMR2	XXXX 0000b
0223h	Flash Memory Control Register 3	FMR3	XXXX 0000b
0224h			
0225h			
0226h			
0227h			
0228h			
0229h			
022Ah			
022Bh			
022Ch			
022Dh			
022Eh			
022Fh			
0230h	Flash Memory Control Register 6	FMR6	XX0X XX00b
0231h			
0232h			
0233h			
0234h			
0235h			
0236h			
0237h			
0238h			
0239h			
023Ah			
023Bh			
023Ch			
023Dh			
023Eh			
023Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.10 SFR Information (10) (1)

Address	Register	Symbol	Reset Value
0240h			
0241h			
0242h			
0243h			
0244h			
0245h			
0246h			
0247h			
0248h	UART0 Transmit/Receive Mode Register	U0MR	00h
0249h	UART0 Bit Rate Register	U0BRG	XXh
024Ah	UART0 Transmit Buffer Register	U0TB	XXh
024Bh			XXh
024Ch	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000b
024Dh	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010b
024Eh	UART0 Receive Buffer Register	U0RB	XXh
024Fh			XXh
0250h			
0251h			
0252h			
0253h			
0254h			
0255h			
0256h			
0257h			
0258h	UART1 Transmit/Receive Mode Register	U1MR	00h
0259h	UART1 Bit Rate Register	U1BRG	XXh
025Ah	UART1 Transmit Buffer Register	U1TB	XXh
025Bh			XXh
025Ch	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000b
025Dh	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010b
025Eh	UART1 Receive Buffer Register	U1RB	XXh
025Fh			XXh
0260h			
0261h			
0262h			
0263h			
0264h	UART2 Special Mode Register 4	U2SMR4	00h
0265h	UART2 Special Mode Register 3	U2SMR3	000X 0X0Xb
0266h	UART2 Special Mode Register 2	U2SMR2	X000 0000b
0267h	UART2 Special Mode Register	U2SMR	X000 0000b
0268h	UART2 Transmit/Receive Mode Register	U2MR	00h
0269h	UART2 Bit Rate Register	U2BRG	XXh
026Ah	UART2 Transmit Buffer Register	U2TB	XXh
026Bh			XXh
026Ch	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000b
026Dh	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010b
026Eh	UART2 Receive Buffer Register	U2RB	XXh
026Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	Reset Value
0270h			
0271h			
0272h			
0273h			
0274h			
0275h			
0276h			
0277h			
0278h			
0279h			
027Ah			
027Bh			
027Ch			
027Dh			
027Eh			
027Fh			
0280h			
0281h			
0282h			
0283h			
0284h			
0285h			
0286h			
0287h			
0288h			
0289h			
028Ah			
028Bh			
028Ch			
028Dh			
028Eh			
028Fh			
0290h			
0291h			
0292h			
0293h			
0294h			
0295h			
0296h			
0297h			
0298h	UART4 Transmit/Receive Mode Register	U4MR	00h
0299h	UART4 Bit Rate Register	U4BRG	XXh
029Ah	UART4 Transmit Buffer Register	U4TB	XXh
029Bh			XXh
029Ch	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000b
029Dh	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010b
029Eh	UART4 Receive Buffer Register	U4RB	XXh
029Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	Reset Value
02A0h			
02A1h			
02A2h			
02A3h			
02A4h			
02A5h			
02A6h			
02A7h			
02A8h	UART3 Transmit/Receive Mode Register	U3MR	00h
02A9h	UART3 Bit Rate Register	U3BRG	XXh
02AAh	UART3 Transmit Buffer Register	U3TB	XXh
02ABh			XXh
02ACh	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000b
02ADh	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010b
02AEh	UART3 Receive Buffer Register	U3RB	XXh
02AFh			XXh
02B0h	I2C0 Data Shift Register	S00	XXh
02B1h			
02B2h	I2C0 Address Register 0	S0D0	0000 000Xb
02B3h	I2C0 Control Register 0	S1D0	00h
02B4h	I2C0 Clock Control Register	S20	00h
02B5h	I2C0 Start/Stop Condition Control Register	S2D0	0001 1010b
02B6h	I2C0 Control Register 1	S3D0	0011 0000b
02B7h	I2C0 Control Register 2	S4D0	00h
02B8h	I2C0 Status Register 0	S10	0001 000Xb
02B9h	I2C0 Status Register 1	S11	XXXX X000b
02BAh	I2C0 Address Register 1	S0D1	0000 000Xb
02BBh	I2C0 Address Register 2	S0D2	0000 000Xb
02BCh			
02BDh			
02BEh			
02BFh			
02C0h	Time Measurement Register 0	G1TM0	XXh
02C1h	Waveform Generation Register 0	G1PO0	XXh
02C2h	Time Measurement Register 1	G1TM1	XXh
02C3h	Waveform Generation Register 1	G1PO1	XXh
02C4h	Time Measurement Register 2	G1TM2	XXh
02C5h	Waveform Generation Register 2	G1PO2	XXh
02C6h	Time Measurement Register 3	G1TM3	XXh
02C7h	Waveform Generation Register 3	G1PO3	XXh
02C8h	Time Measurement Register 4	G1TM4	XXh
02C9h	Waveform Generation Register 4	G1PO4	XXh
02CAh	Time Measurement Register 5	G1TM5	XXh
02CBh	Waveform Generation Register 5	G1PO5	XXh
02CCh	Time Measurement Register 6	G1TM6	XXh
02CDh	Waveform Generation Register 6	G1PO6	XXh
02CEh	Time Measurement Register 7	G1TM7	XXh
02CFh	Waveform Generation Register 7	G1PO7	XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.13 SFR Information (13) (1)

Address	Register	Symbol	Reset Value
02D0h	Waveform Generation Control Register 0	G1POCR0	0X00 XX00b
02D1h	Waveform Generation Control Register 1	G1POCR1	0X00 XX00b
02D2h	Waveform Generation Control Register 2	G1POCR2	0X00 XX00b
02D3h	Waveform Generation Control Register 3	G1POCR3	0X00 XX00b
02D4h	Waveform Generation Control Register 4	G1POCR4	0X00 XX00b
02D5h	Waveform Generation Control Register 5	G1POCR5	0X00 XX00b
02D6h	Waveform Generation Control Register 6	G1POCR6	0X00 XX00b
02D7h	Waveform Generation Control Register 7	G1POCR7	0X00 XX00b
02D8h	Time Measurement Control Register 0	G1TMCR0	00h
02D9h	Time Measurement Control Register 1	G1TMCR1	00h
02DAh	Time Measurement Control Register 2	G1TMCR2	00h
02DBh	Time Measurement Control Register 3	G1TMCR3	00h
02DCh	Time Measurement Control Register 4	G1TMCR4	00h
02DDh	Time Measurement Control Register 5	G1TMCR5	00h
02DEh	Time Measurement Control Register 6	G1TMCR6	00h
02DFh	Time Measurement Control Register 7	G1TMCR7	00h
02E0h	Base Timer Register	G1BT	XXh
02E1h			XXh
02E2h	Base Timer Control Register 0	G1BCR0	00h
02E3h	Base Timer Control Register 1	G1BCR1	00h
02E4h	Time Measurement Prescaler Register 6	G1TPR6	00h
02E5h	Time Measurement Prescaler Register 7	G1TPR7	00h
02E6h	Function Enable Register	G1FE	00h
02E7h	Function Select Register	G1FS	00h
02E8h	Base Timer Reset Register	G1BTRR	XXh
02E9h			XXh
02EAh	Count Source Divide Register	G1DV	00h
02EBh			
02ECh	Waveform Output Master Enable Register	G1OER	00h
02EDh			
02EEh	Timer S I/O Control Register 0	G1IOR0	00h
02EFh	Timer S I/O Control Register 1	G1IOR1	00h
02F0h	Interrupt Request Register	G1IR	XXh
02F1h	Interrupt Enable Register 0	G1IE0	00h
02F2h	Interrupt Enable Register 1	G1IE1	00h
02F3h			
02F4h			
02F5h			
02F6h			
02F7h			
02F8h			
02F9h			
02FAh			
02FBh			
02FCh			
02FDh			
02FEh	$\overline{\text{NMI}}$ Digital Debounce Register	NDDR	FFh
02FFh	P1_7 Digital Debounce Register	P17DDR	FFh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.14 SFR Information (14) (1)

Address	Register	Symbol	Reset Value
0300h			
0301h			
0302h	Timer A1-1 Register	TA11	XXh
0303h			XXh
0304h	Timer A2-1 Register	TA21	XXh
0305h			XXh
0306h	Timer A4-1 Register	TA41	XXh
0307h			XXh
0308h	Three-Phase PWM Control Register 0	INVC0	00h
0309h	Three-Phase PWM Control Register 1	INVC1	00h
030Ah	Three-Phase Output Buffer Register 0	IDB0	XX11 1111b
030Bh	Three-Phase Output Buffer Register 1	IDB1	XX11 1111b
030Ch	Dead Time Timer	DTT	XXh
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XXh
030Eh	Position-Data-Retain Function Control Register	PDRF	XXXX 0000b
030Fh			
0310h			
0311h			
0312h			
0313h			
0314h			
0315h			
0316h			
0317h			
0318h	Port Function Control Register	PFCR	0011 1111b
0319h			
031Ah			
031Bh			
031Ch			
031Dh			
031Eh			
031Fh			
0320h	Count Start Flag	TABSR	00h
0321h			
0322h	One-Shot Start Flag	ONSF	00h
0323h	Trigger Select Register	TRGSR	00h
0324h	Increment/Decrement Flag	UDF	00h
0325h			
0326h	Timer A0 Register	TA0	XXh
0327h			XXh
0328h	Timer A1 Register	TA1	XXh
0329h			XXh
032Ah	Timer A2 Register	TA2	XXh
032Bh			XXh
032Ch	Timer A3 Register	TA3	XXh
032Dh			XXh
032Eh	Timer A4 Register	TA4	XXh
032Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.15 SFR Information (15) (1)

Address	Register	Symbol	Reset Value
0330h	Timer B0 Register	TB0	XXh
0331h			XXh
0332h	Timer B1 Register	TB1	XXh
0333h			XXh
0334h	Timer B2 Register	TB2	XXh
0335h			XXh
0336h	Timer A0 Mode Register	TA0MR	00h
0337h	Timer A1 Mode Register	TA1MR	00h
0338h	Timer A2 Mode Register	TA2MR	00h
0339h	Timer A3 Mode Register	TA3MR	00h
033Ah	Timer A4 Mode Register	TA4MR	00h
033Bh	Timer B0 Mode Register	TB0MR	00XX 0000b
033Ch	Timer B1 Mode Register	TB1MR	00XX 0000b
033Dh	Timer B2 Mode Register	TB2MR	00XX 0000b
033Eh	Timer B2 Special Mode Register	TB2SC	X000 0000b
033Fh			
0340h	Real-Time Clock Second Data Register	RTCSEC	00h
0341h	Real-Time Clock Minute Data Register	RTCMIN	X000 0000b
0342h	Real-Time Clock Hour Data Register	RTCHR	XX00 0000b
0343h	Real-Time Clock Day Data Register	RTCWK	XXXX X000b
0344h	Real-Time Clock Control Register 1	RTCCR1	0000 X00Xb
0345h	Real-Time Clock Control Register 2	RTCCR2	X000 0000b
0346h	Real-Time Clock Count Source Select Register	RTCCSR	XXX0 0000b
0347h			
0348h	Real-Time Clock Second Compare Data Register	RTCCSEC	X000 0000b
0349h	Real-Time Clock Minute Compare Data Register	RTCCMIN	X000 0000b
034Ah	Real-Time Clock Hour Compare Data Register	RTCCHR	X000 0000b
034Bh			
034Ch			
034Dh			
034Eh			
034Fh			
0350h			
0351h			
0352h			
0353h			
0354h			
0355h			
0356h			
0357h			
0358h			
0359h			
035Ah			
035Bh			
035Ch			
035Dh			
035Eh			
035Fh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.16 SFR Information (16) (1)

Address	Register	Symbol	Reset Value
0360h	Pull-Up Control Register 0	PUR0	00h
0361h	Pull-Up Control Register 1	PUR1	00h
0362h	Pull-Up Control Register 2	PUR2	00h
0363h			
0364h			
0365h			
0366h	Port Control Register	PCR	0XX0 0XX0b
0367h			
0368h			
0369h			
036Ah			
036Bh			
036Ch			
036Dh			
036Eh			
036Fh			
0370h	Pin Assignment Control Register	PACR	0XXX X000b
0371h			
0372h			
0373h			
0374h			
0375h			
0376h			
0377h			
0378h			
0379h			
037Ah			
037Bh			
037Ch	Count Source Protection Mode Register	CSPR	00h (2)
037Dh	Watchdog Timer Refresh Register	WDTR	XXh
037Eh	Watchdog Timer Start Register	WDTS	XXh
037Fh	Watchdog Timer Control Register	WDC	00XX XXXXb
0380h			
0381h			
0382h			
0383h			
0384h			
0385h			
0386h			
0387h			
0388h			
0389h			
038Ah			
038Bh			
038Ch			
038Dh			
038Eh			
038Fh			

X: Undefined

Notes:
1. The blank areas are reserved. No access is allowed.
2. When the CSPROINI bit in the OFS1 address is 0, the reset value is 1000 0000b.

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Table 4.17 SFR Information (17) (1)

Address	Register	Symbol	Reset Value
0390h	DMA2 Source Select Register	DM2SL	00h
0391h			
0392h	DMA3 Source Select Register	DM3SL	00h
0393h			
0394h			
0395h			
0396h			
0397h			
0398h	DMA0 Source Select Register	DM0SL	00h
0399h			
039Ah	DMA1 Source Select Register	DM1SL	00h
039Bh			
039Ch			
039Dh			
039Eh			
039Fh			
03A0h			
03A1h			
03A2h			
03A3h			
03A4h			
03A5h			
03A6h			
03A7h			
03A8h			
03A9h			
03AAh			
03ABh			
03ACh			
03ADh			
03AEh			
03AFh			
03B0h			
03B1h			
03B2h			
03B3h			
03B4h	SFR Snoop Address Register	CRCSAR	XXXX XXXXb
03B5h			00XX XXXXb
03B6h	CRC Mode Register	CRCMR	0XXX XXX0b
03B7h			
03B8h			
03B9h			
03BAh			
03BBh			
03BCh	CRC Data Register	CRCD	XXh
03BDh			XXh
03BEh	CRC Input Register	CRCIN	XXh
03BFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.18 SFR Information (18) (1)

Address	Register	Symbol	Reset Value
03C0h	A/D Register 0	AD0	XXXX XXXXb
03C1h			0000 00XXb
03C2h	A/D Register 1	AD1	XXXX XXXXb
03C3h			0000 00XXb
03C4h	A/D Register 2	AD2	XXXX XXXXb
03C5h			0000 00XXb
03C6h	A/D Register 3	AD3	XXXX XXXXb
03C7h			0000 00XXb
03C8h	A/D Register 4	AD4	XXXX XXXXb
03C9h			0000 00XXb
03CAh	A/D Register 5	AD5	XXXX XXXXb
03CBh			0000 00XXb
03CCh	A/D Register 6	AD6	XXXX XXXXb
03CDh			0000 00XXb
03CEh	A/D Register 7	AD7	XXXX XXXXb
03CFh			0000 00XXb
03D0h			
03D1h			
03D2h	A/D Trigger Control Register	ADTRGCON	XXXX 00XXb
03D3h			
03D4h	A/D Control Register 2	ADCON2	0000 X00Xb
03D5h			
03D6h	A/D Control Register 0	ADCON0	0000 0XXXb
03D7h	A/D Control Register 1	ADCON1	0000 X000b
03D8h			
03D9h			
03DAh			
03DBh			
03DCh			
03DDh			
03DEh			
03DFh			
03E0h	Port P0 Register	P0	XXh
03E1h	Port P1 Register	P1	XXh
03E2h	Port P0 Direction Register	PD0	00h
03E3h	Port P1 Direction Register	PD1	00h
03E4h	Port P2 Register	P2	XXh
03E5h	Port P3 Register	P3	XXh
03E6h	Port P2 Direction Register	PD2	00h
03E7h	Port P3 Direction Register	PD3	00h
03E8h			
03E9h			
03EAh			
03EBh			
03ECh	Port P6 Register	P6	XXh
03EDh	Port P7 Register	P7	XXh
03EEh	Port P6 Direction Register	PD6	00h
03EFh	Port P7 Direction Register	PD7	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.19 SFR Information (19) (1)

Address	Register	Symbol	Reset Value
03F0h	Port P8 Register	P8	XXh
03F1h	Port P9 Register	P9	XXh
03F2h	Port P8 Direction Register	PD8	00h
03F3h	Port P9 Direction Register	PD9	000X 0000b
03F4h	Port P10 Register	P10	XXh
03F5h			
03F6h	Port P10 Direction Register	PD10	00h
03F7h			
03F8h			
03F9h			
03FAh			
03FBh			
03FCh			
03FDh			
03FEh			
03FFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.20 SFR Information (20) (1)

Address	Register	Symbol	Reset Value
D500h	CAN0 Mailbox 0: Message Identifier	C0MB0	XXh
D501h			XXh
D502h			XXh
D503h			XXh
D504h			
D505h	CAN0 Mailbox 0: Data Length		XXh
D506h	CAN0 Mailbox 0: Data Field		XXh
D507h			XXh
D508h			XXh
D509h			XXh
D50Ah			XXh
D50Bh			XXh
D50Ch			XXh
D50Dh			XXh
D50Eh	CAN0 Mailbox 0: Time Stamp		XXh
D50Fh			XXh
D510h	CAN0 Mailbox 1: Message Identifier	C0MB1	XXh
D511h			XXh
D512h			XXh
D513h			XXh
D514h			
D515h	CAN0 Mailbox 1: Data Length		XXh
D516h	CAN0 Mailbox 1: Data Field		XXh
D517h			XXh
D518h			XXh
D519h			XXh
D51Ah			XXh
D51Bh			XXh
D51Ch			XXh
D51Dh			XXh
D51Eh	CAN0 Mailbox 1: Time Stamp		XXh
D51Fh			XXh
D520h	CAN0 Mailbox 2: Message Identifier	C0MB2	XXh
D521h			XXh
D522h			XXh
D523h			XXh
D524h			
D525h	CAN0 Mailbox 2: Data Length		XXh
D526h	CAN0 Mailbox 2: Data Field		XXh
D527h			XXh
D528h			XXh
D529h			XXh
D52Ah			XXh
D52Bh			XXh
D52Ch			XXh
D52Dh			XXh
D52Eh	CAN0 Mailbox 2: Time Stamp		XXh
D52Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.21 SFR Information (21) (1)

Address	Register	Symbol	Reset Value
D530h	CAN0 Mailbox 3: Message Identifier	C0MB3	XXh
D531h			XXh
D532h			XXh
D533h			XXh
D534h			
D535h	CAN0 Mailbox 3: Data Length		XXh
D536h	CAN0 Mailbox 3: Data Field		XXh
D537h			XXh
D538h			XXh
D539h			XXh
D53Ah			XXh
D53Bh			XXh
D53Ch			XXh
D53Dh			XXh
D53Eh	CAN0 Mailbox 3: Time Stamp		XXh
D53Fh			XXh
D540h	CAN0 Mailbox 4: Message Identifier	C0MB4	XXh
D541h			XXh
D542h			XXh
D543h			XXh
D544h			
D545h	CAN0 Mailbox 4: Data Length		XXh
D546h	CAN0 Mailbox 4: Data Field		XXh
D547h			XXh
D548h			XXh
D549h			XXh
D54Ah			XXh
D54Bh			XXh
D54Ch			XXh
D54Dh			XXh
D54Eh	CAN0 Mailbox 4: Time Stamp		XXh
D54Fh			XXh
D550h	CAN0 Mailbox 5: Message Identifier	C0MB5	XXh
D551h			XXh
D552h			XXh
D553h			XXh
D554h			
D555h	CAN0 Mailbox 5: Data Length		XXh
D556h	CAN0 Mailbox 5: Data Field		XXh
D557h			XXh
D558h			XXh
D559h			XXh
D55Ah			XXh
D55Bh			XXh
D55Ch			XXh
D55Dh			XXh
D55Eh	CAN0 Mailbox 5: Time Stamp		XXh
D55Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.22 SFR Information (22) (1)

Address	Register	Symbol	Reset Value
D560h	CAN0 Mailbox 6: Message Identifier	C0MB6	XXh
D561h			XXh
D562h			XXh
D563h			XXh
D564h			
D565h	CAN0 Mailbox 6: Data Length		XXh
D566h	CAN0 Mailbox 6: Data Field		XXh
D567h			XXh
D568h			XXh
D569h			XXh
D56Ah			XXh
D56Bh			XXh
D56Ch			XXh
D56Dh			XXh
D56Eh	CAN0 Mailbox 6: Time Stamp		XXh
D56Fh			XXh
D570h	CAN0 Mailbox 7: Message Identifier	C0MB7	XXh
D571h			XXh
D572h			XXh
D573h			XXh
D574h			
D575h	CAN0 Mailbox 7: Data Length		XXh
D576h	CAN0 Mailbox 7: Data Field		XXh
D577h			XXh
D578h			XXh
D579h			XXh
D57Ah			XXh
D57Bh			XXh
D57Ch			XXh
D57Dh			XXh
D57Eh	CAN0 Mailbox 7: Time Stamp		XXh
D57Fh			XXh
D580h	CAN0 Mailbox 8: Message Identifier	C0MB8	XXh
D581h			XXh
D582h			XXh
D583h			XXh
D584h			
D585h	CAN0 Mailbox 8: Data Length		XXh
D586h	CAN0 Mailbox 8: Data Field		XXh
D587h			XXh
D588h			XXh
D589h			XXh
D58Ah			XXh
D58Bh			XXh
D58Ch			XXh
D58Dh			XXh
D58Eh	CAN0 Mailbox 8: Time Stamp		XXh
D58Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.23 SFR Information (23) (1)

Address	Register	Symbol	Reset Value
D590h	CAN0 Mailbox 9: Message Identifier	C0MB9	XXh
D591h			XXh
D592h			XXh
D593h			XXh
D594h			
D595h	CAN0 Mailbox 9: Data Length		XXh
D596h	CAN0 Mailbox 9: Data Field		XXh
D597h			XXh
D598h			XXh
D599h			XXh
D59Ah			XXh
D59Bh			XXh
D59Ch			XXh
D59Dh			XXh
D59Eh	CAN0 Mailbox 9: Time Stamp		XXh
D59Fh			XXh
D5A0h	CAN0 Mailbox 10: Message Identifier	C0MB10	XXh
D5A1h			XXh
D5A2h			XXh
D5A3h			XXh
D5A4h			
D5A5h	CAN0 Mailbox 10: Data Length		XXh
D5A6h	CAN0 Mailbox 10: Data Field		XXh
D5A7h			XXh
D5A8h			XXh
D5A9h			XXh
D5AAh			XXh
D5ABh			XXh
D5ACh			XXh
D5ADh			XXh
D5AEh	CAN0 Mailbox 10: Time Stamp		XXh
D5AFh			XXh
D5B0h	CAN0 Mailbox 11: Message Identifier	C0MB11	XXh
D5B1h			XXh
D5B2h			XXh
D5B3h			XXh
D5B4h			
D5B5h	CAN0 Mailbox 11: Data Length		XXh
D5B6h	CAN0 Mailbox 11: Data Field		XXh
D5B7h			XXh
D5B8h			XXh
D5B9h			XXh
D5BAh			XXh
D5BBh			XXh
D5BCh			XXh
D5BDh			XXh
D5BEh	CAN0 Mailbox 11: Time Stamp		XXh
D5BFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.24 SFR Information (24) (1)

Address	Register	Symbol	Reset Value
D5C0h	CAN0 Mailbox 12: Message Identifier	C0MB12	XXh
D5C1h			XXh
D5C2h			XXh
D5C3h			XXh
D5C4h			
D5C5h	CAN0 Mailbox 12: Data Length		XXh
D5C6h	CAN0 Mailbox 12: Data Field		XXh
D5C7h			XXh
D5C8h			XXh
D5C9h			XXh
D5CAh			XXh
D5CBh			XXh
D5CCh			XXh
D5CDh			XXh
D5CEh	CAN0 Mailbox 12: Time Stamp		XXh
D5CFh			XXh
D5D0h	CAN0 Mailbox 13: Message Identifier	C0MB13	XXh
D5D1h			XXh
D5D2h			XXh
D5D3h			XXh
D5D4h			
D5D5h	CAN0 Mailbox 13: Data Length		XXh
D5D6h	CAN0 Mailbox 13: Data Field		XXh
D5D7h			XXh
D5D8h			XXh
D5D9h			XXh
D5DAh			XXh
D5DBh			XXh
D5DCh			XXh
D5DDh			XXh
D5DEh	CAN0 Mailbox 13: Time Stamp		XXh
D5DFh			XXh
D5E0h	CAN0 Mailbox 14: Message Identifier	C0MB14	XXh
D5E1h			XXh
D5E2h			XXh
D5E3h			XXh
D5E4h			
D5E5h	CAN0 Mailbox 14: Data Length		XXh
D5E6h	CAN0 Mailbox 14: Data Field		XXh
D5E7h			XXh
D5E8h			XXh
D5E9h			XXh
D5EAh			XXh
D5EBh			XXh
D5ECh			XXh
D5EDh			XXh
D5EEh	CAN0 Mailbox 14: Time Stamp		XXh
D5EFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.25 SFR Information (25) (1)

Address	Register	Symbol	Reset Value
D5F0h	CAN0 Mailbox 15: Message Identifier	C0MB15	XXh
D5F1h			XXh
D5F2h			XXh
D5F3h			XXh
D5F4h			
D5F5h	CAN0 Mailbox 15: Data Length		XXh
D5F6h	CAN0 Mailbox 15: Data Field		XXh
D5F7h			XXh
D5F8h			XXh
D5F9h			XXh
D5FAh			XXh
D5FBh			XXh
D5FCh			XXh
D5FDh			XXh
D5FEh	CAN0 Mailbox 15: Time Stamp		XXh
D5FFh			XXh
D600h	CAN0 Mailbox 16: Message Identifier	C0MB16	XXh
D601h			XXh
D602h			XXh
D603h			XXh
D604h			
D605h	CAN0 Mailbox 16: Data Length		XXh
D606h	CAN0 Mailbox 16: Data Field		XXh
D607h			XXh
D608h			XXh
D609h			XXh
D60Ah			XXh
D60Bh			XXh
D60Ch			XXh
D60Dh			XXh
D60Eh	CAN0 Mailbox 16: Time Stamp		XXh
D60Fh			XXh
D610h	CAN0 Mailbox 17: Message Identifier	C0MB17	XXh
D611h			XXh
D612h			XXh
D613h			XXh
D614h			
D615h	CAN0 Mailbox 17: Data Length		XXh
D616h	CAN0 Mailbox 17: Data Field		XXh
D617h			XXh
D618h			XXh
D619h			XXh
D61Ah			XXh
D61Bh			XXh
D61Ch			XXh
D61Dh			XXh
D61Eh	CAN0 Mailbox 17: Time Stamp		XXh
D61Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.26 SFR Information (26) (1)

Address	Register	Symbol	Reset Value
D620h	CAN0 Mailbox 18: Message Identifier	C0MB18	XXh
D621h			XXh
D622h			XXh
D623h			XXh
D624h			
D625h	CAN0 Mailbox 18: Data Length		XXh
D626h	CAN0 Mailbox 18: Data Field		XXh
D627h			XXh
D628h			XXh
D629h			XXh
D62Ah			XXh
D62Bh			XXh
D62Ch			XXh
D62Dh			XXh
D62Eh	CAN0 Mailbox 18: Time Stamp		XXh
D62Fh			XXh
D630h	CAN0 Mailbox 19: Message Identifier	C0MB19	XXh
D631h			XXh
D632h			XXh
D633h			XXh
D634h			
D635h	CAN0 Mailbox 19: Data Length		XXh
D636h	CAN0 Mailbox 19: Data Field		XXh
D637h			XXh
D638h			XXh
D639h			XXh
D63Ah			XXh
D63Bh			XXh
D63Ch			XXh
D63Dh			XXh
D63Eh	CAN0 Mailbox 19: Time Stamp		XXh
D63Fh			XXh
D640h	CAN0 Mailbox 20: Message Identifier	C0MB20	XXh
D641h			XXh
D642h			XXh
D643h			XXh
D644h			
D645h	CAN0 Mailbox 20: Data Length		XXh
D646h	CAN0 Mailbox 20: Data Field		XXh
D647h			XXh
D648h			XXh
D649h			XXh
D64Ah			XXh
D64Bh			XXh
D64Ch			XXh
D64Dh			XXh
D64Eh	CAN0 Mailbox 20: Time Stamp		XXh
D64Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.27 SFR Information (27) (1)

Address	Register	Symbol	Reset Value
D650h	CAN0 Mailbox 21: Message Identifier	C0MB21	XXh
D651h			XXh
D652h			XXh
D653h			XXh
D654h			
D655h	CAN0 Mailbox 21: Data Length		XXh
D656h	CAN0 Mailbox 21: Data Field		XXh
D657h			XXh
D658h			XXh
D659h			XXh
D65Ah			XXh
D65Bh			XXh
D65Ch			XXh
D65Dh			XXh
D65Eh	CAN0 Mailbox 21: Time Stamp		XXh
D65Fh			XXh
D660h	CAN0 Mailbox 22: Message Identifier	C0MB22	XXh
D661h			XXh
D662h			XXh
D663h			XXh
D664h			
D665h	CAN0 Mailbox 22: Data Length		XXh
D666h	CAN0 Mailbox 22: Data Field		XXh
D667h			XXh
D668h			XXh
D669h			XXh
D66Ah			XXh
D66Bh			XXh
D66Ch			XXh
D66Dh			XXh
D66Eh	CAN0 Mailbox 22: Time Stamp		XXh
D66Fh			XXh
D670h	CAN0 Mailbox 23: Message Identifier	C0MB23	XXh
D671h			XXh
D672h			XXh
D673h			XXh
D674h			
D675h	CAN0 Mailbox 23: Data Length		XXh
D676h	CAN0 Mailbox 23: Data Field		XXh
D677h			XXh
D678h			XXh
D679h			XXh
D67Ah			XXh
D67Bh			XXh
D67Ch			XXh
D67Dh			XXh
D67Eh	CAN0 Mailbox 23: Time Stamp		XXh
D67Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.28 SFR Information (28) (1)

Address	Register	Symbol	Reset Value
D680h	CAN0 Mailbox 24: Message Identifier	C0MB24	XXh
D681h			XXh
D682h			XXh
D683h			XXh
D684h			
D685h	CAN0 Mailbox 24: Data Length		XXh
D686h	CAN0 Mailbox 24: Data Field		XXh
D687h			XXh
D688h			XXh
D689h			XXh
D68Ah			XXh
D68Bh			XXh
D68Ch			XXh
D68Dh			XXh
D68Eh	CAN0 Mailbox 24: Time Stamp		XXh
D68Fh			XXh
D690h	CAN0 Mailbox 25: Message Identifier	C0MB25	XXh
D691h			XXh
D692h			XXh
D693h			XXh
D694h			
D695h	CAN0 Mailbox 25: Data Length		XXh
D696h	CAN0 Mailbox 25: Data Field		XXh
D697h			XXh
D698h			XXh
D699h			XXh
D69Ah			XXh
D69Bh			XXh
D69Ch			XXh
D69Dh			XXh
D69Eh	CAN0 Mailbox 25: Time Stamp		XXh
D69Fh			XXh
D6A0h	CAN0 Mailbox 26: Message Identifier	C0MB26	XXh
D6A1h			XXh
D6A2h			XXh
D6A3h			XXh
D6A4h			
D6A5h	CAN0 Mailbox 26: Data Length		XXh
D6A6h	CAN0 Mailbox 26: Data Field		XXh
D6A7h			XXh
D6A8h			XXh
D6A9h			XXh
D6AAh			XXh
D6ABh			XXh
D6ACh			XXh
D6ADh			XXh
D6AEh	CAN0 Mailbox 26: Time Stamp		XXh
D6AFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.29 SFR Information (29) (1)

Address	Register	Symbol	Reset Value
D6B0h	CAN0 Mailbox 27: Message Identifier	C0MB27	XXh
D6B1h			XXh
D6B2h			XXh
D6B3h			XXh
D6B4h			
D6B5h	CAN0 Mailbox 27: Data Length		XXh
D6B6h	CAN0 Mailbox 27: Data Field		XXh
D6B7h			XXh
D6B8h			XXh
D6B9h			XXh
D6BAh			XXh
D6BBh			XXh
D6BCh			XXh
D6BDh			XXh
D6BEh	CAN0 Mailbox 27: Time Stamp		XXh
D6BFh			XXh
D6C0h	CAN0 Mailbox 28: Message Identifier	C0MB28	XXh
D6C1h			XXh
D6C2h			XXh
D6C3h			XXh
D6C4h			
D6C5h	CAN0 Mailbox 28: Data Length		XXh
D6C6h	CAN0 Mailbox 28: Data Field		XXh
D6C7h			XXh
D6C8h			XXh
D6C9h			XXh
D6CAh			XXh
D6CBh			XXh
D6CCh			XXh
D6CDh			XXh
D6CEh	CAN0 Mailbox 28: Time Stamp		XXh
D6CFh			XXh
D6D0h	CAN0 Mailbox 29: Message Identifier	C0MB29	XXh
D6D1h			XXh
D6D2h			XXh
D6D3h			XXh
D6D4h			
D6D5h	CAN0 Mailbox 29: Data Length		XXh
D6D6h	CAN0 Mailbox 29: Data Field		XXh
D6D7h			XXh
D6D8h			XXh
D6D9h			XXh
D6DAh			XXh
D6DBh			XXh
D6DCh			XXh
D6DDh			XXh
D6DEh	CAN0 Mailbox 29: Time Stamp		XXh
D6DFh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.30 SFR Information (30) (1)

Address	Register	Symbol	Reset Value
D6E0h	CAN0 Mailbox 30: Message Identifier	C0MB30	XXh
D6E1h			XXh
D6E2h			XXh
D6E3h			XXh
D6E4h			
D6E5h	CAN0 Mailbox 30: Data Length		XXh
D6E6h	CAN0 Mailbox 30: Data Field		XXh
D6E7h			XXh
D6E8h			XXh
D6E9h			XXh
D6EAh			XXh
D6EBh			XXh
D6ECh			XXh
D6EDh			XXh
D6EEh	CAN0 Mailbox 30: Time Stamp		XXh
D6EFh			XXh
D6F0h	CAN0 Mailbox 31: Message Identifier	C0MB31	XXh
D6F1h			XXh
D6F2h			XXh
D6F3h			XXh
D6F4h			
D6F5h	CAN0 Mailbox 31: Data Length		XXh
D6F6h	CAN0 Mailbox 31: Data Field		XXh
D6F7h			XXh
D6F8h			XXh
D6F9h			XXh
D6FAh			XXh
D6FBh			XXh
D6FCh			XXh
D6FDh			XXh
D6FEh	CAN0 Mailbox 31: Time Stamp		XXh
D6FFh			XXh
D700h	CAN0 Mask Register 0	C0MKR0	XXh
D701h			XXh
D702h			XXh
D703h			XXh
D704h	CAN0 Mask Register 1	C0MKR1	XXh
D705h			XXh
D706h			XXh
D707h			XXh
D708h	CAN0 Mask Register 2	C0MKR2	XXh
D709h			XXh
D70Ah			XXh
D70Bh			XXh
D70Ch	CAN0 Mask Register 3	C0MKR3	XXh
D70Dh			XXh
D70Eh			XXh
D70Fh			XXh

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.31 SFR Information (31) (1)

Address	Register	Symbol	Reset Value
D710h	CAN0 Mask Register 4	C0MKR4	XXh
D711h			XXh
D712h			XXh
D713h			XXh
D714h	CAN0 Mask Register 5	C0MKR5	XXh
D715h			XXh
D716h			XXh
D717h			XXh
D718h	CAN0 Mask Register 6	C0MKR6	XXh
D719h			XXh
D71Ah			XXh
D71Bh			XXh
D71Ch	CAN0 Mask Register 7	C0MKR7	XXh
D71Dh			XXh
D71Eh			XXh
D71Fh			XXh
D720h	CAN0 FIFO Receive ID Compare Register 0	C0FIDCR0	XXh
D721h			XXh
D722h			XXh
D723h			XXh
D724h	CAN0 FIFO Receive ID Compare Register 1	C0FIDCR1	XXh
D725h			XXh
D726h			XXh
D727h			XXh
D728h	CAN0 Mask Invalid Register	C0MKIVLR	XXh
D729h			XXh
D72Ah			XXh
D72Bh			XXh
D72Ch	CAN0 Mailbox Interrupt Enable Register	C0MIER	XXh
D72Dh			XXh
D72Eh			XXh
D72Fh			XXh
D730h to D79Fh			
D7A0h	CAN0 Message Control Register 0	C0MCTL0	00h
D7A1h	CAN0 Message Control Register 1	C0MCTL1	00h
D7A2h	CAN0 Message Control Register 2	C0MCTL2	00h
D7A3h	CAN0 Message Control Register 3	C0MCTL3	00h
D7A4h	CAN0 Message Control Register 4	C0MCTL4	00h
D7A5h	CAN0 Message Control Register 5	C0MCTL5	00h
D7A6h	CAN0 Message Control Register 6	C0MCTL6	00h
D7A7h	CAN0 Message Control Register 7	C0MCTL7	00h
D7A8h	CAN0 Message Control Register 8	C0MCTL8	00h
D7A9h	CAN0 Message Control Register 9	C0MCTL9	00h
D7AAh	CAN0 Message Control Register 10	C0MCTL10	00h
D7ABh	CAN0 Message Control Register 11	C0MCTL11	00h
D7ACh	CAN0 Message Control Register 12	C0MCTL12	00h
D7ADh	CAN0 Message Control Register 13	C0MCTL13	00h
D7AEh	CAN0 Message Control Register 14	C0MCTL14	00h
D7AFh	CAN0 Message Control Register 15	C0MCTL15	00h

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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Table 4.32 SFR Information (32) (1)

Address	Register	Symbol	Reset Value
D7B0h	CAN0 Message Control Register 16	C0MCTL16	00h
D7B1h	CAN0 Message Control Register 17	C0MCTL17	00h
D7B2h	CAN0 Message Control Register 18	C0MCTL18	00h
D7B3h	CAN0 Message Control Register 19	C0MCTL19	00h
D7B4h	CAN0 Message Control Register 20	C0MCTL20	00h
D7B5h	CAN0 Message Control Register 21	C0MCTL21	00h
D7B6h	CAN0 Message Control Register 22	C0MCTL22	00h
D7B7h	CAN0 Message Control Register 23	C0MCTL23	00h
D7B8h	CAN0 Message Control Register 24	C0MCTL24	00h
D7B9h	CAN0 Message Control Register 25	C0MCTL25	00h
D7BAh	CAN0 Message Control Register 26	C0MCTL26	00h
D7BBh	CAN0 Message Control Register 27	C0MCTL27	00h
D7BCh	CAN0 Message Control Register 28	C0MCTL28	00h
D7BDh	CAN0 Message Control Register 29	C0MCTL29	00h
D7BEh	CAN0 Message Control Register 30	C0MCTL30	00h
D7BFh	CAN0 Message Control Register 31	C0MCTL31	00h
D7C0h	CAN0 Control Register	C0CTLR	0000 0101b
D7C1h			00h
D7C2h	CAN0 Status Register	C0STR	0000 0101b
D7C3h			00h
D7C4h	CAN0 Bit Configuration Register	C0BCR	00h
D7C5h			00h
D7C6h			00h
D7C7h	CAN0 Clock Select Register	C0CLKR	00h
D7C8h	CAN0 Receive FIFO Control Register	C0RFCR	1000 0000b
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR	XXh
D7CAh	CAN0 Transmit FIFO Control Register	C0TFCR	1000 0000b
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR	XXh
D7CCh	CAN0 Error Interrupt Enable Register	C0EIER	00h
D7CDh	CAN0 Error Interrupt Source Judge Register	C0EIFR	00h
D7CEh	CAN0 Receive Error Count Register	C0RECR	00h
D7CFh	CAN0 Transmit Error Count Register	C0TECR	00h
D7D0h	CAN0 Error Code Store Register	C0ECSR	00h
D7D1h	CAN0 Channel Search Support Register	C0CSSR	XXh
D7D2h	CAN0 Mailbox Search Status Register	C0MSSR	1000 0000b
D7D3h	CAN0 Mailbox Search Mode Register	C0MSMR	0000 0000b
D7D4h	CAN0 Time Stamp Register	C0TSR	00h
D7D5h			00h
D7D6h	CAN0 Acceptance Filter Support Register	C0AFSR	XXh
D7D7h			XXh
D7D8h	CAN0 Test Control Register	C0TCR	00h
D7D9h			
D7DAh			
D7DBh			
D7DCh			
D7DDh			
D7DEh			
D7DFh			

X: Undefined

Note:
1. The blank areas are reserved. No access is allowed.

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4.2 Notes on SFRs

4.2.1 Register Settings

Table 4.33 lists Registers with Write-Only Bits and registers whose function differs between reading and writing. Set these registers with immediate values. Do not use read-modify-write instructions. When establishing the next value by altering the existing value, write the existing value to the RAM as well as to the register. Transfer the next value to the register after making changes in the RAM.
Read-modify-write instructions can be used when writing to the no register bits.

Table 4.33 Registers with Write-Only Bits

Address	Register	Symbol
0249h	UART0 Bit Rate Register	U0BRG
024Bh to 024Ah	UART0 Transmit Buffer Register	U0TB
0259h	UART1 Bit Rate Register	U1BRG
025Bh to 025Ah	UART1 Transmit Buffer Register	U1TB
0269h	UART2 Bit Rate Register	U2BRG
026Bh to 026Ah	UART2 Transmit Buffer Register	U2TB
0299h	UART4 Bit Rate Register	U4BRG
029Bh to 029Ah	UART4 Transmit Buffer Register	U4TB
02A9h	UART3 Bit Rate Register	U3BRG
02ABh to 02AAh	UART3 Transmit Buffer Register	U3TB
02B6h	I2C0 Control Register 1	S3D0
02B8h	I2C0 Status Register 0	S10
0303h to 0302h	Timer A1-1 Register	TA11
0305h to 0304h	Timer A2-1 Register	TA21
0307h to 0306h	Timer A4-1 Register	TA41
030Ah	Three-Phase Output Buffer Register 0	IDB0
030Bh	Three-Phase Output Buffer Register 1	IDB1
030Ch	Dead Time Timer	DTT
030Dh	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2
0327h to 0326h	Timer A0 Register	TA0
0329h to 0328h	Timer A1 Register	TA1
032Bh to 032Ah	Timer A2 Register	TA2
032Dh to 032Ch	Timer A3 Register	TA3
032Fh to 032Eh	Timer A4 Register	TA4
037Dh	Watchdog Timer Refresh Register	WDTR
037Eh	Watchdog Timer Start Register	WDTS
D7C9h	CAN0 Receive FIFO Pointer Control Register	C0RFPCR
D7CBh	CAN0 Transmit FIFO pointer Control Register	C0TFPCR

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Table 4.34 Read-Modify-Write Instructions

Function	Mnemonic
Transfer	MOV*Dir*
Bit processing	BCLR, BM*Cnd*, BNOT, BSET, BTSTC, and BTSTS
Shifting	ROLC, RORC, ROT, SHA, and SHL
Arithmetic operation	ABS, ADC, ADCF, ADD, DEC, DIV, DIVU, DIVX, EXTS, INC, MUL, MULU, NEG, SBB, and SUB
Decimal operation	DADC, DADD, DSBB, and DSUB
Logical operation	AND, NOT, OR, and XOR
Jump	ADJNZ, SBJNZ

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5. Electrical Characteristics

5.1 Electrical Characteristics (Common to 3 V and 5 V)

5.1.1 Absolute Maximum Rating

Table 5.1 Absolute Maximum Ratings

Symbol	Characteristic		Condition	Rated Value	Unit
V_{CC}	Supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage		$V_{CC} = AV_{CC}$	-0.3 to 6.5	V
V_{REF}	Analog reference voltage			–0.3 to V_{CC} + 0.1 (1)	V
V_I	Input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{\text{RESET}}$, CNVSS		-0.3 to VCC + 0.3	V
V_O	Output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XOUT		-0.3 to VCC + 0.3	V
P_d	Power consumption		-40°C ≤ T_{opr} ≤ 85°C	300	mW
T_{opr}	Operating temperature range	While CPU operation		-40 to 85	°C
		While flash memory program and erase operation	Programming area	0 to 60	
			Data area	-40 to 85	
T_{stg}	Storage temperature range			-65 to 150	°C

Note:
1. Maximum value is 6.5 V.

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5.1.2 Recommended Operating Conditions

Table 5.2 Operating Conditions (1)

V_{CC} = 2.7 V to 5.5 V, T_{opr} = -40°C to 85°C unless otherwise specified.

Symbol	Characteristic		Standard			Unit
			Min.	Typ.	Max.	
V_{CC}	Supply voltage		2.7		5.5	V
AV_{CC}	Analog supply voltage			V_{CC}		V
V_{SS}	Ground voltage			0		V
AV_{SS}	Analog ground voltage			0		V
V_{IH}	High level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	0.7 V_{CC}		V_{CC}	V
		XIN, $\overline{RESET}$, CNVSS	0.8 V_{CC}		V_{CC}	
		SDAMM, SCLMM When I^2C-bus input level selected	0.7 V_{CC}		V_{CC}	V
		SDAMM, SCLMM When SMBUS input level selected	2.1		V_{CC}	V
V_{IL}	Low level input voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	0		0.3 V_{CC}	V
		XIN, $\overline{RESET}$, CNVSS	0		0.2 V_{CC}	V
		SDAMM, SCLMM When I^2C-bus input level selected	0		0.3 V_{CC}	V
		SDAMM, SCLMM When SMBUS input level selected	0		0.8	V
$I_{OH(sum)}$	High peak output current	Sum of $I_{OH(peak)}$ at P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-80.0	mA
$I_{OH(peak)}$	High level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-10.0	mA
$I_{OH(avg)}$	High level average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			-5.0	mA
$I_{OL(sum)}$	Low peak output current	Sum of $I_{OL(peak)}$ atP0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			80.0	mA
$I_{OL(peak)}$	Low level peak output current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			10.0	mA
$I_{OL(avg)}$	Low level average output current (1)	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7			5.0	mA
$f_{(XIN)}$	Main clock input oscillation frequency (2)		2		20	MHz
$f_{(XCIN)}$	Sub clock oscillation frequency			32.768	50	kHz
$f_{(PLL)}$	PLL clock oscillation frequency (2)	Vcc = 2.7 V to 5.5 V	10		25	MHz
		Vcc = 3.0 V to 5.5 V	10		32	
$f_{(BCLK)}$	CPU operation frequency		2		32	MHz
$t_{su(PLL)}$	Wait time to stabilize PLL frequency synthesizer	Vcc = 5.0 V			2	ms
		Vcc = 3.0 V			3	

Notes:
1. The mean output current is the mean value within 100 ms.
2. Refer to Figure 5.1 “Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency” for the relationship between main clock oscillation frequency/PLL clock oscillation frequency and supply voltage.

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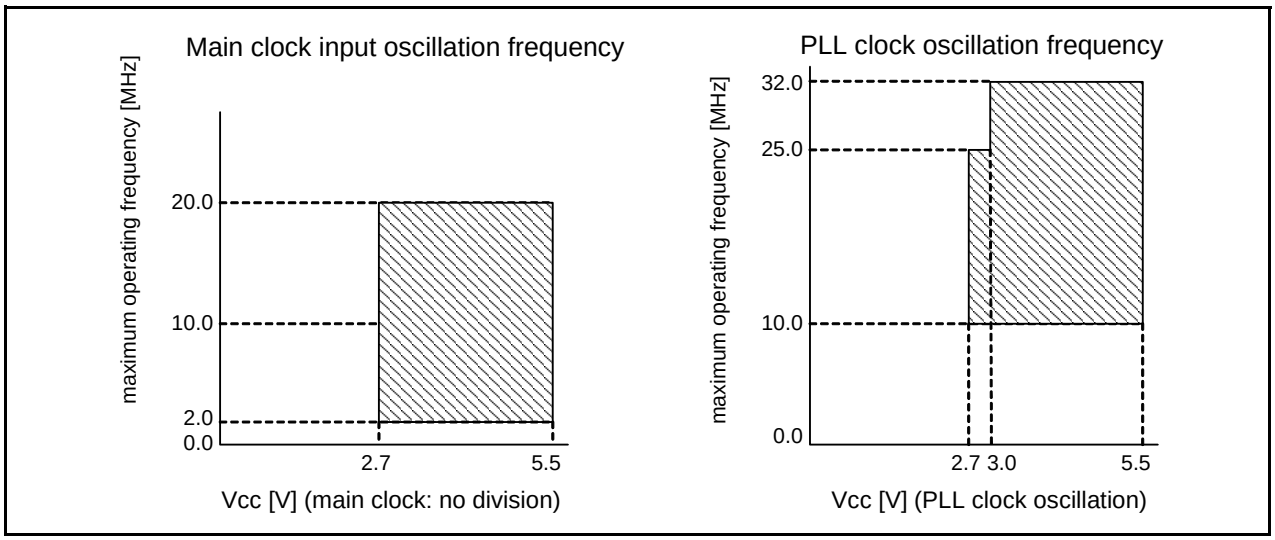


Figure 5.1 Main Clock Input Oscillation Frequency, PLL Clock Oscillation Frequency

Table 5.3 Recommended Operating Conditions (2/2) (1)

V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, and T_{opr} = -40°C to 85°C unless otherwise specified.
The ripple voltage must not excess $V_{r(VCC)}$ and/or $dV_{r(VCC)}/dt$.

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$V_{r(VCC)}$	Allowable ripple voltage	V_{CC} = 5.0 V			0.5	Vp-p
		V_{CC} = 3.0 V			0.3	Vp-p
$dV_{r(VCC)}/dt$	Ripple voltage falling gradient	V_{CC} = 5.0 V			0.3	V/ms
		V_{CC} = 3.0 V			0.3	V/ms

Note:
1. The device is operationally guaranteed under these operating conditions.

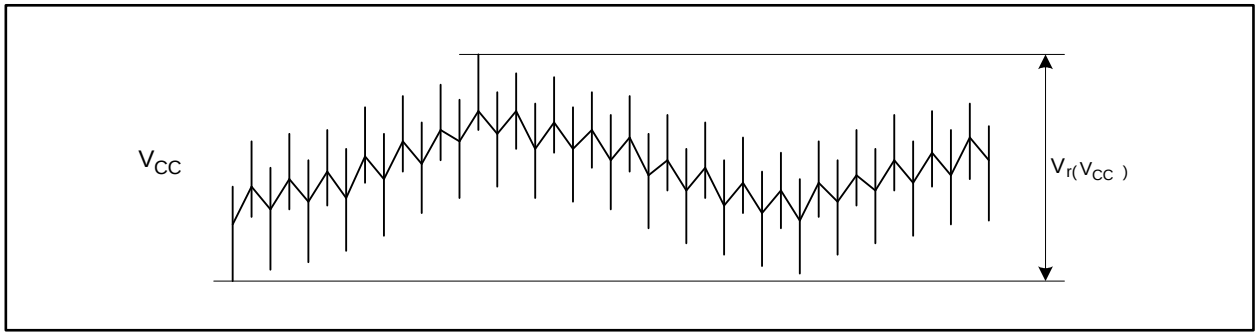


Figure 5.2 Ripple Waveform

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5.1.3 A/D Conversion Characteristics

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Table 5.4 A/D Conversion Characteristics (1, 3)

$V_{CC} = AV_{CC} = V_{REF} = 3.0$ to 5.5 V, $V_{SS} = AV_{SS} = 0$ V at $T_{opr} = -40°C$ to $85°C$ unless otherwise specified

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
—	Resolution	$V_{REF} = V_{CC}$			10	Bits
I_{NL}	Integral non-linearity error	$V_{REF} = V_{CC} = 5.0$ V (2)			±3	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			±5	LSB
—	Absolute accuracy	$V_{REF} = V_{CC} = 5.0$ V (2)			±3	LSB
		$V_{REF} = V_{CC} = 3.3$ V (2)			±5	LSB
ϕAD	A/D operating clock frequency	4.0 V ≤ V_{CC} ≤ 5.5 V	2		25	MHz
		3.2 V ≤ V_{CC} ≤ 4.0 V	2		16	MHz
		3.0 V ≤ V_{CC} ≤ 3.2 V	2		10	MHz
—	Tolerance level impedance			3		kΩ
D_{NL}	Differential non-linearity error	(2)			±1	LSB
—	Offset error	(2)			±3	LSB
—	Gain error	(2)			±3	LSB
t_{CONV}	10-bit conversion time	$V_{REF} = V_{CC} = 5$V, ϕAD = 25 MHz	1.60			µs
t_{samp}	Sampling time		0.6			µs
V_{REF}	Reference voltage		3.0		V_{CC}	V
V_{IA}	Analog Input voltage (4)		0		V_{REF}	V

Notes:
1. Use when $AV_{CC} = V_{CC}$
2. Flash memory rewrite disabled. Except for the analog input pin, set the pins to be measured as input ports and connect them to V_{SS}. See Figure 5.3 “A/D Accuracy Measure Circuit”.
3. This applies when using one of the A/D converter circuits, with the ADSTBY bit for the unused A/D converter set to 0 (A/D operation stopped (standby)).
4. When analog input voltage is over reference voltage, the result of A/D conversion is 3FFh.

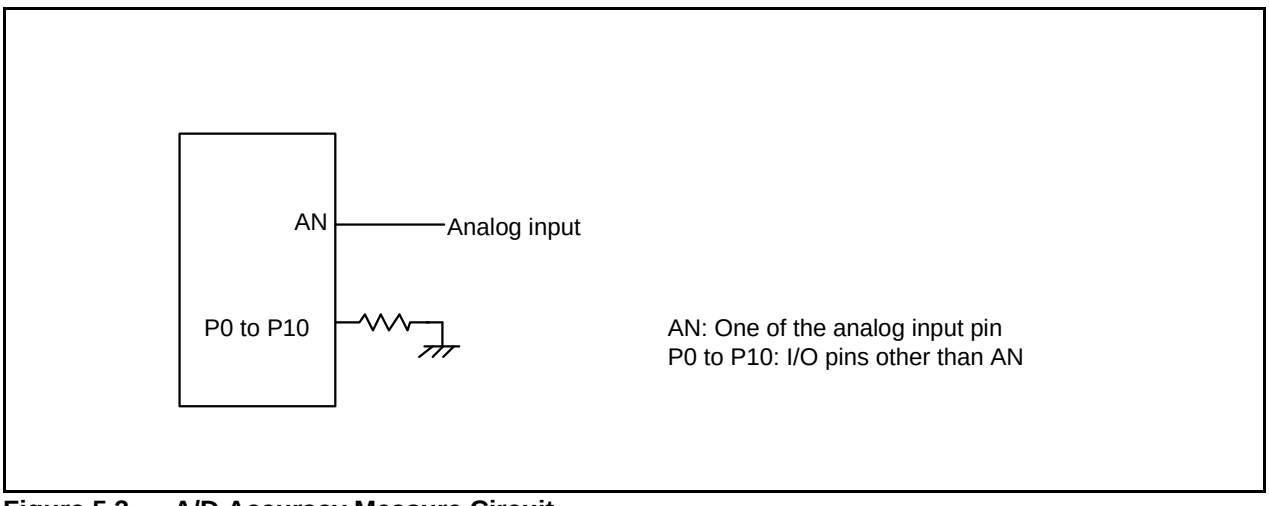


Figure 5.3 A/D Accuracy Measure Circuit

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5.1.4 Flash Memory Electrical Characteristics

Table 5.5 CPU Clock When Operating Flash Memory ($f_{(BCLK)}$)

V_{CC} = 2.7 to 5.5 V, at T_{opr} = -40°C to 85°C unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	CPU rewrite mode				10 (1)	MHz
$f_{(SLOW_R)}$	Slow read mode				5 (3)	MHz
-	Low current consumption read mode			fC(32.768)	35	kHz
-	Data flash read	2.7 V < V_{CC} ≤ 3.0 V			16 (2)	MHz
		3.0 V < V_{CC} ≤ 5.5 V			20 (2)	

Notes:
1. Set the PM17 bit in the PM1 register to 1 (one wait).
2. When the frequency is over this value, set the FMR17 bit in the FMR1 register to 0 (one wait) or the PM17 bit in the PM1 register to 1 (one wait)
3. Set the PM17 bit in the PM1 register to 1 (one wait). When using the 125 kHz on-chip oscillator clock or sub clock as the CPU clock source, a wait is not necessary.

Table 5.6 Flash Memory (Program ROM 1, 2) Electrical Characteristics

V_{CC} = 2.7 to 5.5 V at T_{opr} = 0°C to 60°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1, 3, 4)	V_{CC} = 3.3 V, T_{opr} = 25°C	1,000 (2)			times
-	2 words program time	V_{CC} = 3.3 V, T_{opr} = 25°C		150	4000	µs
	Lock bit program time	V_{CC} = 3.3 V, T_{opr} = 25°C		70	3000	µs
-	Block erase time	V_{CC} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f_{(BCLK)}}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f_{(BCLK)}}$	µs
-	Program, erase voltage		2.7		5.5	V
-	Read voltage	Topr= -40°C to 85°C	2.7		5.5	V
-	Program, erase temperature		0		60	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:
1. Definition of program and erase cycles:
   The program and erase cycles refer to the number of per-block erasures. If the program and erase cycles are n (n = 1,000), each block can be erased n times. For example, if a 64 KB block is erased after writing 2 word data 16,384 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. It is advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

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Table 5.7 Flash Memory (Data Flash) Electrical Characteristics

V_{CC} = 2.7 to 5.5 V at T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
-	Program and erase cycles (1, 3, 4)	V_{CC} = 3.3 V, T_{opr} = 25°C	10,000 (2)			times
-	2 words program time	V_{CC} = 3.3 V, T_{opr} = 25°C		300	4000	µs
-	Lock bit program time	V_{CC} = 3.3 V, T_{opr} = 25°C		140	3000	µs
-	Block erase time	V_{CC} = 3.3 V, T_{opr} = 25°C		0.2	3.0	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend				$5 + \frac{3}{f(BCLK)}$	ms
-	Interval from erase start/restart until following suspend request		0			µs
-	Suspend interval necessary for auto-erasure to complete (7)		20			ms
-	Time from suspend until erase restart				$30 + \frac{1}{f(BCLK)}$	µs
-	Program, erase voltage		2.7		5.5	V
-	Read voltage		2.7		5.5	V
-	Program, erase temperature		–40		85	°C
t_{PS}	Flash memory circuit stabilization wait time				50	µs
-	Data hold time (6)	Ambient temperature = 55°C	20			year

Notes:

1. Definition of program and erase cycles
   The program and erase cycles refer to the number of per-block erasures.
   If the program and erase cycles are n (n = 10,000), each block can be erased n times.
   For example, if a 4 KB block is erased after writing 2 word data 1,024 times, each to a different address, this counts as one program and erase cycles. Data cannot be written to the same address more than once without erasing the block (rewrite prohibited).
2. Cycles to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 256 groups before erasing them all in one operation. In addition, averaging the erasure cycles between blocks A and B can further reduce the actual erasure cycles. It is also advisable to retain data on the erasure cycles of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program and erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. After an erase start or erase restart, if an interval of at least 20 ms is not set before the next suspend request, the erase sequence cannot be completed.

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5.1.5 Voltage Detector and Power Supply Circuit Electrical Characteristics

Table 5.8 Voltage Detector 0 Electrical Characteristics

The measurement condition is V_{CC} = 2.7 to 5.5 V, T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level V_{det0}	When V_{CC} is falling.	2.70	2.85	3.00	V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)				100	µs

Note:
1. Necessary time until the voltage detector operates when setting to 1 again after setting the VC25 bit in the VCR2 register to 0.

Table 5.9 Voltage Detector 2 Electrical Characteristics

The measurement condition is V_{CC} = 2.7 to 5.5 V, T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
Vdet2_0	Voltage detection level Vdet2_0	When V_{CC} is falling		3.21		V
Vdet2_1	Voltage detection level Vdet2_1			3.36		V
Vdet2_2	Voltage detection level Vdet2_2			3.51		V
Vdet2_3	Voltage detection level Vdet2_3			3.66		V
Vdet2_4	Voltage detection level Vdet2_4		3.51	3.81	4.11	V
Vdet2_5	Voltage detection level Vdet2_5			3.96		V
Vdet2_6	Voltage detection level Vdet2_6			4.10		V
Vdet2_7	Voltage detection level Vdet2_7			4.25		V
-	Hysteresis width at the rising of V_{CC} in voltage detector 2			0.15		V
$t_{d(E-A)}$	Waiting time until voltage detector operation starts (1)				100	µs

Note:
1. Necessary time until the voltage detector operates after setting to 1 again after setting the VC27 bit in the VCR2 register to 0.

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Table 5.10 Power-On Reset Circuit

The measurement condition is T_{opr} = -40°C to 85°C, unless otherwise specified.

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient		2.0		50000	mV/ms
t_{fth}	External power V_{CC} fall gradient				50000	mV/ms
V_{por}	Voltage at which power-on reset enabled (1)				0.1	V
$t_{w(por)}$	Hold time at which power-on reset enabled		1.0			ms

Note:
1. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS1 address to 0.

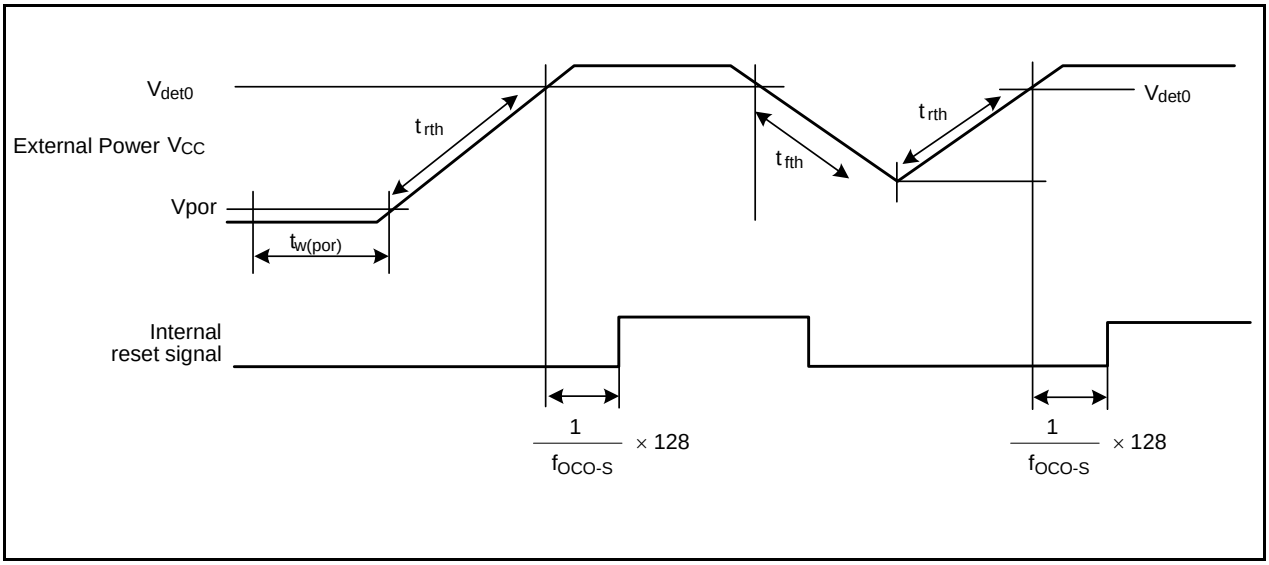


Figure 5.4 Power-On Reset Circuit Electrical Characteristics

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Measuring Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during powering-on	VCC = 3.0 V to 5.5V			5	ms
$t_{d(R-S)}$	STOP release time				300	µs
$td_{(W-S)}$	Low power mode wait mode release time				300	µs

Note:
1. When V_{CC} = 5 V.

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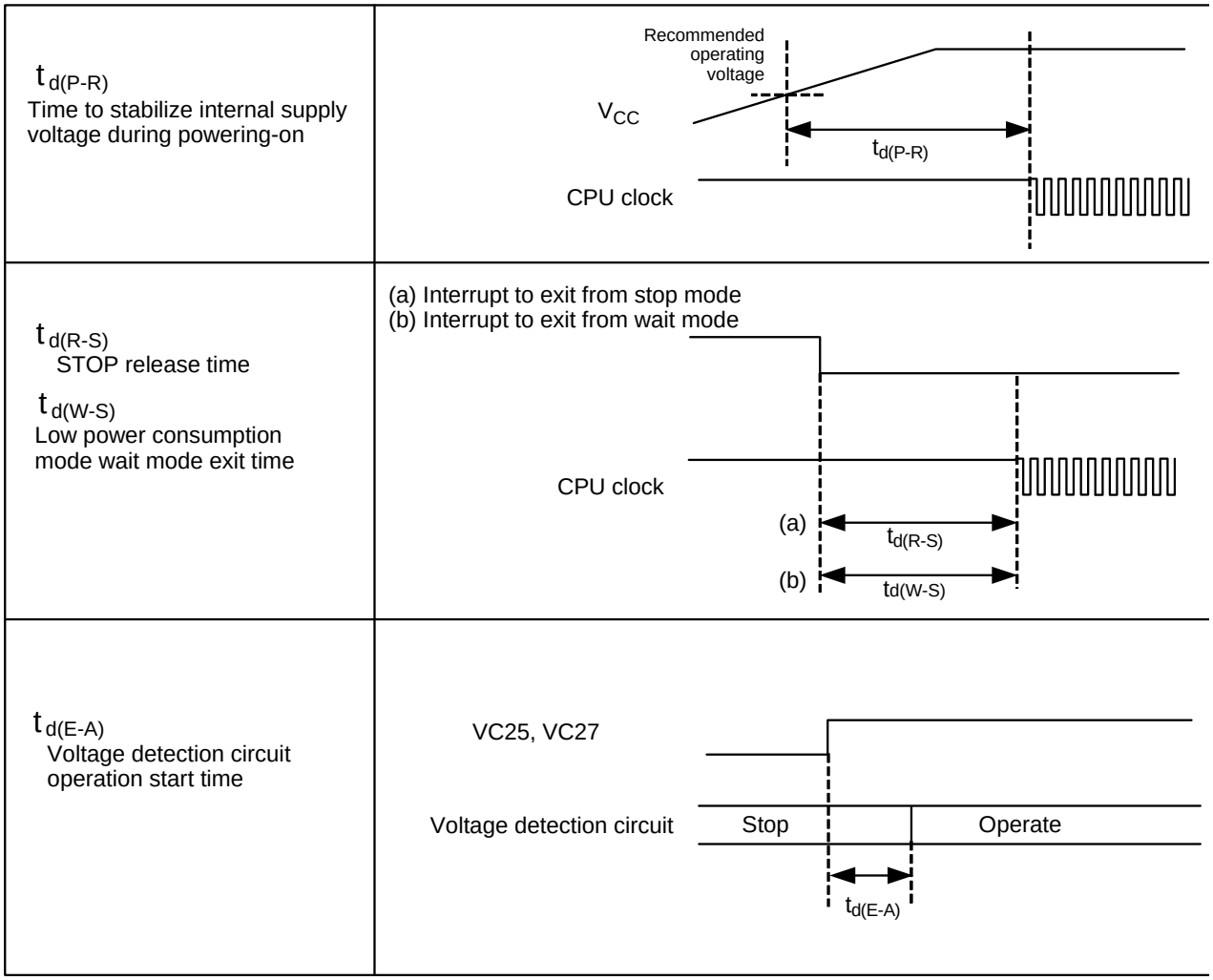


Figure 5.5 Power Supply Circuit Timing Diagram

5.1.6 Oscillator Electrical Characteristics

Table 5.12 125kHz On-Chip Oscillator Electrical Characteristics

V_{CC} = 2.7 to 5.5 V, T_{opr} = –40°C to 85°C, unless otherwise specified

Symbol	Characteristic	Condition	Standard			Unit
			Min.	Typ.	Max.	
f_{OCO-S}	125 kHz on-chip oscillator oscillation frequency		100	125	150	kHz
$tsu(f_{OCO-S})$	Wait time until 125 kHz on-chip oscillator stabilizes	2.7 V ≤ V_{CC} ≤ 5.5 V			20	µs
f_{WDT}	Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency		100	125	150	kHz

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5.2 Electrical Characteristics (V_{CC} = 5 V)

5.2.1 Electrical Characteristics

V_{CC} = 5 V

Table 5.13 Electrical Characteristics (1)

V_{CC} = 4.2 to 5.5 V, V_{SS} = 0 V at T_{opr} = -40°C to 85°C, $f_{(BCLK)}$ = 32 MHz unless otherwise specified.

Symbol	Parameter		Measuring Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	I_{OH}=–5 mA	V_{CC}–2.0		V_{CC}	V
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	I_{OH} = –200 µA	V_{CC}–0.3		V_{CC}	V
V_{OH}	HIGH output voltage XOUT	HIGH POWER	I_{OH} = –1 mA	V_{CC}–2.0		V_{CC}	V
		LOW POWER	I_{OH} = –0.5 mA	V_{CC}–2.0		V_{CC}	
	HIGH output voltage XCOUT	HIGH POWER	With no load applied		2.5		V
		LOW POWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	I_{OL} = 5 mA			2.0	V
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	I_{OL} = 200 µA			0.45	V
V_{OL}	LOW output voltage XOUT	HIGH POWER	I_{OL} = 1 mA			2.0	V
		LOW POWER	I_{OL} = 0.5 mA			2.0	
	LOW output voltage XCOUT	HIGH POWER	With no load applied		0		V
		LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS3}$, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0		0.2		0.4V_{CC}	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$		0.2		2.5	V
V_{T+}-V_{T-}	Hysteresis	XIN		0.2		0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS	V_I = 5 V			5.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS	V_I = 0 V			–5.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7	V_I = 0 V	30	50	170	kΩ
R_{fXIN}	Feedback resistance XIN				1.5		MΩ
R_{fXCIN}	Feedback resistance XCIN				15		MΩ
V_{RAM}	RAM retention voltage		At stop mode	2.0			V

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V_{CC} = 5 V

Table 5.14 Electrical Characteristics (2)

T_{opr} = –40°C to 85°C unless otherwise specified.

Symbol	Parameter		Measuring Condition		Standard			Unit
					Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} =4.2V to 5.5 V) In single-chip mode, the output pins are open and other pins are V_{SS}		High speed mode	$f_{(BCLK)}$ = 32 MHz, XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operates		28	42	mA
				$f_{(BCLK)}$ = 20 MHz, XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operates		20	30	mA
				$f_{(BCLK)}$ = 16 MHz, XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operates		16		mA
			125 kHz on-chip oscillator mode	Main clock stops 125 kHz on-chip oscillator operates Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		150	500	µA
			Low power mode	$f_{(BCLK)}$ = 32 kHz On Flash memory (1) FMR22 = FMR23 = 1 (Low-current consumption read mode)		160		µA
			Wait mode	Main clock stops 125 kHz on-chip oscillator operates Peripheral clock operates T_{opr} = 25°C		20		µA
				Main clock stops 125 kHz on-chip oscillator operates Peripheral clock operates T_{opr} = 85°C		50		µA
			Stop mode	T_{opr} = 25°C		18	30	µA
				T_{opr} = 85°C		45		µA
			During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 5.0 V		20.0		mA
			During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 5.0 V		30.0		mA
I_{det2}	Low voltage detection dissipation current					3		µA
I_{det0}	Reset area detection dissipation current					6		µA

Note:

1. This indicates the memory in which the program to be executed exists.

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V_{CC} = 5 V

5.2.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = -40°C to 85°C unless otherwise specified)

5.2.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.15 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

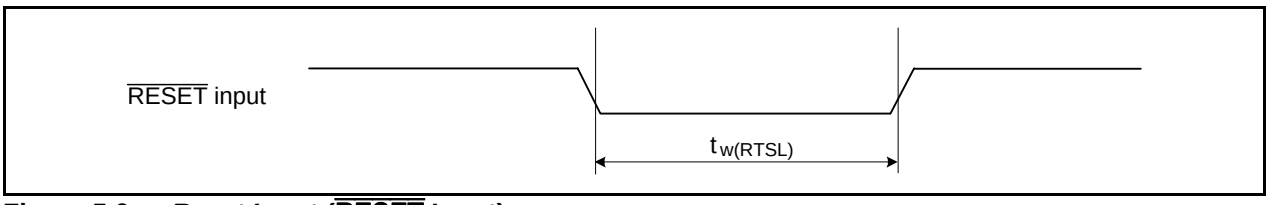


Figure 5.6 Reset Input ($\overline{\text{RESET}}$ Input)

5.2.2.2 External Clock Input

Table 5.16 External Clock Input (XIN Input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 3.0V to 5.0V

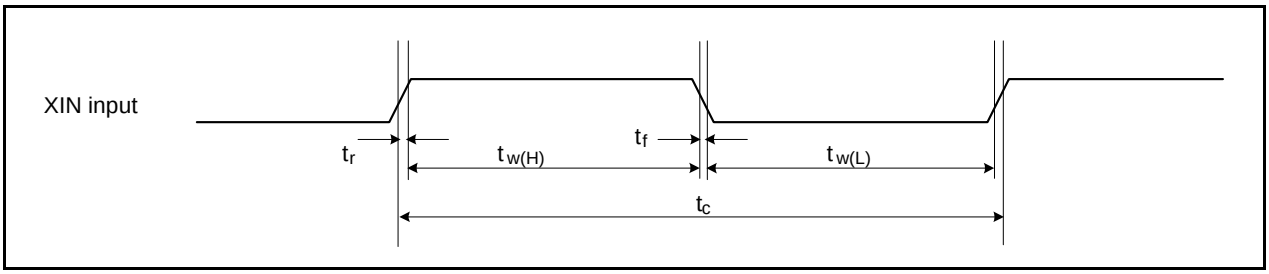


Figure 5.7 External Clock Input (XIN Input)

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V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.2.2.3 Timer A Input

Table 5.17 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	100		ns
$t_{w(TAH)}$	TAiIN input high pulse width	40		ns
$t_{w(TAL)}$	TAiIN input low pulse width	40		ns

Table 5.18 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	400		ns
$t_{w(TAH)}$	TAiIN input high pulse width	200		ns
$t_{w(TAL)}$	TAiIN input low pulse width	200		ns

Table 5.19 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	200		ns
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

Table 5.20 Timer A Input (External Trigger Input in PWM Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	100		ns
$t_{w(TAL)}$	TAiIN input low pulse width	100		ns

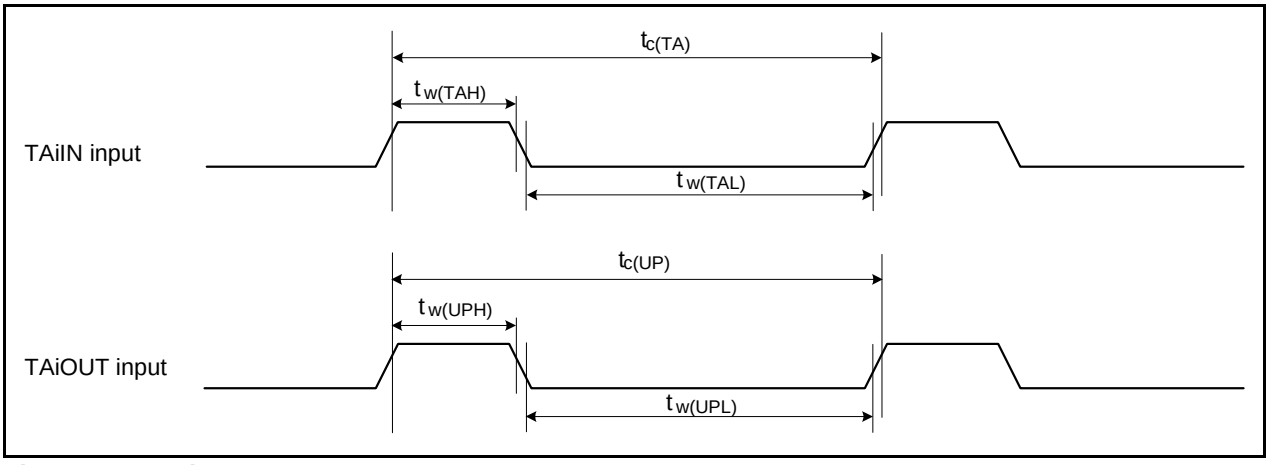


Figure 5.8 Timer A Input

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V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

Table 5.21 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	800		ns
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	200		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	200		ns

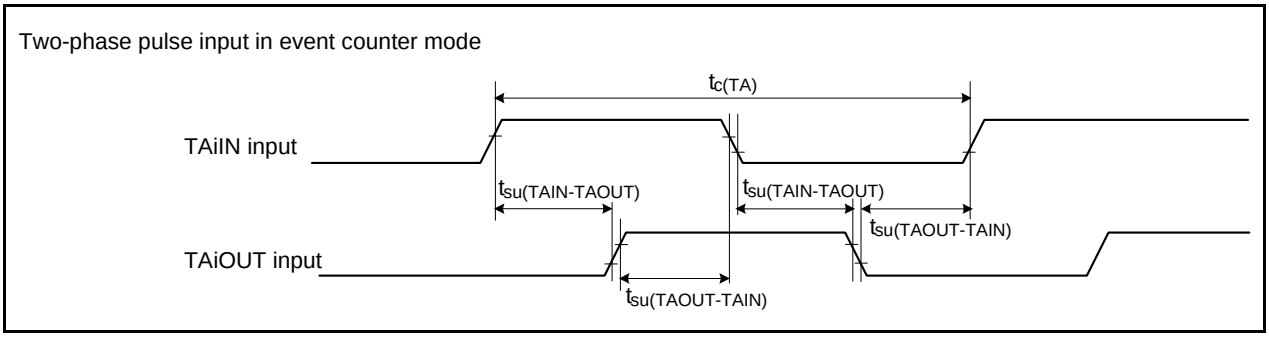


Figure 5.9 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

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V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.2.2.4 Timer B Input

Table 5.22 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	80		ns

Table 5.23 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

Table 5.24 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	400		ns
$t_{w(TBH)}$	TBiIN input high pulse width	200		ns
$t_{w(TBL)}$	TBiIN input low pulse width	200		ns

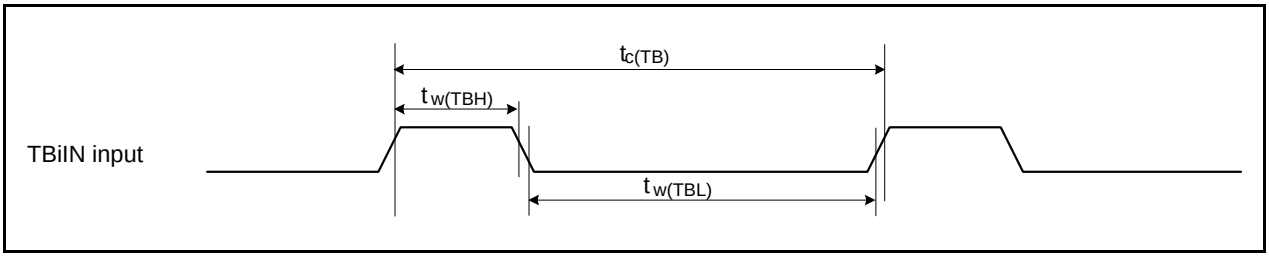


Figure 5.10 Timer B Input

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V_{CC} = 5 V

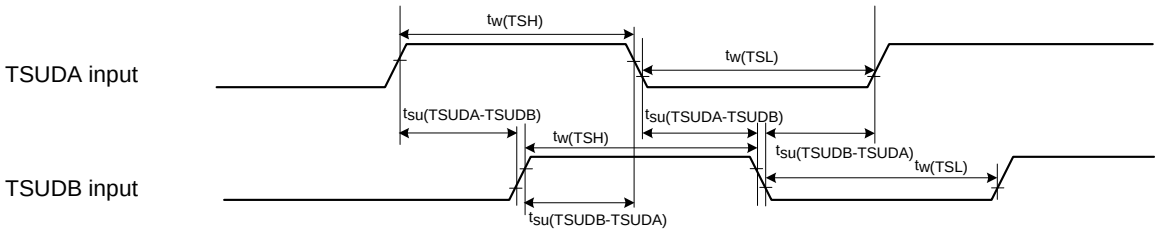
Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.2.2.5 Timer S Input

Table 5.25 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 5.11 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

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V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.2.2.6 Serial Interface

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200		ns
$t_{w(CKH)}$	CLKi input high pulse width	100		ns
$t_{w(CKL)}$	CLKi input low pulse width	100		ns
$t_{d(C-Q)}$	TXDi output delay time		80	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	70		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

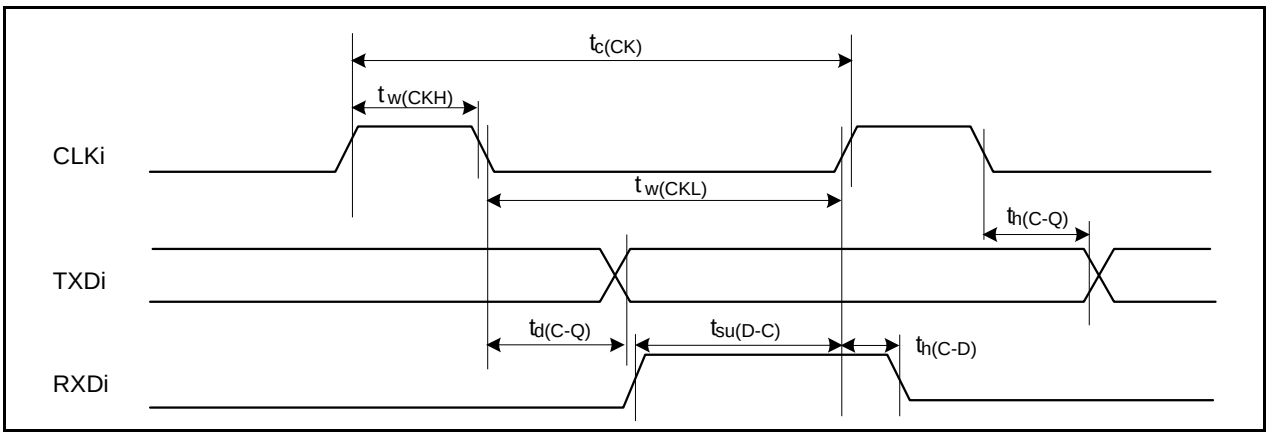


Figure 5.12 Serial Interface

5.2.2.7 External Interrupt $\overline{INTi}$ Input

Table 5.27 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	250		ns

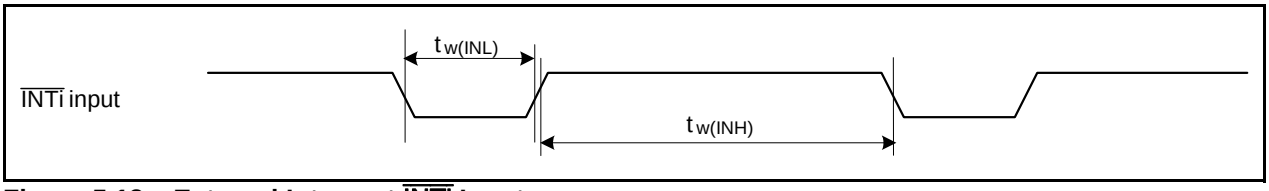


Figure 5.13 External Interrupt $\overline{INTi}$ Input

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V_{CC} = 5 V

Timing Requirements
(V_{CC} = 5 V, V_{SS} = 0 V, at T_{opr} = −40°C to 85°C unless otherwise specified)

5.2.2.8 Multi-master I²C-bus

Table 5.28 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

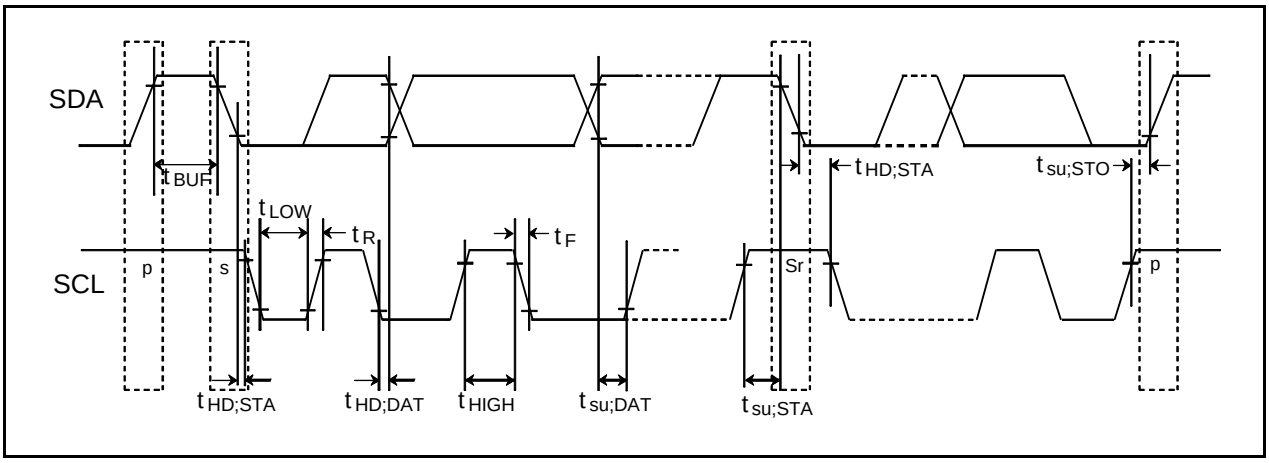


Figure 5.14 Multi-master I²C-bus

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5.3 Electrical Characteristics (V_{CC} = 3 V)

5.3.1 Electrical Characteristics

V_{CC} = 3 V

Table 5.29 Electrical Characteristics (1)

V_{CC} = 2.7 to 3.3V, V_{SS} = 0 V at T_{opr} = −40°C to 85°C, $f_{(BCLK)}$=25 MHz unless otherwise specified.

Symbol	Parameter			Measuring Condition	Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	HIGH output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7		I_{OH} = −1 mA	V_{CC}−0.5		V_{CC}	V
V_{OH}	HIGH output voltage XOUT		HIGH POWER	I_{OH} = −0.1 mA	V_{CC}−0.5		V_{CC}	V
			LOW POWER	I_{OH} = −50 µA	V_{CC}−0.5		V_{CC}	
	HIGH output voltage XCOUT		HIGH POWER	With no load applied		2.5		V
			LOW POWER	With no load applied		1.6		
V_{OL}	LOW output voltage	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7		I_{OL} = 1mA			0.5	V
V_{OL}	LOW output voltage XOUT		HIGH POWER	I_{OL} = 0.1mA			0.5	V
			LOW POWER	I_{OL} = 50µA			0.5	
	LOW output voltage XCOUT		HIGH POWER	With no load applied		0		V
			LOW POWER	With no load applied		0		
V_{T+}-V_{T-}	Hysteresis	TA0IN to TA4IN, TB0IN to TB2IN, $\overline{INT0}$ to $\overline{INT5}$, $\overline{NMI}$, $\overline{ADTRG}$, $\overline{CTS0}$ to $\overline{CTS3}$, SCL2, SDA2, CLK0 to CLK4, TA0OUT to TA4OUT, $\overline{KI0}$ to $\overline{KI3}$, RXD0 to RXD4, ZP, IDU, IDW, IDV, SD, INPC1_0 to INPC1_7, CRX0					0.4V_{CC}	V
V_{T+}-V_{T-}	Hysteresis	$\overline{RESET}$					1.8	V
V_{T+}-V_{T-}	Hysteresis	XIN					0.8	V
I_{IH}	HIGH input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 3V			4.0	µA
I_{IL}	LOW input current	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7 XIN, $\overline{RESET}$, CNVSS		V_I = 0V			−4.0	µA
R_{PULLUP}	Pull-up resistance	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P6_0 to P6_7, P7_0 to P7_7, P8_0 to P8_7, P9_0 to P9_3, P9_5 to P9_7, P10_0 to P10_7		V_I = 0V	50	100	500	kΩ
R_{fXIN}	Feedback resistance XIN					3.0		MΩ
R_{fXCIN}	Feedback resistance XCIN					25		MΩ
V_{RAM}	RAM retention voltage			At stop mode	2.0			V

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V_{CC} = 3 V

Table 5.30 Electrical Characteristics (2)

Topr = –40°C to 85°C unless otherwise specified.

Symbol	Parameter	Measuring Condition		Standard			Unit
				Min.	Typ.	Max.	
I_{CC}	Power supply current (V_{CC} = 3.0 V to 3.6 V) In single-chip mode, the output pins are open and other pins are VSS	High speed mode	$f_{(BCLK)}$ = 25 MHz, XIN = 8 MHz (square wave), PLL multiply-by-8 125 kHz on-chip oscillator operates		26	40	mA
			$f_{(BCLK)}$ = 20 MHz, XIN = 20 MHz (square wave), 125 kHz on-chip oscillator operates		19	28	mA
			$f_{(BCLK)}$ = 16 MHz, XIN = 16 MHz (square wave), 125 kHz on-chip oscillator operates		15		mA
		125 kHz on-chip oscillator mode	Main clock stops 125 kHz on-chip oscillator operates Divide-by-8 FMR22 = FMR23 = 1 (Low-current consumption read mode)		150	500	µA
		Low power mode	$f_{(BCLK)}$ = 32 kHz On Flash memory (1) FMR22 = FMR23 = 1 (Low-current consumption read mode)		160		µA
		Wait mode	Main clock stops 125 kHz on-chip oscillator operates Peripheral clock operates Topr = 25°C		20		µA
			Main clock stops 125 kHz on-chip oscillator operates Peripheral clock operates T_{opr} = 85°C		50		µA
		Stop mode	T_{opr} = 25°C		17	27	µA
			T_{opr} = 85°C		45		µA
		During flash memory program	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		20.0		mA
		During flash memory erase	$f_{(BCLK)}$ = 10 MHz, PM17 = 1 (one wait) V_{CC} = 3.0 V		30.0		mA
I_{det2}	Low voltage detection dissipation current				3		µA
I_{det0}	Reset area detection dissipation current				6		µA

Note:

1. This indicates the memory in which the program to be executed exists.

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V_{CC} = 3 V

5.3.2 Timing Requirements (Peripheral Functions and Others)

(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = -40°C to 85°C unless otherwise specified)

5.3.2.1 Reset Input ($\overline{\text{RESET}}$ Input)

Table 5.31 Reset Input ($\overline{\text{RESET}}$ Input)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(RSTL)}$	$\overline{\text{RESET}}$ input low pulse width	10		µs

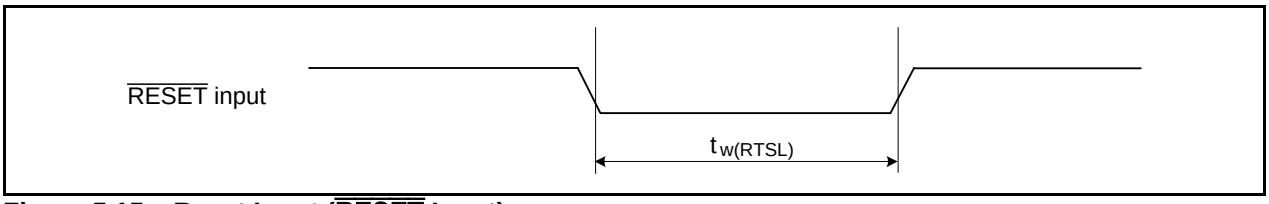


Figure 5.15 Reset Input ($\overline{\text{RESET}}$ Input)

5.3.2.2 External Clock Input

Table 5.32 External Clock Input (XIN input) (1)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External clock input cycle time	50		ns
$t_{w(H)}$	External clock input high pulse width	20		ns
$t_{w(L)}$	External clock input low pulse width	20		ns
t_r	External clock rise time		9	ns
t_f	External clock fall time		9	ns

Note:
1. The condition is V_{CC} = 2.7V to 3.0V.

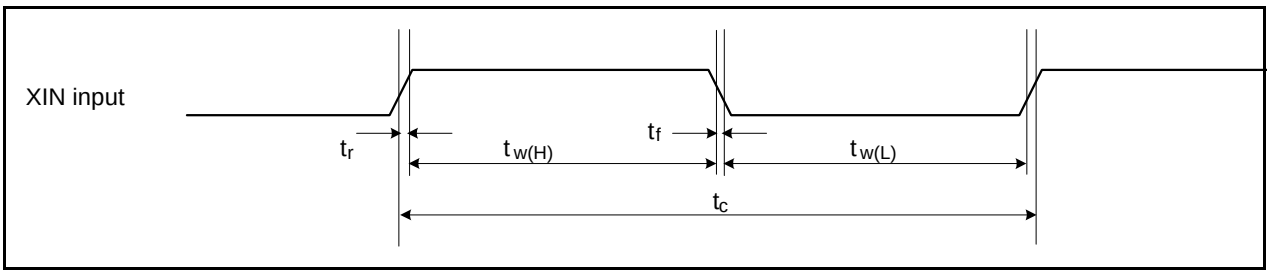


Figure 5.16 External Clock Input (XIN Input)

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V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.3.2.3 Timer A Input

Table 5.33 Timer A Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	150		ns
$t_{w(TAH)}$	TAiIN input high pulse width	60		ns
$t_{w(TAL)}$	TAiIN input low pulse width	60		ns

Table 5.34 Timer A Input (Gating Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	600		ns
$t_{w(TAH)}$	TAiIN input high pulse width	300		ns
$t_{w(TAL)}$	TAiIN input low pulse width	300		ns

Table 5.35 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	300		ns
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

Table 5.36 Timer A Input (External Trigger Input in PWM Mode and Programmable Output Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN input high pulse width	150		ns
$t_{w(TAL)}$	TAiIN input low pulse width	150		ns

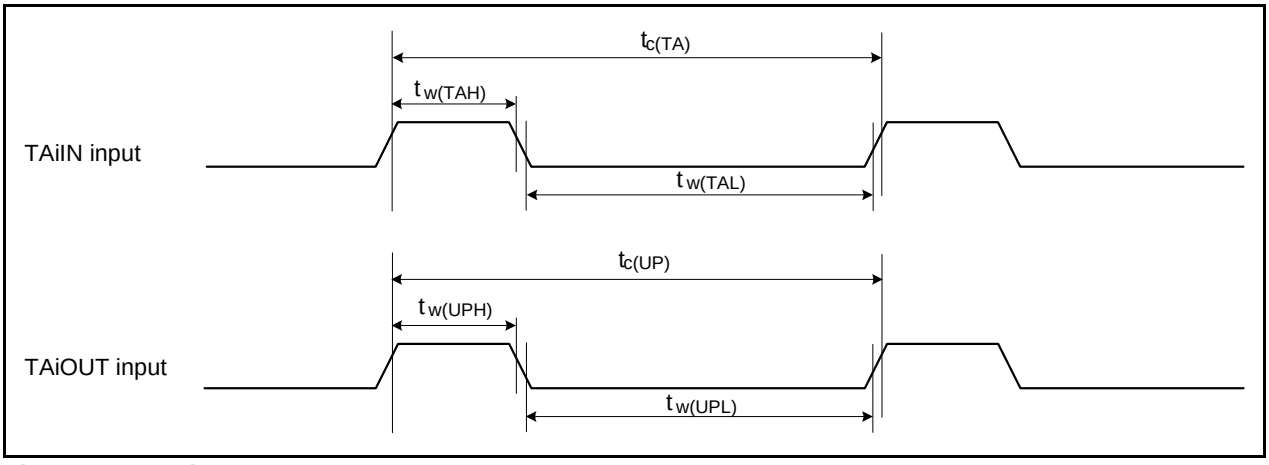


Figure 5.17 Timer A Input

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V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

Table 5.37 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN input cycle time	2		µs
$t_{su(TAIN-TAOUT)}$	TAiOUT input setup time	500		ns
$t_{su(TAOUT-TAIN)}$	TAiIN input setup time	500		ns

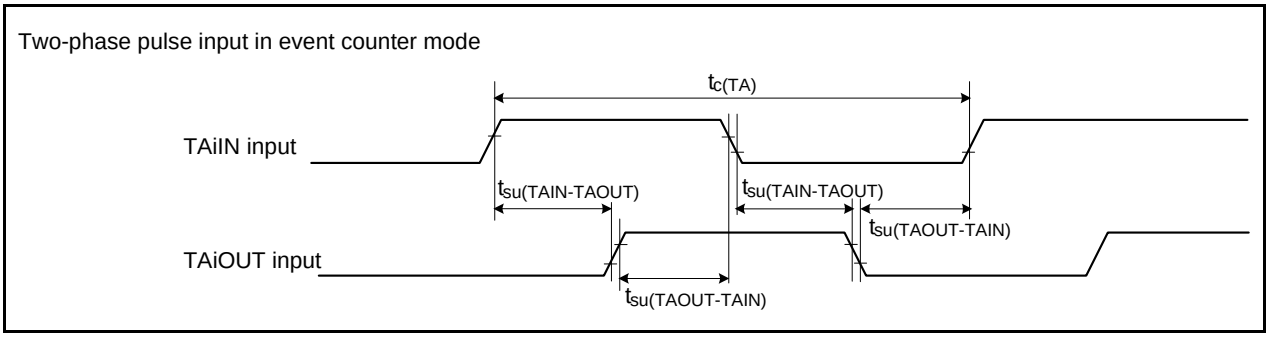


Figure 5.18 Timer A Input (Two-Phase Pulse Input in Event Counter Mode)

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V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.3.2.4 Timer B Input

Table 5.38 Timer B Input (Counter Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time (counted on one edge)	150		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on one edge)	60		ns
$t_{w(TBL)}$	TBiIN input low pulse width (counted on one edge)	60		ns
$t_{c(TB)}$	TBiIN input cycle time (counted on both edges)	300		ns
$t_{w(TBH)}$	TBiIN input high pulse width (counted on both edges)	120		ns
$t_{w(TBL)}$	TBiIN Input low pulse width (counted on both edges)	120		ns

Table 5.39 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

Table 5.40 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN input cycle time	600		ns
$t_{w(TBH)}$	TBiIN input high pulse width	300		ns
$t_{w(TBL)}$	TBiIN input low pulse width	300		ns

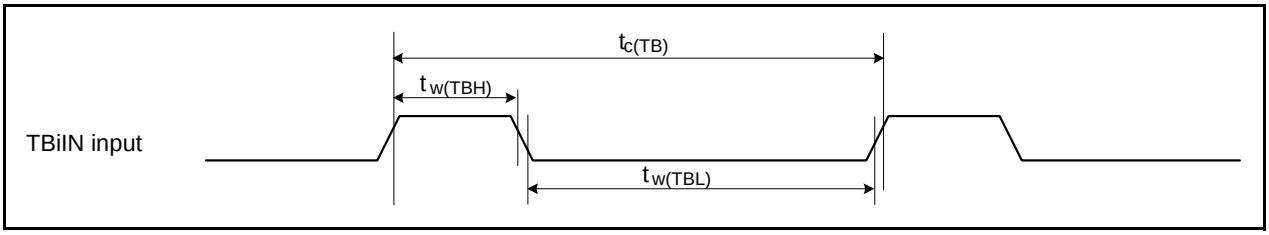


Figure 5.19 Timer B Input

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V_{CC} = 3 V

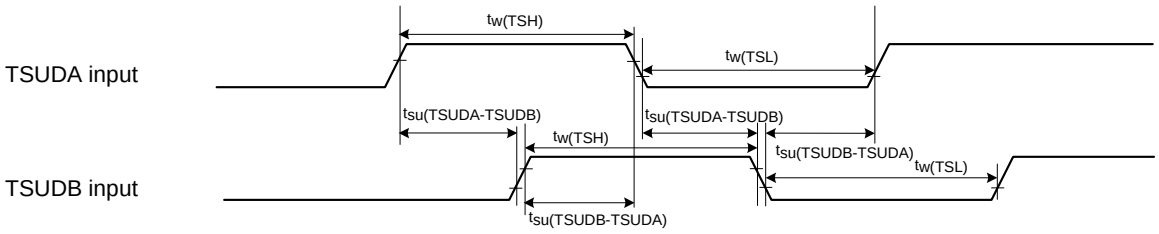
Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.3.2.5 Timer S Input

Table 5.41 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TSH)}$	TSUDA, TSUDB input high pulse width	2		µs
$t_{w(TSL)}$	TSUDA, TSUDB input low pulse width	2		µs
$t_{su(TSUDA-TSUDB)}$	TSUDB input setup time	1		µs
$t_{su(TSUDB-TSUDA)}$	TSUDA input setup time	1		µs

Two-phase pulse input in two-phase pulse signal processing mode



Note:
1. When the TSUDA and TSUDB phases are interchanged, $t_{su(TSUDA-TSUDB)}$ and $t_{su(TSUDB-TSUDA)}$ are also interchanged.

Figure 5.20 Timer S Input (Two-Phase Pulse Input in Two-Phase Pulse Signal Processing Mode)

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V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.3.2.6 Serial Interface

Table 5.42 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300		ns
$t_{w(CKH)}$	CLKi input high pulse width	150		ns
$t_{w(CKL)}$	CLKi input low pulse width	150		ns
$t_{d(C-Q)}$	TXDi output delay time		160	ns
$t_{h(C-Q)}$	TXDi hold time	0		ns
$t_{su(D-C)}$	RXDi input setup time	100		ns
$t_{h(C-D)}$	RXDi input hold time	90		ns

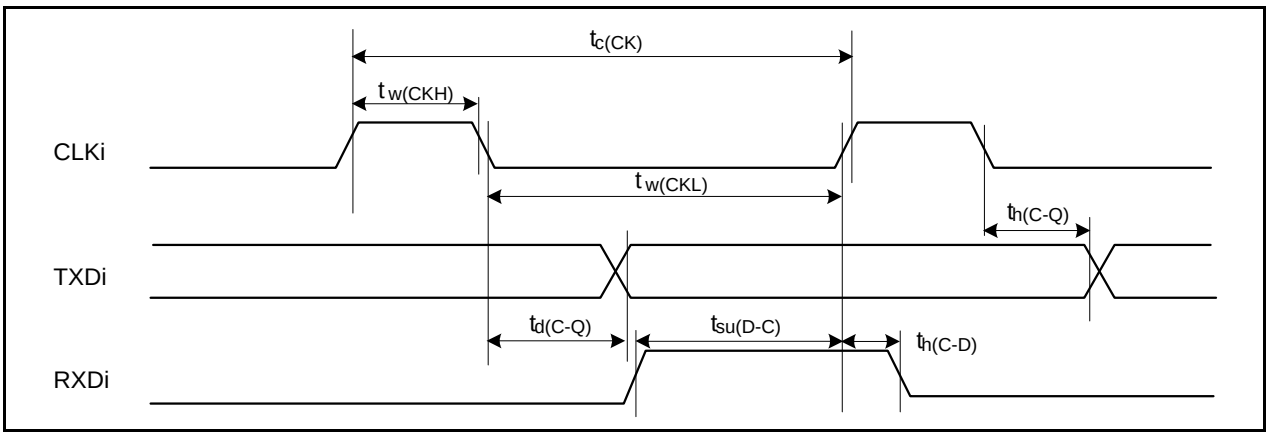


Figure 5.21 Serial Interface

5.3.2.7 External Interrupt $\overline{INTi}$ Input

Table 5.43 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ input high pulse width	380		ns
$t_{w(INL)}$	$\overline{INTi}$ input low pulse width	380		ns

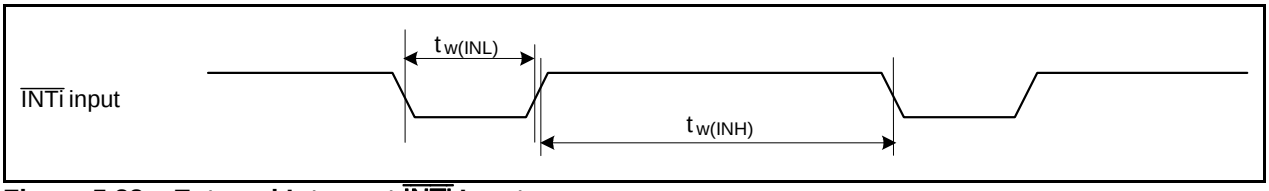


Figure 5.22 External Interrupt $\overline{INTi}$ Input

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V_{CC} = 3 V

Timing Requirements
(V_{CC} = 3 V, V_{SS} = 0 V, at T_{opr} = –40°C to 85°C unless otherwise specified)

5.3.2.8 Multi-master I²C-bus

Table 5.44 Multi-master I²C-bus

Symbol	Parameter	Standard Clock Mode		Fast-mode		Unit
		Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	4.7		1.3		µs
$t_{HD;STA}$	Hold time in start condition	4.0		0.6		µs
t_{LOW}	Hold time in SCL clock 0 status	4.7		1.3		µs
t_R	SCL, SDA signals' rising time		1000	20 + 0.1 Cb	300	ns
$t_{HD;DAT}$	Data hold time	0		0	0.9	µs
t_{HIGH}	Hold time in SCL clock 1 status	4.0		0.6		µs
f_F	SCL, SDA signals' falling time		300	20 + 0.1 Cb	300	ns
$t_{su;DAT}$	Data setup time	250		100		ns
$t_{su;STA}$	Setup time in restart condition	4.7		0.6		µs
$t_{su;STO}$	Stop condition setup time	4.0		0.6		µs

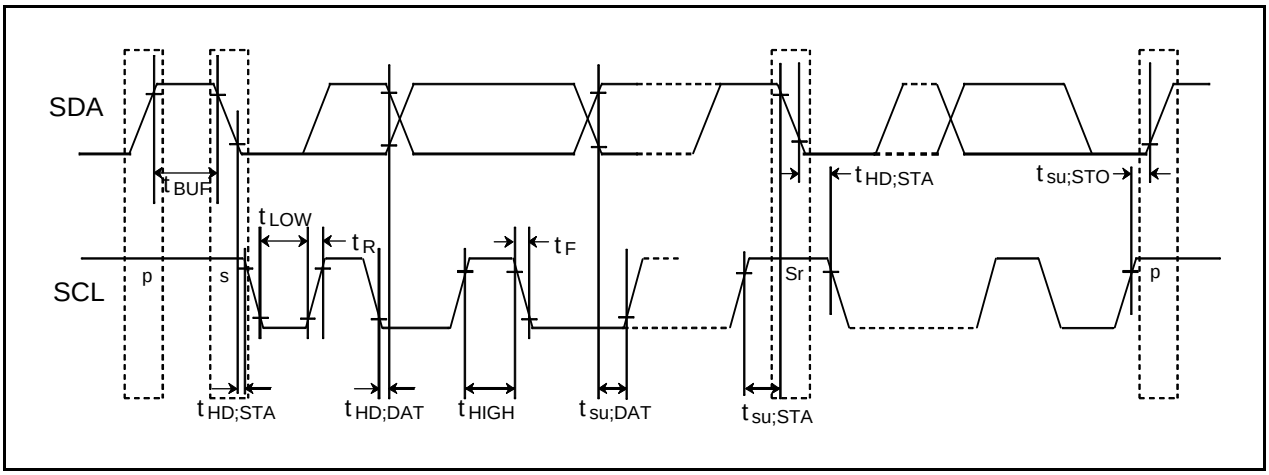


Figure 5.23 Multi-master I²C-bus

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REVISION HISTORY	M16C/5LD Group, M16C/56D Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.10	Dec.01, 2009	—	First edition issued
1.20	Nov. 25, 2011	Overall	Specified Renesas Electronics sales office as a contact.
		Overall	Modified register names are as follows: • 0075h “CAN0 Receive Completion Interrupt Control Register” to “CAN0 Reception Complete Interrupt Control Register” • 0076h “CAN0 Transmit Completion Interrupt Control Register” to “CAN0 Transmission Complete Interrupt Control Register” • 0071h “CAN0 Wakeup Interrupt Control Register” to “CAN0 Wake-up Interrupt Control Register” • 037Ch “Count Source Protect Mode Register” to “Count Source Protection Mode Register”
		Overall	Changed terminologies are as follows: • “voltage detector 2” to “voltage monitor 2” • “oscillation stop detection reset” to “oscillator stop detect reset” • “detection circuit” to “detector” • “Oscillation stop and re-oscillation detect” to “Oscillator stop/restart detect” • “oscillation/oscillator circuit” to “oscillator” • “oscillator” to “a crystal/ceramic resonator” • “oscillator manufacturer” to “manufacturer of crystal/ceramic resonator” • “on-chip oscillator oscillation circuit” to “on-chip oscillator”
		Overview	
		3, 5	Table 1.2, Table 1.4 Specifications (2/2) (80-pin, 64-pin): Added the Current Consumption row, and added note 1.
		8, 9	Figure 1.3, Figure 1.4 Block Diagram (80-pin, 64-pin): • Deleted “8-bit” from the description for the UART/clock synchronous serial interface. • Deleted “(8-bit x 1 channel)” from the description for the Real-time clock. • Added “(1 channel)” to the description for the Multi-master I^2C-bus. • Moved “dedicated 125 kHz on-chip oscillator for the watchdog timer” to description for the watchdog timer.
		10, 13	Figure 1.5, Figure 1.6 Pin Assignments (80-pin, 64-pin): Added TSUDA and TSUDB to pins P8_0 and P8_1, respectively.
		11, 14	Table 1.7, Table 1.9 Pin Names (1/2) (80-pin, 64-pin): Added TSUDA and TSUDB to pins P8_0 and P8_1, respectively.
		16	Table 1.11 Pin Functions (64-Pin and 80-Pin Packages) (1/2): • Deleted “pin” or “pins” from “input pin/pins” and “output pin/pins”. • Changed “low active input” to “input”. • Added “Pins” to “AVCC and AVSS” in the Description column of the Analog power supply row. • Deleted “Low active input pin.” from the Reset input row. • Changed the description in the Description column of the CNVSS row. • Added footnote reference number (1) in the Sub clock input and output rows in the Description column. • Deleted “INT2 is used to input Z-phase of timer A” in the Description column of the $\overline{\text{INT}}$ interrupt input row. • Added UART0 to UART3 in the Signal Name column of the Serial interface row. • Added UART2 to the Signal Name column of the I^2C mode row.
		17	Table 1.12 Pin Functions (64-Pin and 80-Pin Packages) (2/2): • Deleted “pin” or “pins” from “input pin/pins” and “output pin/pins”. • Changed “low active input” to “input”. • Added “TSUDA, TSUDB” to the Pin Name in the Timer S row. • Changed “Input pin” to “Receive data input” and “Output pin” to “Transmit data output” in the Description column of the CAN Module row. • In the Description column of the I/O port row, changed the explanation of the direction register, and changed “4 input ports” to “4 bits”.

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REVISION HISTORY	M16C/5LD Group, M16C/56D Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.20	Nov. 25, 2011	18	Table 1.13 Pin Functions (80-Pin Package Only): • Deleted “pin” or “pins” from “input pin/pins” and “output pin/pins”. • Added UART4 to the Signal Name column of the Serial interface row. • In the Description column of the I/O port row, changed the explanation of the direction register, and changed “4 input ports” to “4 bits”.
		Memory	
		23	Figure 3.1 Memory Map: • Added note 2. • Added footnote reference numbers (1) and (2).
		Special Function Registers (SFRs)	
		56	4.2.1 Register Settings: Added the description regarding read-modify-write instructions.
		57	Table 4.34 Read-Modify-Write Instructions: Added.
		Electrical Characteristics	
		Chap. 5.	Specified symbols for the following pins according to the change in Timer S. • P8_0, P8_0 (A-phase) to TSUDA • P8_1, P8_1 (B-phase) to TSUDB
		Common to 3 V and 5 V	
		58	Table 5.1 Absolute Maximum Ratings: Deleted VREF from the V_I.
		59	Table 5.2 Operating Conditions (1): • Changed the minimum value of V_{CC} from “3.0”. • Changed the maximum value of $I_{OH(sum)}$ from “80”. • Changed the maximum value of $I_{OL(sum)}$ from “-80.”
		61	Table 5.4 A/D Conversion Characteristics $^{(1, 3)}$: Changed note 3.
		64	Table 5.9 Voltage Detector 2 Electrical Characteristics: Added Vdet2_0 to Vdet2_3, and Vdet2_5 to Vdet2_7.
		65	Table 5.11 Power Supply Circuit Timing Characteristics: Changed the maximum value of td(W-S) from “150”.
		66	Figure 5.5 Power Supply Circuit Timing Diagram: Changed “Low voltage detection circuit” to “Voltage detection circuit”
		66	Table 5.12 125kHz On-Chip Oscillator Electrical Characteristics: Added the Dedicated 125 kHz on-chip oscillator for the watchdog timer oscillation frequency.
		Vcc = 5 V	
		67	Table 5.13 Electrical Characteristics (1): Changed the maximum value of V_T+-V_{T-}, which includes TA0IN and others in Hysteresis, from “2.5”.
		73	5.2.2.5 Timer S Input: Added.
		75	Figure 5.14 Multi-master I^2C-bus: Changed t_{HD};DTA to t_{HD};DAT and t_{su};DTA to t_{su};DAT.
		Vcc = 3 V	
		76	Table 5.29 Electrical Characteristics (1): Changed the maximum value of V_T+-V_{T-}, which includes TA0IN and others in Hysteresis, from “1.8”.
		82	5.3.2.5 Timer S Input: Added.
		84	Figure 5.23 Multi-master I^2C-bus: Changed t_{HD};DTA to t_{HD};DAT and t_{su};DTA to t_{su};DAT.

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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