

## FEATURES

- SPI interface with error detection**
- Includes CRC, invalid read/write address, and SCLK count error detection**
- Supports burst mode and daisy-chain mode**
- Industry-standard SPI Mode 0 and Mode 3 interface compatible**
- Guaranteed break-before-make switching allowing external wiring of switches to deliver multiplexer configurations**
- $1.5\ \Omega$  typical on resistance at  $25^\circ\text{C}$**
- $0.3\ \Omega$  typical on resistance flatness at  $25^\circ\text{C}$**
- $0.1\ \Omega$  typical on resistance match between channels at  $25^\circ\text{C}$**
- $V_{SS}$  to  $V_{DD}$  analog signal range**
- Fully specified at  $\pm 15\text{ V}$ ,  $\pm 5\text{ V}$ , and  $+12\text{ V}$**
- $1.8\text{ V}$  logic compatibility with  $2.7\text{ V} \leq V_L \leq 3.3\text{ V}$**
- 24-lead LFCSP**

## APPLICATIONS

- Automated test equipment**
- Data acquisition systems**
- Battery-powered systems**
- Sample-and-hold systems**
- Audio signal routing**
- Video signal routing**
- Communications systems**
- Relay replacement**

## GENERAL DESCRIPTION

The **ADGS1412** contains four independent single-pole/single-throw (SPST) switches. A serial peripheral interface (SPI) controls the switches. The SPI interface has robust error detection features such as cyclic redundancy check (CRC) error detection, invalid read/write address detection, and SCLK count error detection.

It is possible to daisy-chain multiple **ADGS1412** devices together. Daisy-chain mode enables the configuration of multiple devices with a minimal amount of digital lines. The **ADGS1412** can also operate in burst mode to decrease the time between SPI commands.

iCMOS construction ensures ultralow power dissipation, making the device ideally suited for portable and battery-powered instruments.

Each switch conducts equally well in both directions when on, and each switch has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked.

## FUNCTIONAL BLOCK DIAGRAM

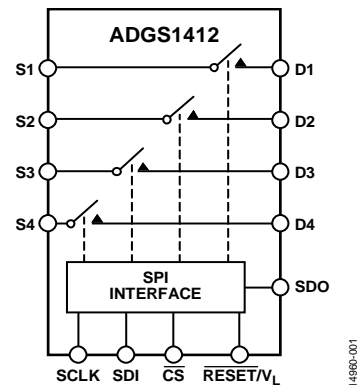


Figure 1.

The on-resistance profile is flat over the full analog input range, which ensures good linearity and low distortion when switching audio signals.

## PRODUCT HIGHLIGHTS

1. SPI interface removes the need for parallel conversion, logic traces and reduces general-purpose input/output (GPIO) channel count.
2. Daisy-chain mode removes additional logic traces when multiple devices are used.
3. CRC error detection, invalid read/write address detection, and SCLK count error detection ensures a robust digital interface.
4. CRC and error detection capabilities allow the use of the **ADGS1412** in safety critical systems.
5. Guaranteed break-before-make switching allows the use of the **ADGS1412** in multiplexer configurations with external wiring.
6. Minimum distortion.

Rev. B

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## REVISION HISTORY

### 8/2017—Rev. A to Rev. B

Changes to Product Title, Features Section, and Product Highlights Section .....	1
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### 3/2017—Rev. 0 to Rev. A

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Change to $V_{DD} = 15\text{ V}$ , $V_{SS} = -15\text{ V}$ ( $\theta_{JA} = 54^\circ\text{C/W}$ ) Parameter, Table 5 .....	7
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### 10/2016—Revision 0: Initial Version

## SPECIFICATIONS

## ±15 V DUAL SUPPLY

$V_{DD} = +15\text{ V} \pm 10\%$ ,  $V_{SS} = -15\text{ V} \pm 10\%$ ,  $V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ , and  $GND = 0\text{ V}$ , unless otherwise noted.

Table 1.

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V <sub>DD</sub> to V <sub>SS</sub>	V	V <sub>S</sub> = ±10 V, I <sub>S</sub> = −10 mA, see Figure 29 V <sub>DD</sub> = +13.5 V, V <sub>SS</sub> = −13.5 V V <sub>S</sub> = ±10 V, I <sub>S</sub> = −10 mA
On Resistance, R <sub>ON</sub>	1.5 1.8	2.3	2.6	Ω typ Ω max	
On-Resistance Match Between Channels, ΔR <sub>ON</sub>	0.1			Ω typ	
On-Resistance Flatness, R <sub>FLAT (ON)</sub>	0.18	0.19	0.21	Ω max	V <sub>S</sub> = ±10 V, I <sub>S</sub> = −10 mA
	0.3			Ω typ	
	0.36	0.4	0.45	Ω max	
LEAKAGE CURRENTS					
Source Off Leakage, I <sub>S</sub> (Off)	±0.03 ±0.55	±2	±12.5	nA typ nA max	V <sub>DD</sub> = +16.5 V, V <sub>SS</sub> = −16.5 V V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓ 10 V, see Figure 32
Drain Off Leakage, I <sub>D</sub> (Off)	±0.03 ±0.55	±2	±12.5	nA typ nA max	V <sub>S</sub> = ±10 V, V <sub>D</sub> = ∓ 10 V, see Figure 32
Channel On Leakage, I <sub>D</sub> (On), I <sub>S</sub> (On)	±0.15 ±2	±4	±30	nA typ nA max	V <sub>S</sub> = V <sub>D</sub> = ±10 V, see Figure 28
DIGITAL OUTPUT					
Output Voltage Low, V <sub>OL</sub>			0.4 0.2	V max V max	I <sub>SINK</sub> = 5 mA I <sub>SINK</sub> = 1 mA Output voltage (V <sub>OUT</sub> ) = ground voltage (V <sub>GND</sub> ) or V <sub>L</sub>
High Impedance Leakage Current	0.001		±0.1	μA typ μA max	
High Impedance Output Capacitance	4			pF typ	
DIGITAL INPUTS					
Input Voltage High, V <sub>INH</sub>			2 1.35	V min V min	3.3 V < V <sub>L</sub> ≤ 5.5 V 2.7 V ≤ V <sub>L</sub> ≤ 3.3 V 3.3 V < V <sub>L</sub> ≤ 5.5 V 2.7 V ≤ V <sub>L</sub> ≤ 3.3 V
Low, V <sub>INL</sub>			0.8 0.8	V max V max	
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	0.001		±0.1	μA typ μA max	
Digital Input Capacitance, C <sub>IN</sub>	4			pF typ	V <sub>IN</sub> = V <sub>GND</sub> or V <sub>L</sub>
DYNAMIC CHARACTERISTICS <sup>1</sup>					
t <sub>ON</sub>	400			ns typ	Load resistance (R <sub>L</sub> ) = 300 Ω, load capacitance (C <sub>L</sub> ) = 35 pF
t <sub>OFF</sub>	475 160	480	485	ns max ns typ	V <sub>S</sub> = 10 V, see Figure 37 R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
	190	210	225	ns max	V <sub>S</sub> = 10 V, see Figure 37
	215			ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF
Break-Before-Make Time Delay, t <sub>D</sub>			170	ns min	V <sub>S1</sub> = V <sub>S2</sub> = 10 V, see Figure 36
Charge Injection, Q <sub>INJ</sub>	−20			pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF, see Figure 38
Off Isolation	−76			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 31
Channel to Channel Crosstalk	−100			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 30
Total Harmonic Distortion + Noise	0.014			% typ	R <sub>L</sub> = 110 Ω, 15 V p-p, f = 20 Hz to 20 kHz, see Figure 33

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
–3 dB Bandwidth	170			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , see Figure 34
Insertion Loss	–0.2			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\ \text{pF}$ , $f = 1\ \text{MHz}$ , see Figure 34
$C_S$ (Off)	22			pF typ	$V_S = 0\ \text{V}$ , $f = 1\ \text{MHz}$
$C_D$ (Off)	23			pF typ	$V_S = 0\ \text{V}$ , $f = 1\ \text{MHz}$
$C_D$ (On), $C_S$ (On)	113			pF typ	$V_S = 0\ \text{V}$ , $f = 1\ \text{MHz}$
POWER REQUIREMENTS					
$I_{DD}$	0.001			$\mu\text{A typ}$	$V_{DD} = +16.5\ \text{V}$ , $V_{SS} = -16.5\ \text{V}$ All switches open
			1	$\mu\text{A max}$	
	220			$\mu\text{A typ}$	All switches closed, $V_L = 5.5\ \text{V}$
			380	$\mu\text{A max}$	
	230			$\mu\text{A typ}$	All switches closed, $V_L = 2.7\ \text{V}$
Load current ( $I_L$ )			380	$\mu\text{A max}$	
Inactive	6.3		8.0	$\mu\text{A typ}$	Digital inputs = 0 V or $V_L$
				$\mu\text{A max}$	
Inactive, SCLK = 1 MHz	14			$\mu\text{A typ}$	$\overline{CS} = V_L$ and $SDI = 0\ \text{V}$ or $V_L$ , $V_L = 5\ \text{V}$
	7			$\mu\text{A typ}$	$\overline{CS} = V_L$ and $SDI = 0\ \text{V}$ or $V_L$ , $V_L = 3\ \text{V}$
SCLK = 50 MHz	390			$\mu\text{A typ}$	$\overline{CS} = V_L$ and $SDI = 0\ \text{V}$ or $V_L$ , $V_L = 5\ \text{V}$
	210			$\mu\text{A typ}$	$\overline{CS} = V_L$ and $SDI = 0\ \text{V}$ or $V_L$ , $V_L = 3\ \text{V}$
Inactive, SDI = 1 MHz	15			$\mu\text{A typ}$	$\overline{CS}$ and $SCLK = 0\ \text{V}$ or $V_L$ , $V_L = 5\ \text{V}$
	7.5			$\mu\text{A typ}$	$\overline{CS}$ and $SCLK = 0\ \text{V}$ or $V_L$ , $V_L = 3\ \text{V}$
SDI = 25 MHz	230			$\mu\text{A typ}$	$\overline{CS}$ and $SCLK = 0\ \text{V}$ or $V_L$ , $V_L = 5\ \text{V}$
	120			$\mu\text{A typ}$	$\overline{CS}$ and $SCLK = 0\ \text{V}$ or $V_L$ , $V_L = 3\ \text{V}$
Active at 50 MHz	1.8			$\text{mA typ}$	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5\ \text{V}$
		2	2.1	$\text{mA max}$	
	0.7			$\text{mA typ}$	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7\ \text{V}$
			1.0	$\text{mA max}$	
$I_{SS}$	0.001			$\mu\text{A typ}$	Digital inputs = 0 V or $V_L$
			1.0	$\mu\text{A max}$	
$V_{DD}/V_{SS}$			$\pm 4.5/\pm 16.5$	V min/ V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**±5 V DUAL SUPPLY**

$V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ , and  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 2.**

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			$V_{DD}$ to $V_{SS}$	V	
On Resistance, $R_{ON}$	3.3 4	4.9	5.4	$\Omega$ typ $\Omega$ max	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ , see Figure 29 $V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$
On-Resistance Match Between Channels, $\Delta R_{ON}$	0.13			$\Omega$ typ	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness, $R_{FLAT(ON)}$	0.22	0.23	0.25	$\Omega$ max	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
	0.9			$\Omega$ typ	
	1.1	1.24	1.31	$\Omega$ max	
LEAKAGE CURRENTS					
Source Off Leakage, $I_S$ (Off)	$\pm 0.03$ $\pm 0.55$	$\pm 2$	$\pm 12.5$	nA typ nA max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ , see Figure 32
Drain Off Leakage, $I_D$ (Off)	$\pm 0.03$ $\pm 0.55$	$\pm 2$	$\pm 12.5$	nA typ nA max	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ , see Figure 32
Channel On Leakage, $I_D$ (On), $I_S$ (On)	$\pm 0.05$ $\pm 1.0$	$\pm 4$	$\pm 30$	nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$ , see Figure 28
DIGITAL OUTPUT					
Output Voltage Low, $V_{OL}$			0.4 0.2	V max V max	$I_{SINK} = 5\text{ mA}$ $I_{SINK} = 1\text{ mA}$
High Impedance Leakage Current	0.001		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{OUT} = V_{GND}$ or $V_L$
High Impedance Output Capacitance	4			pF typ	
DIGITAL INPUTS					
Input Voltage High, $V_{INH}$			2 1.35	V min V min	$3.3\text{ V} < V_L \leq 5.5\text{ V}$ $2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Low, $V_{INL}$			0.8 0.8	V max V max	$3.3\text{ V} < V_L \leq 5.5\text{ V}$ $2.7\text{ V} \leq V_L \leq 3.3\text{ V}$
Input Current, $I_{INL}$ or $I_{INH}$	0.001		$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{GND}$ or $V_L$
Digital Input Capacitance, $C_{IN}$	4			pF typ	
DYNAMIC CHARACTERISTICS <sup>1</sup>					
$t_{ON}$	510 645	680	710	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ , see Figure 37
$t_{OFF}$	280 365	400	435	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3\text{ V}$ , see Figure 37
Break-Before-Make Time Delay, $t_D$	245		200	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_{S1} = V_{S2} = 3\text{ V}$ , see Figure 36
Charge Injection, $Q_{INJ}$	10			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , see Figure 38
Off Isolation	–76			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 31
Channel to Channel Crosstalk	–100			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 30
Total Harmonic Distortion + Noise	0.03			% typ	$R_L = 110\ \Omega$ , $5\text{ V p-p}$ , $f = 20\text{ Hz}$ to $20\text{ kHz}$ , see Figure 33
–3 dB Bandwidth	130			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , see Figure 34
Insertion Loss	–0.3			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , see Figure 34
$C_S$ (Off)	32			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (Off)	33			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$
$C_D$ (On), $C_S$ (On)	116			pF typ	$V_S = 0\text{ V}$ , $f = 1\text{ MHz}$

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			μA typ	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$
			1.0	μA max	Digital inputs = 0 V or $V_L$ , $V_L = 5.5\text{ V}$
	14		20	μA typ	All switches closed, $V_L = 2.7\text{ V}$
				μA max	
$I_L$					
Inactive	6.3			μA typ	Digital inputs = 0 V or $V_L$
			8.0	μA max	
Inactive, SCLK = 1 MHz	14			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$
	7			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$
SCLK = 50 MHz	390			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$
	210			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$
Inactive, SDI = 1 MHz	15			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$
	7.5			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$
SDI = 25 MHz	230			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$
	120			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5\text{ V}$
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7\text{ V}$
			1.0	mA max	
$I_{SS}$	0.001			μA typ	Digital inputs = 0 V or $V_L$
			1.0	μA max	
$V_{DD}/V_{SS}$			±4.5/±16.5	V min/ V max	GND = 0 V

<sup>1</sup> Guaranteed by design; not subject to production test.

**12 V SINGLE SUPPLY**

$V_{DD} = 12\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ , and  $GND = 0\text{ V}$ , unless otherwise noted.

**Table 3.**

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments			
ANALOG SWITCH								
Analog Signal Range			0 V to V <sub>DD</sub>	V	V <sub>S</sub> = 0 V to 10 V, I <sub>S</sub> = −10 mA, see Figure 29 V <sub>DD</sub> = 10.8 V, V <sub>SS</sub> = 0 V V <sub>S</sub> = 0 V to 10 V, I <sub>S</sub> = −10 mA			
On Resistance, R <sub>ON</sub>	2.8	4.3	4.8	Ω typ				
	3.5			Ω max				
On-Resistance Match Between Channels, ΔR <sub>ON</sub>	0.13			Ω typ				
On-Resistance Flatness, R <sub>FLAT</sub> (ON)	0.21	0.23	0.25	Ω max	V <sub>S</sub> = 0 V to 10 V, I <sub>S</sub> = −10 mA			
	0.6			Ω typ				
	1.1			Ω max				
LEAKAGE CURRENTS								
Source Off Leakage, I <sub>S</sub> (Off)	±0.02	±2	±12.5	nA typ	V <sub>DD</sub> = 13.2 V, V <sub>SS</sub> = 0 V V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V, see Figure 32			
	±0.55			nA max				
Drain Off Leakage, I <sub>D</sub> (Off)	±0.02	±2	±12.5	nA typ	V <sub>S</sub> = 1 V/10 V, V <sub>D</sub> = 10 V/1 V, see Figure 32			
	±0.55			nA max				
Channel On Leakage, I <sub>D</sub> (On), I <sub>S</sub> (On)	±0.15	±4	±30	nA typ	V <sub>S</sub> = V <sub>D</sub> = 1 V/10 V, see Figure 28			
	±1.5			nA max				
DIGITAL OUTPUT								
Output Voltage Low, V <sub>OL</sub>			0.4	V max	I <sub>SINK</sub> = 5 mA I <sub>SINK</sub> = 1 mA V <sub>OUT</sub> = V <sub>GND</sub> or V <sub>L</sub>			
			0.2	V max				
High Impedance Leakage Current	0.001		±0.1	μA typ				
				μA max				
High Impedance Output Capacitance	4			pF typ				
DIGITAL INPUTS								
Input Voltage High, V <sub>INH</sub>			2	V min	3.3 V < V <sub>L</sub> ≤ 5.5 V 2.7 V ≤ V <sub>L</sub> ≤ 3.3 V 3.3 V < V <sub>L</sub> ≤ 5.5 V 2.7 V ≤ V <sub>L</sub> ≤ 3.3 V V <sub>IN</sub> = V <sub>GND</sub> or V <sub>L</sub>			
			1.35	V min				
Low, V <sub>INL</sub>			0.8	V max				
			0.8	V max				
Input Current, I <sub>INL</sub> or I <sub>INH</sub>	0.001		±0.1	μA typ				
				μA max				
Digital Input Capacitance, C <sub>IN</sub>	4			pF typ				
DYNAMIC CHARACTERISTICS <sup>1</sup>								
t <sub>ON</sub>	470	615	300	ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = 8 V, see Figure 37			
	570			ns max				
t <sub>OFF</sub>	170	240	265	ns typ	R <sub>L</sub> = 300 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = 8 V, see Figure 37			
	215			ns max				
Break-Before-Make Time Delay, t <sub>D</sub>	280			ns typ		225	ns min	V <sub>S1</sub> = V <sub>S2</sub> = 8 V, see Figure 36
				ns min			pC typ	
Charge Injection, Q <sub>INJ</sub>	10			pC typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 31			
Off Isolation	−76			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 30			
Channel to Channel Crosstalk	−100			dB typ	R <sub>L</sub> = 110 Ω, 6 V p-p, f = 20 Hz to 20 kHz, see Figure 33			
Total Harmonic Distortion + Noise	0.06			% typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, see Figure 34			
−3 dB Bandwidth	130			MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, see Figure 34			
Insertion Loss	−0.3			dB typ	V <sub>S</sub> = 6 V, f = 1 MHz			
C <sub>S</sub> (Off)	29			pF typ	V <sub>S</sub> = 6 V, f = 1 MHz			
C <sub>D</sub> (Off)	30			pF typ	V <sub>S</sub> = 6 V, f = 1 MHz			
C <sub>D</sub> (On), C <sub>S</sub> (On)	116			pF typ	V <sub>S</sub> = 6 V, f = 1 MHz			

Parameter	+25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
$I_{DD}$	0.001			μA typ	$V_{DD} = 13.2\text{ V}$ All switches open
			1.0	μA max	
	220			μA typ	All switches closed, $V_L = 5.5\text{ V}$
			380	μA max	
$I_L$	250			μA typ	All switches closed, $V_L = 2.7\text{ V}$
			430	μA max	
Inactive	6.3			μA typ	Digital inputs = 0 V or $V_L$
			8.0	μA max	
Inactive, SCLK = 1 MHz	14			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$
	7			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$
SCLK = 50 MHz	390			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 5\text{ V}$
	210			μA typ	$\overline{CS} = V_L$ and SDI = 0 V or $V_L$ , $V_L = 3\text{ V}$
Inactive, SDI = 1 MHz	15			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$
	7.5			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$
SDI = 25 MHz	230			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 5\text{ V}$
	120			μA typ	$\overline{CS}$ and SCLK = 0 V or $V_L$ , $V_L = 3\text{ V}$
Active at 50 MHz	1.8			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 5.5\text{ V}$
			2.1	mA max	
	0.7			mA typ	Digital inputs toggle between 0 V and $V_L$ , $V_L = 2.7\text{ V}$
			1.0	mA max	
$V_{DD}$			5/20	V min/ V max	GND = 0 V, $V_{SS} = 0\text{ V}$

<sup>1</sup> Guaranteed by design; not subject to production test.



**CONTINUOUS CURRENT PER CHANNEL, Sx OR Dx****Table 4. Four Channels On**

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx <sup>1</sup>				
$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V} (\theta_{JA} = 54^\circ\text{C/W})$	297	165	79	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V} (\theta_{JA} = 54^\circ\text{C/W})$	240	142	74	mA maximum
$V_{DD} = 5\text{ V}, V_{SS} = -5\text{ V} (\theta_{JA} = 54^\circ\text{C/W})$	224	135	72	mA maximum

<sup>1</sup> Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

**Table 5. One Channel On**

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, Sx OR Dx <sup>1</sup>				
$V_{DD} = 15\text{ V}, V_{SS} = -15\text{ V} (\theta_{JA} = 54^\circ\text{C/W})$	531	235	87	mA maximum
$V_{DD} = 12\text{ V}, V_{SS} = 0\text{ V} (\theta_{JA} = 54^\circ\text{C/W})$	433	210	85	mA maximum
$V_{DD} = 5\text{ V}, V_{SS} = -5\text{ V} (\theta_{JA} = 54^\circ\text{C/W})$	404	202	84	mA maximum

<sup>1</sup> Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

**TIMING CHARACTERISTICS**

$V_L = 2.7\text{ V}$  to  $5.5\text{ V}$ ,  $GND = 0\text{ V}$ , and all specifications  $T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted. Guaranteed by design and characterization, not production tested.

**Table 6.**

Parameter	Limit	Unit	Test Conditions/Comments
TIMING CHARACTERISTICS			
$t_1$	20	ns min	SCLK period
$t_2$	8	ns min	SCLK high pulse width
$t_3$	8	ns min	SCLK low pulse width
$t_4$	10	ns min	$\overline{CS}$ falling edge to SCLK active edge
$t_5$	6	ns min	Data setup time
$t_6$	8	ns min	Data hold time
$t_7$	10	ns min	SCLK active edge to $\overline{CS}$ rising edge
$t_8$	20	ns max	$\overline{CS}$ falling edge to SDO data available
$t_9^1$	20	ns max	SCLK falling edge to SDO data available
$t_{10}$	20	ns max	$\overline{CS}$ rising edge to SDO returns to high impedance
$t_{11}$	20	ns min	$\overline{CS}$ high time between SPI commands
$t_{12}$	8	ns min	$\overline{CS}$ falling edge to SCLK becomes stable
$t_{13}$	8	ns min	$\overline{CS}$ rising edge to SCLK becomes stable

<sup>1</sup> Measured with the 1 k $\Omega$  pull-up resistor to  $V_L$  and 20 pF load.  $t_9$  determines the maximum SCLK frequency when SDO is used.

Timing Diagrams

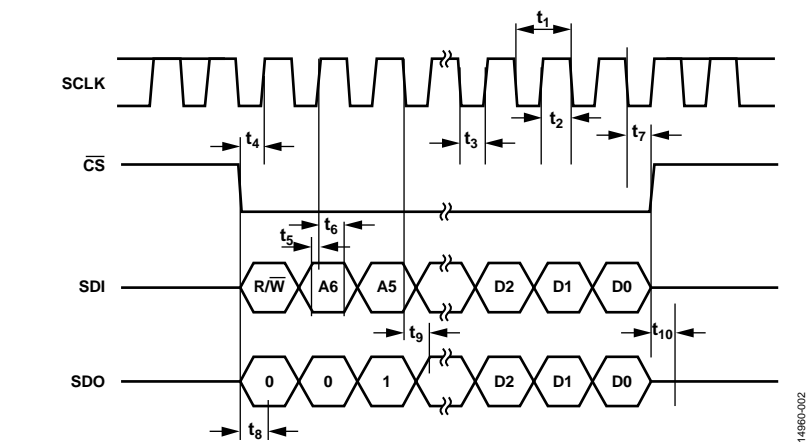


Figure 2. Address Mode Timing Diagram

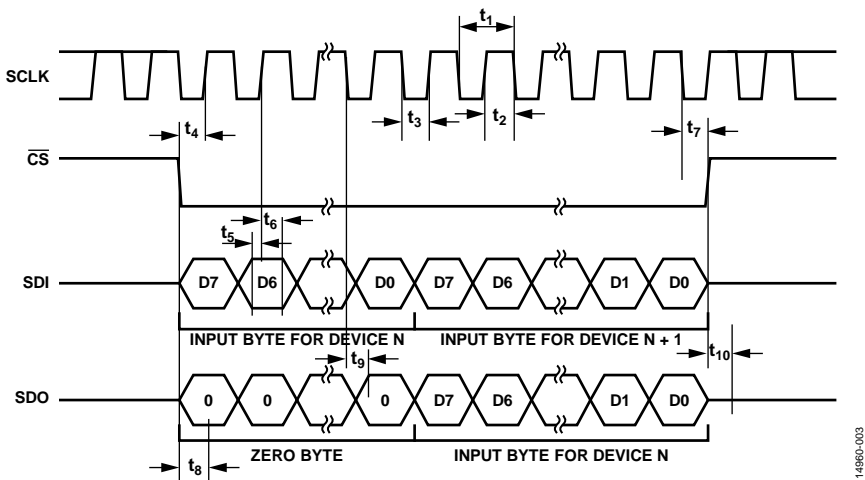


Figure 3. Daisy-Chain Timing Diagram

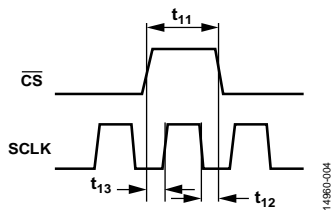


Figure 4. SCLK/ $\overline{CS}$  Timing Relationship

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 7.

Parameter	Rating
$V_{DD}$ to $V_{SS}$	35 V
$V_{DD}$ to GND	−0.3 V to +25 V
$V_{SS}$ to GND	+0.3 V to −25 V
$V_L$ to GND	−0.3 V to +6 V
Analog Inputs <sup>1</sup>	$V_{SS} - 0.3 \text{ V}$ to $V_{DD} + 0.3 \text{ V}$ or 30 mA, whichever occurs first
Digital Inputs <sup>1</sup>	−0.3 V to +6 V
Peak Current, Sx or Dx Pins <sup>2</sup>	600 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, Sx or Dx <sup>2,3</sup>	Data + 15%
Temperature Range	
Operating	−40°C to +125°C
Storage	−65°C to +150°C
Junction Temperature	150°C
Reflow Soldering Peak Temperature, Pb Free	260(+0/−5)°C

<sup>1</sup> Overvoltages at the digital Sx and Dx pins are clamped by internal diodes. Limit current to the maximum ratings given.

<sup>2</sup> Sx refers to the S1 to S4 pins, and Dx refers to the D1 to D4 pins.

<sup>3</sup> See Table 4 and Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Only one absolute maximum rating can be applied at any one time.

### THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 8. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JCB}$ <sup>1</sup>	Unit
CP-24-17 <sup>2</sup>	54	3	°C/W

<sup>1</sup>  $\theta_{JCB}$  is the junction to the bottom of the case value.

<sup>2</sup> Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with four thermal vias. See JEDEC JESD-51.

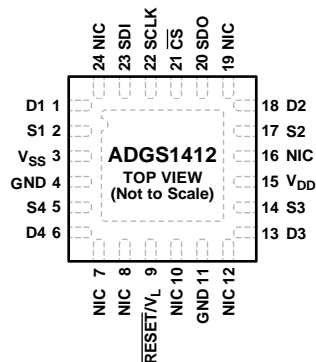
### ESD CAUTION



#### ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



## NOTES

1. NIC = NOT INTERNALLY CONNECTED.
2. THE EXPOSED PAD IS CONNECTED INTERNALLY. FOR INCREASED RELIABILITY OF THE SOLDER JOINTS AND MAXIMUM THERMAL CAPABILITY, IT IS RECOMMENDED THAT THE PAD BE SOLDERED TO THE SUBSTRATE,  $V_{SS}$ .

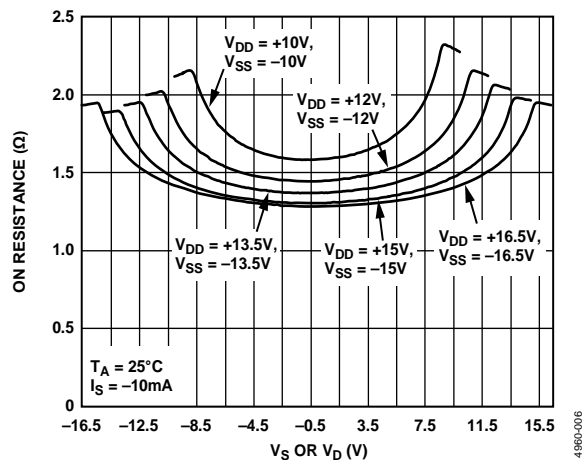
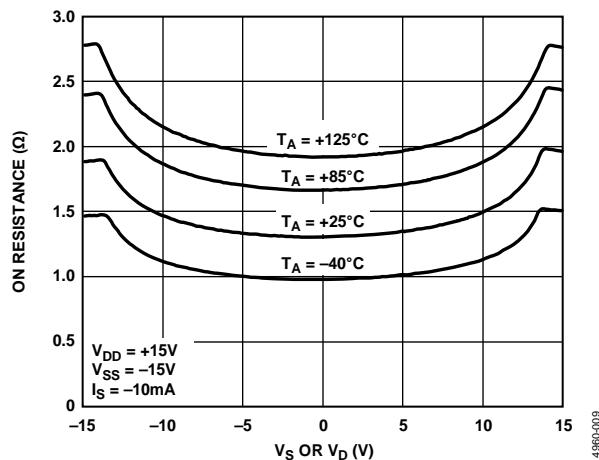
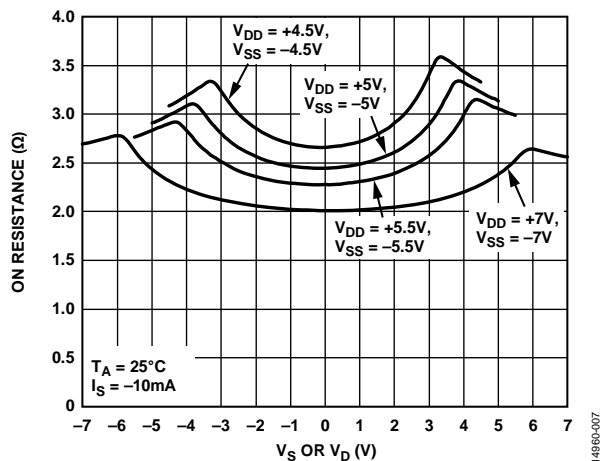
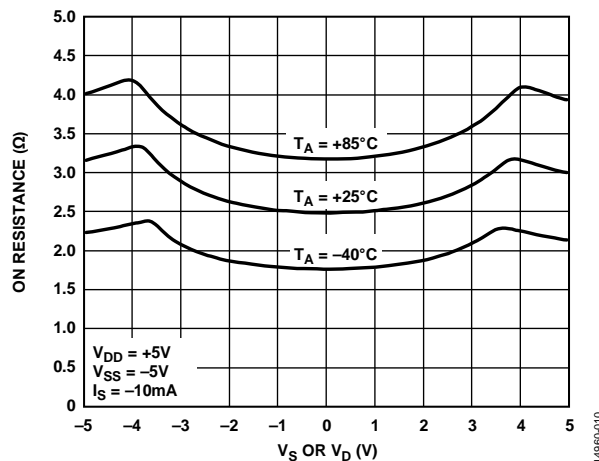
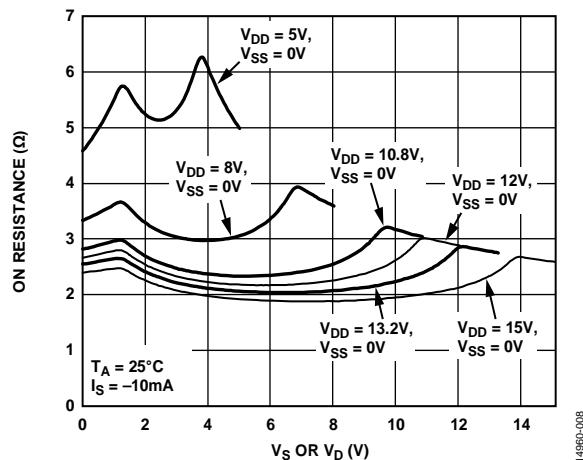
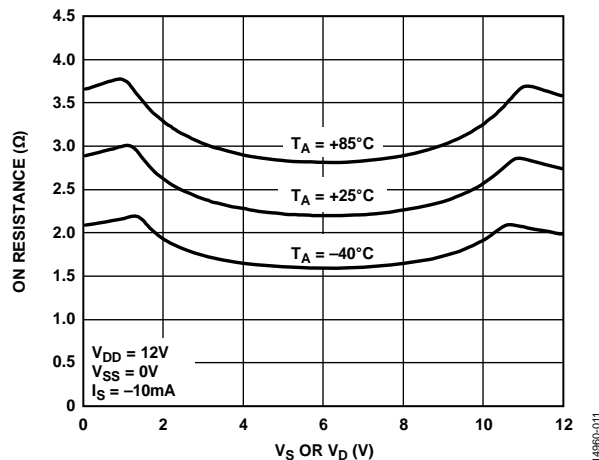
14960-005

Figure 5. Pin Configuration

Table 9. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	D1	Drain Terminal 1. This pin can be an input or output.
2	S1	Source Terminal 1. This pin can be an input or output.
3	$V_{SS}$	Most Negative Power Supply Potential. In single-supply applications, tie this pin to ground.
4, 11	GND	Ground (0 V) Reference.
5	S4	Source Terminal 4. This pin can be an input or output.
6	D4	Drain Terminal 4. This pin can be an input or output.
7, 8, 10, 12, 16, 19, 24	NIC	Not Internally Connected.
9	$\overline{\text{RESET}}/V_L$	$\overline{\text{RESET}}$ /Logic Power Supply Input ( $V_L$ ). Under normal operation, drive the $\overline{\text{RESET}}/V_L$ pin with a 2.7 V to 5.5 V supply. Pull the $\overline{\text{RESET}}$ pin low to complete a hardware reset. After a reset, all switches open, and the appropriate registers are set to their default.
13	D3	Drain Terminal 3. This pin can be an input or output.
14	S3	Source Terminal 3. This pin can be an input or output.
15	$V_{DD}$	Most Positive Power Supply Potential.
17	S2	Source Terminal 2. This pin can be an input or output.
18	D2	Drain Terminal 2. This pin can be an input or output.
20	SDO	Serial Data Output. This pin can be used for daisy chaining a number of these devices together or for reading back the data stored in a register for diagnostic purposes. The serial data is propagated on the falling edge of SCLK. Pull this open-drain output to $V_L$ with an external resistor.
21	$\overline{\text{CS}}$	Active Low Control Input. $\overline{\text{CS}}$ is the frame synchronization signal for the input data.
22	SCLK	Serial Clock Input. Data is captured on the positive edge of SCLK. Data can be transferred at rates of up to 50 MHz.
23	SDI	Serial Data Input. Data is captured on the positive edge of SCLK.
	EPAD	Exposed Pad. The exposed pad is connected internally. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the exposed pad be soldered to the substrate, $V_{SS}$ .

## TYPICAL PERFORMANCE CHARACTERISTICS

Figure 6. On Resistance vs.  $V_S$  or  $V_D$  for Various Dual SuppliesFigure 9. On Resistance vs.  $V_S$  or  $V_D$  for Various Temperatures,  $\pm 15$  V Dual SupplyFigure 7. On Resistance vs.  $V_S$  or  $V_D$  for Various Dual SuppliesFigure 10. On Resistance vs.  $V_S$  or  $V_D$  for Various Temperatures,  $\pm 5$  V Dual SupplyFigure 8. On Resistance vs.  $V_S$  or  $V_D$  for Various Single SuppliesFigure 11. On Resistance vs.  $V_S$  or  $V_D$  for Various Temperatures, 12 V Single Supply

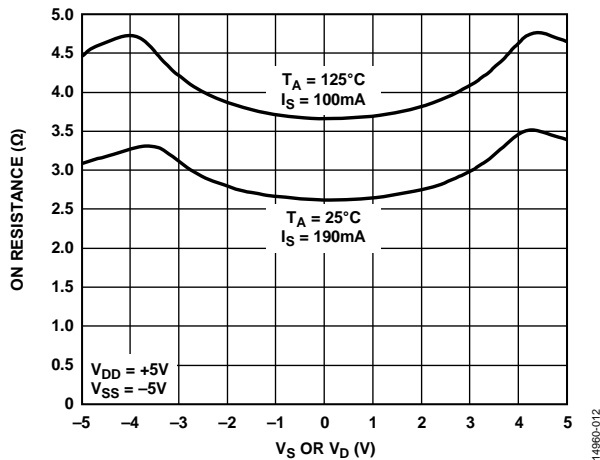


Figure 12. On Resistance vs.  $V_S$  or  $V_D$  for Various Current Levels and Temperatures,  $\pm 5$  V Dual Supply

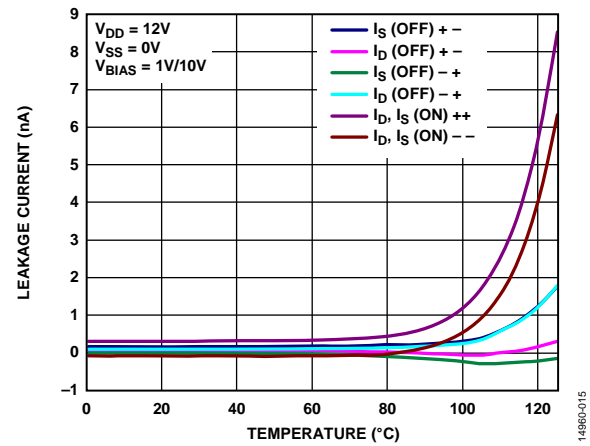


Figure 15. Leakage Current vs. Temperature, 12 V Single Supply

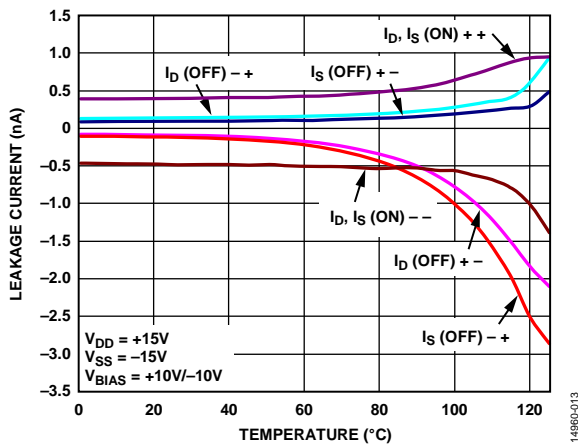


Figure 13. Leakage Current vs. Temperature,  $\pm 15$  V Dual Supply

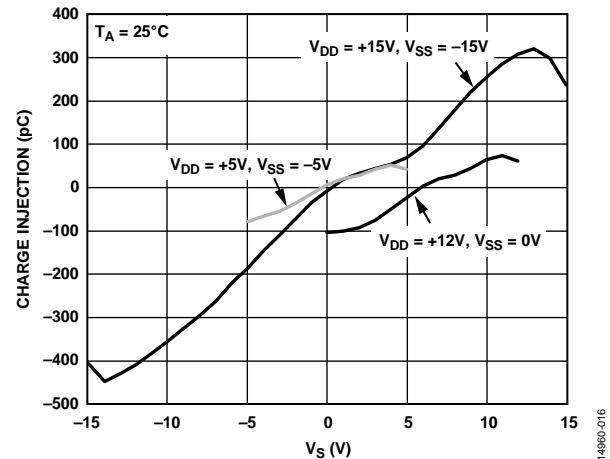


Figure 16. Charge Injection vs. Source Voltage ( $V_S$ )

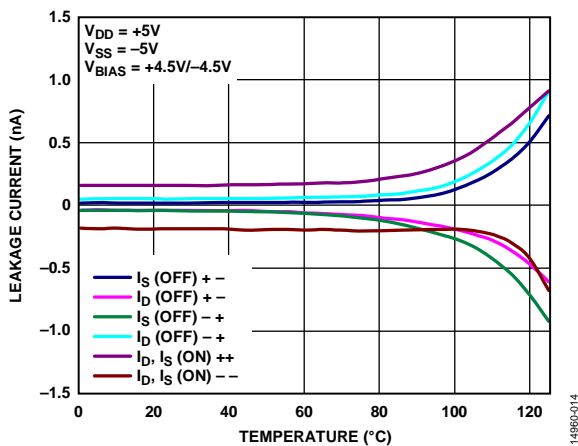


Figure 14. Leakage Current vs. Temperature,  $\pm 5$  V Dual Supply

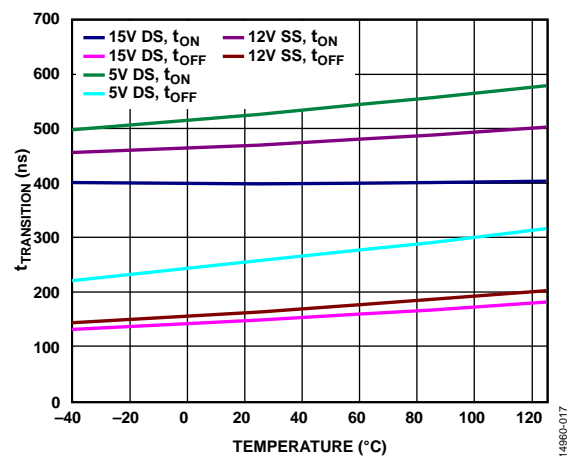
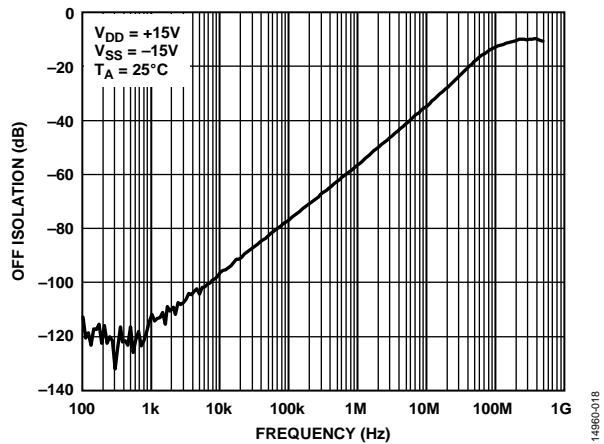
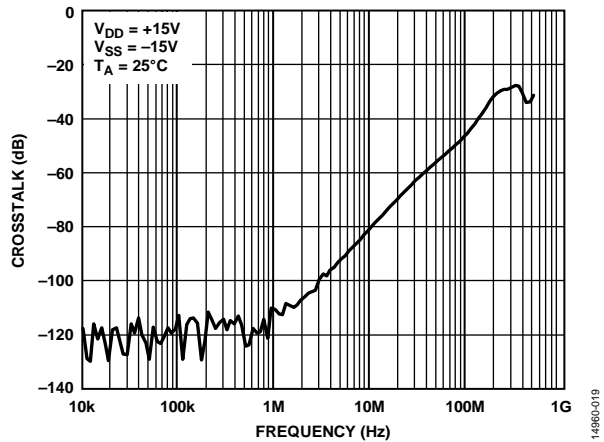
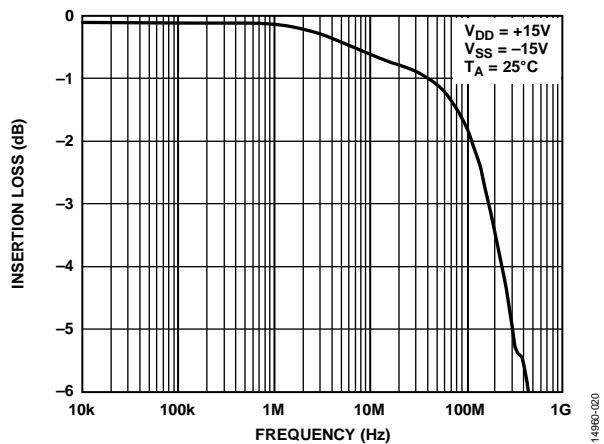
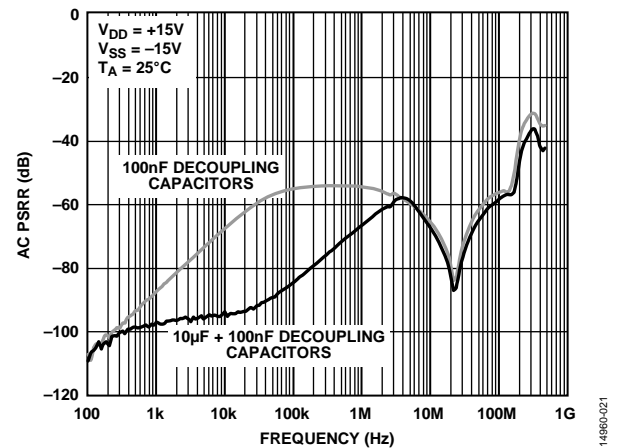
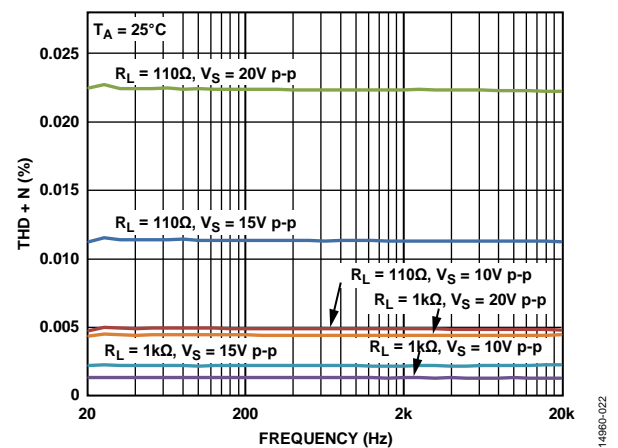
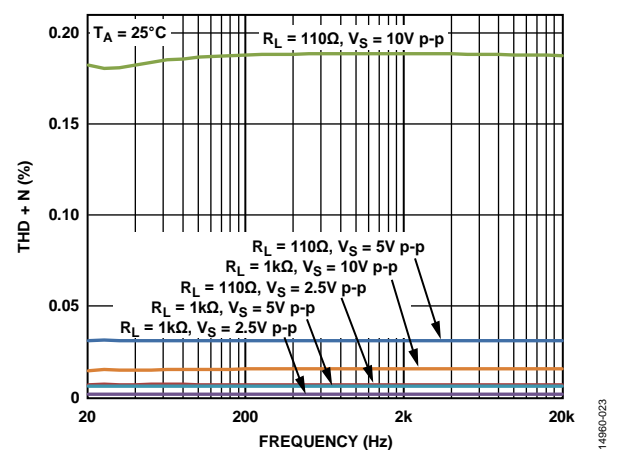


Figure 17.  $t_{ON}/t_{OFF}$  Time vs. Temperature for Single Supply (SS) and Dual Supply (DS)

Figure 18. Off Isolation vs. Frequency,  $\pm 15$  V Dual SupplyFigure 19. Crosstalk vs. Frequency,  $\pm 15$  V Dual SupplyFigure 20. Insertion Loss vs. Frequency,  $\pm 15$  V Dual SupplyFigure 21. AC Power Supply Rejection Ratio (AC PSRR) vs. Frequency,  $\pm 15$  V Dual SupplyFigure 22. THD + N vs. Frequency,  $\pm 15$  V Dual SupplyFigure 23. THD + N vs. Frequency,  $\pm 5$  V Dual Supply

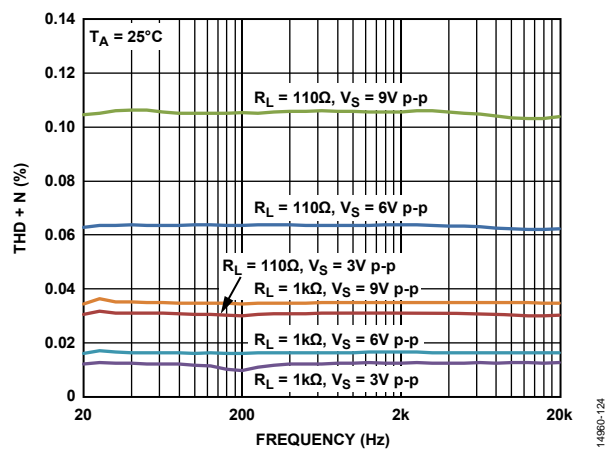


Figure 24. THD + N vs. Frequency, 12 V Single Supply

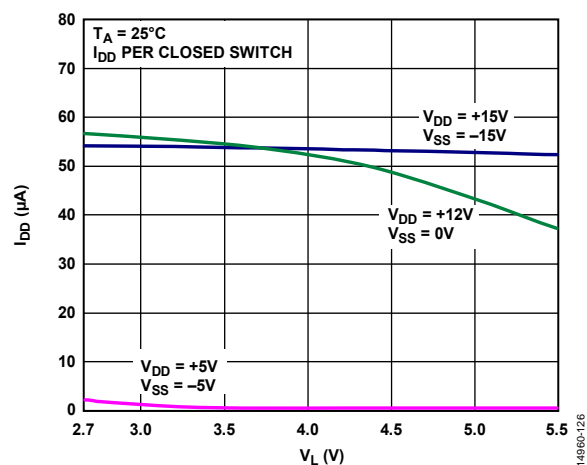
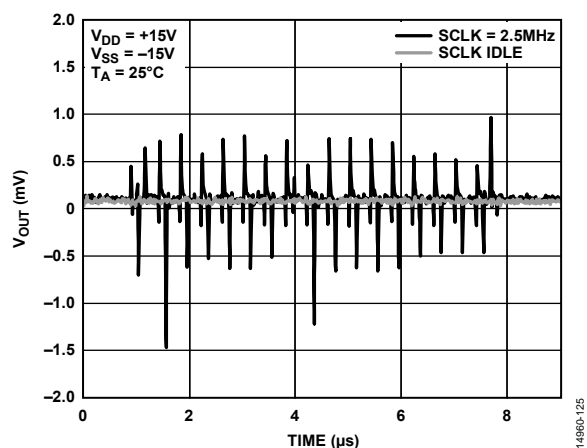
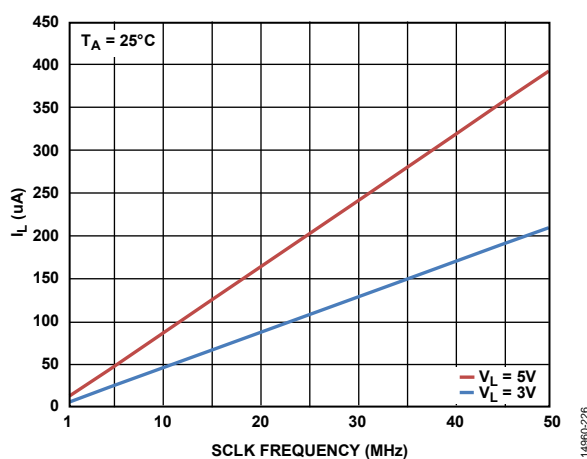
Figure 26.  $I_{DD}$  vs.  $V_L$ 

Figure 25. Digital Feedthrough

Figure 27.  $I_L$  vs. SCLK Frequency when  $\overline{CS}$  High



## TEST CIRCUITS

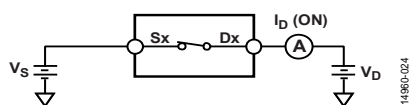


Figure 28. On Leakage

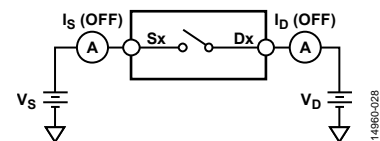


Figure 32. Off Leakage

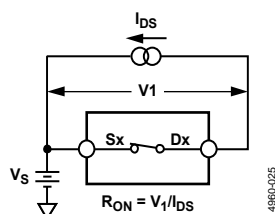


Figure 29. On Resistance

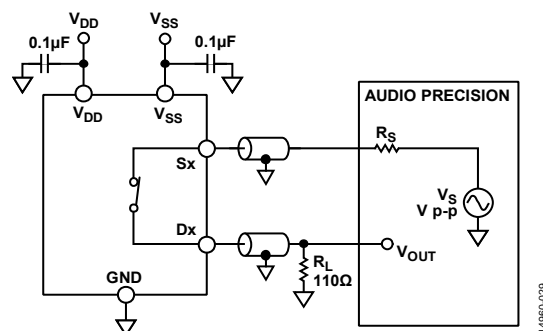
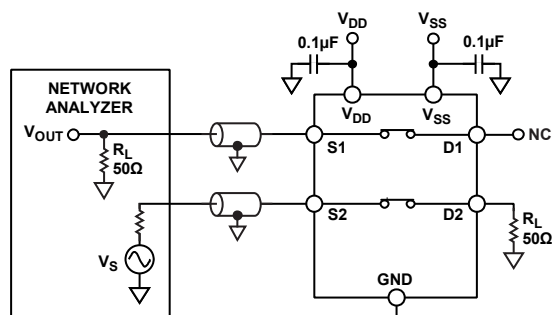
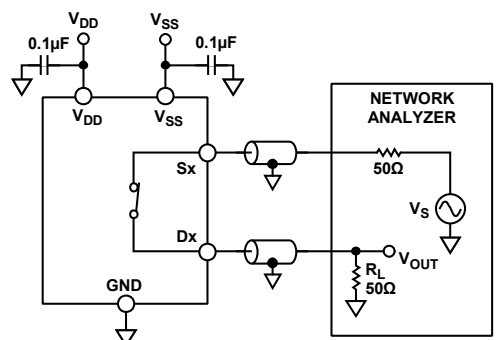


Figure 33. THD + Noise



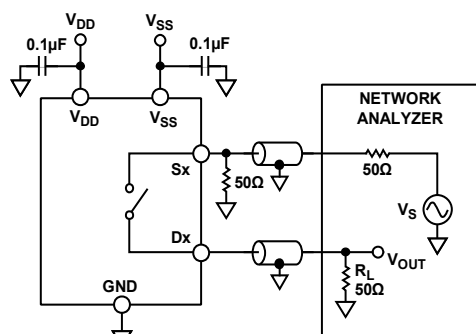
$$\text{CHANNEL TO CHANNEL CROSSTALK} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 30. Channel to Channel Crosstalk



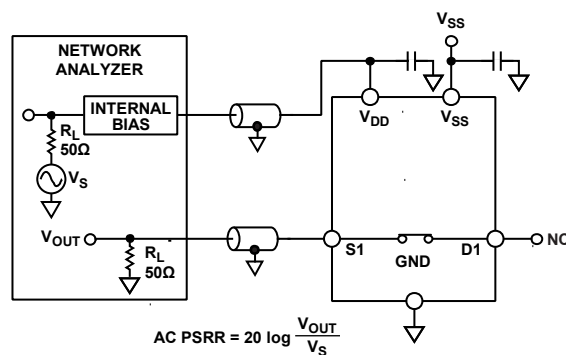
$$\text{INSERTION LOSS} = 20 \log \frac{V_{OUT \text{ WITH SWITCH}}}{V_S \text{ WITHOUT SWITCH}}$$

Figure 34. -3 dB Bandwidth



$$\text{OFF ISOLATION} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 31. Off Isolation

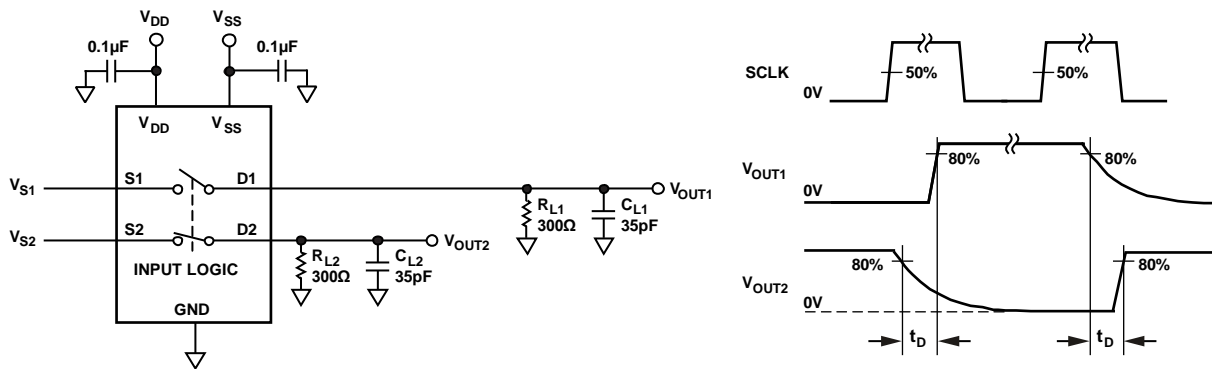
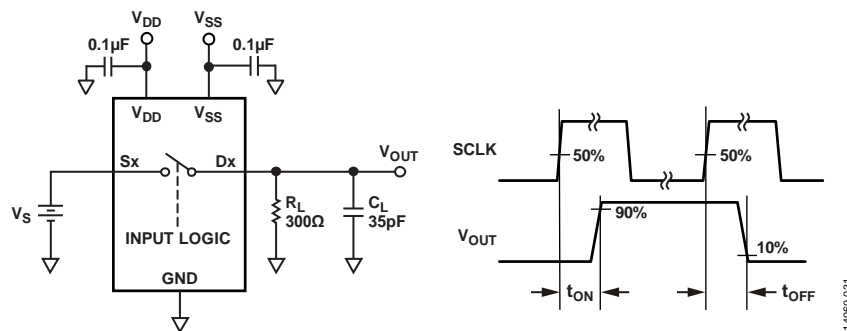
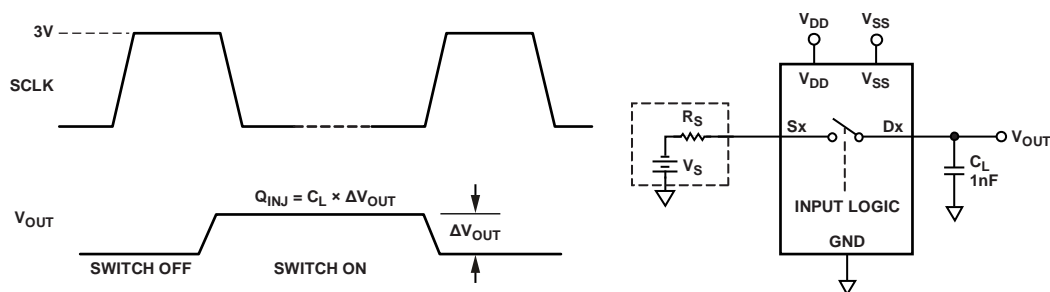


$$\text{AC PSRR} = 20 \log \frac{V_{OUT}}{V_S}$$

Figure 35. AC PSRR

## NOTES

1. BOARD AND COMPONENT EFFECTS ARE NOT DE-EMBEDDED FROM THE AC PSRR MEASUREMENT.

Figure 36. Break-Before-Make Time Delay,  $t_D$ Figure 37. Switching Times,  $t_{ON}$  and  $t_{OFF}$ Figure 38. Charge Injection,  $Q_{INJ}$

## TERMINOLOGY

### **I<sub>DD</sub>**

I<sub>DD</sub> represents the positive supply current.

### **I<sub>SS</sub>**

I<sub>SS</sub> represents the negative supply current.

### **V<sub>D</sub>, V<sub>S</sub>**

V<sub>D</sub> and V<sub>S</sub> represent the analog voltage on Terminal Dx and Terminal Sx, respectively.

### **R<sub>ON</sub>**

R<sub>ON</sub> represents the ohmic resistance between Terminal Dx and Terminal Sx.

### **ΔR<sub>ON</sub>**

ΔR<sub>ON</sub> represents the difference between the R<sub>ON</sub> of any two channels.

### **R<sub>FLAT (ON)</sub>**

Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range is represented by R<sub>FLAT (ON)</sub>.

### **I<sub>S</sub> (Off)**

I<sub>S</sub> (Off) is the source leakage current with the switch off.

### **I<sub>D</sub> (Off)**

I<sub>D</sub> (Off) is the drain leakage current with the switch off.

### **I<sub>D</sub> (On), I<sub>S</sub> (On)**

I<sub>D</sub> (On) and I<sub>S</sub> (On) represent the channel leakage currents with the switch on.

### **V<sub>INL</sub>**

V<sub>INL</sub> is the maximum input voltage for Logic 0.

### **V<sub>INH</sub>**

V<sub>INH</sub> is the minimum input voltage for Logic 1.

### **I<sub>INL</sub>, I<sub>INH</sub>**

I<sub>INL</sub> and I<sub>INH</sub> represent the low and high input currents of the digital inputs.

### **C<sub>D</sub> (Off)**

C<sub>D</sub> (Off) represents the off switch drain capacitance, which is measured with reference to ground.

### **C<sub>S</sub> (Off)**

C<sub>S</sub> (Off) represents the off switch source capacitance, which is measured with reference to ground.

### **C<sub>D</sub> (On), C<sub>S</sub> (On)**

C<sub>D</sub> (On) and C<sub>S</sub> (On) represent on switch capacitances, which are measured with reference to ground.

### **C<sub>IN</sub>**

C<sub>IN</sub> is the digital input capacitance.

### **t<sub>ON</sub>**

t<sub>ON</sub> represents the delay between applying the digital control input and the output switching on.

### **t<sub>OFF</sub>**

t<sub>OFF</sub> represents the delay between applying the digital control input and the output switching off.

### **Off Isolation**

Off isolation is a measure of unwanted signal coupling through an off switch.

### **Charge Injection**

Charge injection is a measure of the glitch impulse transferred from the digital input to the analog output during switching.

### **Crosstalk**

Crosstalk is a measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

### **–3 dB Bandwidth**

Bandwidth is the frequency at which the output is attenuated by 3 dB.

### **On Response**

On response is the frequency response of the on switch.

### **Insertion Loss**

Insertion loss is the loss due to the on resistance of the switch.

### **Total Harmonic Distortion + Noise (THD + N)**

The ratio of the harmonic amplitude plus noise of the signal to the fundamental is represented by THD + N.

### **AC Power Supply Rejection Ratio (AC PSRR)**

AC PSRR is the ratio of the amplitude of signal on the output to the amplitude of the modulation. AC PSRR is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

THEORY OF OPERATION

The ADGS1412 is a set of serially controlled, quad SPST switches with error detection features. SPI Mode 0 and Mode 3 can be used with the device, and it operates with SCLK frequencies up to 50 MHz. The default mode for the ADGS1412 is address mode in which the registers of the device are accessed by a 16-bit SPI command that is bounded by  $\overline{CS}$ . The SPI command becomes 24 bit if the user enables CRC error detection. Other error detection features include SCLK count error and invalid read/write error. If any of these SPI interface errors occur, they are detectable by reading the error flags register. The ADGS1412 can also operate in two other modes, namely burst mode and daisy-chain mode.

The interface pins of the ADGS1412 are  $\overline{CS}$ , SCLK, SDI, and SDO. Hold  $\overline{CS}$  low when using the SPI interface. Data is captured on the SDI on the rising edge of SCLK, and data is propagated out on the SDO on the falling edge of SCLK. SDO has an open-drain output; thus, connect a pull-up to this output. When not pulled low by the ADGS1412, SDO is in a high impedance state.

ADDRESS MODE

Address mode is the default mode for the ADGS1412 upon power up. A single SPI frame in address mode is bounded by a  $\overline{CS}$  falling edge and the succeeding  $\overline{CS}$  rising edge. It is comprised of 16 SCLK cycles. The timing diagram for address mode is shown in Figure 39. The first SDI bit indicates if the SPI command is a read or write command. When the first bit is set to 0, a write command is issued, and if the first bit is set to 1, a read command is issued. The next seven bits determine the target register address. The remaining eight bits provide the data to the addressed register. The last eight bits are ignored during a read command, because during these clock cycles, SDO propagates out the data contained in the addressed register.

The target register address of an SPI command is determined on the eighth SCLK rising edge. Data from this register propagates out on SDO from the 9<sup>th</sup> to the 16<sup>th</sup> SCLK falling edge during SPI reads. A register write occurs on the 16<sup>th</sup> SCLK rising edge during SPI writes.

During any SPI command, SDO sends out eight alignment bits on the first eight SCLK falling edges. The alignment bits observed at SDO are 0x25.

ERROR DETECTION FEATURES

Protocol and communication errors on the SPI interface are detectable. There are three detectable errors, which are incorrect SCLK count error detection, invalid read/write address error detection, and CRC error detection. Each of these errors has a corresponding enable bit in the error configuration register. In addition, there is an error flag bit for each of these errors in the error flags register.

Cyclic Redundancy Check (CRC) Error Detection

The CRC error detection feature extends a valid SPI frame by 8 SCLK cycles. These eight extra cycles are needed to send the CRC byte for that SPI frame. The CRC byte is calculated by the SPI block using the 16-bit payload: the R/W bit, Register Address Bits[6:0], and Register Data Bits[7:0]. The CRC polynomial used in the SPI block is  $x^8 + x^2 + x^1 + 1$  with a seed value of 0. For a timing diagram with CRC enabled, see Figure 40. Register writes occur at the 24<sup>th</sup> SCLK rising edge with CRC error checking enabled.

During an SPI write, the microcontroller/central processing unit (CPU) provides the CRC byte through SDI. The SPI block checks the CRC byte just before the 24th SCLK rising edge. On this same edge, the register write is prevented if an incorrect CRC byte is received by the SPI interface. The CRC error flag is asserted in the error flags register in the case of the incorrect CRC byte being detected.

During an SPI read, the CRC byte is provided to the microcontroller through SDO.

The CRC error detection feature is disabled by default and can be configured by the user through the error configuration register.

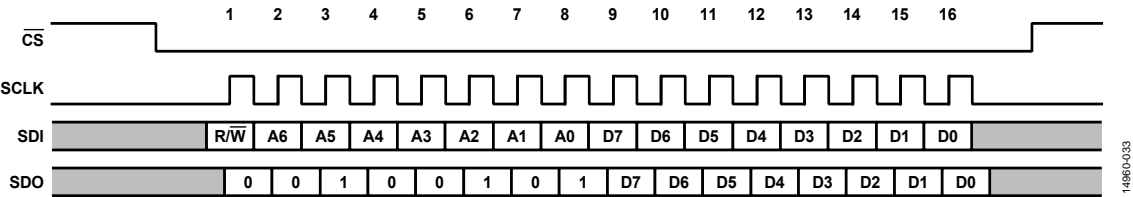


Figure 39. Address Mode Timing Diagram

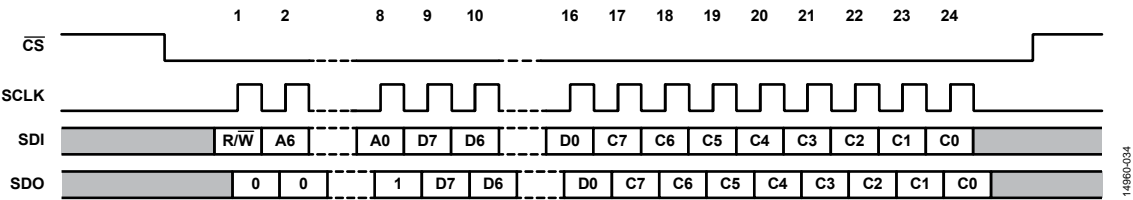


Figure 40. Timing Diagram with CRC Enabled

### SCLK Count Error Detection

SCLK count error detection allows the user to detect if an incorrect number of SCLK cycles are sent by the microcontroller/CPU. When in address mode, with CRC disabled, 16 SCLK cycles are expected. If 16 SCLK cycles are not detected, the SCLK count error flag asserts in the error flags register. When less than 16 SCLK cycles are received by the device, a write to the register map never occurs. When the ADGS1412 receives more than 16 SCLK cycles, a write to the memory map still occurs at the 16<sup>th</sup> SCLK rising edge, and the flag asserts in the error flags register. With CRC enabled, the expected number of SCLK cycles becomes 24. SCLK count error detection is enabled by default and can be configured by the user through the error configuration register.

### Invalid Read/Write Address Error

An invalid read/write address error detects when a nonexistent register address is a target for a read or write. In addition, this error asserts when a write to a read only register is attempted. The invalid read/write address error flag asserts in the error flags register when an invalid read/write address error happens. The invalid read/write address error is detected on the ninth SCLK rising edge, which means a write to the register never occurs when an invalid address is targeted. Invalid read/write address error detection is enabled by default and can be disabled by the user through the error configuration register.

### CLEARING THE ERROR FLAGS REGISTER

To clear the error flags register, write the special 16-bit SPI frame, 0x6CA9, to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must also send the correct CRC byte for a successful error clear command. At the 16<sup>th</sup> or 24<sup>th</sup> SCLK rising edge, the error flags register resets to zero.

### BURST MODE

The SPI interface can accept consecutive SPI commands without the need to deassert the  $\overline{CS}$  line, which is called burst mode. Burst mode is enabled through the burst enable register. This mode uses the same 16-bit command to communicate with the device. In addition, the response of the device at SDO is still aligned with the corresponding SPI command. Figure 41 shows an example of SDI and SDO during burst mode.

The invalid read/write address and CRC error checking functions operate similarly during burst mode as they do during address mode. However, SCLK count error detection operates in a slightly different manner. The total number of SCLK cycles within a given  $\overline{CS}$  frame are counted, and if the total is not a multiple of 16, or a multiple of 24 when CRC is enabled, the SCLK count error flag asserts.

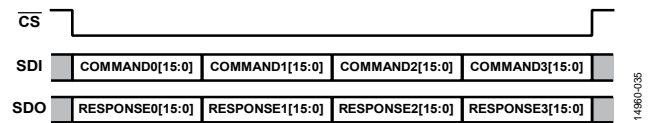


Figure 41. Burst Mode Frame

### SOFTWARE RESET

When in address mode, the user can initiate a software reset. To do so, write two consecutive SPI commands, 0xA3 followed by 0x05, targeting Register 0x0B. After a software reset, all register values are set to default.

### DAISY-CHAIN MODE

The connection of several ADGS1412 devices in a daisy-chain configuration is possible, and Figure 42 illustrates this setup. All devices share the same  $\overline{CS}$  and SCLK line, whereas the SDO of a device forms a connection to the SDI of the next device, creating a shift register. In daisy-chain mode, SDO is an 8 cycle delayed version of SDI. When in daisy-chain mode, all commands target the switch data register. Therefore, it is not possible to make configuration changes while in daisy-chain mode.

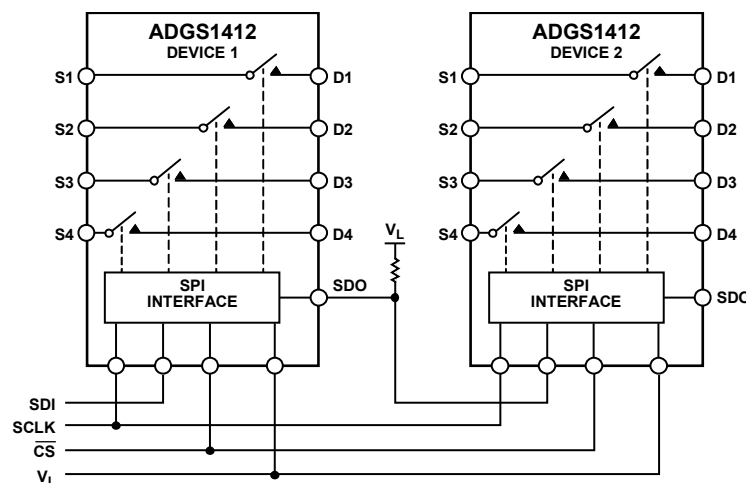


Figure 42. Two ADGS1412 Devices Connected in a Daisy-Chain Configuration

The ADGS1412 can only enter daisy-chain mode when in address mode by sending the 16-bit SPI command, 0x2500 (see Figure 43). When the ADGS1412 receives this command, the SDO of the device sends out the same command because the alignment bits at SDO are 0x25, which allows multiple daisy-connected devices to enter daisy-chain mode in a single SPI frame. A hardware reset is required to exit daisy-chain mode.

For the timing diagram of a typical daisy-chain SPI frame, see Figure 44. When CS goes high, Device 1 writes Command 0, Bits[7:0] to its switch data register, Device 2 writes Command 1, Bits[7:0] to its switches, and so on. The SPI block uses the last eight bits it received through SDI to update the switches. After entering daisy-chain mode, the first eight bits sent out by SDO on each device in the chain are 0x00. When CS goes high, the internal shift register value does not reset back to zero.

An SCLK rising edge reads in data on SDI while data is propagated out SDO on an SCLK falling edge. The expected number of SCLK cycles must be a multiple of eight before CS goes high. When this is not the case, the SPI interface sends the last eight bits received to the switch data register.

POWER-ON RESET

The digital section of the ADGS1412 goes through an initialization phase during V<sub>L</sub> power up. This initialization also occurs after a hardware or software reset. After V<sub>L</sub> power-up or a reset, ensure that a minimum of 120 μs from the time of power-up or reset before any SPI command is issued. Ensure that V<sub>L</sub> does not drop out during the 120 μs initialization phase because it may result in incorrect operation of the ADGS1412.

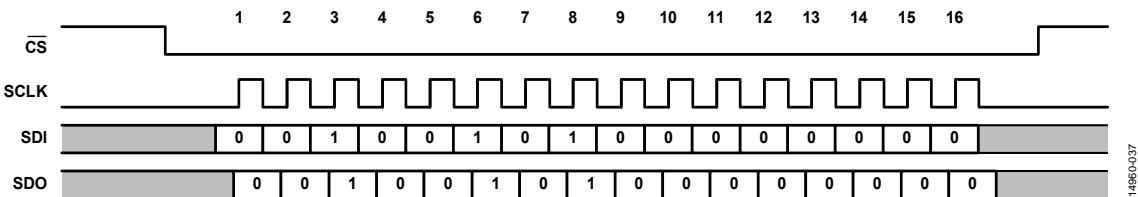


Figure 43. SPI Command to Enter Daisy-Chain Mode

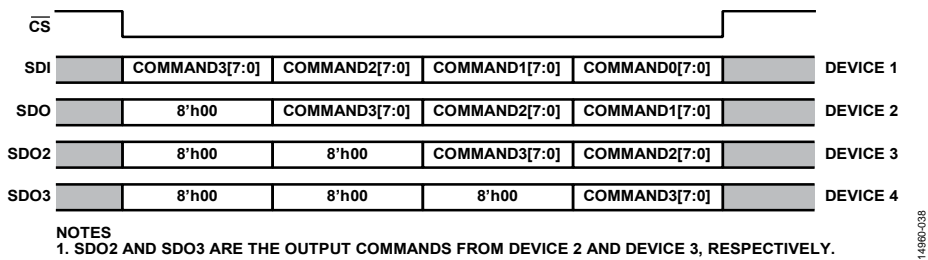


Figure 44. Example of an SPI Frame Where Four ADGS1412 Devices Connect in Daisy-Chain Mode

## APPLICATIONS INFORMATION

### BREAK-BEFORE-MAKE SWITCHING

The [ADGS1412](#) exhibits break-before-make switching action. This feature allows the use of the device in multiplexer applications. Using the device like a multiplexer can be accomplished by externally hardwiring the device into the desired mux configuration, as shown in Figure 45.

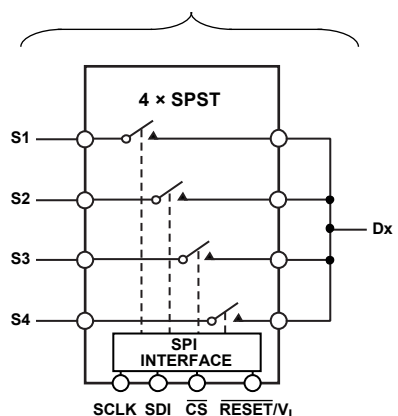


Figure 45. An SPI Controlled Switch Configured into a 4:1 Mux

### DIGITAL INPUT BUFFERS

There are input buffers present on the digital input pins ( $\overline{CS}$ , SCLK, and SDI). These buffers are active at all times. Therefore, there is current draw from the  $V_L$  supply if SCLK or SDI is toggling, regardless of whether  $\overline{CS}$  is active. For typical values of this current draw, refer to the Specifications section and Figure 27.

### POWER SUPPLY RAILS

To guarantee correct operation of the [ADGS1412](#), 0.1  $\mu\text{F}$  decoupling capacitors are required.

The [ADGS1412](#) can operate with bipolar supplies between  $\pm 4.5\text{ V}$  and  $\pm 16.5\text{ V}$ . The supplies on  $V_{DD}$  and  $V_{SS}$  do not have to be symmetrical; however, the  $V_{DD}$  to  $V_{SS}$  range must not exceed 33 V. The [ADGS1412](#) can also operate with single supplies between 5 V and 20 V with  $V_{SS}$  connected to GND.

The voltage range that can be supplied to  $V_L$  is from 2.7 V to 5.5 V.

The device is fully specified at  $\pm 15\text{ V}$ ,  $\pm 5\text{ V}$ , and  $+12\text{ V}$  analog supply voltage ranges.

### POWER SUPPLY RECOMMENDATIONS

Analog Devices, Inc., has a wide range of power management products to meet the requirements of most high performance signal chains.

An example of a bipolar power solution is shown in Figure 46. The [ADP5070](#) (dual switching regulator) generates a positive and negative supply rail for the [ADGS1412](#), an amplifier, and/or a precision converter in a typical signal chain. Also shown in Figure 46 are two optional low dropout regulators (LDOs), the [ADP7118](#) and [ADP7182](#) positive and negative LDOs respectively, that can be used to reduce the output ripple of the [ADP5070](#) in ultralow noise sensitive applications.

The [ADM7160](#) can be used to generate  $V_L$  voltage that is required to power digital circuitry within the [ADGS1412](#).

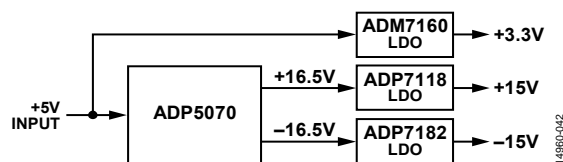


Figure 46. Bipolar Power Solution

Table 10. Recommended Power Management Devices

Product	Description
<a href="#">ADP5070</a>	1 A/0.6 A, dc-to-dc switching regulator with independent positive and negative outputs
<a href="#">ADM7160</a>	5.5 V, 200 mA, ultralow noise, linear regulator
<a href="#">ADP7118</a>	20 V, 200 mA, low noise, CMOS LDO linear regulator
<a href="#">ADP7182</a>	-28 V, -200 mA, low noise, LDO linear regulator

## REGISTER SUMMARY

Table 11. Register Summary

Register (Hex)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default	R/W
0x01	SW_DATA	Reserved				SW4_EN	SW3_EN	SW2_EN	SW1_EN	0x00	R/W
0x02	ERR_CONFIG	Reserved					RW_ERR_EN	SCLK_ERR_EN	CRC_ERR_EN	0x06	R/W
0x03	ERR_FLAGS	Reserved					RW_ERR_FLAG	SCLK_ERR_FLAG	CRC_ERR_FLAG	0x00	R
0x05	BURST_EN	Reserved							BURST_MODE_EN	0x00	R/W
0x0B	SOFT_RESETB	SOFT_RESETB								0x00	R/W



## REGISTER DETAILS

### SWITCH DATA REGISTER

Address: 0x01, Reset: 0x00, Name: SW\_DATA

The switch data register controls the status of the four switches of the [ADGS1412](#).

Table 12. Bit Descriptions for SW\_DATA

Bits	Bit Name	Settings	Description	Default	Access
[7:4]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
3	SW4_EN	0 1	Enable bit for SW4. SW4 open. SW4 closed.	0x0	R/W
2	SW3_EN	0 1	Enable bit for SW3. SW3 open. SW3 closed.	0x0	R/W
1	SW2_EN	0 1	Enable bit for SW2. SW2 open. SW2 closed.	0x0	R/W
0	SW1_EN	0 1	Enable bit for SW1. SW1 open. SW1 closed.	0x0	R/W

### ERROR CONFIGURATION REGISTER

Address: 0x02, Reset: 0x06, Name: ERR\_CONFIG

The error configuration register allows the user to enable and disable the relevant error features as required.

Table 13. Bit Descriptions for ERR\_CONFIG

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
2	RW_ERR_EN	0 1	Enable bit for detecting invalid read/write address. Disabled. Enabled.	0x1	R/W
1	SCLK_ERR_EN	0 1	Enable bit for detecting the correct number of SCLK cycles in an SPI frame. 16 SCLK cycles are expected when CRC is disabled and burst mode is disabled. 24 SCLK cycles are expected when CRC is enabled and burst mode is disabled. A multiple of 16 SCLK cycles are expected when CRC is disabled and burst mode is enabled. A multiple of 24 SCLK cycles are expected when CRC is enabled and burst mode is enabled. Disabled. Enabled.	0x1	R/W
0	CRC_ERR_EN	0 1	Enable bit for CRC error detection. SPI frames are 24 bits wide when enabled. Disabled. Enabled.	0x0	R/W

**ERROR FLAGS REGISTER****Address: 0x03, Reset: 0x00, Name: ERR\_FLAGS**

The error flags register allows the user to determine if an error has occurred. To clear the error flags register, write the special 16-bit SPI command 0x6CA9 to the device. This SPI command does not trigger the invalid R/W address error. When CRC is enabled, the user must include the correct CRC byte during the SPI write for the clear error flags register command to succeed.

**Table 14. Bit Descriptions for ERR\_FLAGS**

Bits	Bit Name	Settings	Description	Default	Access
[7:3]	Reserved		These bits are reserved and are set to 0.	0x0	R
2	RW_ERR_FLAG	0 No error. 1 Error.	Error flag for invalid read/write address. The error flag asserts during an SPI read if the target address does not exist. The error flag also asserts when the target address of an SPI write does not exist or is read only.	0x0	R
1	SCLK_ERR_FLAG	0 No error. 1 Error.	Error flag for the detection of the correct number of SCLK cycles in an SPI frame.	0x0	R
0	CRC_ERR_FLAG	0 No error. 1 Error.	Error flag that determines if a CRC error has occurred during a register write.	0x0	R

**BURST ENABLE REGISTER****Address: 0x05, Reset: 0x00, Name: BURST\_EN**

The burst enable register allows the user to enable or disable burst mode. When enabled, the user can send multiple consecutive SPI commands without deasserting  $\overline{CS}$ .

**Table 15. Bit Descriptions for BURST\_EN**

Bits	Bit Name	Settings	Description	Default	Access
[7:1]	Reserved		These bits are reserved; set these bits to 0.	0x0	R
0	BURST_MODE_EN	0 Disabled. 1 Enabled.	Burst mode enable bit.	0x0	R/W

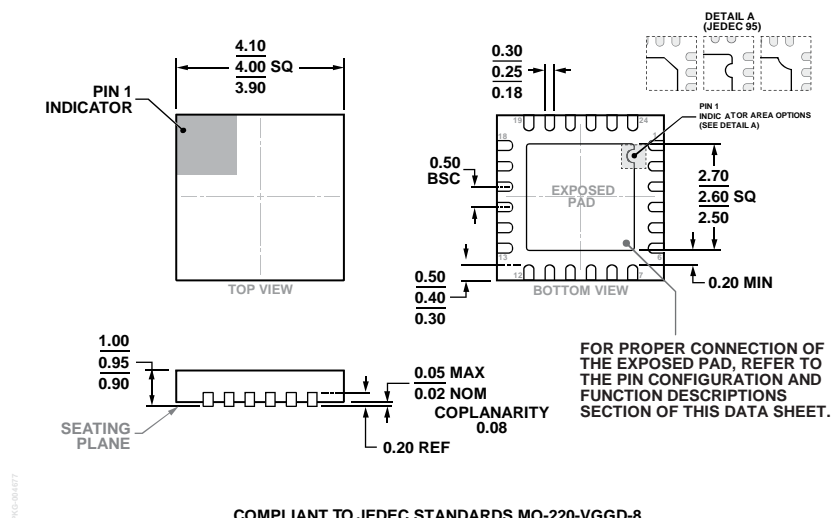
**SOFTWARE RESET REGISTER****Address: 0x0B, Reset: 0x00, Name: SOFT\_RESETB**

Use the software reset register to perform a software reset. Consecutively, write 0xA3 followed by 0x05 to this register, and the registers of the device reset to their default state.

**Table 16. Bit Descriptions for SOFT\_RESETB**

Bits	Bit Name	Settings	Description	Default	Access
[7:0]	SOFT_RESETB		To perform a software reset, consecutively write 0xA3 followed by 0x05 to this register.	0x0	R

## OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.

Figure 47. 24-Lead Lead Frame Chip Scale Package [LFCSP]

4 mm × 4 mm Body and 0.95 mm Package Height

(CP-24-17)

Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
ADGS1412BCPZ	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-17
ADGS1412BCPZ-RL7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-17
EVAL-ADGS1412SDZ		Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.