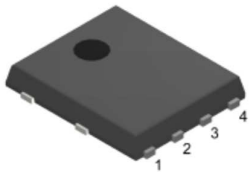
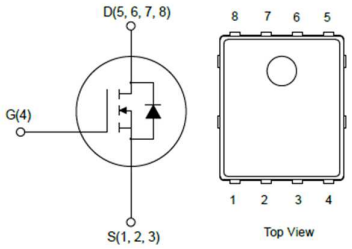
N-Channel Enhancement Mode Logic Level 40V, 0.8mΩ max, 360A STripFET F8 Power MOSFET in a PowerFLAT 5x6 package

Pre-Release Data



PowerFLAT 5x6



Features

Order Code	V_{DS}	$R_{DS(on)}$ max	I_D
STL320N4LF8	40 V	0.8 mΩ at 10V	360 A

- MSL1 grade
- 175ºC operative temperature
- 100% avalanche tested

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F8 with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitances and gate charge for faster and more efficient switching.

Product summary	
Order code	STL320N4LF8
Marking (1)	320N4LF8
Package	PowerFLAT 5x6
Packing	Tape and reel

1 Electrical ratings

(T_C = 25°C unless otherwise specified)

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D (2)	Drain current (continuous) at T_C = 25°C	360	A
	Drain current (continuous) at T_C = 100°C	254	
I_{DM} (3,4)	Drain current (pulsed), t_P = 10µs	1440	A
P_{TOT}	Total power dissipation at T_C = 25°C	188	W
I_{AS}	Single pulse avalanche current (pulse width limited by T_J max)	60	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25°C, I_D = 60A, R_{Gmin} = 25Ω)	590	mJ
T_J	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

Table 2. Thermal data (3)

Symbol	Parameter	Value	Unit
R_{thJA} (5)	Thermal resistance junction-ambient max. (on 2s2p FR-4 board vertical in still air)	20	°C/W
R_{thJC}	Thermal resistance junction-case max.	0.8	°C/W

2 Electrical characteristics

(T_J = 25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0V, I_D = 1mA	40			V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 40V, V_{GS} = 0V			1	µA
		V_{DS} = 40V, V_{GS} = 0V, T_J = 125°C (3)			100	
I_{GSS}	Gate-body leakage current	V_{GS} = 20V, V_{DS} = 0V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250µA	1.2		2.0	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10V, I_D = 60A		0.55	0.8	mΩ
		V_{GS} = 4.5V, I_D = 60A		0.85	1.15	
R_G (3)	Gate resistance			1.2		Ω

Table 4. Dynamic (3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25V, f = 1MHz, V_{GS} = 0V		7657		pF
C_{oss}	Output capacitance			1968		pF
C_{rss}	Reverse transfer capacitance			50		pF
Q_g	Total gate charge	V_{DD} = 20V, I_D = 60A, V_{GS} = 0 to 4.5V		41		nC
		V_{DD} = 20V, I_D = 60A, V_{GS} = 0 to 10V		96		
Q_{gs}	Gate-source charge	V_{DD} = 20V, I_D = 60A, V_{GS} = 0 to 4.5V		20		nC
Q_{gd}	Gate-drain charge			6.9		nC
$Q_{g(sync)}$	Total gate charge, sync. MOSFET	V_{DS} = 0.1V, V_{GS} = 0 to 4.5V		43		nC
Q_{oss}	Output charge	V_{DD} = 20V, V_{GS} = 0V		102		nC

Table 5. Switching times (3)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20V, I_D = 60A, R_G = 4.7Ω, V_{GS} = 10V		12.3		ns
t_r	Rise time			6.3		ns
$t_{d(off)}$	Turn-off delay time			89.2		ns
t_f	Fall time			21		ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} (2,3)	Forward on current (continuous)	T_C = 25°C			135	A
V_{SD}	Forward on voltage	I_{SD} = 60A, V_{GS} = 0V			1.1	V
t_{rr} (3)	Reverse recovery time	I_D = 60A, di/dt = 100A/µs, V_{DD} = 32V		60.1		ns
Q_{rr} (3)	Reverse recovery charge			74.4		nC
I_{RRM} (3)	Reverse recovery current			2.5		A

(1) For engineering samples marking, see *PowerFLAT 5x6 package marking information*.
(2) The value is relevant to R_{thJC}. Current limitations will come from the operative conditions, such as temperature and thermal resistance of the PCB.
(3) Specified by design and evaluated by characterization, not tested in production.
(4) Pulse width is limited by safe operating area.
(5) Defined according to JEDEC standards (JESD51-5, -7).

2.1 Electrical characteristics (curves)

Figure 1. Power dissipation

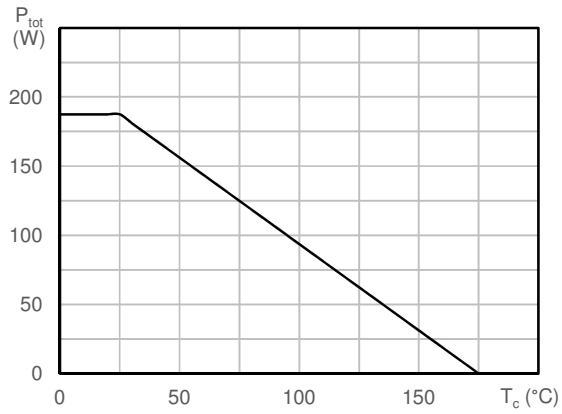


Figure 2. Drain current

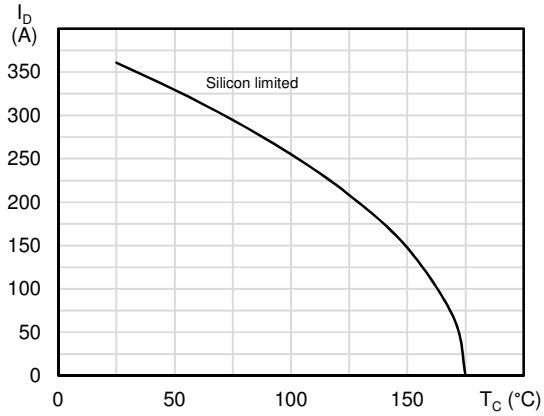


Figure 3. Safe operating area

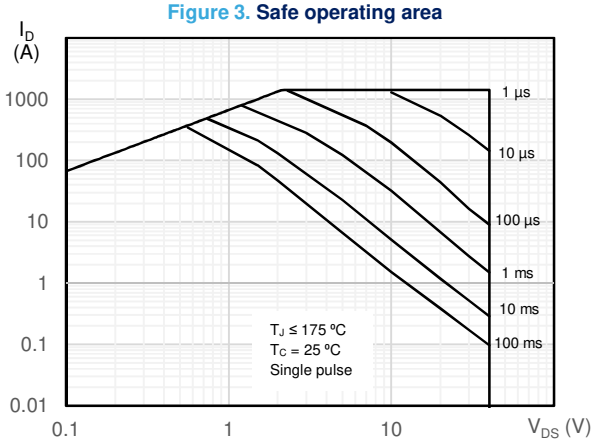


Figure 4. Normalized transient thermal impedance

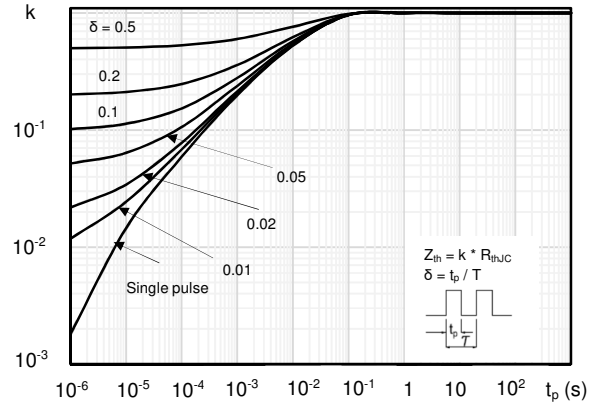


Figure 5. Typ output characteristics

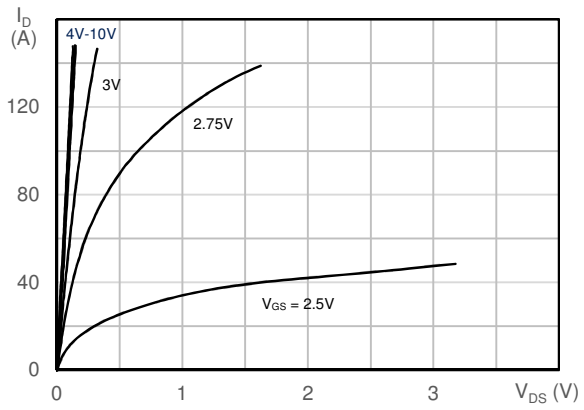


Figure 6. Typ on-resistance vs gate-source voltage

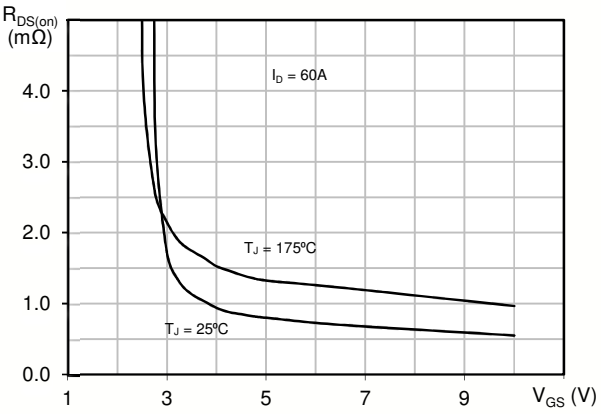


Figure 7. Typ transfer characteristics

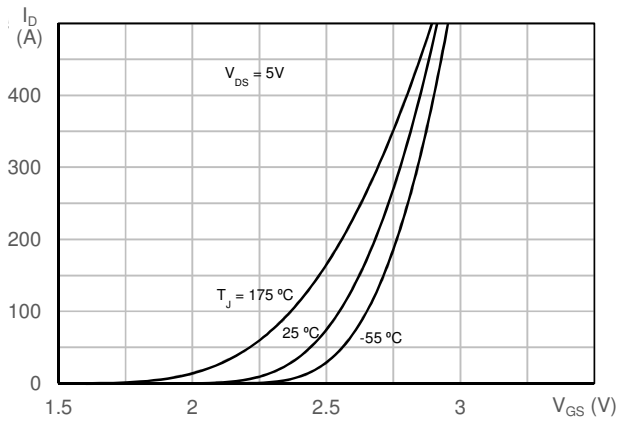


Figure 8. Typ drain-source on-resistance

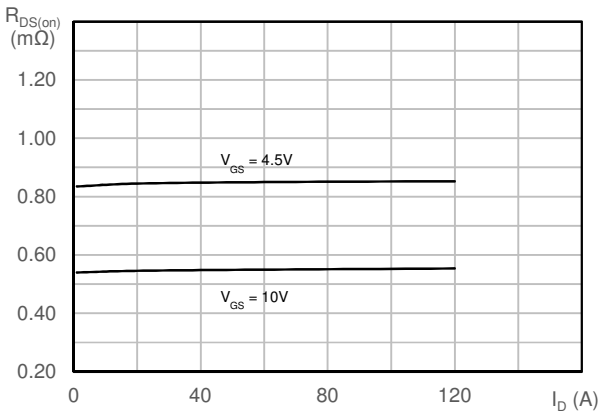


Figure 9. Typ gate charge

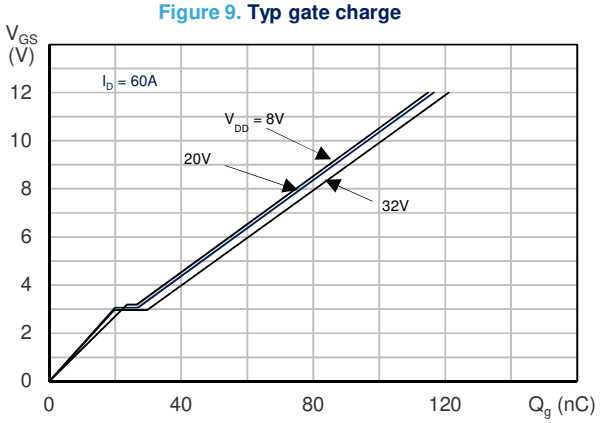


Figure 10. Typ capacitances

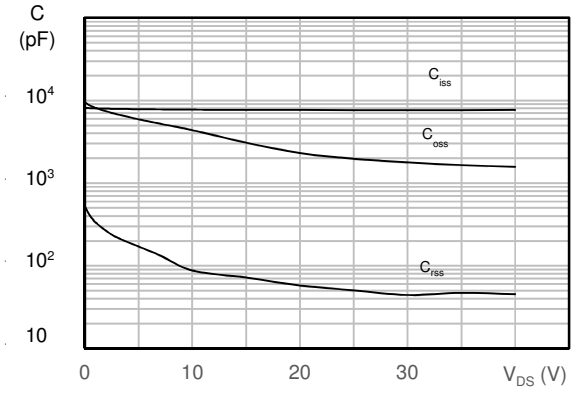


Figure 11. Avalanche characteristics

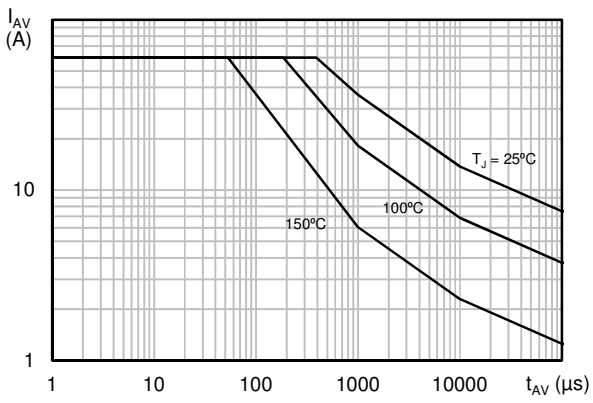


Figure 12. Avalanche energy

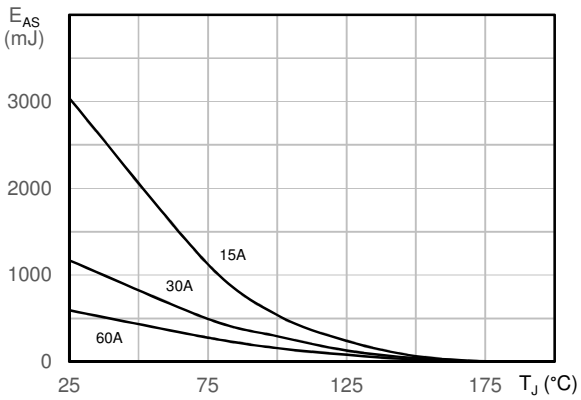


Figure 13. **Normalized on-resistance vs temperature**

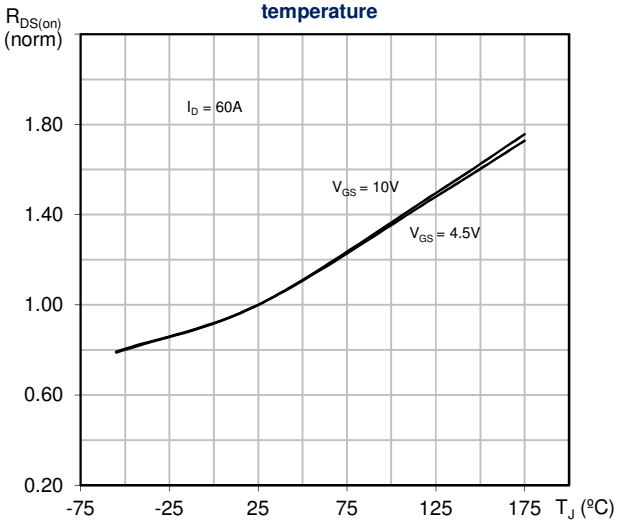


Figure 14. **Normalized $V_{(BR)DSS}$ vs temperature**

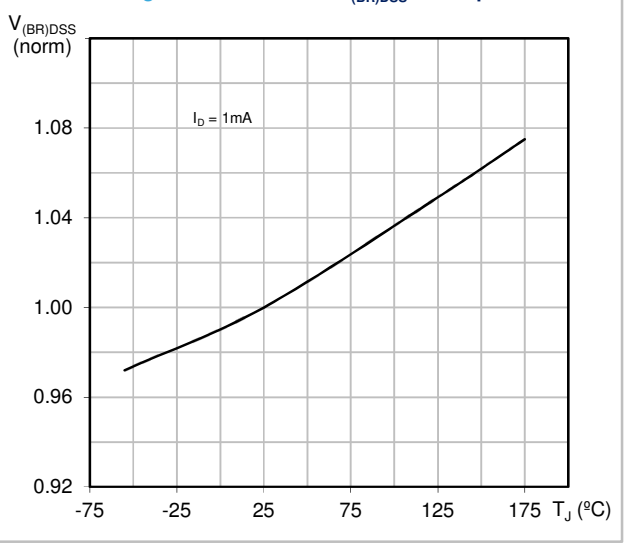


Figure 15. **Normalized gate threshold voltage vs temperature**

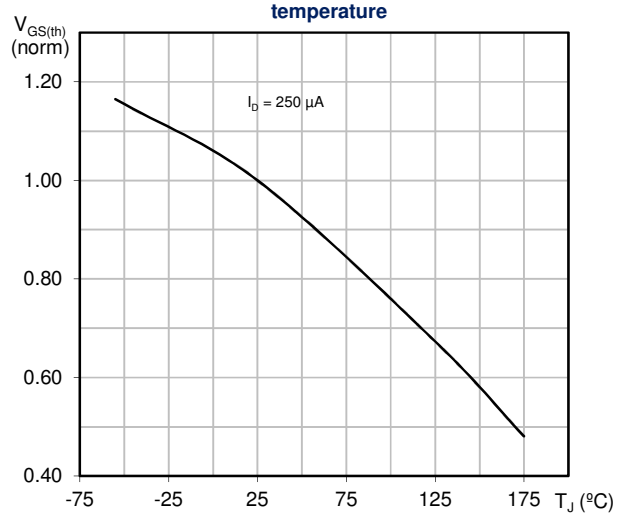
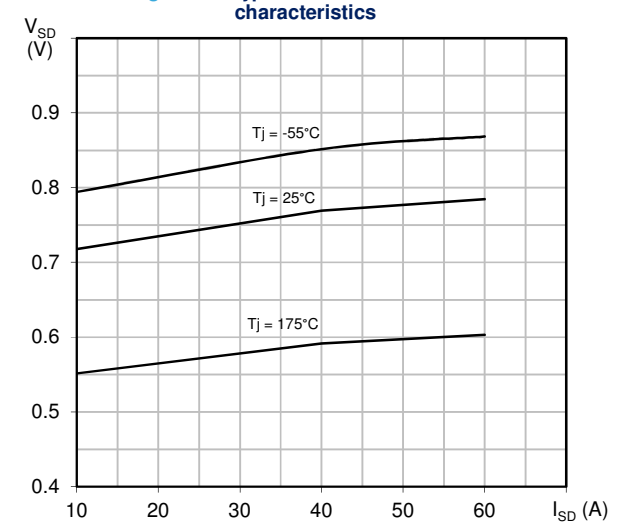
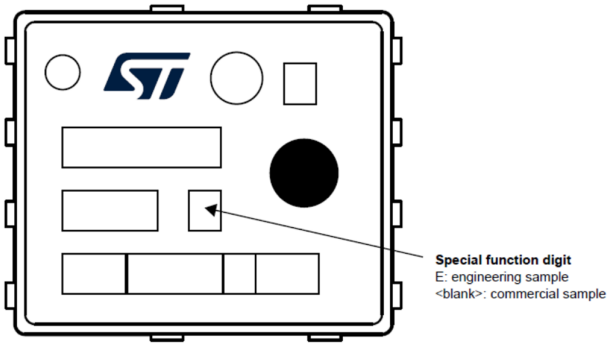


Figure 16. **Typ reverse diode forward characteristics**



3 PowerFLAT 5x6 package marking information

Figure 17. PowerFLAT 5x6 package marking information



Notes: Engineering Samples are clearly identified with a dedicated special symbol in the marking of each unit. These samples are intented to be used for electrical compatibility evaluation only. Usage for any other purpose may be agreed only upon written authorization by ST. ST is not liable for any customer usage in production and/or in reliability qualification trials.

Commercial Samples are fully qualified parts from ST standard production with no usage restrictions.

Revision History

Table 7. Document revision history

Date	Revision	Changes
3-Mar-2022	0.1	Pre-release data