

3.3 V 1:2 Fanout Differential LVPECL/LVDS to LVTTTL Translator

MC100EPT26

Description

The MC100EPT26 is a 1:2 Fanout Differential LVPECL/LVDS to LVTTTL translator. Because LVPECL (Positive ECL) or LVDS levels are used only +3.3 V and ground are required. The small outline 8-lead package and the 1:2 fanout design of the EPT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The V_{BB} output allows the EPT26 to be used in a Single-Ended input mode. In this mode the V_{BB} output is tied to the $\overline{D0}$ input for a non-inverting buffer or the D0 input for an inverting buffer. If used, the V_{BB} pin should be bypassed to ground with $> 0.01 \mu\text{F}$ capacitor. For a Single-Ended direct connection, use an external voltage reference source such as a resistor divider. Do not use V_{BB} for a Single-Ended direct connection or port to another device.

Features

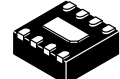
- 1.4 ns Typical Propagation Delay
- Maximum Frequency = $> 275 \text{ MHz}$ Typical
- The 100 Series Contains Temperature Compensation
- Operating Range: $V_{CC} = 3.0 \text{ V}$ to 3.6 V with $GND = 0 \text{ V}$
- 24 mA TTL outputs
- Q Outputs Will Default LOW with Inputs Open or at V_{EE}
- V_{BB} Output
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



SOIC-8 NB
D SUFFIX
CASE 751-07

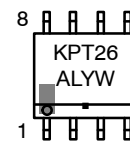


TSSOP-8
DT SUFFIX
CASE 948R-02

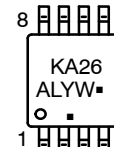


DFN8
MN SUFFIX
CASE 506AA

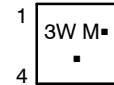
MARKING DIAGRAMS*



SOIC-8 NB



TSSOP-8



DFN8

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT26DG	SOIC-8 NB (Pb-Free)	98 Units/Tube
MC100EPT26DR2G	SOIC-8 NB (Pb-Free)	2500 Tape & Reel
MC100EPT26DTG	TSSOP-8 (Pb-Free)	100 Tape & Reel
MC100RPT26DTR2G	TSSOP-8 (Pb-Free)	2500 Tape & Reel
MC100EPT26MNR4G	DFN8 (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

MC100EPT26

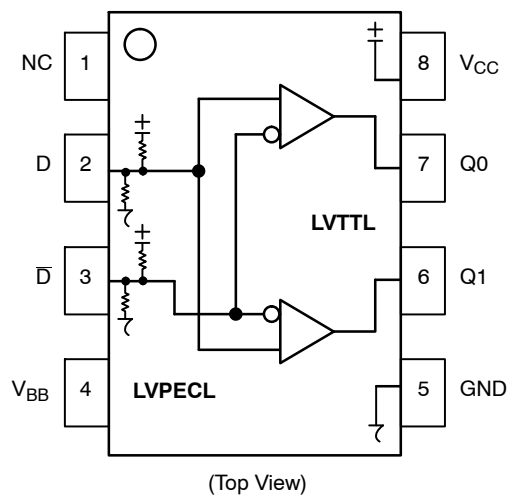


Figure 1. 8-Lead Pinout and Logic Diagram

Table 1. PIN DESCRIPTION

Pin	Function
Q0, Q1	LVTTTL Outputs
D0**, D1**	Differential LVPECL Inputs Pair
V _{CC}	Positive Supply
V _{BB}	Output Reference Voltage
GND	Ground
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

** Pins will default to V_{CC}/2 when left open.

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	50 kΩ
Internal Input Pullup Resistor	50 kΩ
ESD Protection Human Body Model Machine Model Charged Device Model	> 1.5 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC-8 NB TSSOP-8 DFN8	Level 1 Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	117 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note [AND8003/D](#).

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		3.8	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \leq V_{CC}$	0 to 3.8	V
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
T_A	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 NB SOIC-8 NB	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8 NB	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C
θ_{JC}	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

Table 4. PECL INPUT DC CHARACTERISTICS ($V_{CC} = 3.3$ V; GND = 0.0 V (Note 3))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	V
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current D $\bar{D}$	-150 -150			-150 -150			-150 -150			μA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. Input parameters vary 1:1 with V_{CC} .

4. V_{IHCMR} min varies 1:1 with GND, V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.



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Table 5. TTL OUTPUT DC CHARACTERISTICS ($V_{CC} = 3.3 \text{ V}$; $GND = 0.0 \text{ V}$; $T_A = -40^\circ\text{C}$ to 85°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage	$I_{OH} = -3.0 \text{ mA}$	2.4			V
V_{OL}	Output LOW Voltage	$I_{OL} = 24 \text{ mA}$			0.5	V
I_{CCH}	Power Supply Current		10	25	35	mA
I_{CCL}	Power Supply Current		15	34	40	mA
I_{OS}	Output Short Circuit Current		-50		-150	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

Table 6. AC CHARACTERISTICS ($V_{CC} = 3.0 \text{ V}$ to 3.6 V ; $GND = 0.0 \text{ V}$ (Note 5))

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{\max}$	Maximum Frequency (Figure 2)	275	350		275	350		275	350		MHz
t_{PLH} , t_{PHL}	Propagation Delay to Output Differential (Note 6)	1.2	1.5	2.0	1.2	1.5	2.0	1.3	1.7	2.2	ns
t_{SK+} , t_{SK-} , t_{SKPP}	Within Device Skew + + Within Device Skew - - Device-to-Device Skew (Note 7)		15	60		15	60		20	85	ps
t_{JITTER}	Random Clock Jitter (RMS) (Figure 2) @ $\leq 200 \text{ MHz}$ @ $> 200 \text{ MHz}$		6	30		6	30		6	30	ps
V_{PP}	Input Voltage Swing (Differential Configuration)	150	800	1200	150	800	1200	150	800	1200	mV
t_r , t_f	Output Rise/Fall Times (0.8 V–2.0 V) Q , $\bar{Q}$	330	600	950	330	600	950	330	650	950	ps

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

5. Measured with a 750 mV 50% duty-cycle clock source. $R_L = 500 \Omega$ to GND and $C_L = 20 \text{ pF}$ to GND. Refer to Figure 3.

6. Reference ($V_{CC} = 3.3 \text{ V} \pm 5\%$; $GND = 0 \text{ V}$)

7. Skews are measured between outputs under identical transitions.

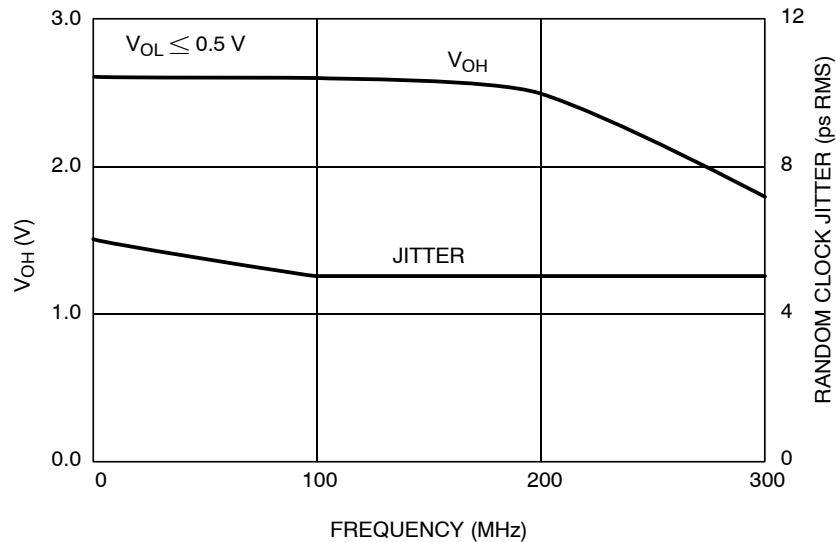


Figure 2. Typical V_{OH} / Jitter versus Frequency (25°C)



MC100EPT26

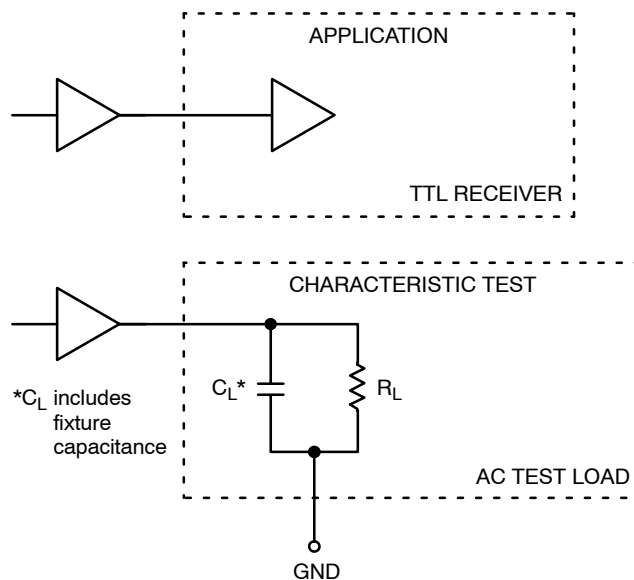


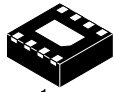
Figure 3. TTL Output Loading Used for Device Evaluation

Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

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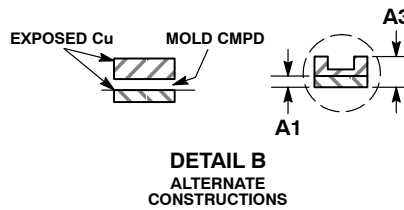
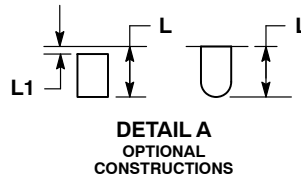
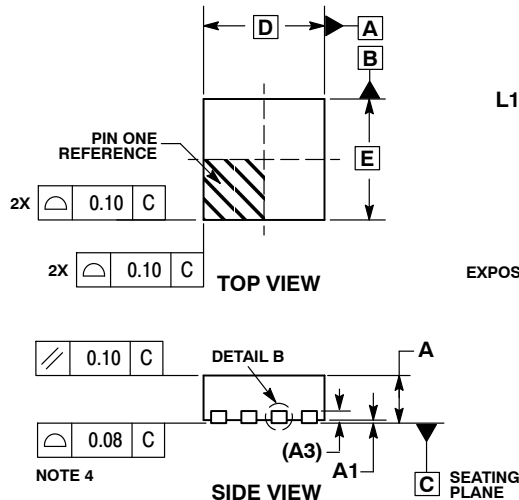




SCALE 4:1

DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

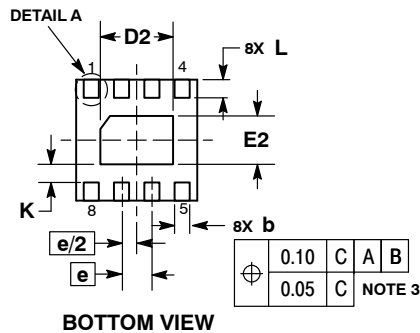
DATE 04 MAY 2016



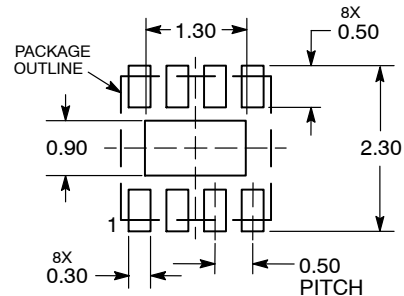
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.30	REF
L	0.25	0.35
L1		0.10



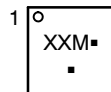
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

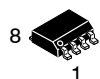


XX = Specific Device Code
M = Date Code
▪ = Pb-Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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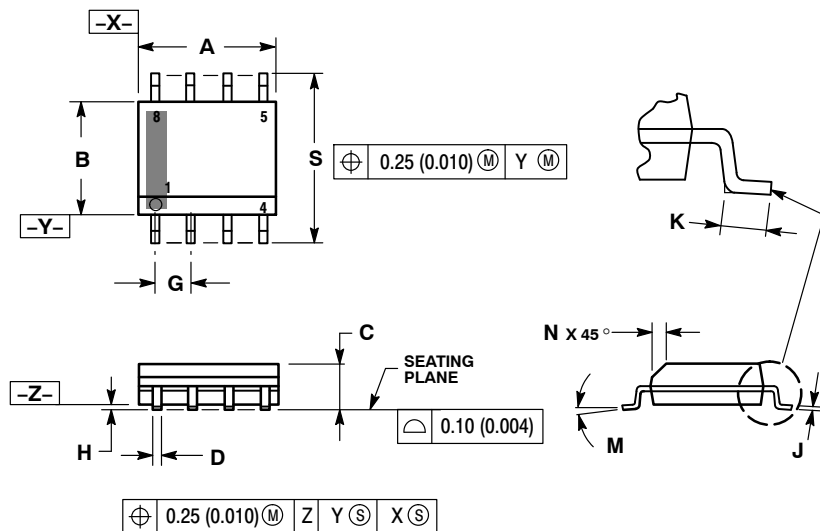
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CASE 751-07
ISSUE AK

DATE 16 FEB 2011

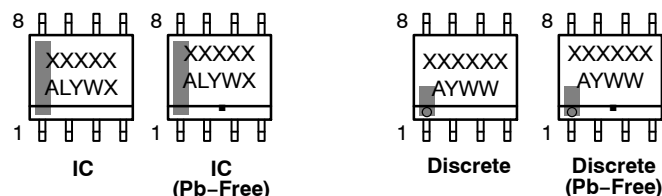
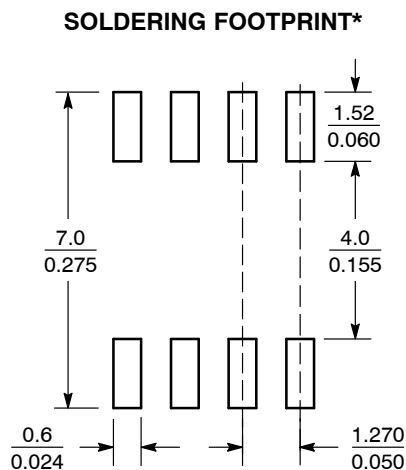


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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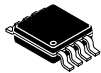
SOIC-8 NB
CASE 751-07
ISSUE AK

DATE 16 FEB 2011

STYLE 1: PIN 1. EMITTER 2. COLLECTOR 3. COLLECTOR 4. EMITTER 5. EMITTER 6. BASE 7. BASE 8. EMITTER	STYLE 2: PIN 1. COLLECTOR, DIE, #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. BASE, #2 6. EMITTER, #2 7. BASE, #1 8. EMITTER, #1	STYLE 3: PIN 1. DRAIN, DIE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. GATE, #2 6. SOURCE, #2 7. GATE, #1 8. SOURCE, #1	STYLE 4: PIN 1. ANODE 2. ANODE 3. ANODE 4. ANODE 5. ANODE 6. ANODE 7. ANODE 8. COMMON CATHODE
STYLE 5: PIN 1. DRAIN 2. DRAIN 3. DRAIN 4. DRAIN 5. GATE 6. GATE 7. SOURCE 8. SOURCE	STYLE 6: PIN 1. SOURCE 2. DRAIN 3. DRAIN 4. SOURCE 5. SOURCE 6. GATE 7. GATE 8. SOURCE	STYLE 7: PIN 1. INPUT 2. EXTERNAL BYPASS 3. THIRD STAGE SOURCE 4. GROUND 5. DRAIN 6. GATE 3 7. SECOND STAGE Vd 8. FIRST STAGE Vd	STYLE 8: PIN 1. COLLECTOR, DIE #1 2. BASE, #1 3. BASE, #2 4. COLLECTOR, #2 5. COLLECTOR, #2 6. EMITTER, #2 7. EMITTER, #1 8. COLLECTOR, #1
STYLE 9: PIN 1. EMITTER, COMMON 2. COLLECTOR, DIE #1 3. COLLECTOR, DIE #2 4. EMITTER, COMMON 5. EMITTER, COMMON 6. BASE, DIE #2 7. BASE, DIE #1 8. EMITTER, COMMON	STYLE 10: PIN 1. GROUND 2. BIAS 1 3. OUTPUT 4. GROUND 5. GROUND 6. BIAS 2 7. INPUT 8. GROUND	STYLE 11: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. DRAIN 2 7. DRAIN 1 8. DRAIN 1	STYLE 12: PIN 1. SOURCE 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 13: PIN 1. N.C. 2. SOURCE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN	STYLE 14: PIN 1. N-SOURCE 2. N-GATE 3. P-SOURCE 4. P-GATE 5. P-DRAIN 6. P-DRAIN 7. N-DRAIN 8. N-DRAIN	STYLE 15: PIN 1. ANODE 1 2. ANODE 1 3. ANODE 1 4. ANODE 1 5. CATHODE, COMMON 6. CATHODE, COMMON 7. CATHODE, COMMON 8. CATHODE, COMMON	STYLE 16: PIN 1. EMITTER, DIE #1 2. BASE, DIE #1 3. EMITTER, DIE #2 4. BASE, DIE #2 5. COLLECTOR, DIE #2 6. COLLECTOR, DIE #2 7. COLLECTOR, DIE #1 8. COLLECTOR, DIE #1
STYLE 17: PIN 1. VCC 2. V2OUT 3. V1OUT 4. TXE 5. RXE 6. VEE 7. GND 8. ACC	STYLE 18: PIN 1. ANODE 2. ANODE 3. SOURCE 4. GATE 5. DRAIN 6. DRAIN 7. CATHODE 8. CATHODE	STYLE 19: PIN 1. SOURCE 1 2. GATE 1 3. SOURCE 2 4. GATE 2 5. DRAIN 2 6. MIRROR 2 7. DRAIN 1 8. MIRROR 1	STYLE 20: PIN 1. SOURCE (N) 2. GATE (N) 3. SOURCE (P) 4. GATE (P) 5. DRAIN 6. DRAIN 7. DRAIN 8. DRAIN
STYLE 21: PIN 1. CATHODE 1 2. CATHODE 2 3. CATHODE 3 4. CATHODE 4 5. CATHODE 5 6. COMMON ANODE 7. COMMON ANODE 8. CATHODE 6	STYLE 22: PIN 1. I/O LINE 1 2. COMMON CATHODE/VCC 3. COMMON CATHODE/VCC 4. I/O LINE 3 5. COMMON ANODE/GND 6. I/O LINE 4 7. I/O LINE 5 8. COMMON ANODE/GND	STYLE 23: PIN 1. LINE 1 IN 2. COMMON ANODE/GND 3. COMMON ANODE/GND 4. LINE 2 IN 5. LINE 2 OUT 6. COMMON ANODE/GND 7. COMMON ANODE/GND 8. LINE 1 OUT	STYLE 24: PIN 1. BASE 2. EMITTER 3. COLLECTOR/ANODE 4. COLLECTOR/ANODE 5. CATHODE 6. CATHODE 7. COLLECTOR/ANODE 8. COLLECTOR/ANODE
STYLE 25: PIN 1. VIN 2. N/C 3. REXT 4. GND 5. IOUT 6. IOUT 7. IOUT 8. IOUT	STYLE 26: PIN 1. GND 2. dv/dt 3. ENABLE 4. ILIMIT 5. SOURCE 6. SOURCE 7. SOURCE 8. VCC	STYLE 27: PIN 1. ILIMIT 2. OVLO 3. UVLO 4. INPUT+ 5. SOURCE 6. SOURCE 7. SOURCE 8. DRAIN	STYLE 28: PIN 1. SW_TO_GND 2. DASIC_OFF 3. DASIC_SW_DET 4. GND 5. V_MON 6. VBULK 7. VBULK 8. VIN
STYLE 29: PIN 1. BASE, DIE #1 2. EMITTER, #1 3. BASE, #2 4. EMITTER, #2 5. COLLECTOR, #2 6. COLLECTOR, #2 7. COLLECTOR, #1 8. COLLECTOR, #1	STYLE 30: PIN 1. DRAIN 1 2. DRAIN 1 3. GATE 2 4. SOURCE 2 5. SOURCE 1/DRAIN 2 6. SOURCE 1/DRAIN 2 7. SOURCE 1/DRAIN 2 8. GATE 1		

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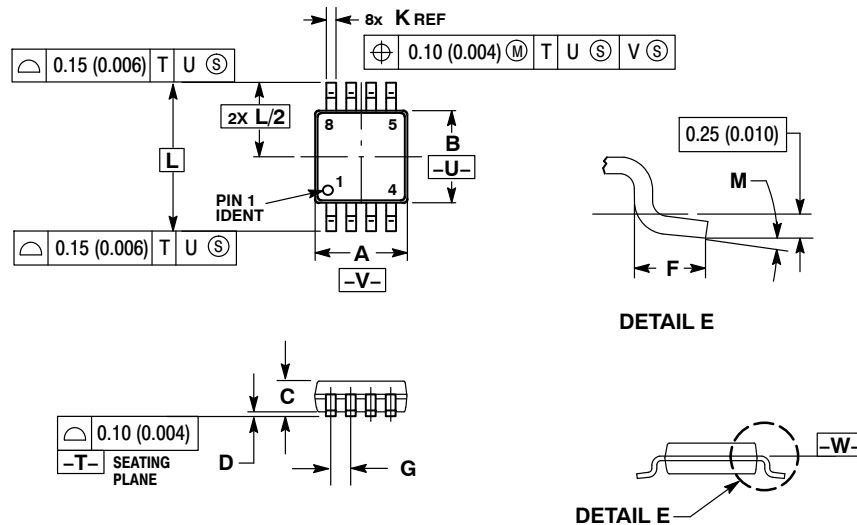
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SCALE 2:1

TSSOP-8 3.00x3.00x0.95
CASE 948R-02
ISSUE A

DATE 07 APR 2000



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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