PI3HDX511D

Ultra-Low Power HDMI 1.4b Redriver/DP Level Shifter (2.5x4.5mm package)

Features

- Ultra-low power HDMI 1.4b compliant Redriver and DisplayPort dual mode Level Shifter
- Operation up to 3.4 Gbps data rate per lane
- Max 4K resolution (4096x2160 at 30fps), 48-bit per pixel Deep Color supports
- Standby current typical 2uA with DDC passive switch mode condition
- Flexible three steps equalization control (2.5, 5, 7.5 dB) and Pre-emphasis control steps (0, 1.5, 2.5 dB)
- Automatic output squelch and HPD function for power saving states management
- DC coupled or AC coupled differential input
- Integrated DDC level shifter
- Single power supply: 3.3V
- Integrated ESD protection on I/O pins: 8kV contact and 8kV HBM
- Package: 30-pin QFN(ZL30, 2.5x4.5mm)

Description

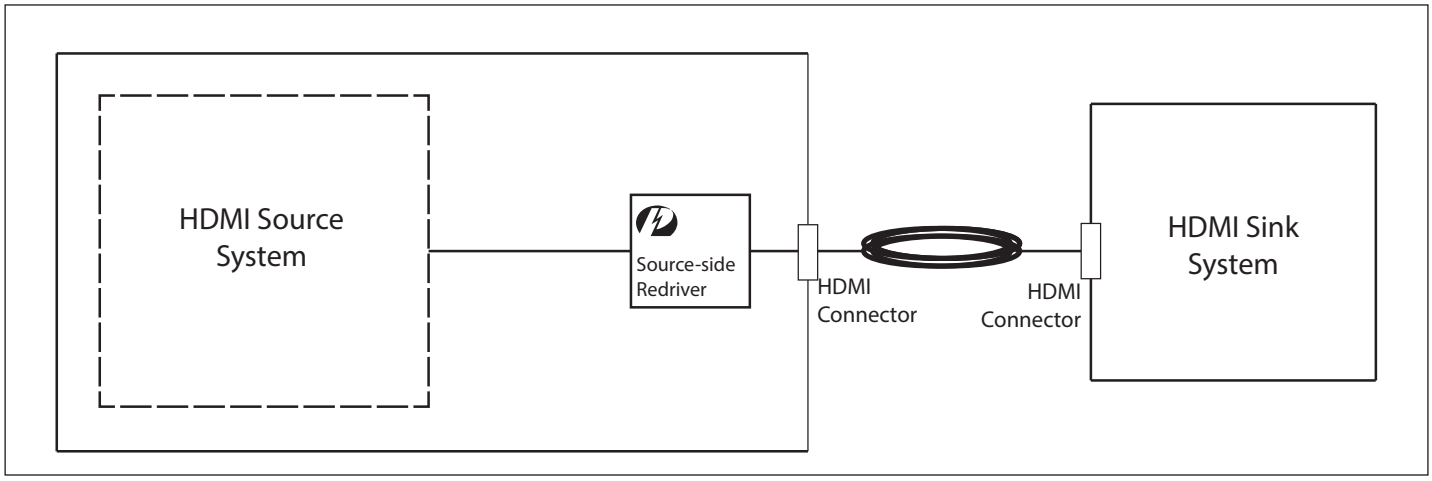
PI3HDX511D is a HDMI 1.4b Redriver and DisplayPort dual mode Level Shifter with compact QFN package(2.5x4.5mm). Ultra-low power consumption with small foot print is ideal solution to extend system's battery operation hours for the mobility system with extremely space constraint form factors.

In addition, it also supports smart power states managements function with squelch/HPD detection function, automatically disable TMDS signal outputs with no TMDS data/clock input signal presents.

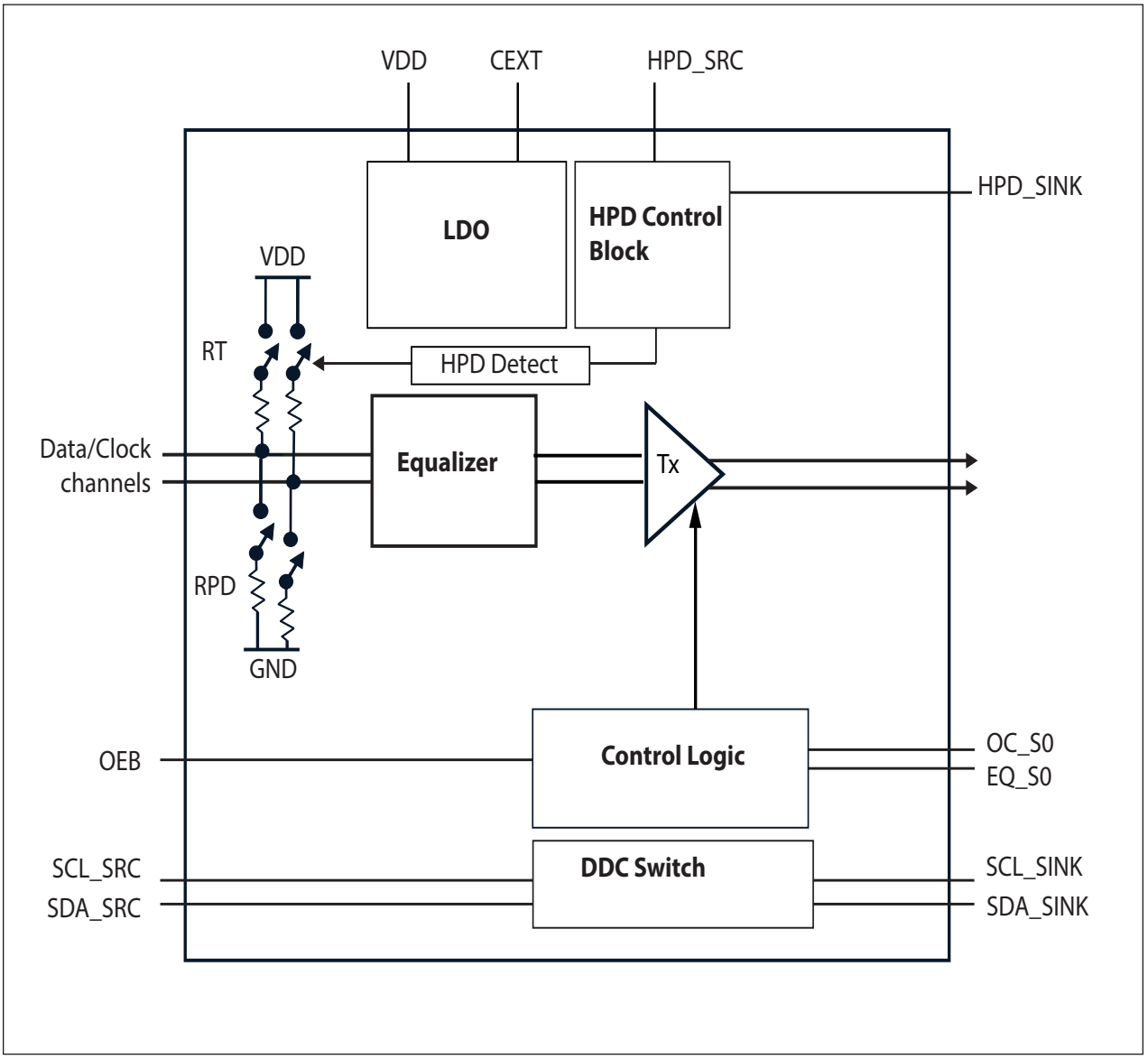
Application

- Notebook/Tablet computers
- Active Cable, Dongle

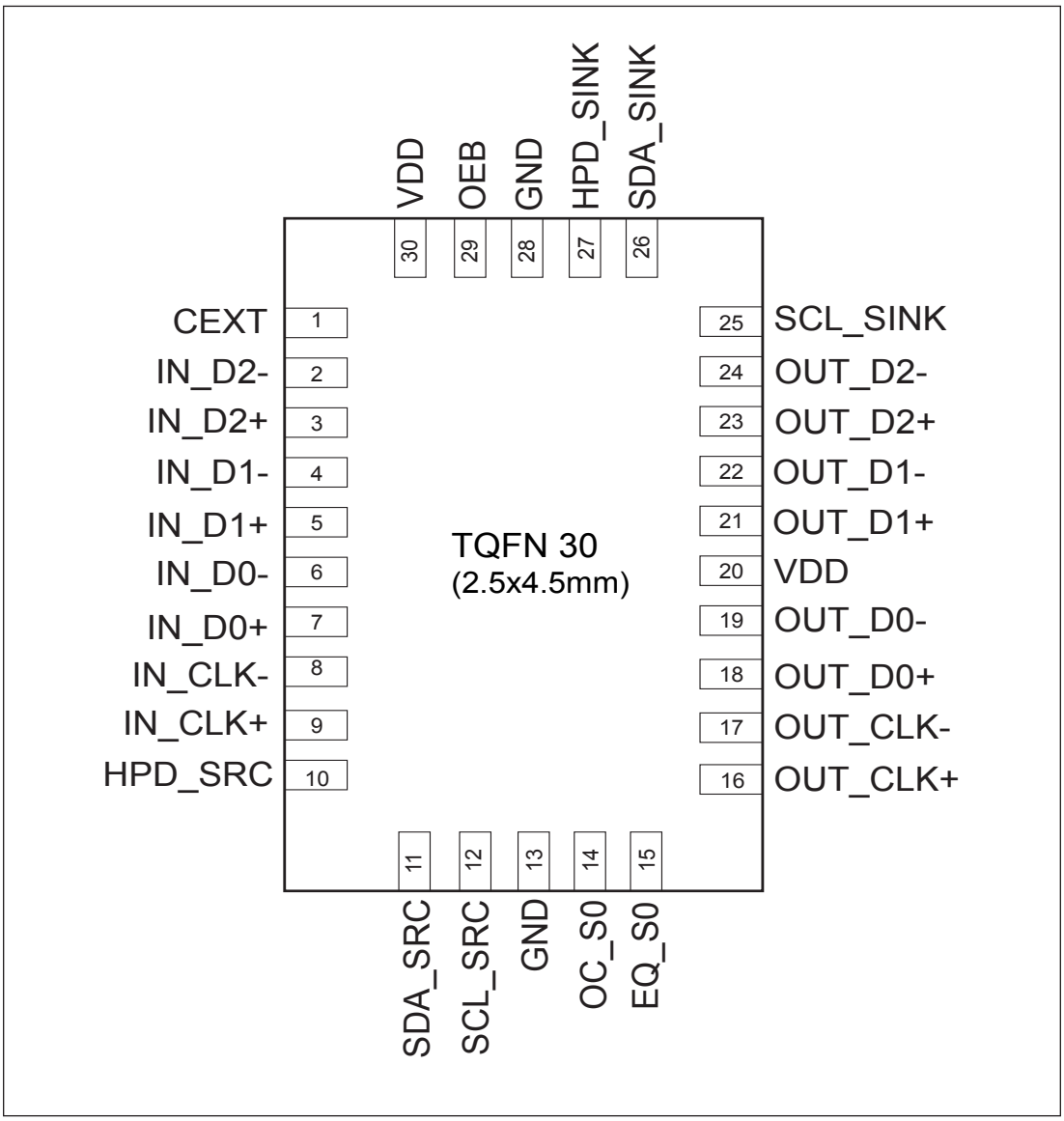
Typical Application Block Diagram



Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type	Description
20, 30	VDD	PWR	3.3V power supply. Add external 0.1uF decoupling capacitor to GND
1	CEXT	PWR	LDO output for internal core supplier. Add external capacitor (2.2uF-4.7uF) to GND
13, 28	GND	GND	Ground
27	HPD_SINK	I	Sink side hot plug detector; internal pull-down at 120 Kohm.
10	HPD_SRC	O	HPD output to source side
2 3 4 5 6 7 8 9	IN_D2- IN_D2+ IN_D1- IN_D1+ IN_D0- IN_D0+ IN_CLK- IN_CLK+	I	TMDS inputs. RT=50Ohm; RPD=200Kohm.
24 23 22 21 20 19 18 17 16	OUT_D2- OUT_D2+ OUT_D1- OUT_D1+ OUT_D0- OUT_D0+ OUT_CLK- OUT_CLK+	O	TMDS outputs.
12	SCL_SRC	IO	Source side DDC Clock
11	SDA_SRC	IO	Source side DDC Data
25	SCL_SINK	IO	Sink side DDC Clock for connector
26	SDA_SINK	IO	Sink side DDC Data for connector
14	OC_S0	I	TMDS output three-level pre-emphasis selection. Internal 50% of VDD
15	EQ_S0	I	TMDS input three-level equalization selection. Internal 50% of VDD
29	OEB	I	Output Enable control. Active "Low". Internal 100 Kohm pull-down.

Functional Description

Squelch

Automatic output squelch function disables TMDS output when no Input signal presents. Output Disable (Squelch) Mode uses TMDS Clock channel signal detection. When low voltage levels on the TMDS input clock signals are detected, Squelch state enables and TMDS output port signals shall disable; when the TMDS clock input signal levels are above a pre-determined threshold voltage, output ports shall return to the normal voltage swing levels.

Hot Plug Detect Sink HPD_SINK Shut Down

When HPD_SINK pin is floating or tie to GND, TMDS outputs shall shut down to sleep mode; HPD_SINK does not control DDC channel.

Pre-emphasis Control OC_S0 Truth Table

Output pre-emphasis setting	Functional Description	
OC_S0	Single-end Vswing	Pre-emphasis
"0"	500 mV	0 dB
"NC" or VDD/2	500 mV	1.5 dB
"1"	500 mV	2.5 dB

TMDS Data channel EQ Truth Table

EQ_S0	Functional Description	Note
"0"	2.5 dB	TMDS Clock(CLK) channel EQ is always fixed as 3dB without pre-emphasis.
"NC" or VDD/2	5 dB	
"1"	7.5 dB	

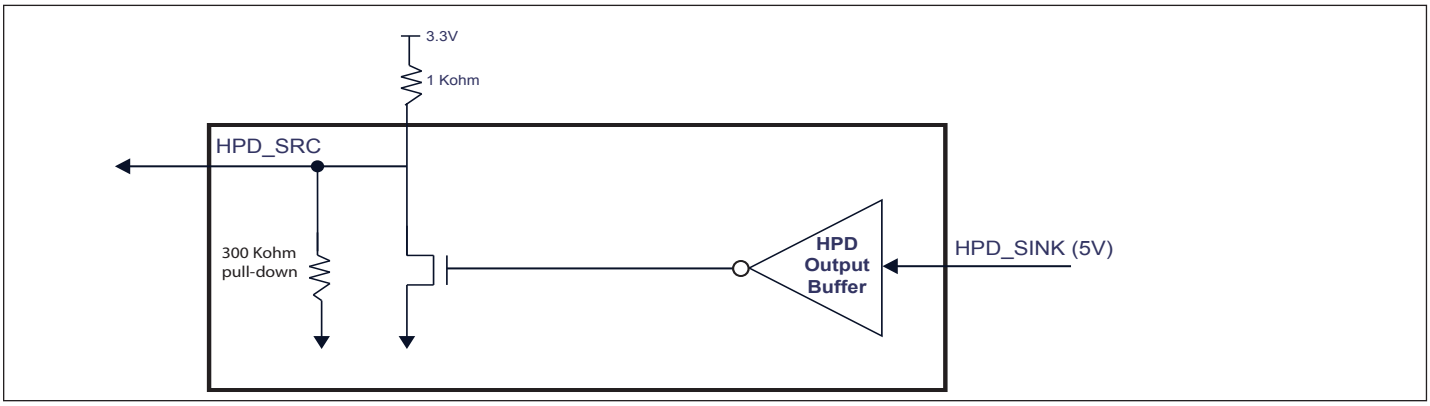
OEB Truth Table

OEB	Functional Description
"0"	Normal operation mode
"1"	Power down mode

Sink side Hot Plug Detect HPD_SINK Truth Table

HPD_SINK	Functional Description
"1"	Normal mode
"0"	Disable output signal for power saving mode

Source side HPD_SRC Output Diagram



Note:
(1). Open drain buffer is recommended with external pull-up resistor to < 4.5V power supply.

Absolute Maximum Ratings

Item	Absolute Rating*1
Supply Voltage to Ground Potential	4.5V
All Inputs and Outputs	-0.5V to 4.5V
5V tolerance I/O (SDA_SINK,SCL_SINK,HPD_SINK)	-0.5v to 5.5V
Storage Temperature	-65 to +150°C
Junction Temperature	125°C
Soldering Temperature	260°C

Note *1) Stress beyond those lists under "Absolute Maximum Ratings" may cause permanent damage to the device

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient Operating Temperature	-20	25	85	°C
Power Supply Voltage (measured in respect to GND)	2.89	3.3	3.6	V

DC Specification (VDD = 3.3V ±10%)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
IDD	VDD Supply Current	Output Enable (500mV single-end 0dB pre-emphasis, AC coupling Input)		80	100	mA
ISTB	Standby current	VDD=3.6V, DDC passive switch, HPD_SINK= "0" or OEB = "1"		2	20	uA
ISQLH	Squelch current	VDD=3.6V, DDC passive switch, HPD_SINK=3.6V		2.7	4	mA

HPD pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
HPD_SRC pin						
VOL	Output Low Voltage	IOL = 4 mA	0		0.4	V
IOFF	Off leakage current	VDD = 0V, VIN=3.6V			25	uA
IOZ	Output leakage current	VDD = 3.6V, VIN=3.6V			25	
HPD_SINK pin						
IIH	High level digital input current	VIH =5.5V	-10		80	µA
IIL	Low level digital input current	VIL = GND	-10		10	µA
VIH	High level digital input voltage	VDD=3.3V	2.0			V
VIL	Low level digital input voltage	VDD=3.3V	0		0.8	V

Control pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Control pin (OEB with 100 Kohm pull to GND)						
IIH	High level digital input current	VIH =3.3V	-10		40	µA
IIL	Low level digital input current	VIL = GND	-10		10	µA
VIH	High level digital input voltage	VDD=3.3V	2.0			V
VIL	Low level digital input voltage	VDD=3.3V	0		0.8	V
Control pins (EQ_S0, OC_S0 with 100 Kohm pull high and 100 Kohm pull low when TMDS active)						
IIH	High level digital input current	VIH =VDD	-10		40	µA
IIL	Low level digital input current	VIL = GND, VDD=3.3V	-40		10	µA

DDC channel switch

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
ILK	Input leakage current	VIN=5.5V	-10		30	uA
CIO	Input/Output capacitance when passive switch is on	VI peak-peak = 1V, 100 KHz		10		pF
RON	Passive Switch resistance	IO = 3mA, VO = 0.4V		30	50	Ω
VPASS	Switch Output voltage	VI=3.3V, II=100uA, VDD=3.3V	1.5	2.0	2.5	V

TMDS differential pins

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VOH	Single-ended high level output voltage	VDD = 3.3V, ROUT=50Ω	VDD-10		VDD+10	mV
VOL	Single-ended low level output voltage		VDD-600		VDD–400	mV
VSWING	Single-ended output swing voltage		400		600	mV
VOD(O)(1)	Overshoot of output differential voltage				180*1	mV
VOD(U)(2)	Undershoot of output differential voltage				200*2	mV
VOC(SS)	Change in steady-state common- mode output voltage between logic states				5	mV
IOS	Short Circuit output current	Short to VDD	-12		12	mA
RT	Input termination resistance	VIN = 2.9V	45	50	55	Ω
IOZ	Leakage current with high impedance I/O	VDD = 3.6V, VIN = 3.6V			30	µA

Note:

(1) Overshoot of output differential voltage VOD(O) = (VSWING(MAX) * 2) * 15%

(2) Undershoot of output differential voltage VOD(O) = (VSWING(MIN) * 2) * 25%

TMDS differential pins

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
tPD	Propagation delay	VDD = 3.3V, Rout = 50Ω			2000	ps
tR/tF	Differential output signal rise/fall time (20% to 80%). 0dB pre-emphasis			140		
	Differential output signal rise/fall time (20% - 80%). 2.5dB pre-emphasis			115		
tSK(P)	Pulse skew			10	50	
tSK(D)	Intra-pair +/- differential skew			23	50	
tSK(O)	Inter-pair channel to channel differential skew				100	
tJIT(PP)	Peak-to-peak output Clock residual jitter	Data Input = 3.4 Gbps HDMI data patterns		30	60	
tJIT(PP)	Peak-to-peak output Data residual jitter			40	70	
tEN	Enable time	VDD=3.3V			50	us
tDIS	Disable time	VDD=3.3V			20	ns

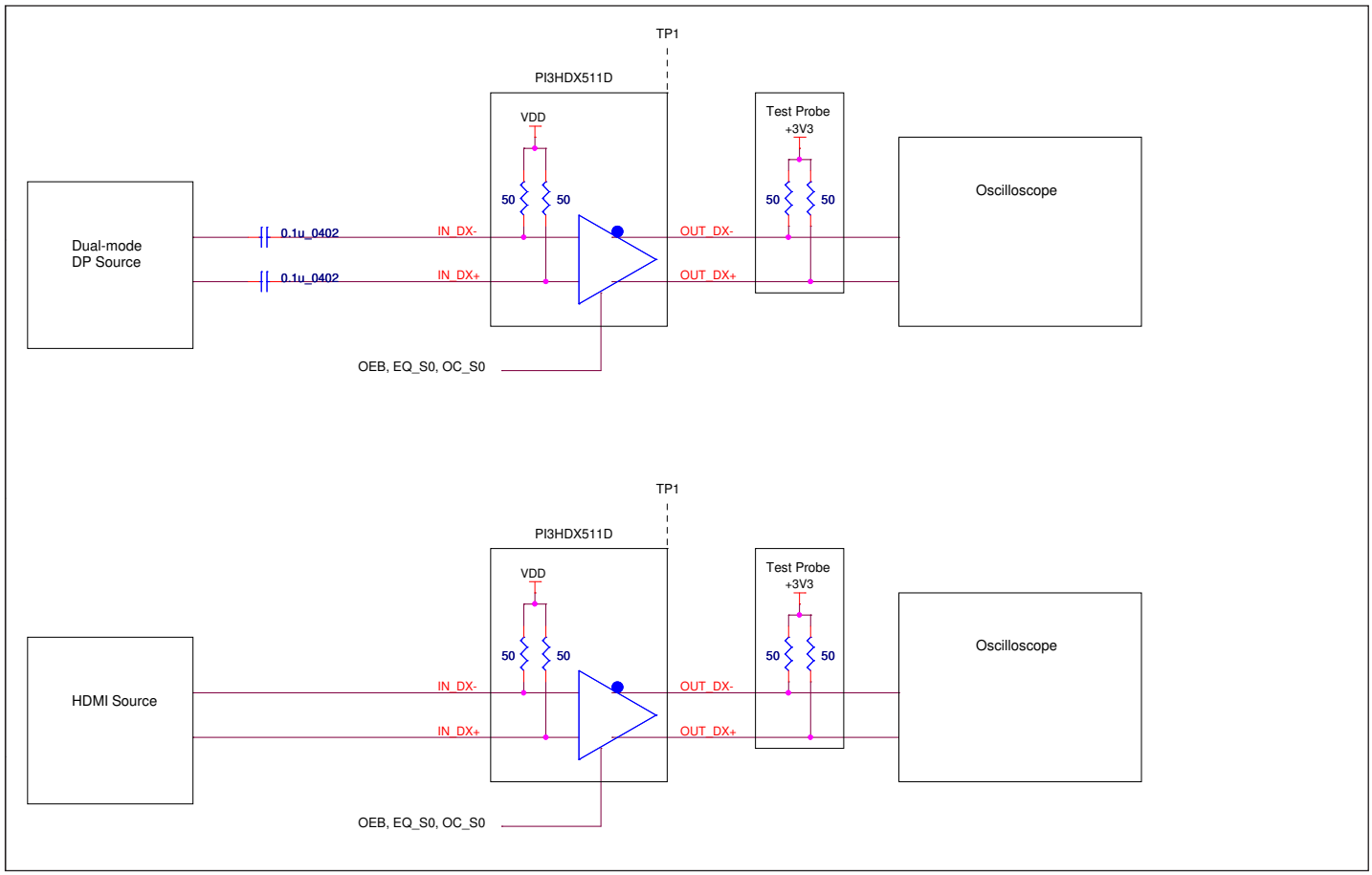
DDC I/O Pins (passive switch)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
tPD(DDC)	Propagation delay	CL = 10pF			5	ns

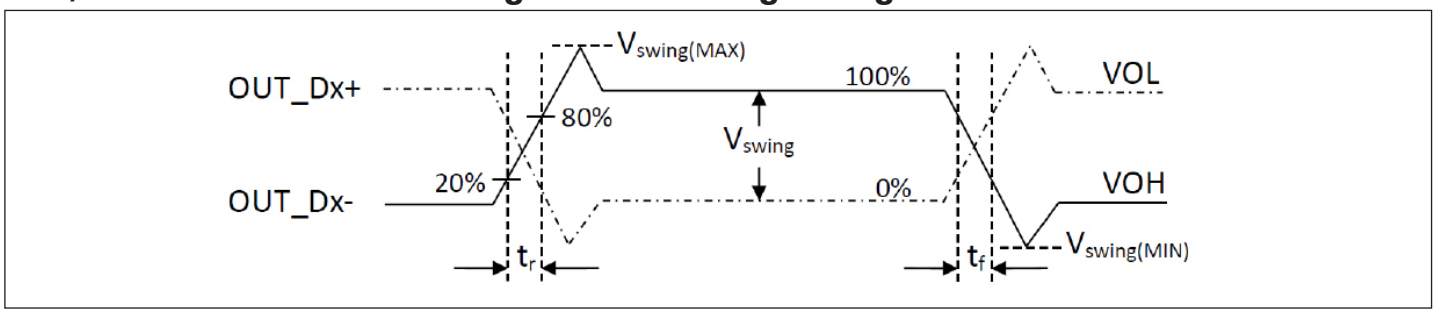
Control and Status Pins (HPD_SINK, HPD_SRC)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
tPD(HPD)	Propagation delay from HPD_SINK to HPD_SRC , HIGH to LOW	CL = 10pF, Pull HIGH resistor 1kΩ for open drain output		10		ns

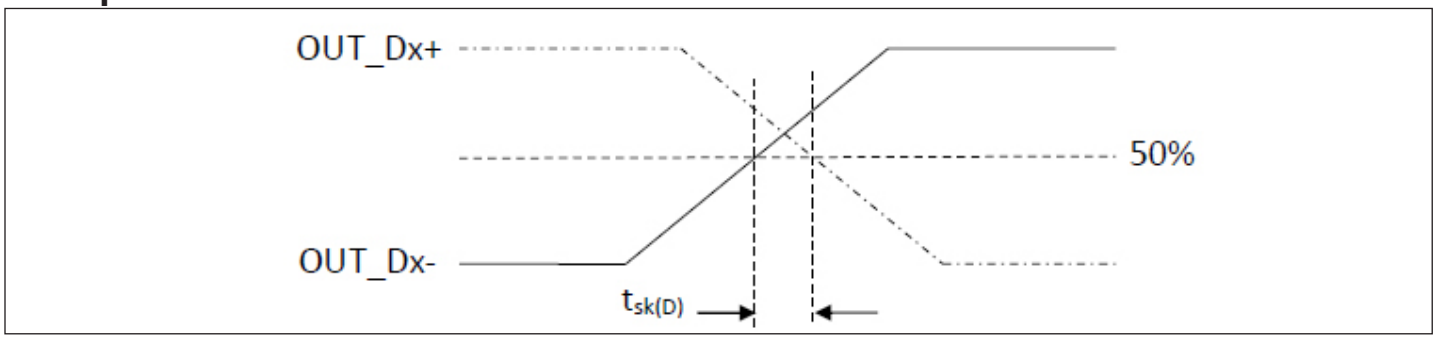
TMDS Input Measurement Test Setup



Rise/Fall Time Definition at Single-ended Swing Voltage

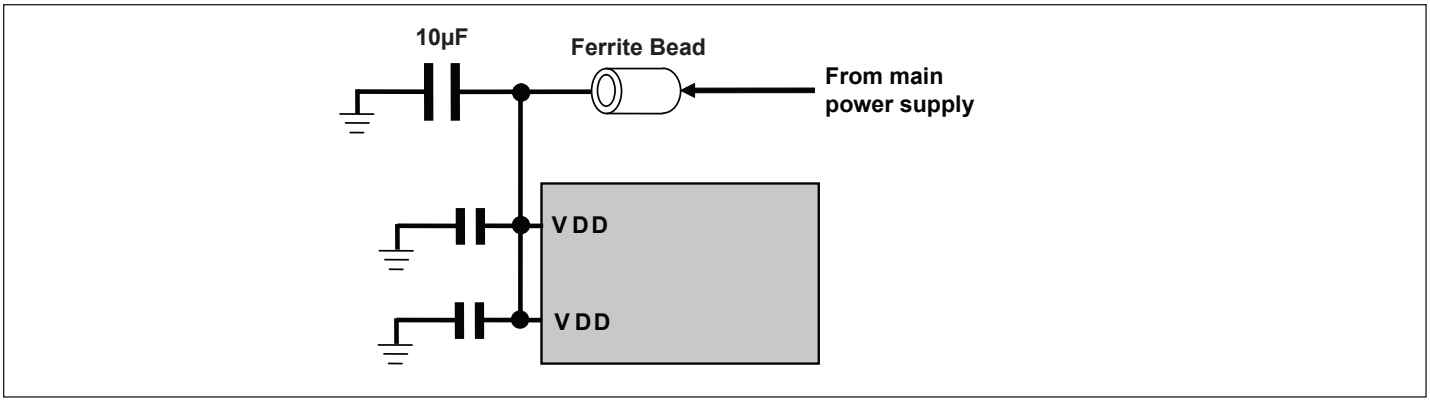


Intra-pair Skew Definition



Decoupling Capacitors near VDD Pins

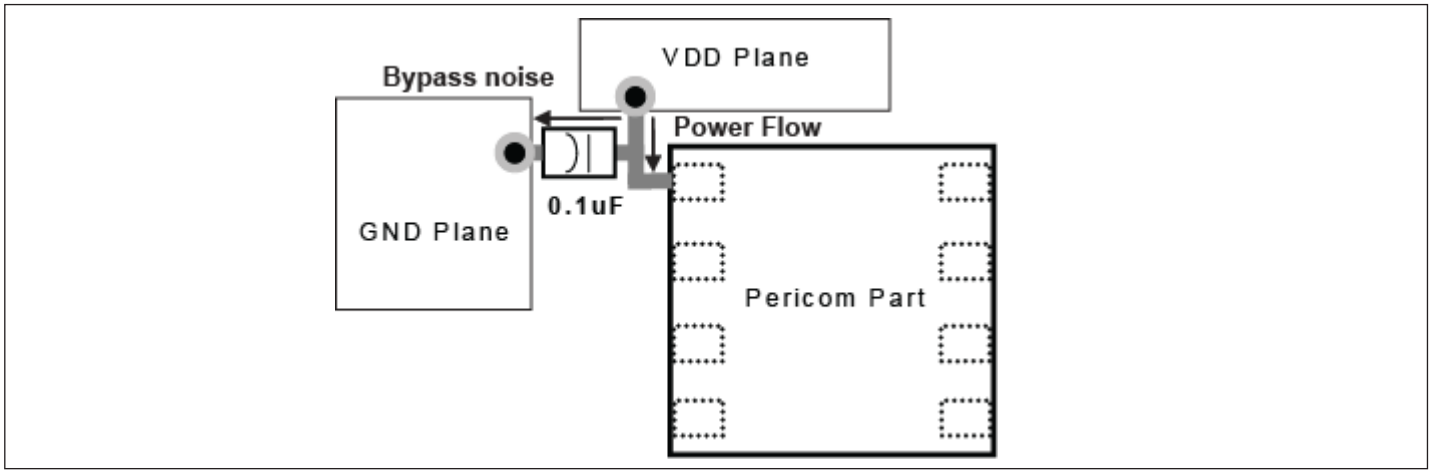
Each VDD pins requires to add 0.1 µF and 10µF decoupling capacitors with optional Ferrite bead in order to isolate the power supply from the other circuitry. The capacitor material do not have special requirements. Ceramic capacitors are generally recommended with X5R or X7R materials.



Decoupling Capacitors and Ferrite Bead near VDD Pins

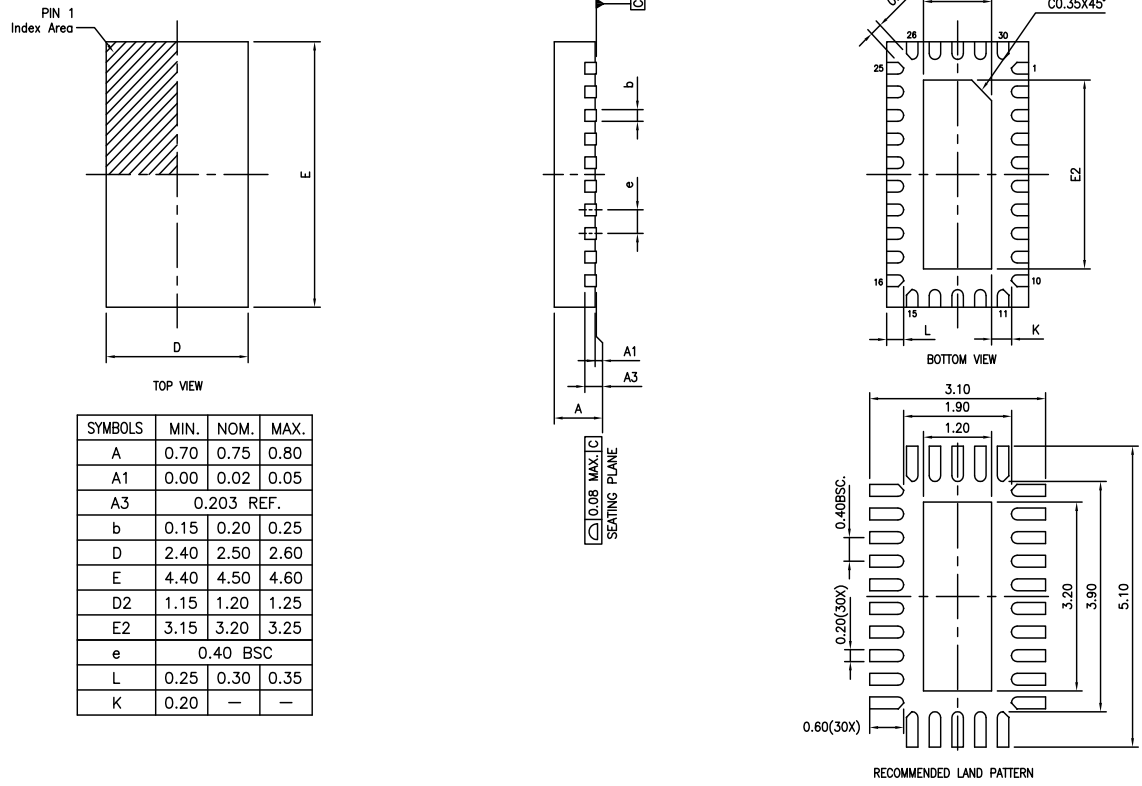
Decoupling Capacitors in PCB Layout

- ➔ Each 0.1 µF decoupling capacitor should be placed as close as possible to each VDD pin.
- ➔ VDD and GND planes should be used to provide a low impedance path for power and ground.
- ➔ Via holes should be placed to connect to VDD and GND planes directly.
- ➔ Trace should be as wide and short as possible.
- ➔ The placement of decoupling capacitor and the way of routing trace should consider the power flowing criteria.
- ➔ 10 µF Capacitor should also be placed closed to our part and should be placed in the middle location of 0.1 µF capacitors.
- ➔ Avoid the large current circuit placed close to our part; especially when it is shared the same VDD and GND planes. Since large current flowing on our VDD or GND planes will generate a potential variation on the VDD or GND of our part.



Decoupling Capacitor location in PCB design

Packaging Mechanical: 30-Contact TQFN (ZL)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	2.40	2.50	2.60
E	4.40	4.50	4.60
D2	1.15	1.20	1.25
E2	3.15	3.20	3.25
e		0.40 BSC	
L	0.25	0.30	0.35
K	0.20	—	—

Notes:
1. All dimensions are in mm. Angles in degrees.
2. Refer JEDEC MO-220.
3. Recommended land pattern is for reference only.

PERICOM Enabling Serial Connectivity

DATE: 10/21/13

DESCRIPTION: 30-contact, Thin Fine Pitch Quad Flat No lead Package (TQFN)

PACKAGE CODE: ZL

DOCUMENT CONTROL #: PD-2172 **REVISION: --**

14-0006

Please check for the latest package information on the Pericom web site at www.pericom.com/support/packaging.

Ordering Information

Ordering Number	Package Code	Package Description
PI3HDX511DZLE	ZL	30-Contact, Thin Fine Pitch Quad Flat No Lead Package (TQFN)

• Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

• E = Pb-free and Green

• X suffix = Tape/Reel

Related Products

Part Number	Product Description
PI3WVR12612	Wide Voltage Range DisplayPort™ & HDMI Video Switch
PI3HDX1204-B	HDMI2.0 Redriver and Displayport Level Shifter for 6Gbps Application
PI3EQXDP1201	Displayport 1.2 redriver with built-in auto test mode
PI3HDX414	1:4 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX412BD	1:2 Active 3.4Gbps HDMI1.4b Splitter/DeMux with Signal Conditioning
PI3HDX621	2:1 Active 3.4Gbps HDMI 1.4b Switch
PI3HDMI336	3:1 Active 2.5Gbps HDMI Switch with I2C control and ARC Transmitter

Reference Information

Document	Description
HDMI1.4	High-Definition Multimedia Interface Specification Version 1.4, HDMI Licensing, LLC