40V +175°C N-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C
40V	11.5mΩ @ V_{GS} = 10V	11.6A
	18mΩ @ V_{GS} = 4.5V	9.3A

Description

This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(ON)}$) yet maintain superior switching performance, making it ideal for high-efficiency power-management applications.

- Power-management functions
- DC-DC converters
- Backlighting

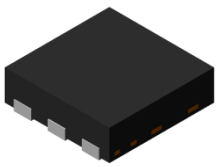
Features

- Rated to +175°C – Ideal for High Ambient Temperature Environments
- 100% Unclamped Inductive Switching, Test in Production – Ensures More Reliable and Robust End Application
- Low $R_{DS(ON)}$ – Ensures On-State Losses Are Minimized
- 0.6mm Profile – Ideal for Low Profile Applications
- PCB Footprint of 4mm^2
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **This part is qualified to JEDEC standards (as references in AEC-Q) for High Reliability. https://www.diodes.com/quality/product-definitions/**
- **An automotive-compliant part is available under a separate datasheet (DMTH4008LFDFWQ)**

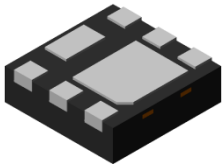
Mechanical Data

- Package: U-DFN2020-6
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish - Matte Tin Annealed over Copper Leadframe; Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.007 grams (Approximate)

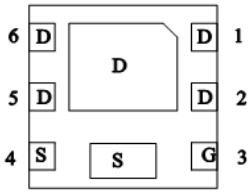
U-DFN2020-6/SWP (Type F)



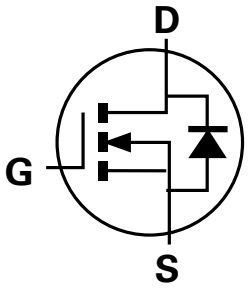
Top View



Bottom View



Pinout
Bottom View



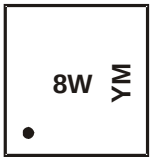
Internal Schematic

Ordering Information (Note 4)

Orderable Part Number	Package	Packing	
		Qty.	Carrier
DMTH4008LFDFW-7	U-DFN2020-6/SWP (Type F)	3,000	Reel
DMTH4008LFDFW-13	U-DFN2020-6/SWP (Type F)	10,000	Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



8W = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: M = 2025)
M = Month (ex: 9 = September)

Date Code Key

Year	2018	-	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034
Code	F	-	M	N	P	R	S	T	U	V	W	X

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic		Symbol	Value	Unit
Drain-Source Voltage		V_{DSS}	40	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current (Note 7) V_{GS} = 10V	T_A = +25°C T_A = +100°C	I_D	11.6 8.2	A
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%)		I_{DM}	80	A
Continuous Source-Drain Diode Current (Note 7)		I_S	2.55	A
Pulsed Source-Drain Diode Current (10µs Pulse, Duty Cycle = 1%)		I_{SM}	80	A
Avalanche Current, L = 0.3mH (Note 8)		I_{AS}	14.7	A
Avalanche Energy, L = 0.3mH (Note 8)		E_{AS}	32.4	mJ

Thermal Characteristics

Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T_A = +25°C	P_D	0.99	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	153	°C/W
Total Power Dissipation (Note 6)	T_A = +25°C	P_D	2.35	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	$R_{\theta JA}$	64.5	°C/W
Thermal Resistance, Junction to Case (Note 7)	T_C = +25°C	$R_{\theta JC}$	14.8	°C/W
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +175	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	V_{GS} = 0V, I_D = 250µA
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	µA	V_{DS} = 32V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(TH)}$	1	1.7	3	V	V_{DS} = V_{GS}, I_D = 250µA
Static Drain-Source On-Resistance	$R_{DS(ON)}$	—	9.1	11.5	mΩ	V_{GS} = 10V, I_D = 10A
			12.9	18		V_{GS} = 4.5V, I_D = 8.5A
Diode Forward Voltage	V_{SD}	—	0.8	1.0	V	V_{GS} = 0V, I_S = 10A
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	—	1030	—	pF	V_{DS} = 20V, V_{GS} = 0V, f = 1MHz
Output Capacitance	C_{oss}	—	324	—		
Reverse Transfer Capacitance	C_{rss}	—	27	—		
Gate Resistance	R_g	—	1.82	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (V_{GS} = 4.5V)	Q_g	—	6.8	—	nC	V_{DD} = 20V, I_D = 10A
Total Gate Charge (V_{GS} = 10V)	Q_g	—	14.2	—		
Gate-Source Charge	Q_{gs}	—	2.0	—		
Gate-Drain Charge	Q_{gd}	—	2.7	—		
Turn-On Delay Time	$t_{D(ON)}$	—	3.1	—	ns	V_{DD} = 20V, V_{GS} = 10V, R_g = 6Ω, I_D = 10A
Turn-On Rise Time	t_R	—	3.1	—		
Turn-Off Delay Time	$t_{D(OFF)}$	—	14.2	—		
Turn-Off Fall Time	t_F	—	5.8	—		
Reverse-Recovery Time	t_{RR}	—	19.6	—	ns	I_F = 10A, di/dt = 100A/µs
Reverse-Recovery Charge	Q_{RR}	—	8.2	—	nC	

Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
7. Thermal resistance from junction to soldering point (on the exposed drain pad).
8. I_{AS} and E_{AS} ratings are based on low frequency and duty cycles to keep T_J =+ 25°C.
9. Short duration pulse test used to minimize self-heating effect.
10. Guaranteed by design. Not subject to product testing.

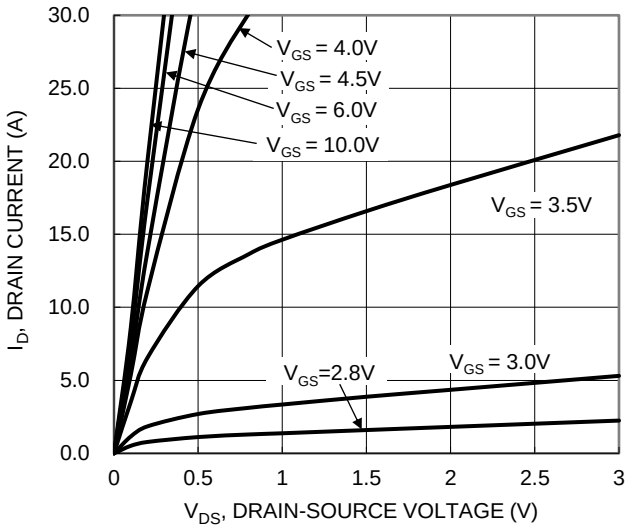


Figure 1. Typical Output Characteristic

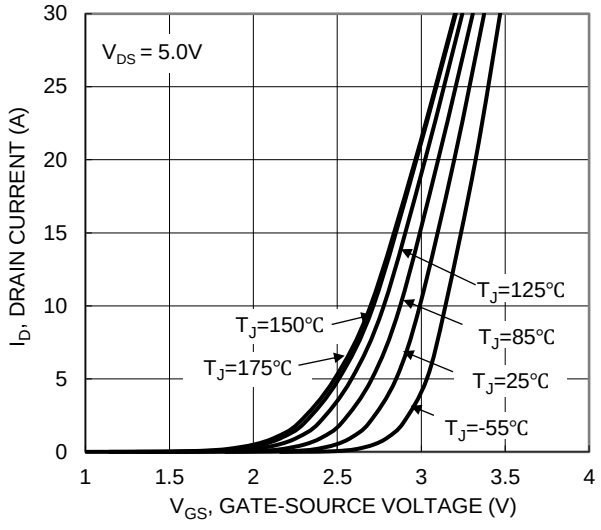


Figure 2. Typical Transfer Characteristic

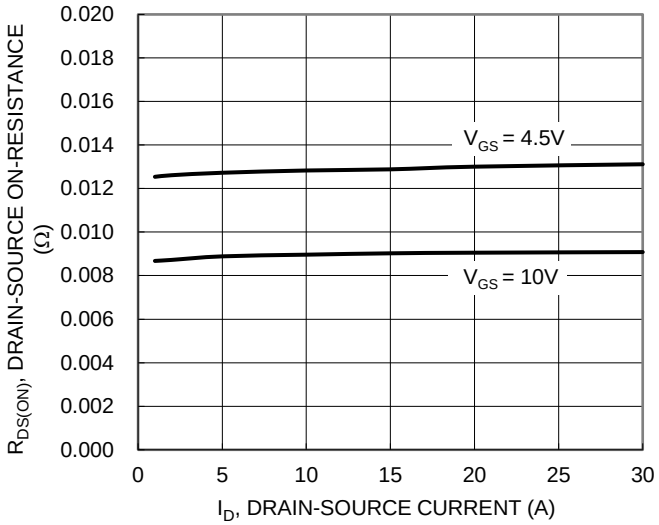


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

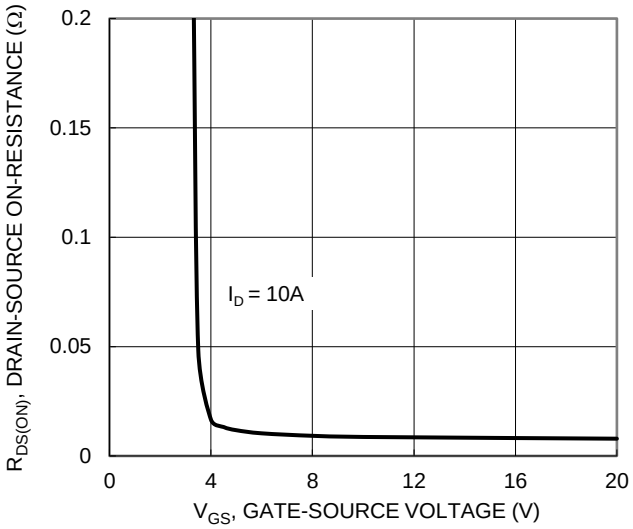


Figure 4. Typical Transfer Characteristic

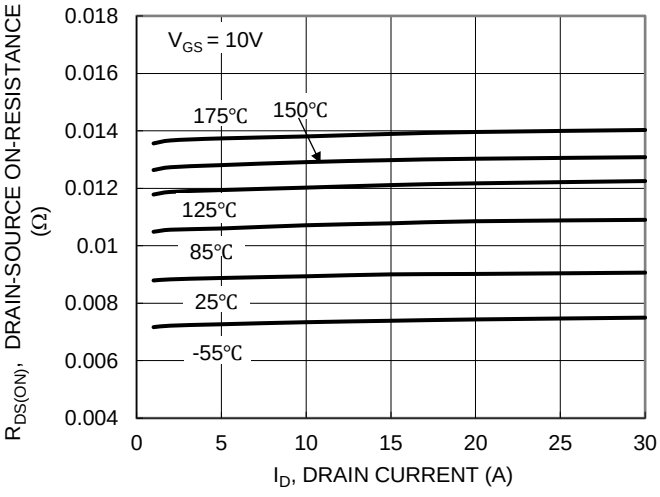


Figure 5. Typical On-Resistance vs. Drain Current and Temperature

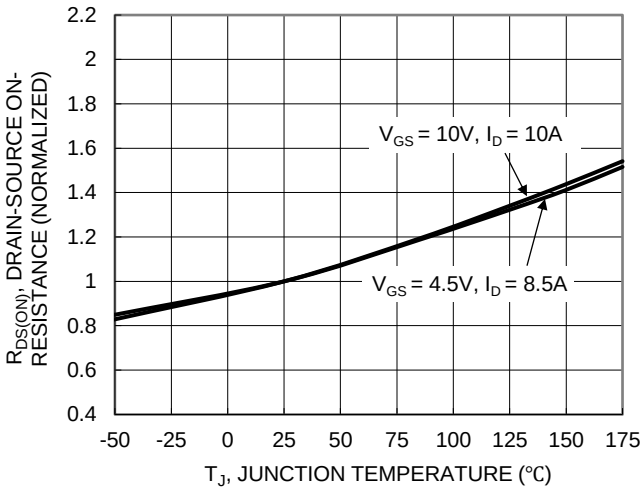


Figure 6. On-Resistance Variation with Temperature

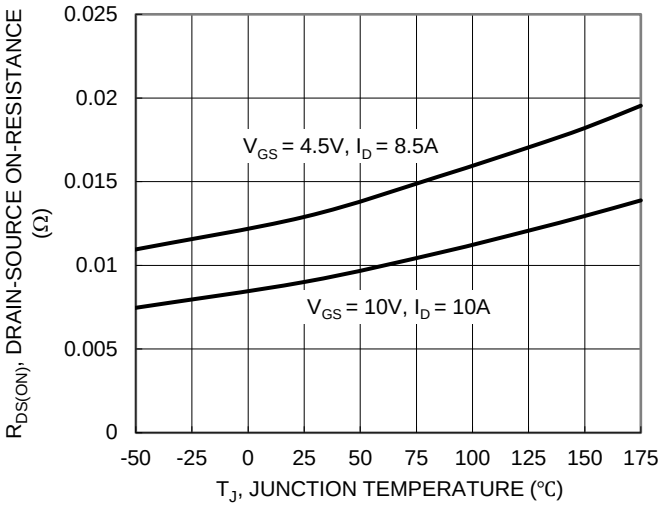


Figure 7. On-Resistance Variation with Temperature

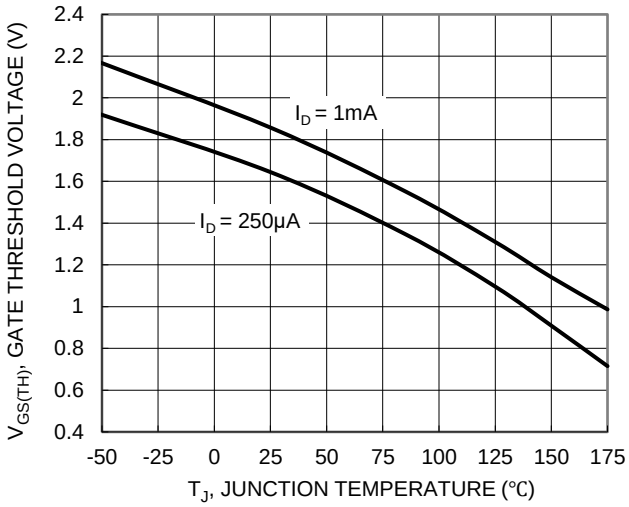


Figure 8. Gate Threshold Variation vs. Junction Temperature

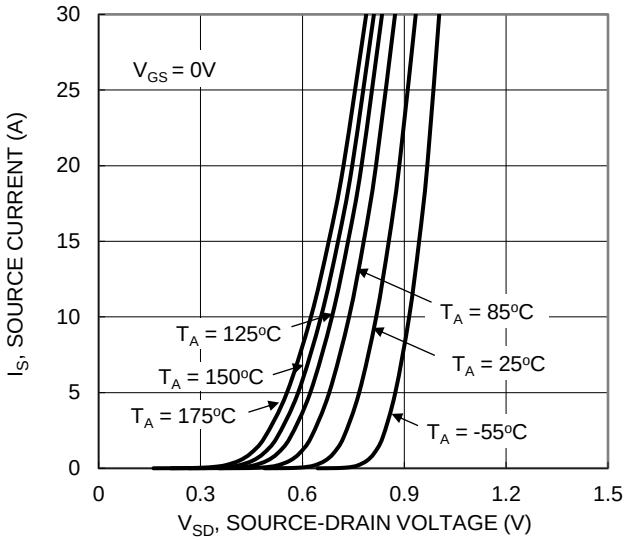


Figure 9. Diode Forward Voltage vs. Current

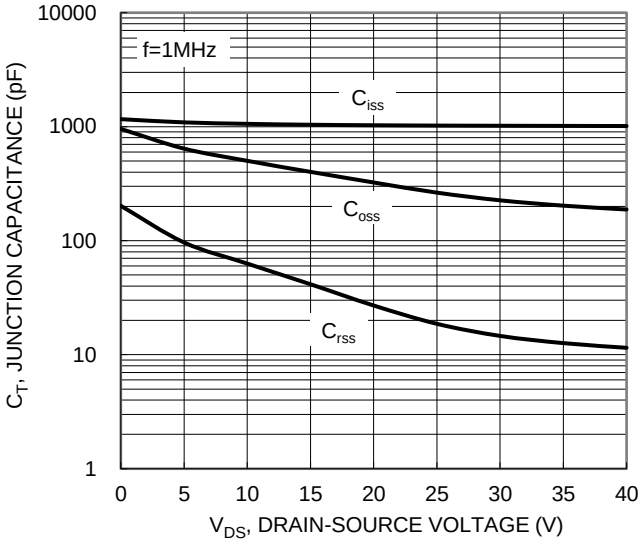


Figure 10. Typical Junction Capacitance

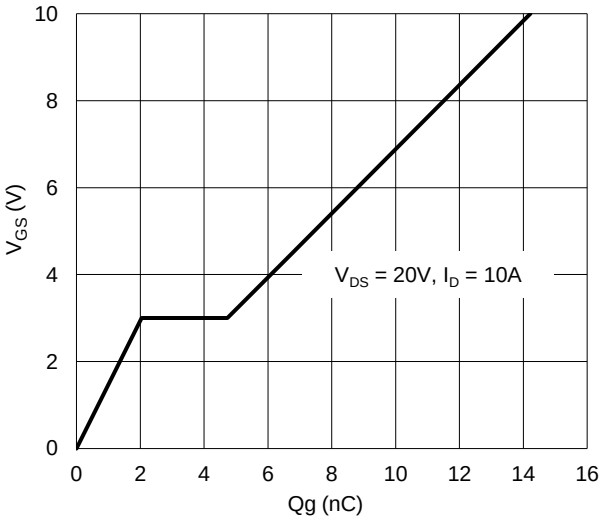


Figure 11. Gate Charge

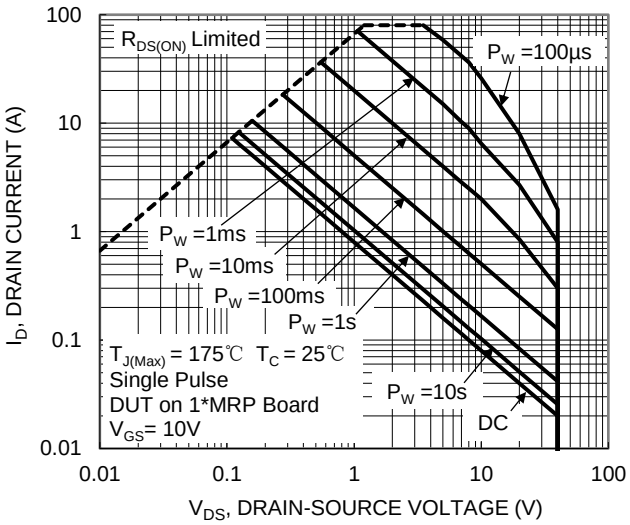


Figure 12. SOA, Safe Operation Area

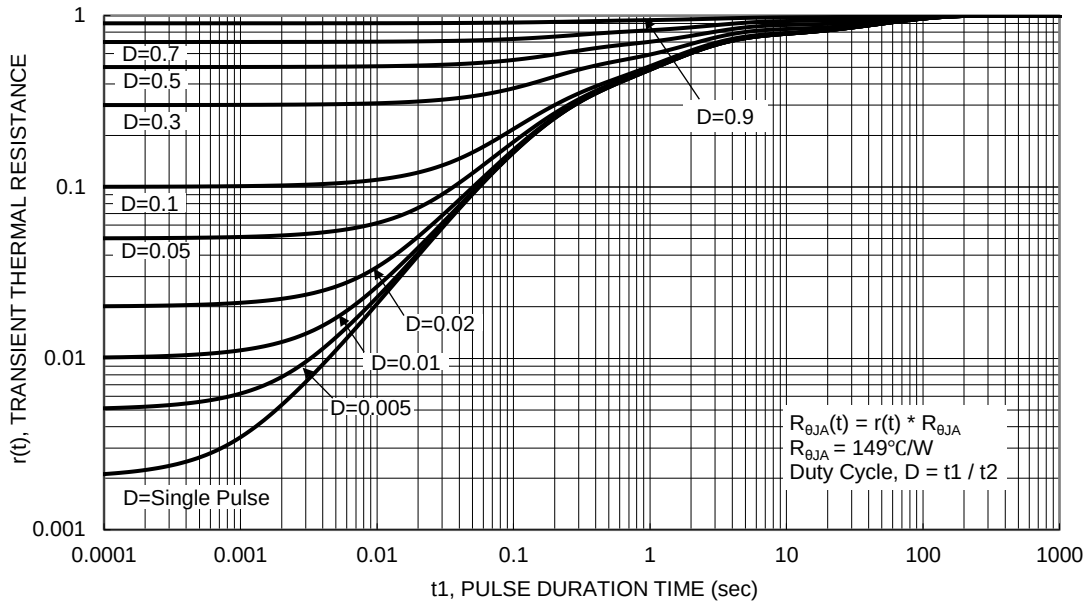
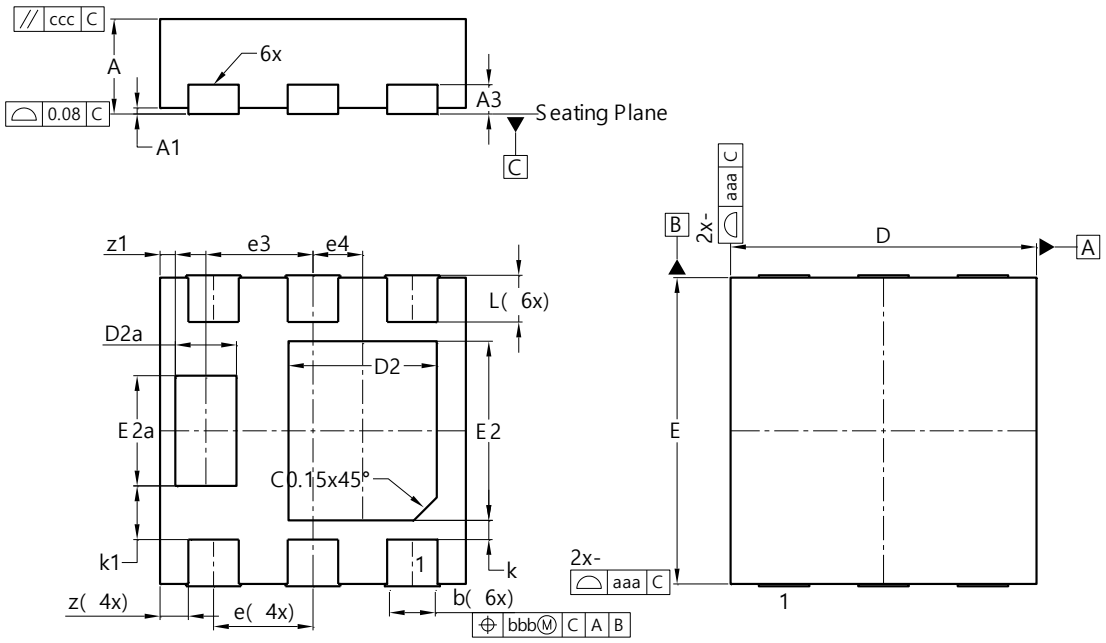


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6/SWP (Type F)

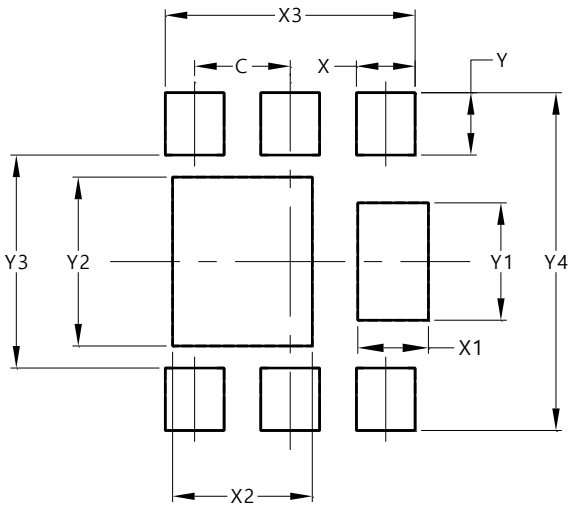


U-DFN2020-6/SWP (Type F)			
Dim	**Min**	**Max**	**Typ**
A	0.59	0.65	0.62
A1	0.00	0.05	0.03
A3	--	--	0.192
b	0.28	0.38	0.33
D	1.95	2.05	2.00
D2	0.87	1.07	0.97
D2a	0.35	0.45	0.40
E	1.95	2.05	2.00
E2	1.07	1.27	1.17
E2a	0.67	0.77	0.72
e	0.65 BSC		
e3	0.70 BSC		
e4	0.325 BSC		
k	--	--	0.125
k1	--	--	0.35
L	0.225	0.355	0.305
z	--	--	0.185
z1	--	--	0.10
aaa	0.250		
bbb	0.100		
ccc	0.100		
All Dimensions in mm			

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

U-DFN2020-6/SWP (Type F)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.480
X2	0.950
X3	1.700
Y	0.425
Y1	0.800
Y2	1.150
Y3	1.450
Y4	2.300

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