MOSFET - Single, N-Channel

100 V, 25 mΩ, 24 A

NTTFD022N10C

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
100 V	25 mΩ @ 10 V	24 A
	61 mΩ @ 6 V	

General Description

This device includes two specialized N−Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q2) and synchronous (Q1) have been designed to provide optimal power efficiency.

Features

Q1: N−Channel

- Max $r_{DS(on)}$ = 25 mΩ at V_{GS} = 10 V, I_D = 7.8 A
- Max $r_{DS(on)}$ = 61 mΩ at V_{GS} = 6, I_D = 3.9 A

Q2: N−Channel

- Max $r_{DS(on)}$ = 25 mΩ at V_{GS} = 10 V, I_D = 7.8 A
- Max $r_{DS(on)}$ = 61 mΩ at V_{GS} = 6, I_D = 3.9 A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- RoHS Compliant

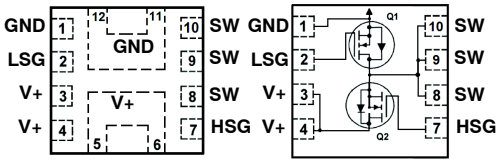
Applications

- Computing
- Communications
- General Purpose Point of Load

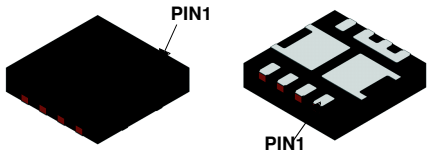
PIN DESCRIPTION

Pin	Name	Description
1, 11, 12	GND (LSS)	Low Side Source
2	LSG	Low Side Gate
3, 4, 5, 6	V + (HSD)	High Side Drain
7	HSG	High Side Gate
8, 9, 10	SW	Switching Node, Low Side Drain

ELECTRICAL CONNECTION



Dual N-Channel MOSFET



Top Bottom

Power Clip 33 Symmetric
(WQFN12)
CASE 510CJ

MARKING DIAGRAM



D022 = Specific Device Code
A = Assembly Plant Code
Y = Numeric Year Code
WW = Work Week Code
ZZ = Assembly Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

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ORDERING INFORMATION AND PACKAGE MARKING

Device	Marking	Package	Shipping†
NTTFD022N10C	D022	WQFN12 (Pb−Free)	3000 Units/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MOSFET MAXIMUM RATINGS (T_A = 25°C, Unless otherwise specified)

Symbol	Parameter			Q1	Q2	Units
V_{DS}	Drain−to−Source Voltage			100	100	V
V_{GS}	Gate−to−Source Voltage			±20	±20	V
I_D	Drain Current (Note 4)	−Continuous	T_C = 25°C	24	24	A
	(Note 4)	−Continuous	T_C = 100°C	14	14	
		−Continuous	T_A = 25°C	6 (Note 1a)	6 (Note 1b)	
		−Pulsed	T_A = 25°C	349	349	
E_{AS}	Single Pulse Avalanche Energy (L = 3 mH, $I_{L(pk)}$ = 5.1 A)		(Note 3)	39	39	mJ
P_D	Power Dissipation for Single Operation		T_C = 25°C	26	26	W
	Power Dissipation for Single Operation		T_A = 25°C	1.7 (Note 1a)	1.7 (Note 1b)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to +150		°C
T_L	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			260	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Q1	Q2	Units
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	4.8	4.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	70 (Note 1a)	70 (Note 1b)	
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	135 (Note 1c)	135 (Note 1c)	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
OFF CHARACTERISTICS							
BV_{DSS}	Drain−to−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	Q1	100			V
		I_D = 250 μA, V_{GS} = 0 V	Q2	100			
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C	Q1		80		mV/°C
		I_D = 250 μA, referenced to 25°C	Q2		80		
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	Q1			1	μA
		V_{DS} = 80 V, V_{GS} = 0 V	Q2			1	
I_{GSS}	Gate−to−Source Leakage Current, Forward	V_{GS} = ±20 V, V_{DS} = 0 V	Q1			±100	nA
		V_{GS} = ±20 V, V_{DS} = 0 V	Q2			±100	

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate−to−Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 44 μA	Q1	2	2.9	4	V
		V_{GS} = V_{DS}, I_D = 44 μA	Q2	2	2.9	4	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate−to−Source Threshold Voltage Temperature Coefficient	I_D = 44 μA, referenced to 25°C	Q1		−9.2		mV/°C
		I_D = 44 μA, referenced to 25°C	Q2		−9.2		
$r_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 7.8 A	Q1		18.7	25	mΩ
		V_{GS} = 6 V, I_D = 3.9 A			28	61	
		V_{GS} = 10 V, I_D = 7.8 A, T_J = 125°C			32.6		
$r_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = 10 V, I_D = 7.8 A	Q2		18.7	25	mΩ
		V_{GS} = 6 V, I_D = 3.9 A			28	61	
		V_{GS} = 10 V, I_D = 7.8 A, T_J = 125°C			32.6		
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 7.8 A	Q1		191		S
		V_{DS} = 5 V, I_D = 7.8 A	Q2		191		
DYNAMIC CHARACTERISTICS							
C_{ISS}	Input Capacitance	Q1: V_{DS} = 50 V, V_{GS} = 0 V, f = 1 Mhz	Q1		585		pF
			Q2		585		
C_{OSS}	Output Capacitance	Q2: V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	Q1		354		pF
			Q2		354		
C_{RSS}	Reverse Transfer Capacitance		Q1		8		pF
			Q2		8		
R_G	Gate Resistance	T_A = 25°C	Q1		1.5		Ω
			Q2		1.5		
SWITCHING CHARACTERISTICS							
$td_{(ON)}$	Turn−On Delay Time	Q1: V_{DD} = 50 V, I_D = 7.8 A, R_{GEN} = 6 Ω	Q1		8.5		ns
			Q2		8.5		
t_r	Rise Time	Q2: V_{DD} = 50 V, I_D = 7.8 A, R_{GEN} = 6 Ω	Q1		3.2		ns
			Q2		3.2		
$t_{D(OFF)}$	Turn−Off Delay Time		Q1		13.3		ns
			Q2		13.3		
t_f	Fall Time		Q1		4.1		ns
			Q2		4.1		
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V	Q1		9.0		nC
			Q2		9.0		
Q_g	Total Gate Charge	V_{GS} = 0 V to 6 V	Q1		5.89		nC
			Q2		5.89		
Q_{gs}	Gate−to−Source Gate Charge	Q1: V_{DD} = 50 V, I_D = 7.8 A	Q1		2.67		nC
		Q2: V_{DD} = 50 V, I_D = 7.8 A	Q2		2.67		
Q_{gd}	Gate−to−Drain “Miller” Charge		Q1		2.0		nC
			Q2		2.0		

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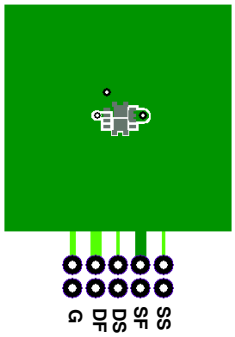
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
DRAIN−SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source−to−Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 7.8 A (Note 2)	Q1		0.82	1.5	V
		V_{GS} = 0 V, I_S = 7.8 A (Note 2)	Q2		0.82	1.5	
t_{rr}	Reverse Recovery Time	Q1: I_F = 7.8 A, di/dt = 300 A/μs Q2: I_F = 7.8 A, di/dt = 300 A/μs	Q1		33		ns
			Q2		33		
Q_{rr}	Reverse Recovery Charge		Q1		35		nC
			Q2		35		
t_{rr}	Reverse Recovery Time	Q1: I_F = 7.8 A, di/dt = 1000 A/μs Q2: I_F = 7.8 A, di/dt = 1000 A/μs	Q1		14		ns
			Q2		14		
Q_{rr}	Reverse Recovery Charge		Q1		91		nC
			Q2		91		

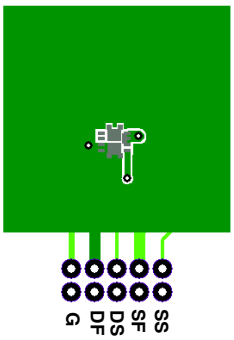
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

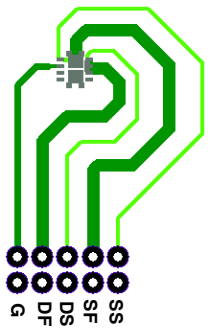
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR−4 material. $R_{\theta CA}$ is determined by the user's board design.



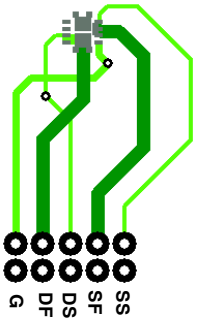
a) 70°C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 70°C/W when mounted on a 1 in^2 pad of 2 oz copper.



c) 135°C/W when mounted on a minimum pad of 2 oz copper.



d) 135°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. Q1: E_{AS} of 39 mJ is based on starting T_J = 25°C; N−ch: L = 3 mH, I_{AS} = 5.1 A, V_{DD} = 80 V, V_{GS} = 10 V. 100% test at L = 3 mH, I_{AS} = 5.3 A. Q2: E_{AS} of 39 mJ is based on starting T_J = 25°C; N−ch: L = 3 mH, I_{AS} = 5.1 A, V_{DD} = 80 V, V_{GS} = 10 V. 100% test at L = 3 mH, I_{AS} = 5.3 A.
4. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro−mechanical application board design.

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TYPICAL CHARACTERISTICS

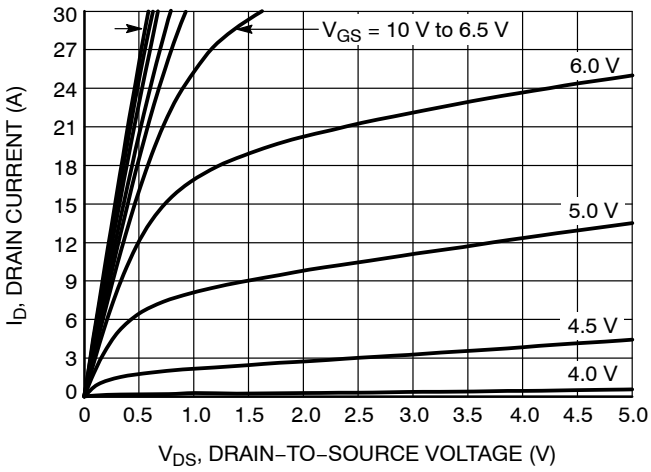


Figure 1. On−Region Characteristics

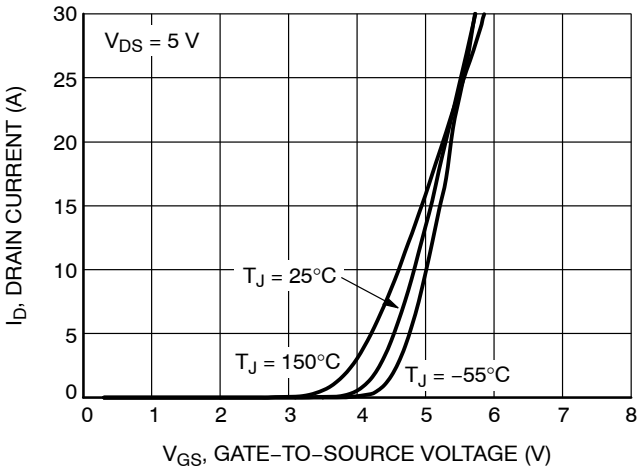


Figure 2. Transfer Characteristics

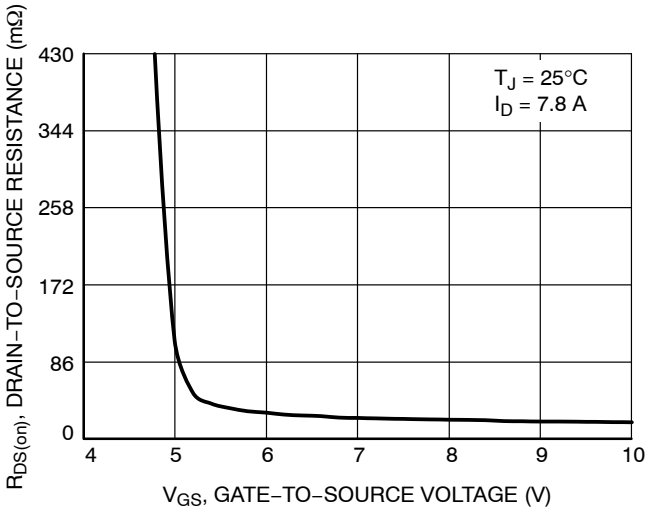


Figure 3. On−Resistance vs. Gate−to−Source Voltage

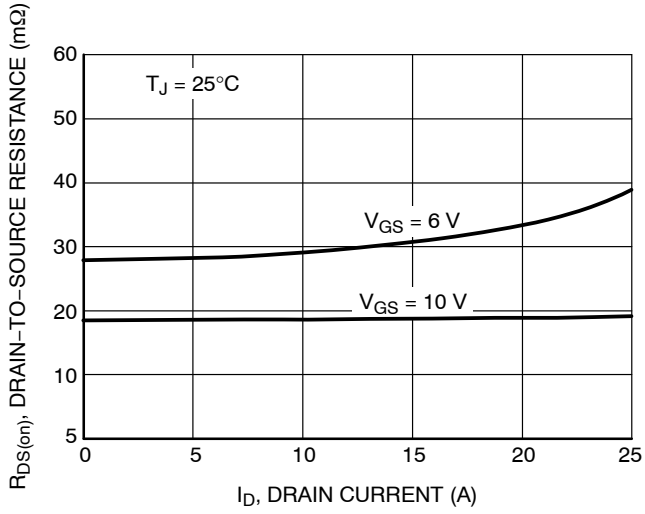


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

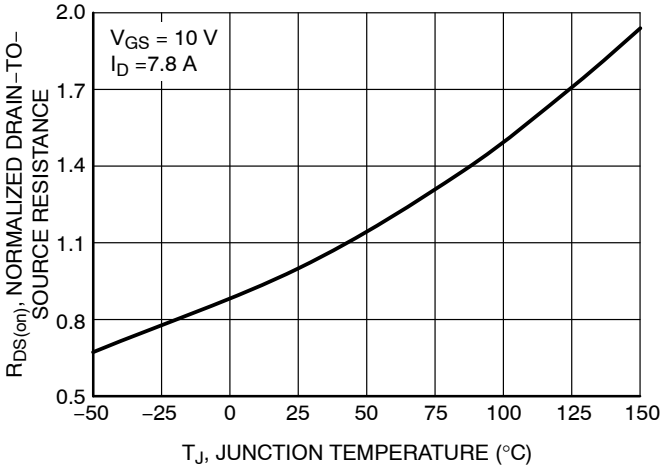


Figure 5. On−Resistance Variation with Temperature

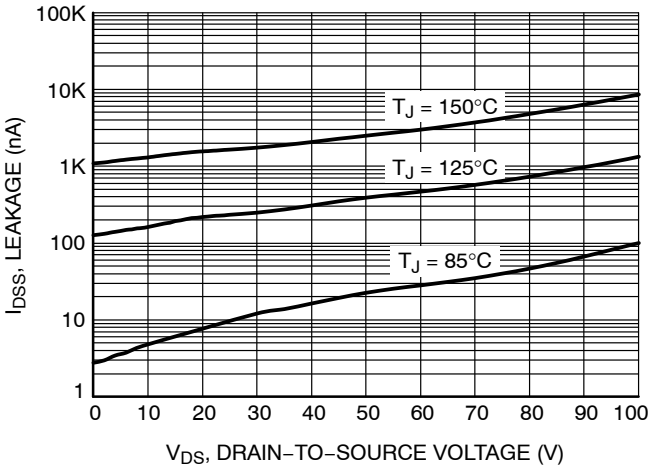


Figure 6. Drain−to−Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

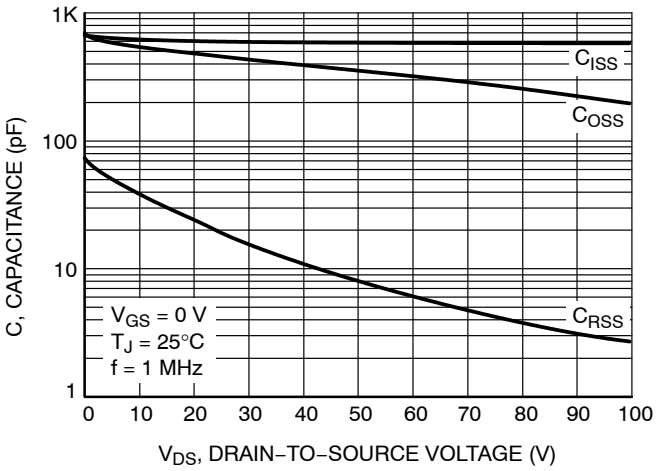


Figure 7. Capacitance Variation

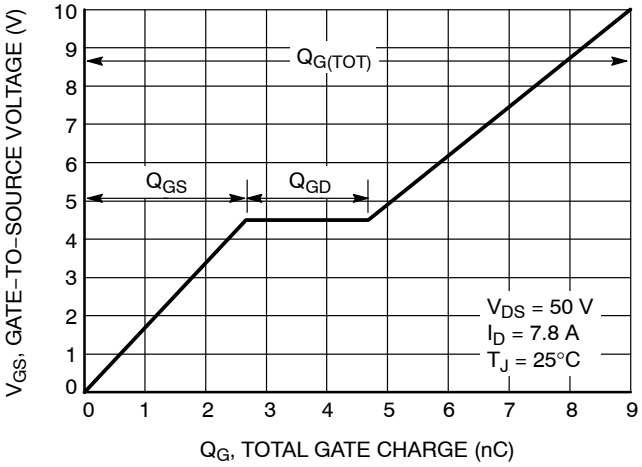


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

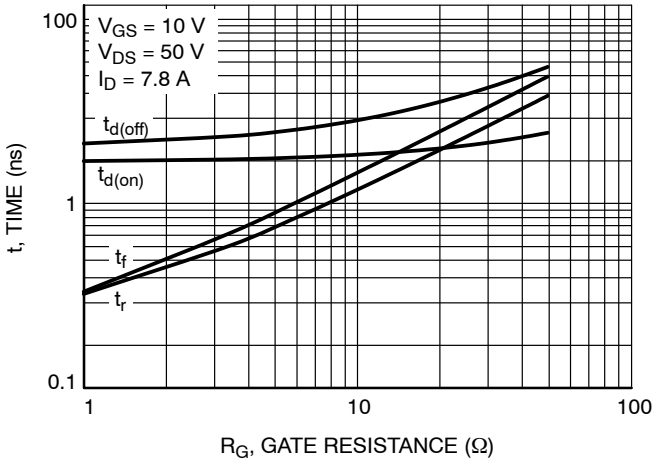


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

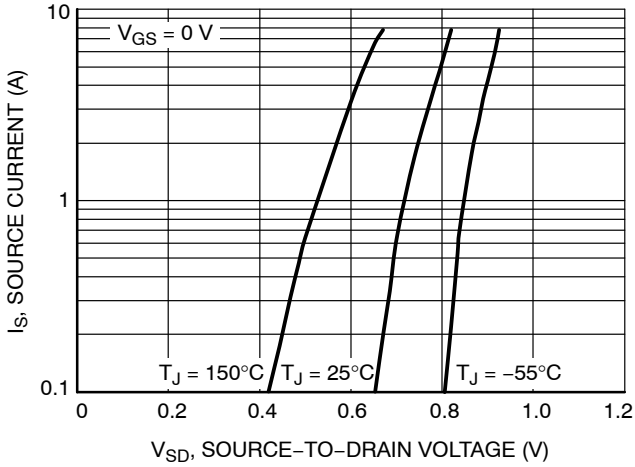


Figure 10. Diode Forward Voltage vs. Current

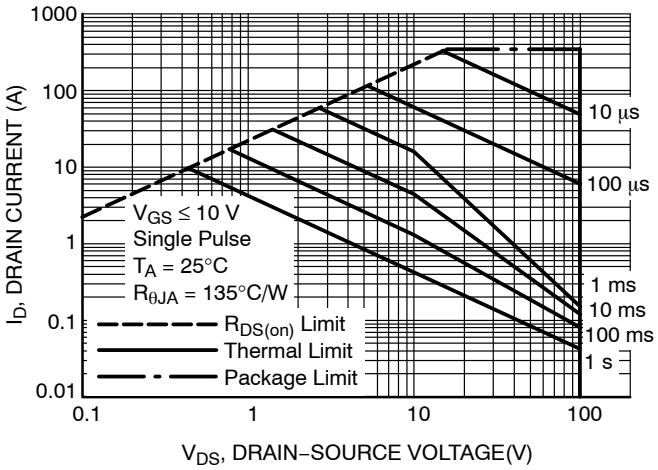


Figure 11. Safe Operating Area

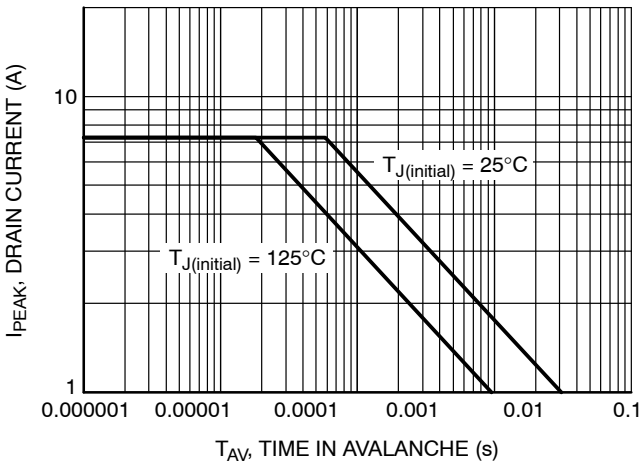


Figure 12. I_{PEAK} vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

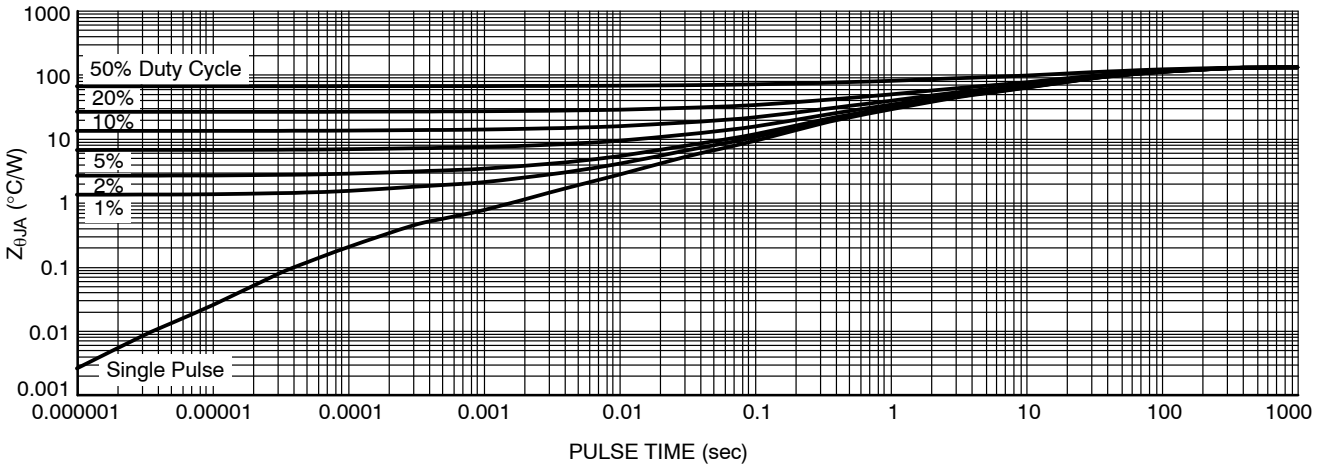
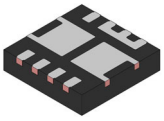


Figure 13. Thermal Characteristics

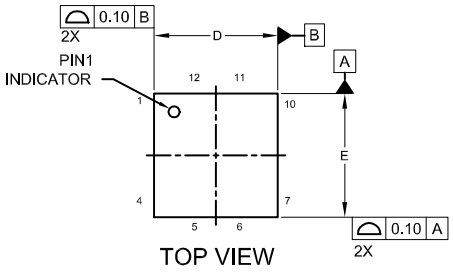
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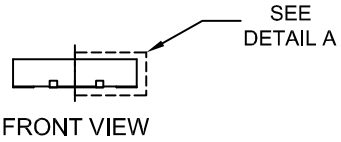


WQFN12 3.3X3.3, 0.65P
CASE 510CJ
ISSUE A

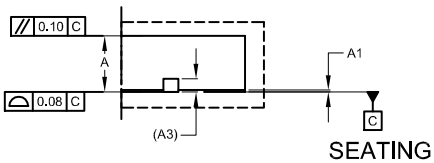
DATE 08 AUG 2022



TOP VIEW

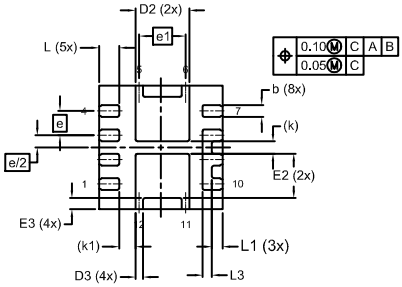


FRONT VIEW



DETAIL 'A'
SCALE 2:1

SEATING
PLANE

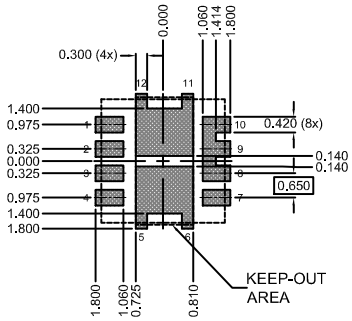


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
5. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

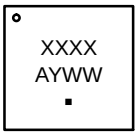
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	--	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	1.34	1.44	1.54
D3	0.10	0.20	0.30
E	3.20	3.30	3.40
E2	1.09	1.19	1.29
E3	0.20	0.30	0.40
e	0.65 BSC		
e/2	0.325 BSC		
e1	1.24 BSC		
k	0.33 REF		
k1	0.43 REF		
L	0.44	0.54	0.64
L1	0.19	0.29	0.39
L3	0.15	0.25	0.35



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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