

DATA SHEET

BF1109; BF1109R; BF1109WR N-channel dual-gate MOS-FETs

Product specification
Supersedes data of 1997 Sep 03

1997 Dec 08



N-channel dual-gate MOS-FETs

BF1109; BF1109R;
BF1109WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier up to 1 GHz
- Internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

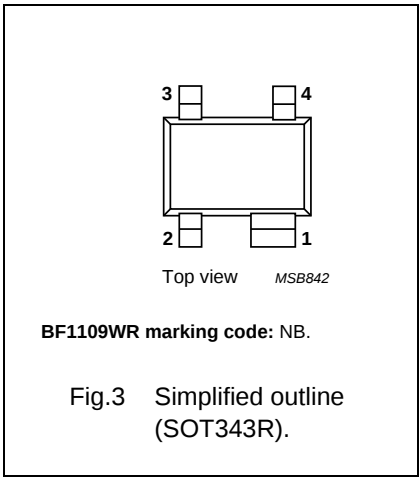
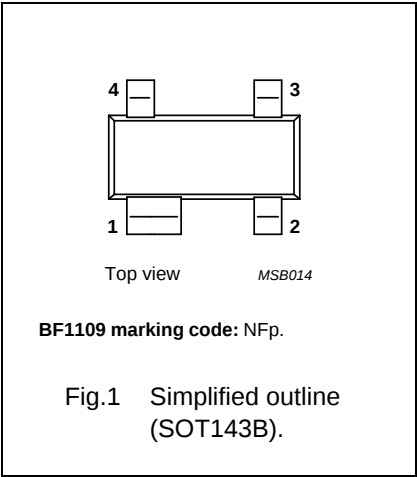
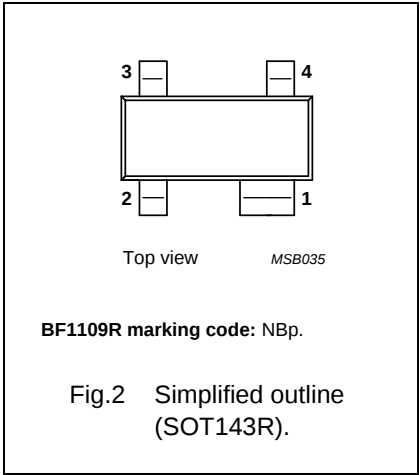
- VHF and UHF applications with 9 V supply voltage, such as television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1109, BF1109R and BF1109WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	11	V
I_D	drain current (DC)		–	–	30	mA
P_{tot}	total power dissipation	$T_{amb} \leq 80\text{ }^{\circ}\text{C}$	–	–	200	mW
$ y_{fs} $	forward transfer admittance		–	30	–	mS
C_{ig1-ss}	input capacitance at gate 1		–	2.2	2.7	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	40	fF
F	noise figure	$f = 800\text{ MHz}$	–	1.5	2.5	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 40 dB AGC	100	–	–	dB μ V
T_j	operating junction temperature		–	–	150	$^{\circ}\text{C}$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

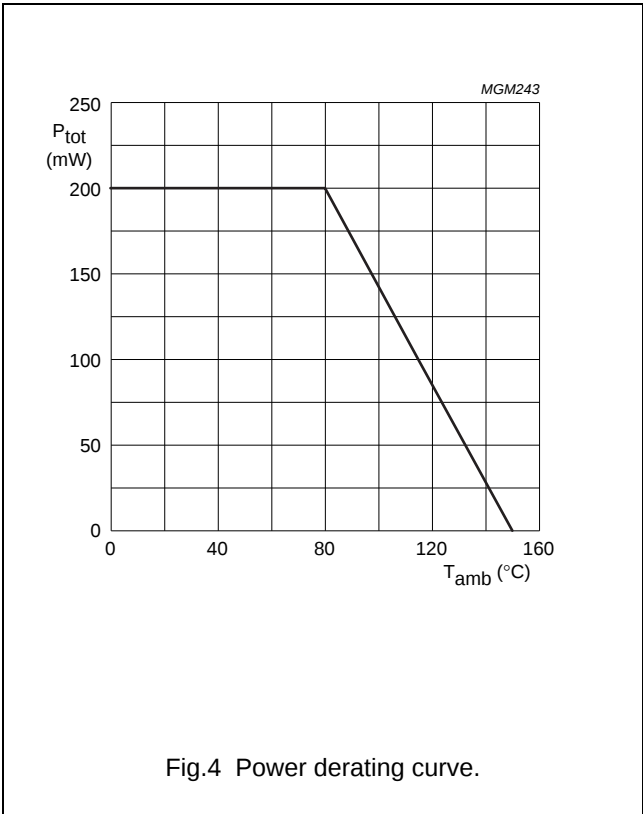
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		–	11	V
I _D	drain current (DC)		–	30	mA
I _{G1}	gate 1 current		–	±10	mA
I _{G2}	gate 2 current		–	±10	mA
P _{tot}	total power dissipation	T _{amb} ≤ 80 °C; note 1	–	200	mW
T _{stg}	storage temperature		–65	+150	°C
T _j	operating junction temperature		–	+150	°C

Note

1. Device mounted on a printed-circuit board.



N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient in free air	note 1	350	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		200	K/W

Note

1. Device mounted on a printed-circuit board.

STATIC CHARACTERISTICS

$T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; $I_D = 10\text{ }\mu\text{A}$	11	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = 0$; $I_{G1-S} = 10\text{ }\mu\text{A}$; $I_D = 0$	11	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; $I_{G2-S} = 10\text{ }\mu\text{A}$	11	–	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	$V_{G1-S} = 9\text{ V}$; $V_{DS} = 9\text{ V}$; $I_D = 20\text{ }\mu\text{A}$	0.3	1.2	V
I_{DSX}	self-biasing drain current	$V_{G2-S} = 4\text{ V}$; $V_{DS} = 9\text{ V}$	8	16	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G1-S} = 9\text{ V}$; $V_{G2-S} = 0$; $I_D = 0$	–	20	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; $V_{G2-S} = 9\text{ V}$	–	20	nA

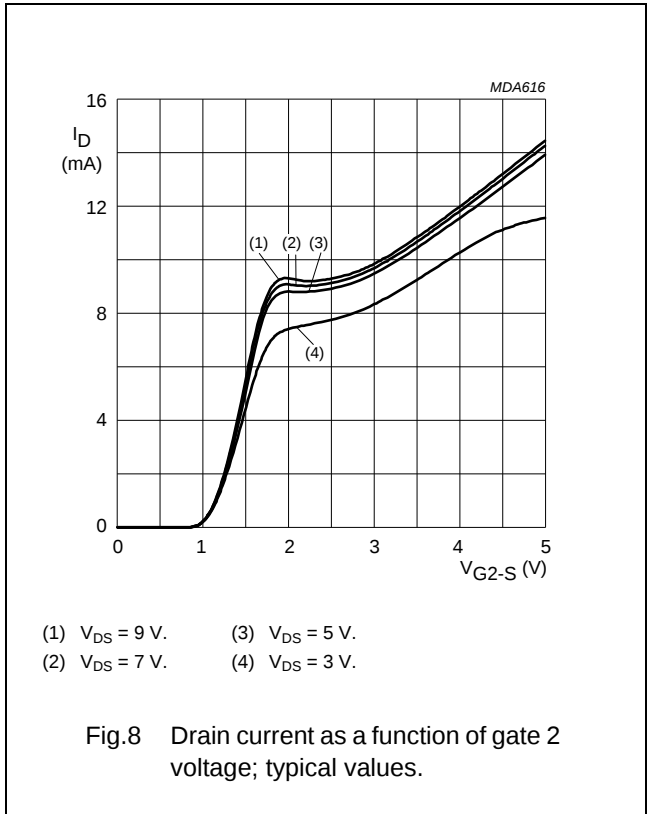
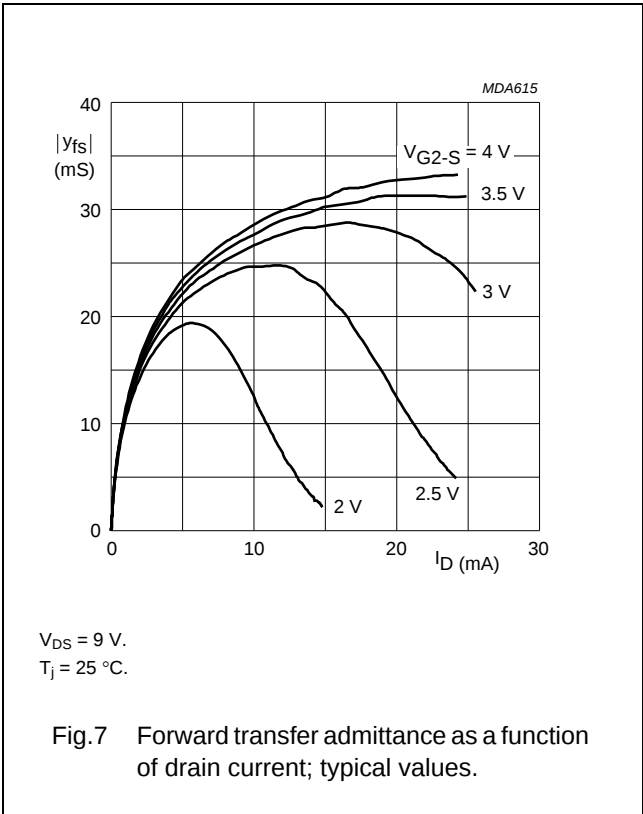
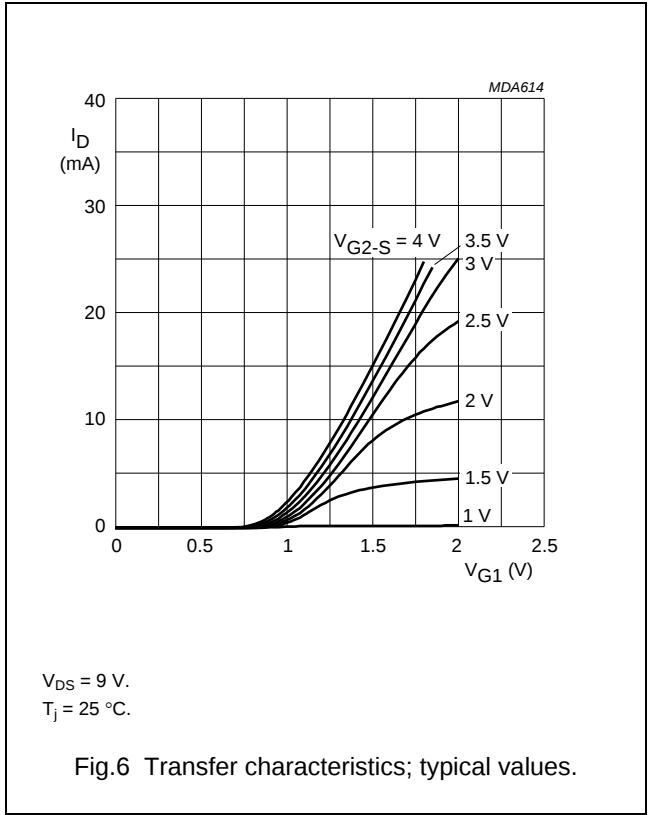
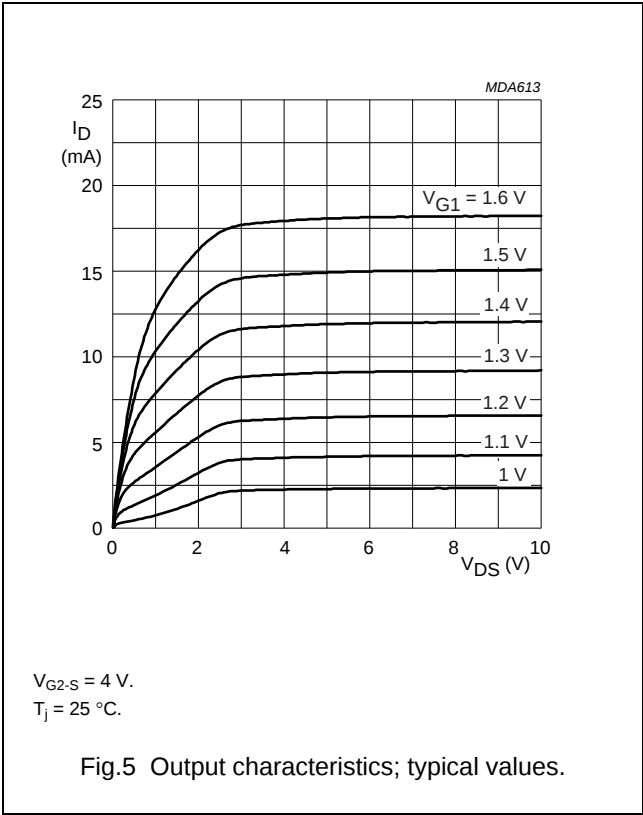
DYNAMIC CHARACTERISTICS

Common source; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $V_{G2-S} = 4\text{ V}$; $V_{DS} = 9\text{ V}$; self-biasing current; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$ y_{fs} $	forward transfer admittance	pulsed; $T_j = 25\text{ }^{\circ}\text{C}$	24	30	–	mS
C_{ig1-ss}	input capacitance at gate 1	$f = 1\text{ MHz}$	–	2.2	2.7	pF
C_{ig2-ss}	input capacitance at gate 2	$f = 1\text{ MHz}$	–	1.5	–	pF
C_{oss}	output capacitance	$f = 1\text{ MHz}$	–	1.3	–	pF
C_{rss}	reverse transfer capacitance	$f = 1\text{ MHz}$	–	25	40	fF
F	noise figure	$f = 800\text{ MHz}$; $Y_S = Y_{S\text{ opt}}$	–	1.5	2.5	dB
G_p	power gain	$G_S = 2\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 0.5\text{ mS}$; $B_L = B_{L\text{ opt}}$; $f = 200\text{ MHz}$; see Fig.16	–	38	–	dB
		$G_S = 3.3\text{ mS}$; $B_S = B_{S\text{ opt}}$; $G_L = 1\text{ mS}$; $B_L = B_{L\text{ opt}}$; $f = 800\text{ MHz}$; see Fig.17	–	20	–	dB
X_{mod}	cross-modulation	input level for $k = 1\%$ at 0 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; see Fig.18	85	–	–	dB μV
		input level for $k = 1\%$ at 40 dB AGC; $f_w = 50\text{ MHz}$; $f_{unw} = 60\text{ MHz}$; see Fig.18	100	–	–	dB μV

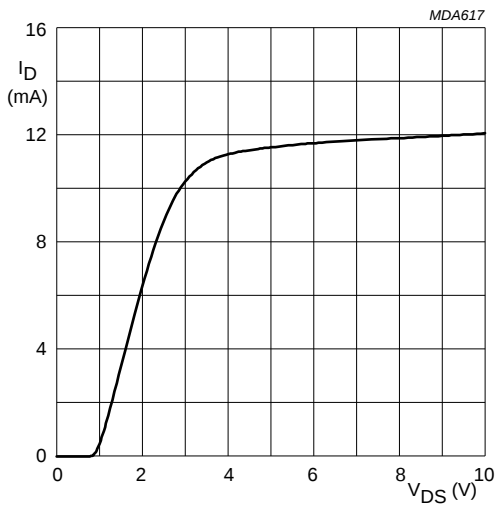
N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR



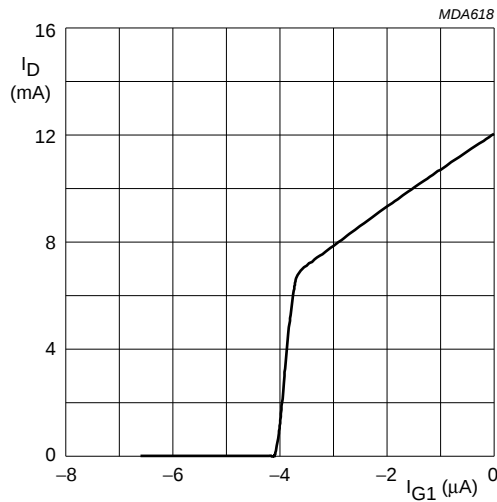
N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR



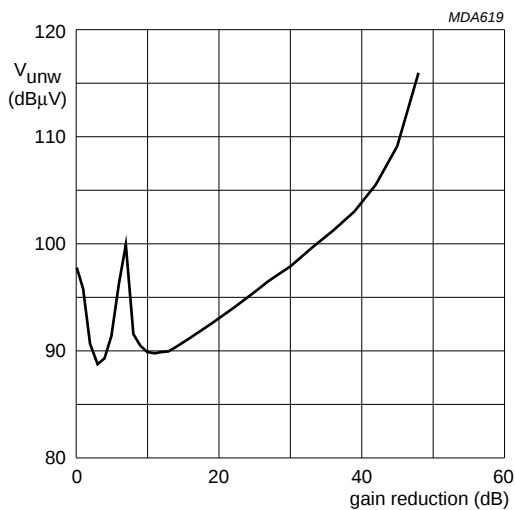
$V_{G2-S} = 4\text{ V}$.
 $T_J = 25\text{ }^{\circ}\text{C}$.

Fig.9 Drain current as a function of drain-source voltage; typical values.



$V_{DS} = 9\text{ V}$; $V_{G2-S} = 4\text{ V}$; $T_J = 25\text{ }^{\circ}\text{C}$.

Fig.10 Drain current as a function of gate 1 current; typical values.

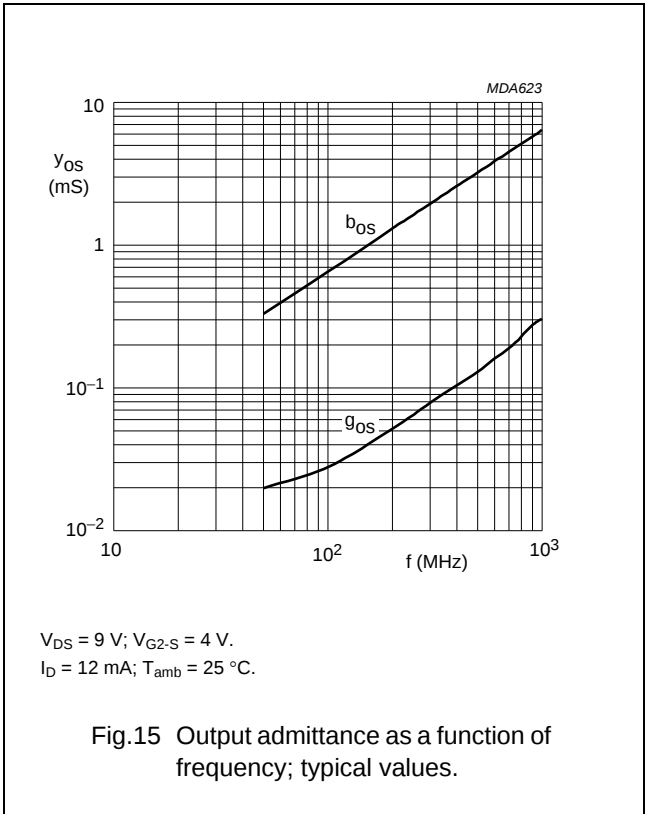
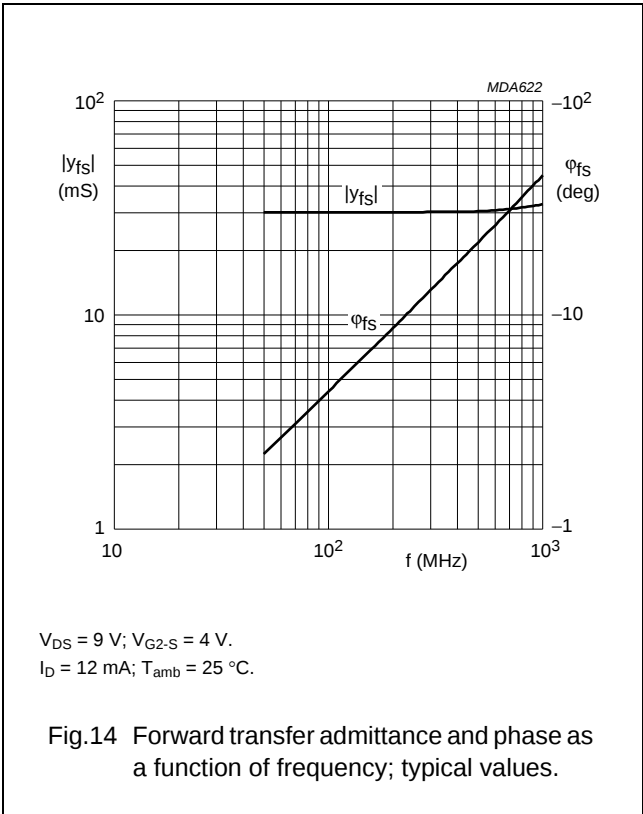
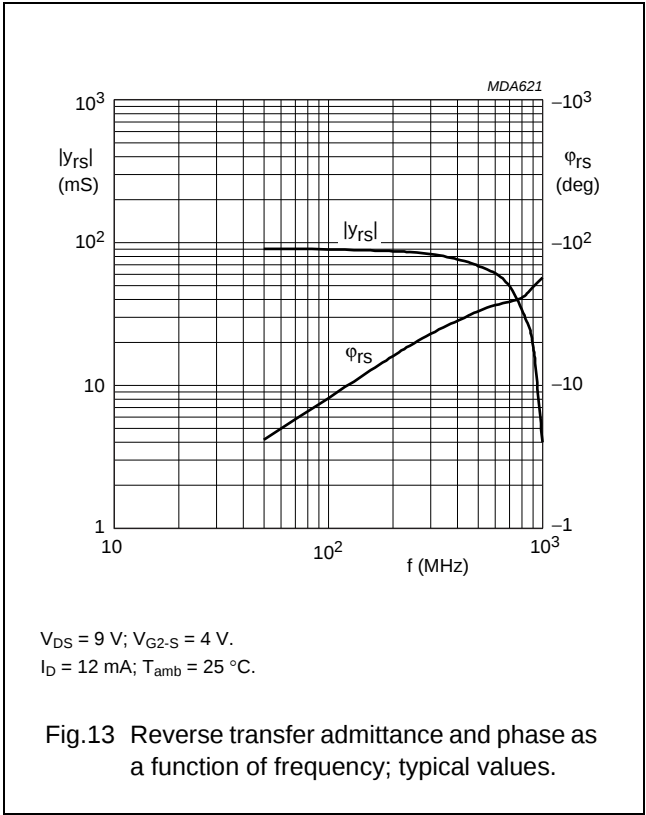
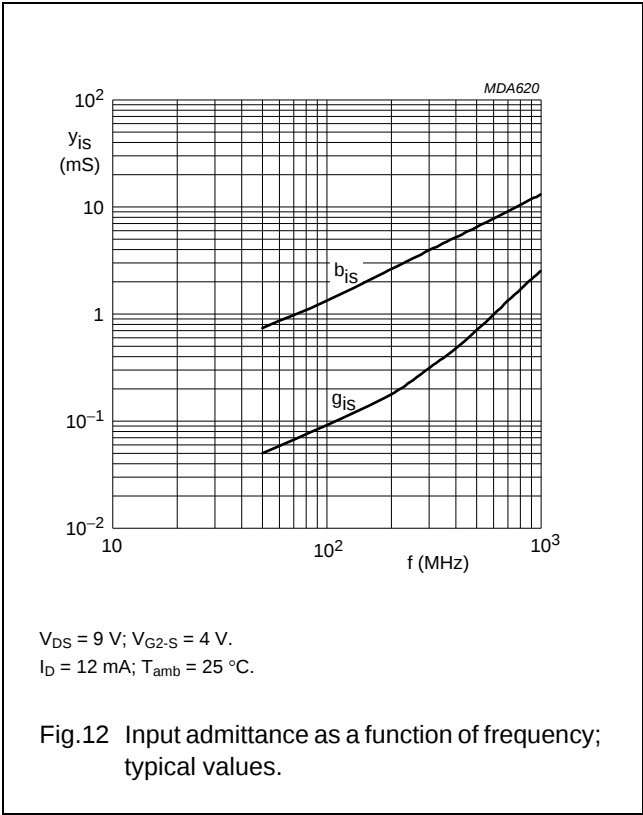


$V_{DS} = 9\text{ V}$; $V_{G2nom} = 4\text{ V}$; $I_{Dnom} = 12\text{ mA}$; $f_w = 50\text{ MHz}$;
 $f_{unw} = 60\text{ MHz}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$.

Fig.11 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values (see Fig.18).

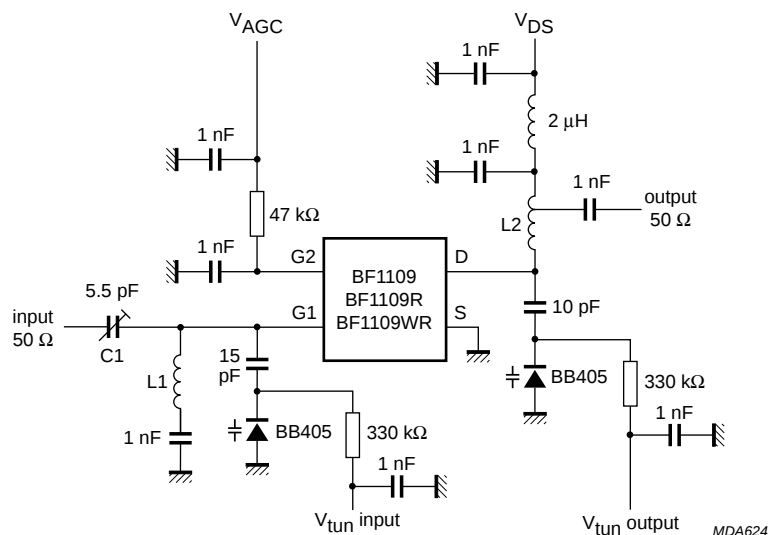
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BF1109; BF1109R; BF1109WR



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BF1109; BF1109R; BF1109WR



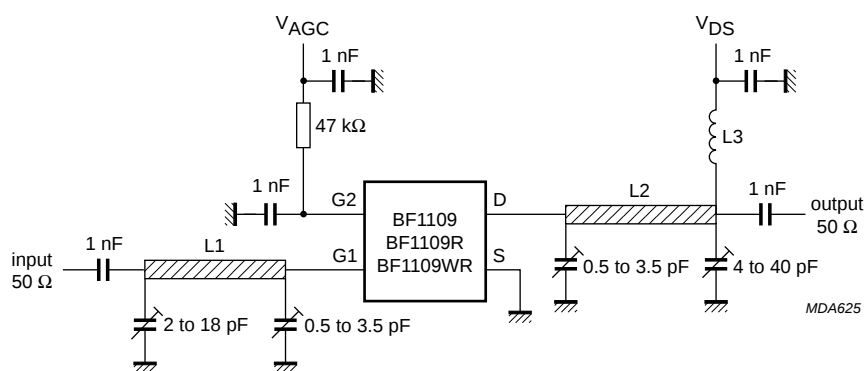
$V_{DS} = 9\text{ V}$, $G_S = 2\text{ mS}$, $G_L = 0.5\text{ mS}$, $f = 200\text{ MHz}$.

$L1 = 45\text{ nH}$, 4 turns, internal diameter = 4 mm, 0.8 mm copper wire.

$L2 = 160\text{ nH}$, 3 turns, internal diameter = 8 mm, 0.8 mm copper wire; tapped at approximately half a turn from the cold side, to set $G_L = 0.5\text{ mS}$.

$C1$ adjusted for $G_S = 2\text{ mS}$.

Fig.16 Gain test circuit.



$V_{DS} = 9\text{ V}$, $G_S = 3.3\text{ mS}$, $G_L = 1\text{ mS}$, $f = 800\text{ MHz}$.

$L1 = 2\text{ cm}$, silvered 0.8 mm copper wire 4 mm above ground plane.

$L2 = 2\text{ cm}$, silvered 0.8 mm copper wire 4 mm above ground plane.

$L3 = 11\text{ turns}$ 0.5 mm copper wire without spacing, internal diameter = 3 mm, $L = \text{approx. } 200\text{ nH}$.

Fig.17 Gain test circuit.

N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

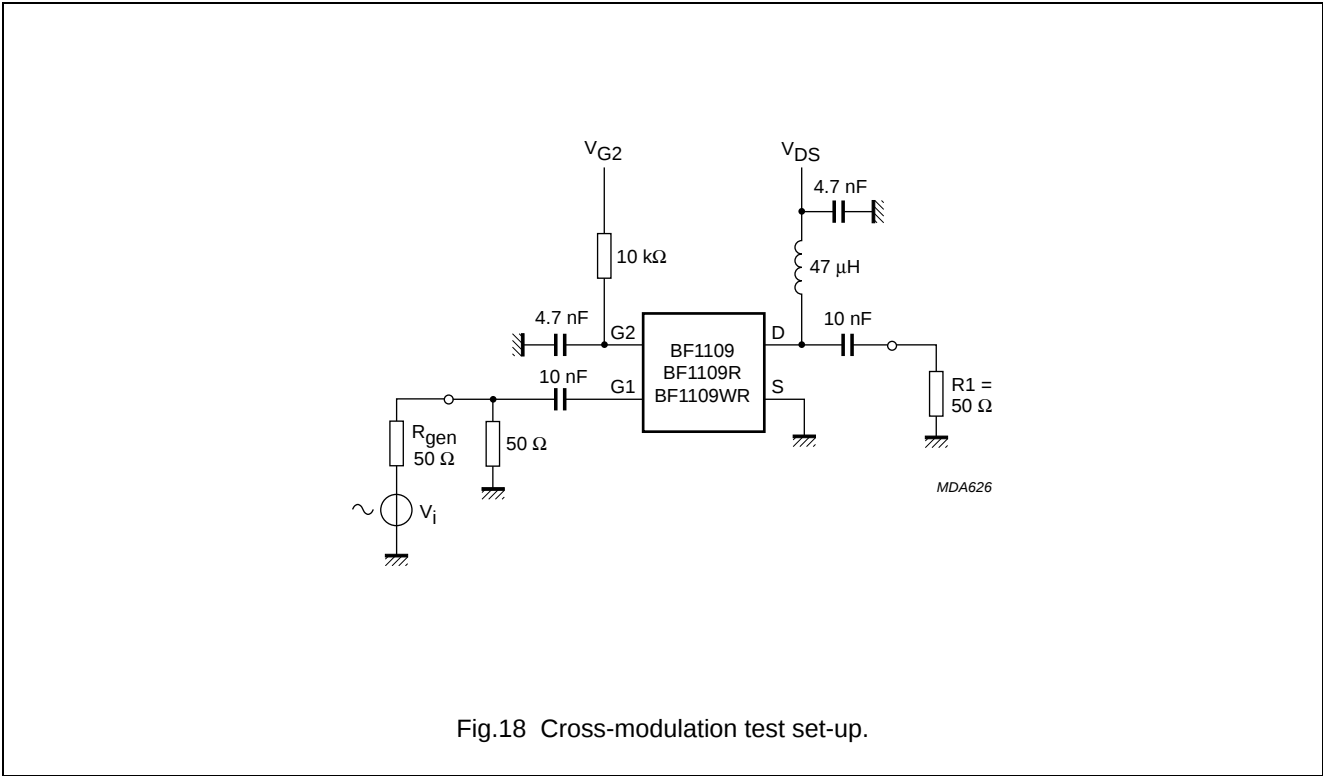


Table 1 Scattering parameters: $V_{DS} = 9\ \text{V}$; $V_{G2-S} = 4\ \text{V}$; $I_D = 12\ \text{mA}$

f (MHz)	S ₁₁		S ₂₁		S ₁₂		S ₂₂	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.995	−3.71	3.013	175.0	0.000	88.2	0.998	−1.8
100	0.992	−7.29	3.002	170.2	0.001	83.7	0.997	−3.5
200	0.984	−14.3	2.967	160.7	0.002	86.2	0.995	−7.0
300	0.973	−21.2	2.922	151.3	0.002	83.2	0.992	−10.5
400	0.961	−27.9	2.869	142.0	0.003	84.1	0.990	−13.9
500	0.944	−34.4	2.793	132.9	0.003	85.7	0.987	−17.2
600	0.926	−40.8	2.730	124.1	0.003	88.4	0.985	−20.5
700	0.906	−46.9	2.660	115.3	0.003	94.6	0.983	−23.7
800	0.887	−52.9	2.605	106.5	0.004	107.2	0.981	−26.8
900	0.868	−58.8	2.527	97.8	0.004	114.9	0.977	−30.0
1000	0.852	−64.3	2.457	89.6	0.004	129.7	0.9377	−33.1

Table 2 Noise data: $V_{DS} = 9\ \text{V}$; $V_{G2-S} = 4\ \text{V}$; $I_D = 12\ \text{mA}$

f (MHz)	F _{min} (dB)	Γ _{opt}		R _n (Ω)
		(ratio)	(deg)	
800	1.5	0.684	40.94	40.4

N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads

SOT143B

Technical drawing of the SOT143B package showing top, side, and bottom views with dimensions D, B, y, E, A, X, H_E, v, w, A, B, e, b_p, 4, 3, 1, 2, b₁, e₁, A, Q, A₁, c, L_p, detail X, and a scale bar from 0 to 2 mm.

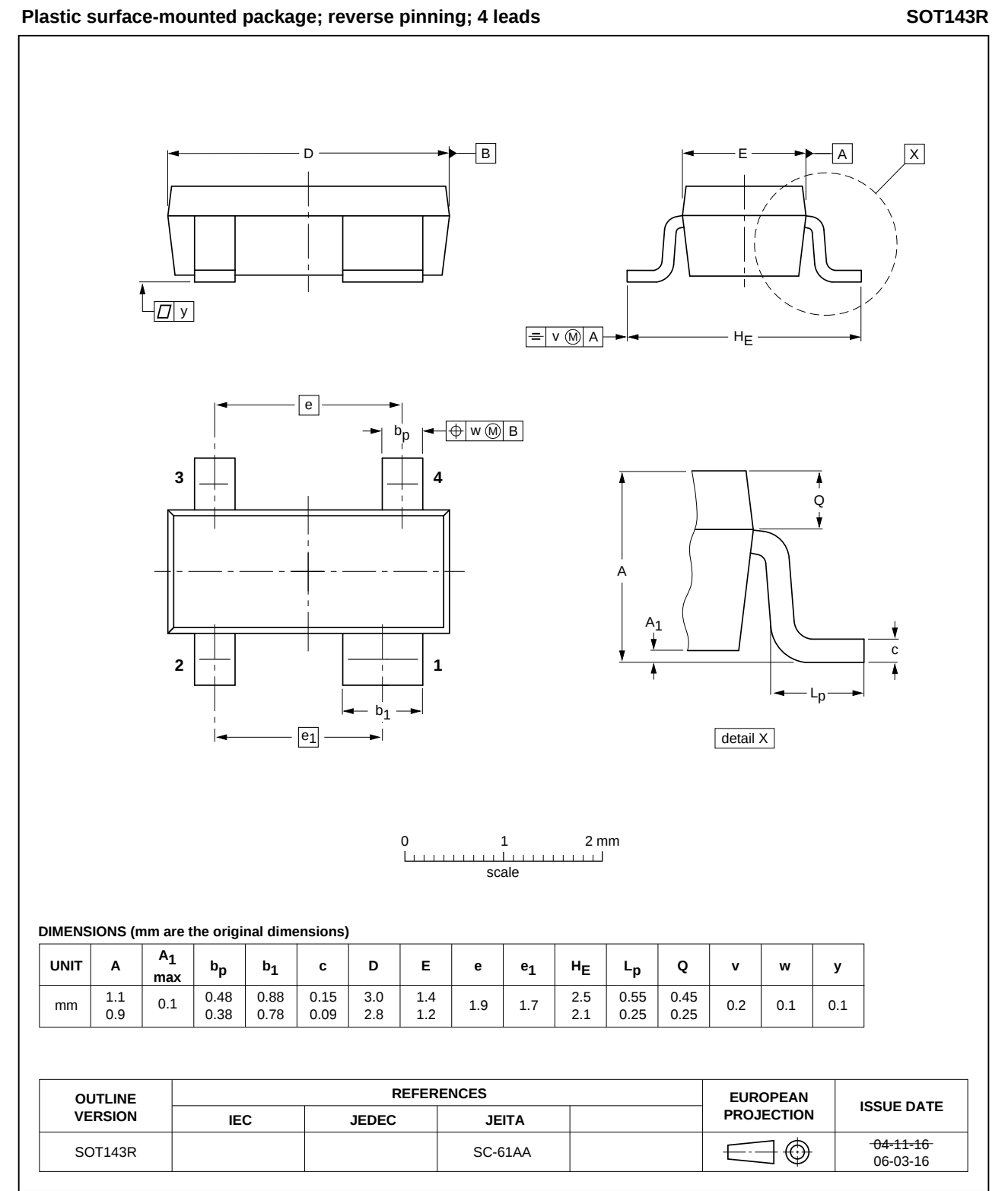
DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						04-11-16 06-03-16

N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

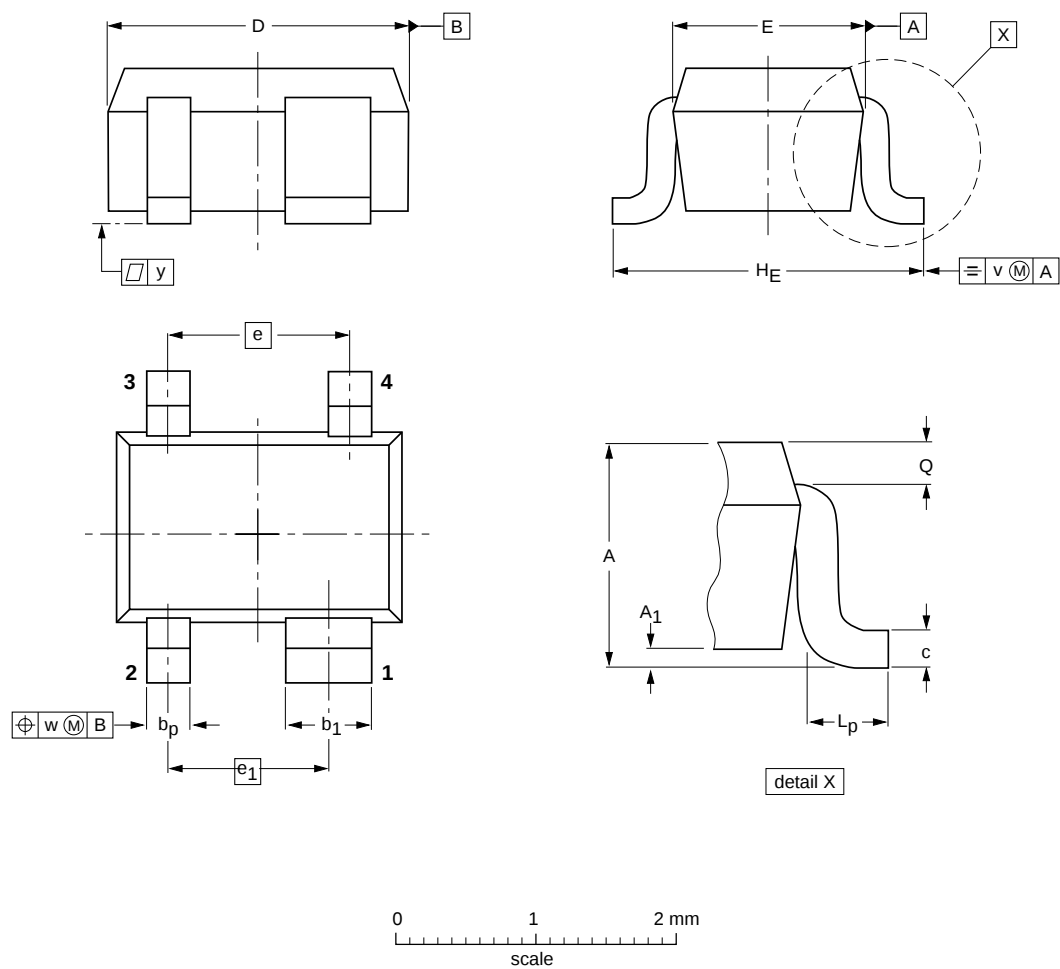


N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

Plastic surface-mounted package; reverse pinning; 4 leads

SOT343R



DIMENSIONS (mm are the original dimensions)

UNIT	A	A ₁ max	b _p	b ₁	c	D	E	e	e ₁	H _E	L _p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21 06-03-16

N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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N-channel dual-gate MOS-FETs

BF1109; BF1109R; BF1109WR

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This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for package outline drawings which were updated to the latest version.

Contact information

For additional information please visit: <http://www.nxp.com>

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