

# NTHS5404T1

## MOSFET – Power, N-Channel, ChipFET

20 V, 7.2 A



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### Features

- Low  $R_{DS(on)}$  for Higher Efficiency
- Logic Level Gate Drive
- Miniature ChipFET Surface Mount Package Saves Board Space
- Pb-Free Package is Available

### Applications

- Power Management in Portable and Battery-Powered Products; i.e., Cellular and Cordless Telephones and PCMCIA Cards

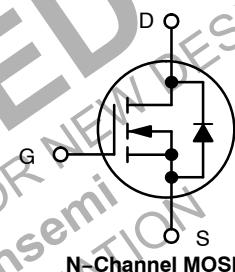
### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	5 Secs	Steady State	Unit
Drain-Source Voltage	$V_{DS}$	20		V
Gate-Source Voltage	$V_{GS}$		$\pm 12$	V
Continuous Drain Current ( $T_J = 150^\circ\text{C}$ ) (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$I_D$	7.2 5.2	5.2 3.8	A
Pulsed Drain Current	$I_{DM}$		$\pm 20$	A
Continuous Source Current (Diode Conduction) (Note 1)	$I_S$	7.2	5.2	A
Maximum Power Dissipation (Note 1) $T_A = 25^\circ\text{C}$ $T_A = 85^\circ\text{C}$	$P_D$	2.5 1.3	1.3 0.7	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150		°C

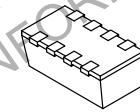
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	$I_D$ MAX
20 V	25 mΩ @ 4.5 V	7.2 A

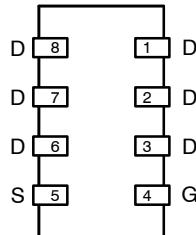


N-Channel MOSFET

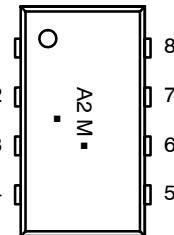


ChipFET  
CASE 1206A  
STYLE 1

### PIN CONNECTIONS



### MARKING DIAGRAM



A2 = Specific Device Code

M = Month Code

■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NTHS5404T1	ChipFET	3000/Tape & Reel
NTHS5404T1G	ChipFET (Pb-Free)	3000/Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTHS5404T1

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Maximum Junction-to-Ambient (Note 2) t ≤ 5 sec Steady State	$R_{\theta JA}$	40 80	50 95	°C/W
Maximum Junction-to-Foot (Drain) Steady State	$R_{\theta JF}$	15	20	°C/W

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
<b>DYNAMIC (Note 4)</b>						
Total Gate Charge	$Q_G$			12	18	nC
Gate-Source Charge	$Q_{GS}$	$V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 5.2 \text{ A}$		2.4		
Gate-Drain Charge	$Q_{GD}$			3.2		
Input Capacitance	$C_{ISS}$			740		pF
Output Capacitance	$C_{OSS}$	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, f = 1.0 \text{ MHz}$		337		
Reverse Transfer Capacitance	$C_{RSS}$			88		
Turn-On Delay Time	$t_{d(on)}$			8.0	15	ns
Rise Time	$t_r$	$V_{DD} = 10 \text{ V}, R_L = 10 \Omega, I_D \approx 1.0 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_G = 6 \Omega$		7.0	15	
Turn-Off Delay Time	$t_{d(off)}$			50	60	
Fall Time	$t_f$			28	40	

## STATIC

Drain-to-Source Breakdown Voltage (Note 3)	$V_{(BR)DSS}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	20	25.1		V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			18.4		mV/°C
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	0.6			V
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			±100	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}$			1.0	μA
		$V_{DS} = 16 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 85^\circ\text{C}$			5.0	
On-State Drain Current (Note 3)	$I_{D(on)}$	$V_{DS} \geq 5.0 \text{ V}, V_{GS} = 4.5 \text{ V}$	20			A
Drain-Source On-State Resistance (Note 3)	$r_{DS(on)}$	$V_{GS} = 4.5 \text{ V}, I_D = 5.2 \text{ A}$		0.025	0.030	Ω
		$V_{GS} = 2.5 \text{ V}, I_D = 4.3 \text{ A}$		0.038	0.045	
Forward Transconductance (Note 3)	$g_{fs}$	$V_{DS} = 10 \text{ V}, I_D = 5.2 \text{ A}$		20		S

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage (Note 3)	$V_{SD}$	$V_{GS} = 0 \text{ V}, I_S = 5.2 \text{ A}$		0.8	1.2	V
Reverse Recovery Time	$t_{rr}$	$V_{GS} = 0 \text{ V}, I_S = 5.2 \text{ A}, \frac{dI_S}{dt} = 100 \text{ A}/\mu\text{s}$		20.9		ns
Charge Time	$t_a$			10.2		
Discharge Time	$t_b$			10.6		
Reverse Recovery Time	$Q_{rr}$			11		

2. Surface Mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

4. Guaranteed by design, not subject to production testing.

## TYPICAL ELECTRICAL CHARACTERISTICS

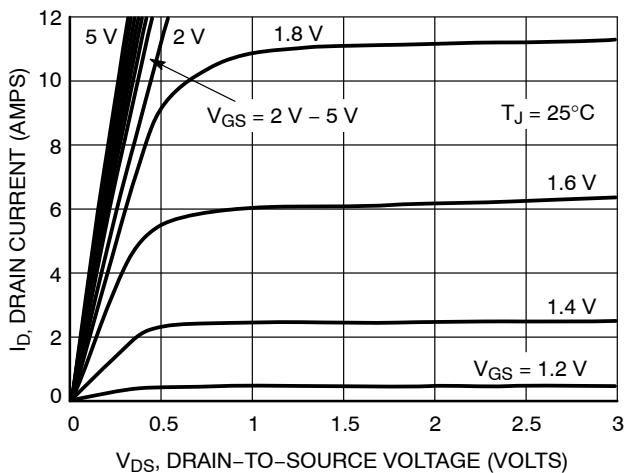


Figure 1. On-Region Characteristics

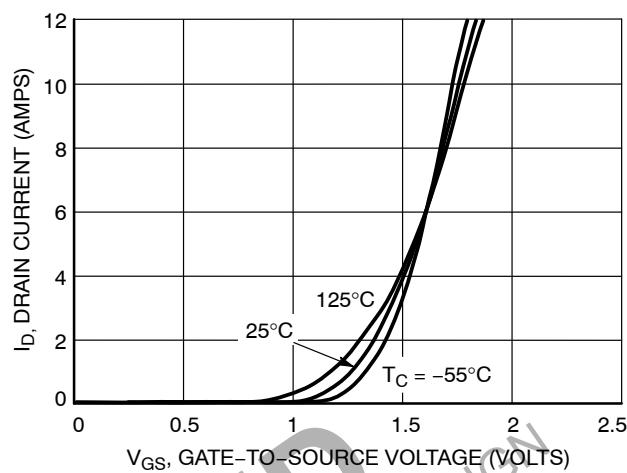


Figure 2. Transfer Characteristics

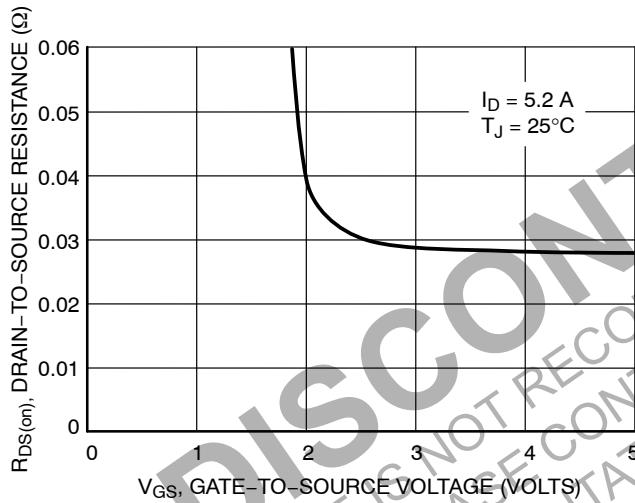


Figure 3. On-Resistance versus Gate-to-Source Voltage

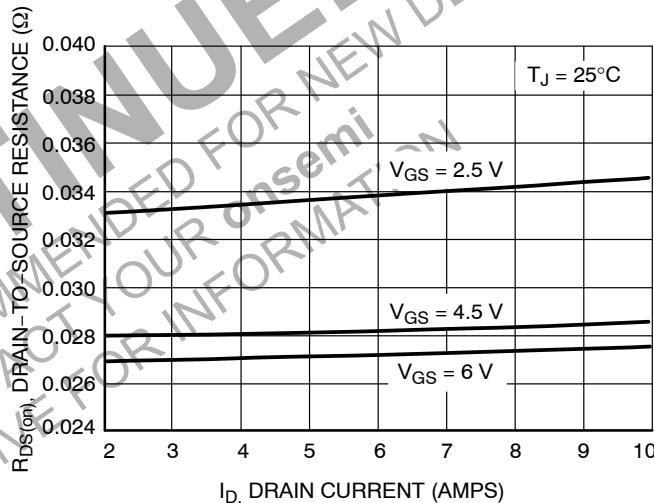


Figure 4. On-Resistance versus Drain Current and Gate Voltage

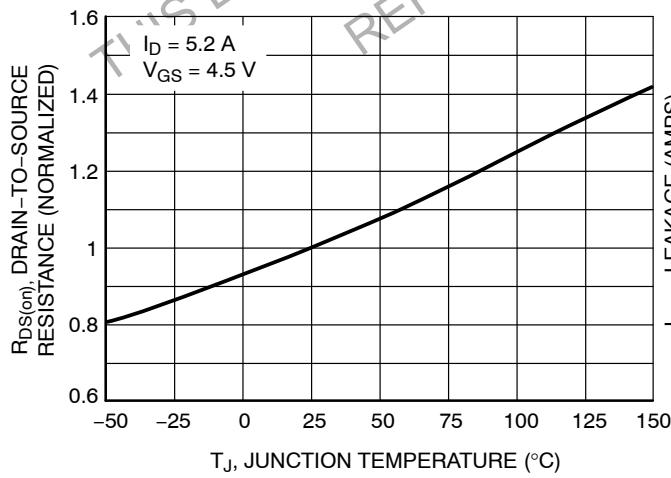


Figure 5. On-Resistance Variation with Temperature

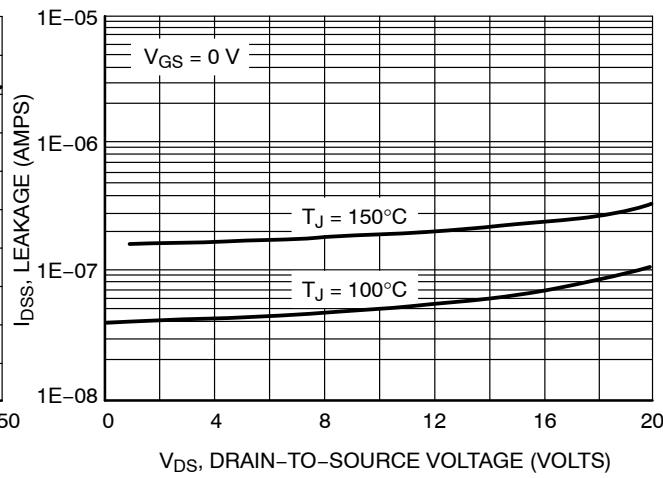
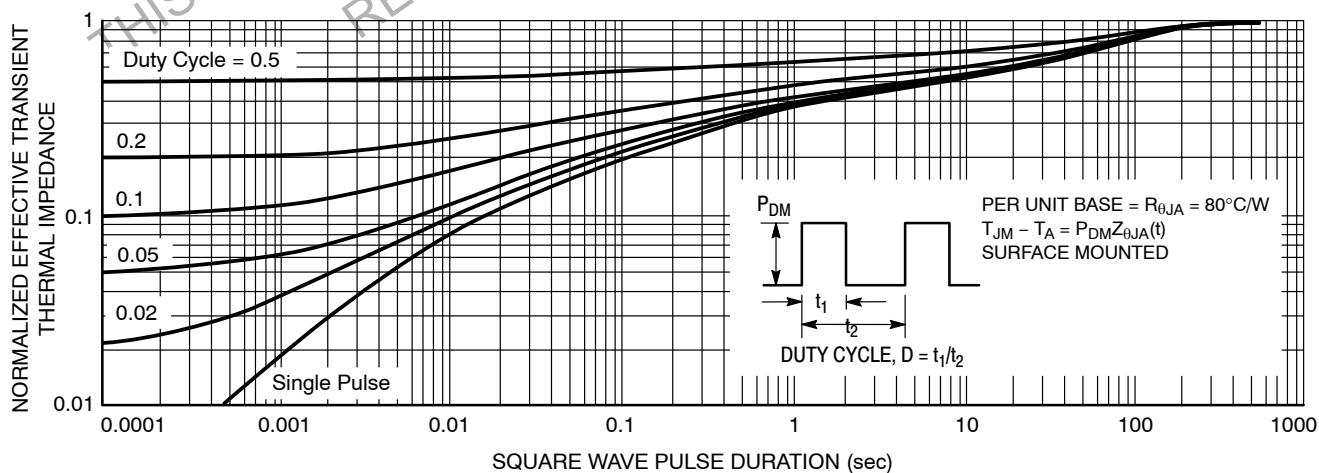
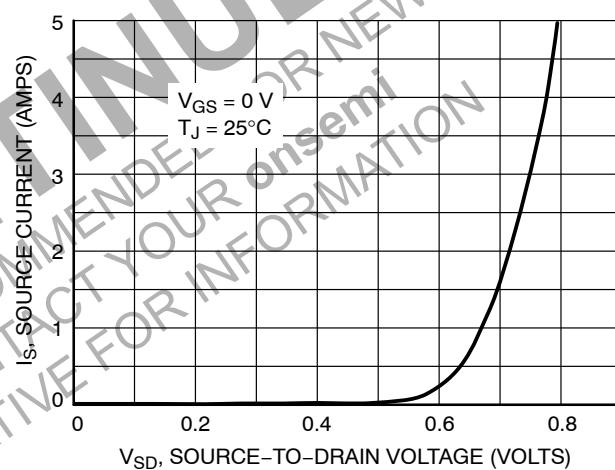
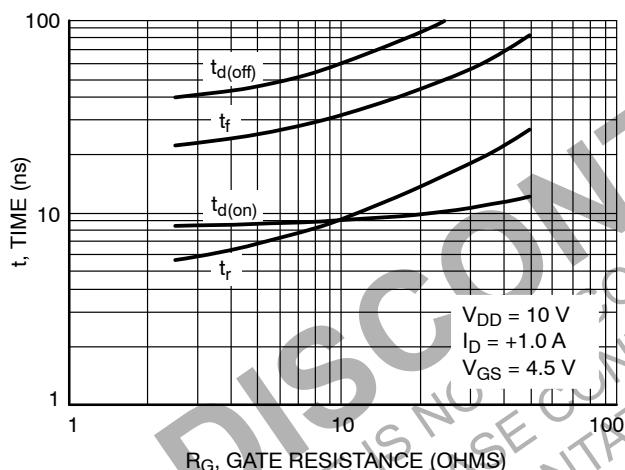
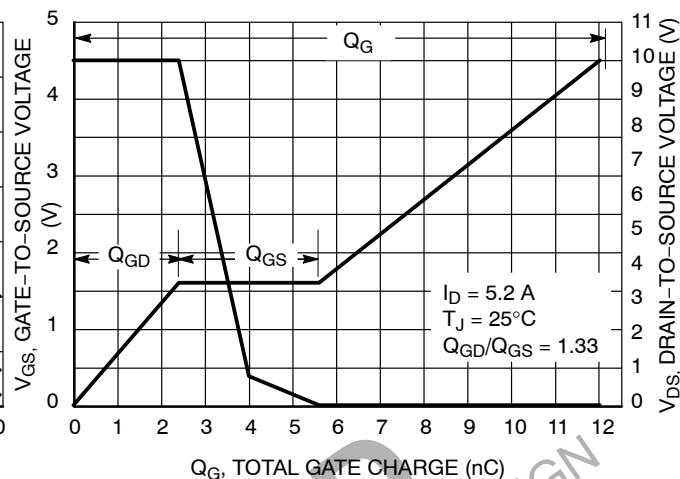
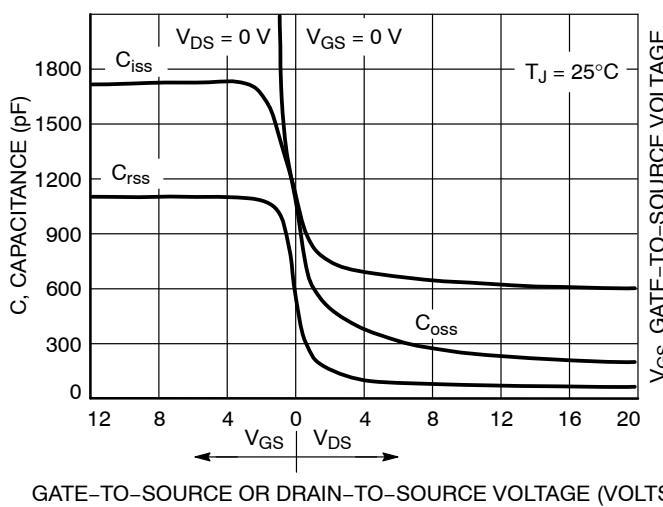


Figure 6. Drain-to-Source Leakage Current versus Voltage

## TYPICAL ELECTRICAL CHARACTERISTICS



## SOLDERING FOOTPRINT\*

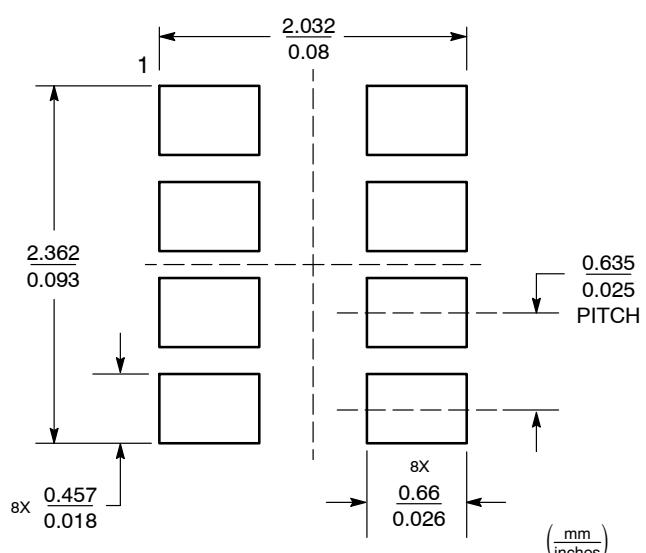


Figure 12. Basic

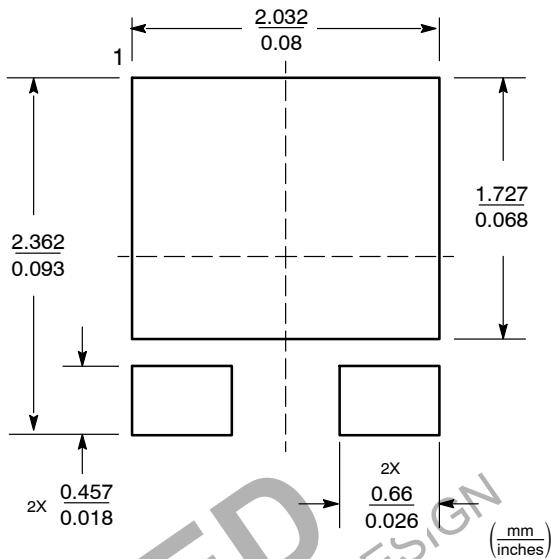
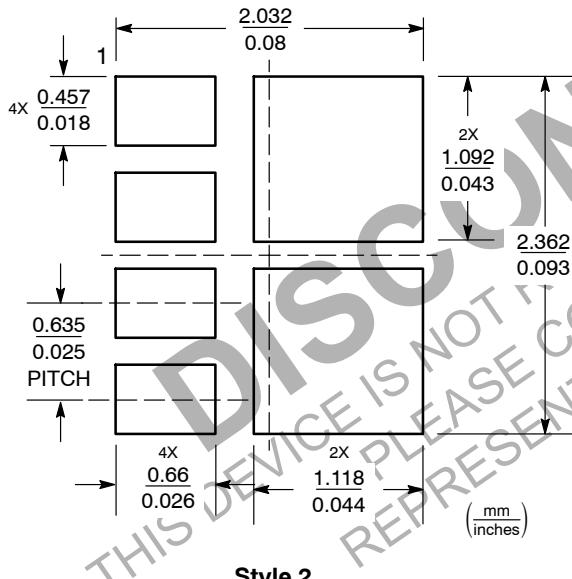
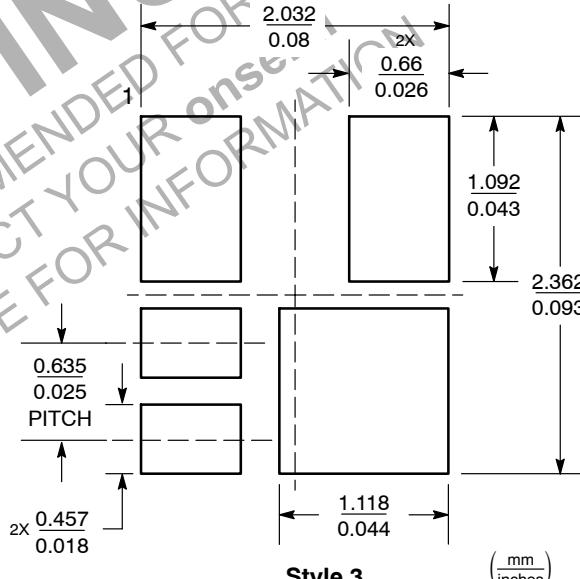


Figure 13. Style 1 and 4

## ADDITIONAL SOLDERING FOOTPRINTS\*



Style 2



Style 3

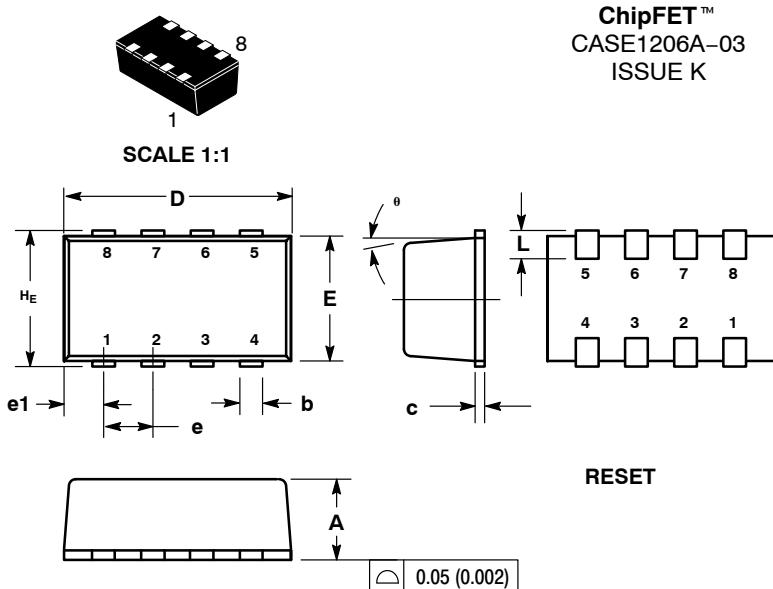
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 12. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 13 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the

confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper lead-frame) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.



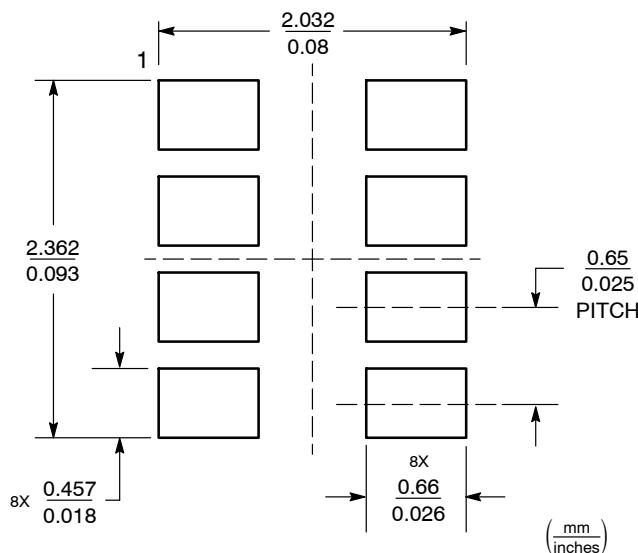
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H <sub>E</sub>	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:	STYLE 2:	STYLE 3:	STYLE 4:	STYLE 5:	STYLE 6:
PIN 1. DRAIN	PIN 1. SOURCE 1	PIN 1. ANODE	PIN 1. COLLECTOR	PIN 1. ANODE	PIN 1. ANODE
2. DRAIN	2. GATE 1	2. ANODE	2. COLLECTOR	2. ANODE	2. DRAIN
3. DRAIN	3. SOURCE 2	3. SOURCE	3. COLLECTOR	3. DRAIN	3. DRAIN
4. GATE	4. GATE 2	4. GATE	4. BASE	4. DRAIN	4. GATE
5. SOURCE	5. DRAIN 2	5. DRAIN	5. Emitter	5. SOURCE	5. SOURCE
6. DRAIN	6. DRAIN 2	6. DRAIN	6. COLLECTOR	6. GATE	6. DRAIN
7. DRAIN	7. DRAIN 1	7. CATHODE	7. COLLECTOR	7. CATHODE	7. DRAIN
8. DRAIN	8. DRAIN 1	8. CATHODE	8. COLLECTOR	8. CATHODE	8. CATHODE / DRAIN

## SOLDERING FOOTPRINT

GENERIC  
MARKING DIAGRAM\*

XXX = Specific Device Code  
M = Month Code  
■ = Pb-Free Package  
(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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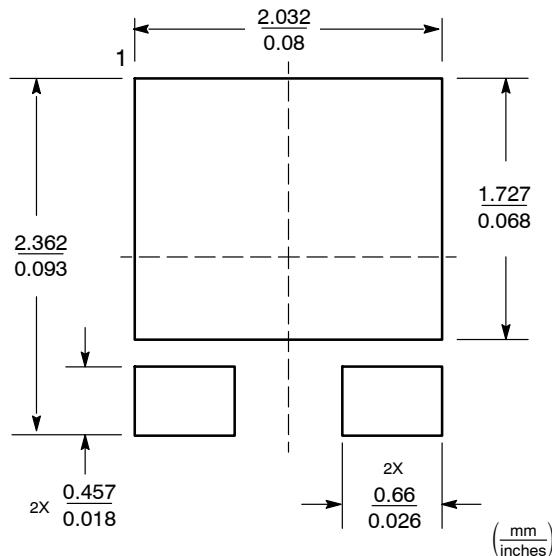
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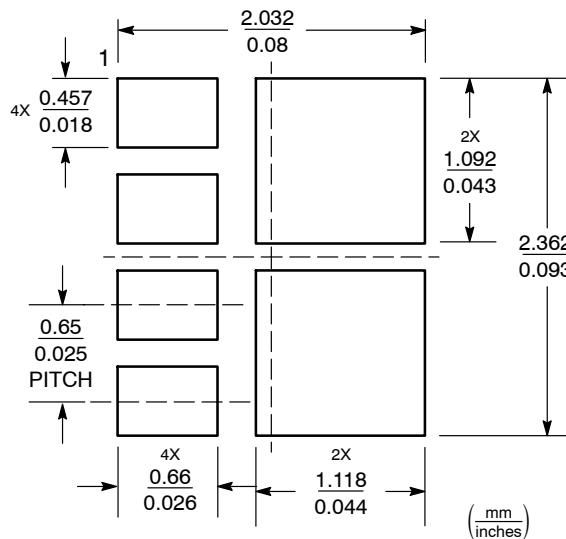
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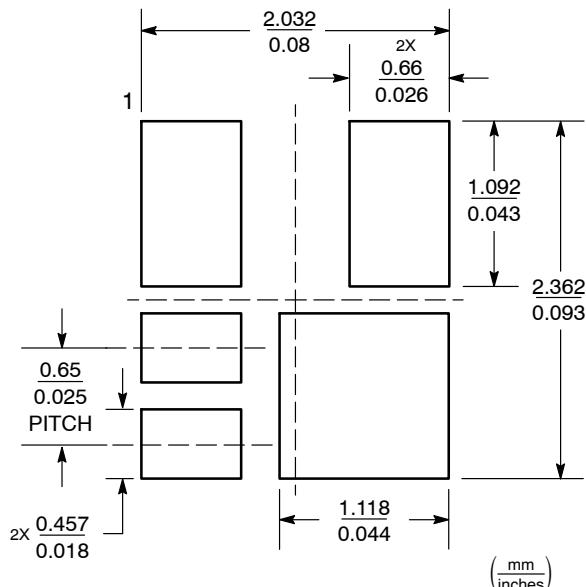
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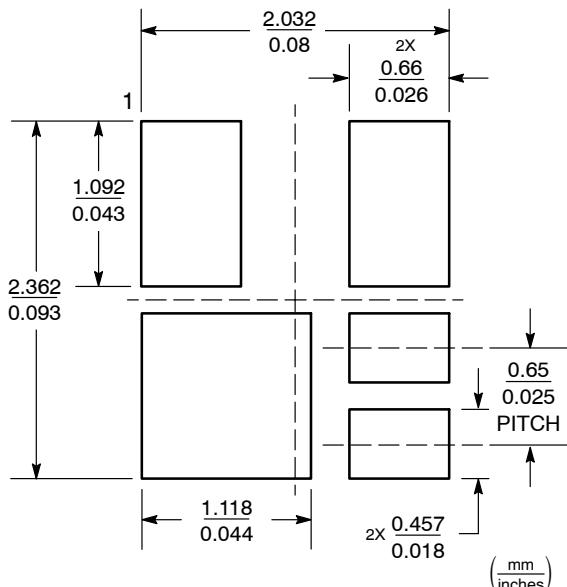
Styles 1 and 4



Style 2



Style 3



Style 5

\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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