# Series String Pixel Controller for Automotive (Front) Lighting

# NCV78343

## Introduction

The NCV78343 is a single−chip pixel controller with embedded switches to control individual LEDs in a series LED string, designed for automotive dynamic lighting applications and in particular for high current LEDs. In order to create a pixel lighting solution, the LEDs need to be powered by current sources such as NCV78763 or NCV78723. The NCV78343 pixel controller devices receive the pixel control parameters from the pixel light ECU which translates the required light pattern or light image into individual pixel dimming data.

One pixel controller device can control up−to 12 pixels of 1× or 2× 1.4 A LEDs per pixel. The maximum LED string voltage has to be limited to 60 V.
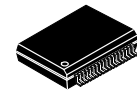
When more than 12 pixels are to be controlled, multiple pixel controllers can be combined in a single system.

The NCV78343 uses two communication interfaces for connection with a microcontroller. A universal asynchronous receiver transmitter (UART), which supports the use of CAN transceiver and multipoint low voltage differential signaling (M−LVDS) for either local connection or connection with the MCU.
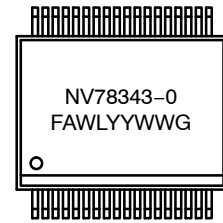
## Features

- Single Chip Compatible with IMS Board (Single Layer)
- 12 Integrated Switches with Multiple Configuration Options
- Minimum of External Components
- Communication Interfaces to the Pixel Light ECU via
  - Integrated M−LVDS
  - UART over CAN Interface
  - Integrated Bridge between M−LVDS and UART
  - Supports up to 32 Devices, 1Mbaud
- No Need for Local MCU and Precise Clock
  - Interface to External I2C EEPROM
  - Integrated 8 bit Analog to Digital Converter
- Dimming Controller
  - PWM + Phase Shift Unit per Channel
- Over Temp Protection
- Individual Open/Short/OV LED Diagnostic Feedback
- Open LED Failure Automatic Bypass
- This is a Pb−Free Device
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

## SAFETY DESIGN – ASIL B

ASIL B Product developed in compliance with ISO 26262 for which a complete safety package is available.

## ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| NCV78343DQ0R2G | SSOP36 EP (P−Free) | 1500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

## Typical Applications

- Dynamic Adaptive Driving Beam Functions
  - Glare−free High Beam
  - Static Swiveling
  - Beam Shaping
  - Light Power Adjustment
- Animated Welcome Functions on Signal Lights
- Wiping Blinker

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## PACKAGE AND PIN DESCRIPTION

| | | | |
|---|---|---|---|
| 1 | C2P | TST1 | 36 |
| 2 | C2N | TST | 35 |
| 3 | NC | SW10 | 34 |
| 4 | SW30 | SW11 | 33 |
| 5 | SW31 | SW12 | 32 |
| 6 | SW32 | SW13 | 31 |
| 7 | SW33 | SW20 | 30 |
| 8 | SW40 | SW21 | 29 |
| 9 | SW41 | SW22 | 28 |
| 10 | SW42 | SW23 | 27 |
| 11 | SW43 | NC | 26 |
| 12 | NC | ADC0/SDA | 25 |
| 13 | RX | ADC1/SCL | 24 |
| 14 | TX | ADC2/ADR | 23 |
| 15 | A | VDD | 22 |
| 16 | B | GND | 21 |
| 17 | NC | A | 20 |
| 18 | VBB | B | 19 |

**Figure 1. Pin Connections – SSOP36–EP (Top View)**

**Table 1. PIN DESCRIPTION**

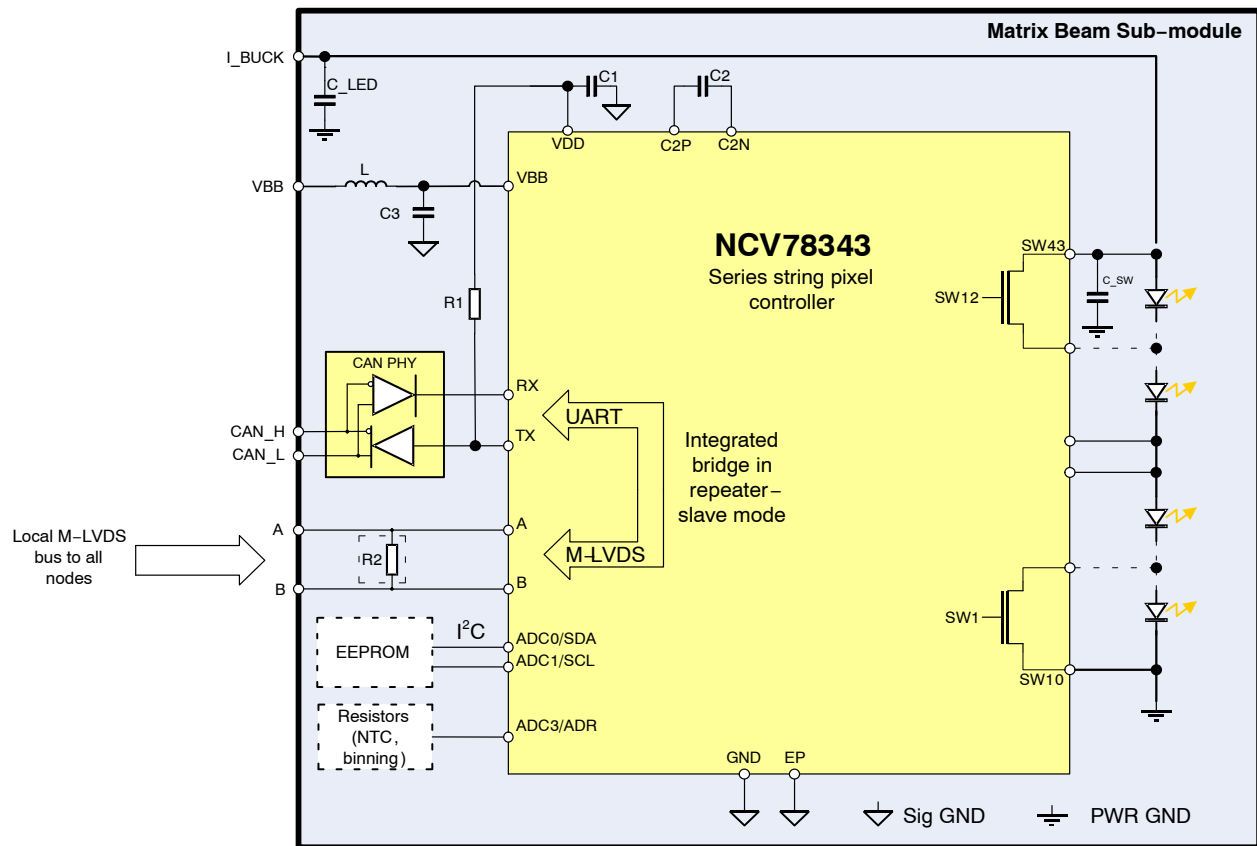| Pin No. SSOP36–EP | Pin Name | Description | I/O Type |
|---|---|---|---|
| 1 | C2P | Switch control capacitor connection | HV in/out |
| 2 | C2N | Switch control capacitor connection | HV in/out |
| 3, 12, 17, 26 | NC | Not used (to be left floating) | NC |
| 31, 32, 33, 34 | SW1y | Power switch to short LED | HV in/out |
| 27, 28, 29, 30 | SW2y | Power switch to short LED | HV in/out |
| 4, 5, 6, 7 | SW3y | Power switch to short LED | HV in/out |
| 8, 9, 10, 11 | SW4y | Power switch to short LED | HV in/out |
| 13 | RX | Receive data input (To be tied to GND when not used) | HV60 in |
| 14 | TX | Transmit data output (To be tied to GND or left floating when not used) | MV out |
| 15, 20 | A | M–LVDS IO pins (internally connected; to be shorted to B when not used) | MV in/out |
| 16, 19 | B | M–LVDS IO pins (internally connected; to be shorted to A when not used) | MV in/out |
| 18 | VBB | Battery supply | HV60 supply |
| 21 | GND | Ground | Ground |
| 22 | VDD | 3V analog and logic supply | LV supply |
| 23 | ADC2/ADR | ADC input 2 / Address | LV in |
| 24 | ADC1/SCL | ADC input 1 / I2C clock | LV in/out |
| 25 | ADC0/SDA | ADC input 0 / I2C data | LV in/out |
| 35 | TST | Internal function. To be tied to GND or left floating | HV70 in |
| 36 | TST1 | Internal function. To be tied to GND | LV in/out |
| EP | EP | To be tied to GND | Exposed Pad |

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**Figure 2. Application Diagram**

### Table 2. EXTERNAL COMPONENTS

| Component | Function | Typ. Value | Unit |
|:---:|:---|:---:|:---:|
| C1 | Cap. for VDD regulator | 470 | nF |
| C2 | Cap. for switch control | 220 | nF |
| C3 | VBB decoupling cap. | 100 | nF |
| C_SW | VLED decoupling cap. | 22 | nF |
| C_LED | VLED decoupling cap. | 22 | nF |
| R1 | Tx pull−up resistor | 100 | kΩ |
| R2 | Terminating resistors (only for the first and last device) | 100 | Ω |
| CAN | CAN transceiver | NCV7344 | |
| M−LVDS | M−LVDS transceiver | NBA3N206S | |
| EEPROM | External EEPROM | CAT24C02 | |
| L | Ferrite bead * | 600 @ 100 MHz | Ω |

\* It is recommended to place a ferrite bead at VBB net close to a VBB decoupling capacitor for a better electromagnetic immunity.

NOTE:   Unused switches to be shorted externally. The switches should be grounded If a full section is not used.
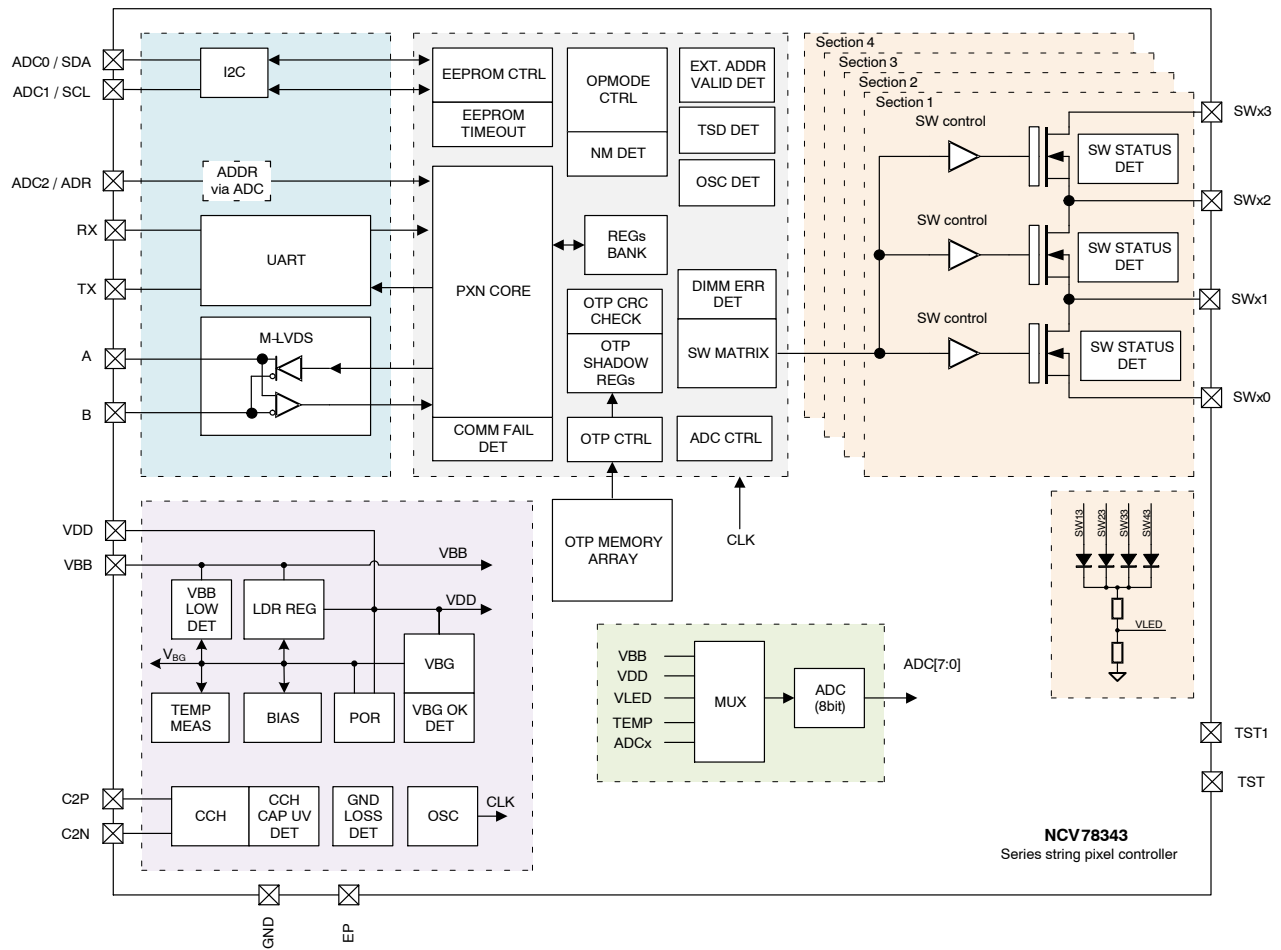
# NCV78343



**Figure 3. Block Diagram**

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The NCV78343 supports two communication interfaces: UART and M−LVDS. It is possible to communicate over both interfaces, where the first example uses the UART interface over CAN physical layer as a master bus from the LED Driver Module to the first NCV78343 chip and the M−LVDS bus for local connection between submodules of each functional lights such as high beam, low beam, turn indicator, etc. The second example uses the M−LVDS bus only.



**Figure 4. System Architecture using CAN−FD and M−LVDS**



**Figure 5. System Architecture using M−LVDS only**

# NCV78343

The advantage of sharing common heatsink for higher currents can be reached by placement of the NCV78343 together with the LEDs on same PCB (IMS type of board supported). This is not necessary for lower currents or application where the LED string is connected over two NCV78343 devices.



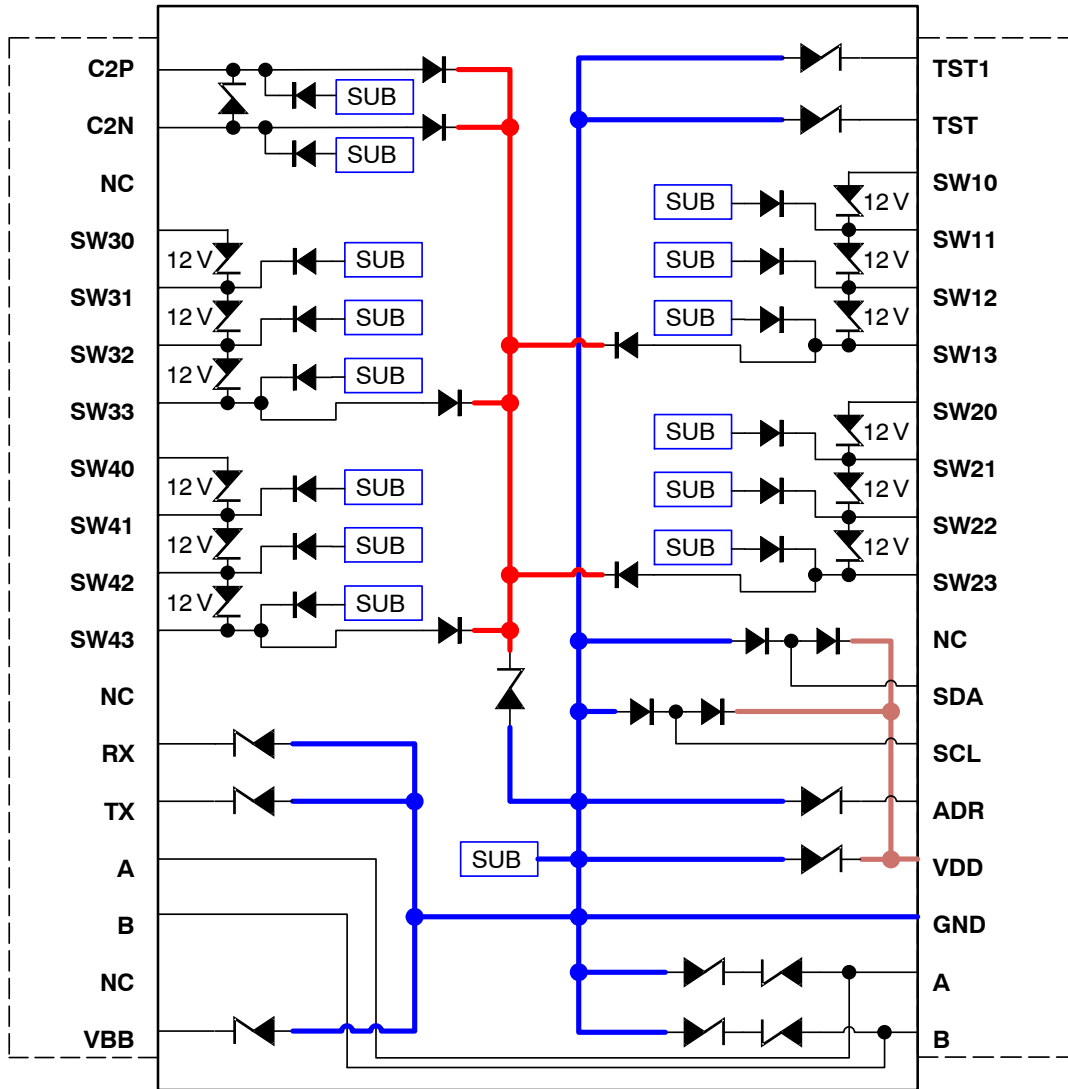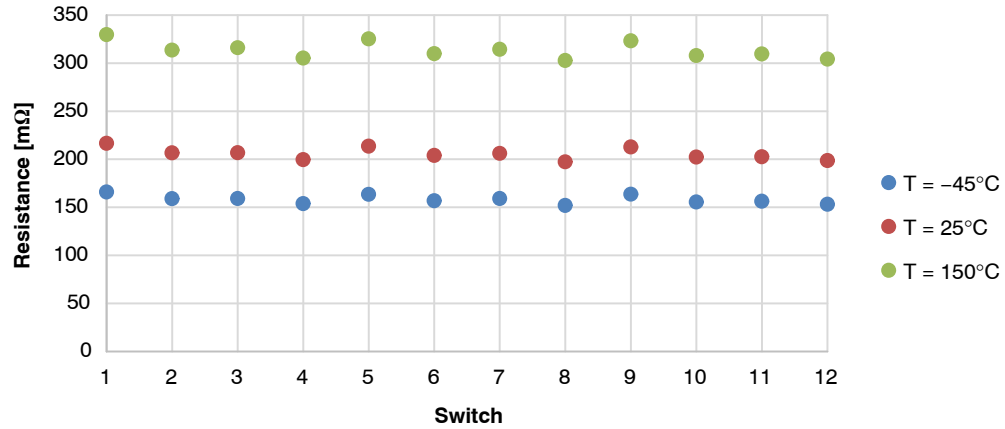**Figure 6. ESD Protection Schematic**

**Typical Switch Resistance**



**Figure 7. Typical Switch Resistance**
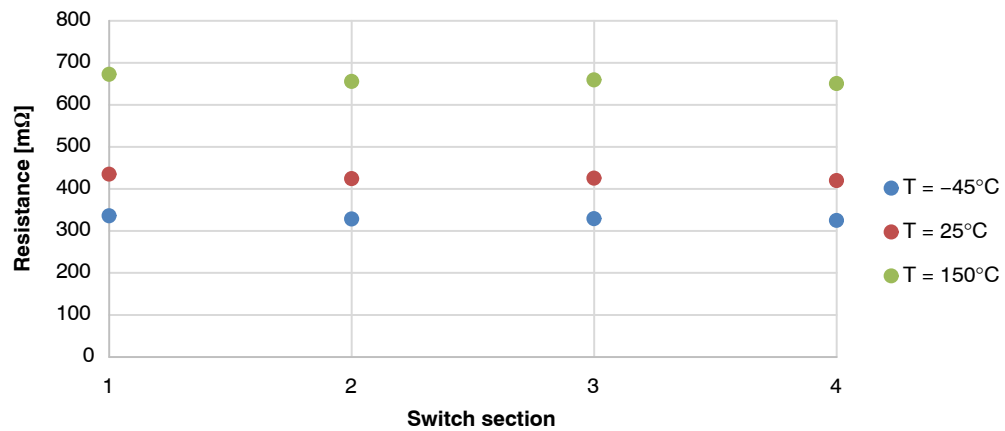
**Typical Switch Section Resistance**



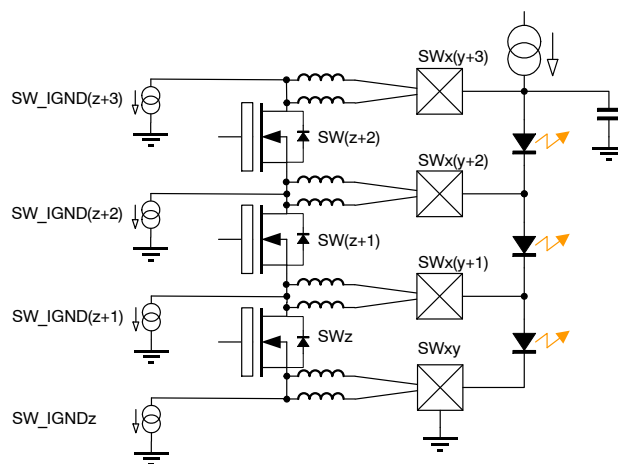**Figure 8. Typical Switch Section Resistance**



**Figure 9. Pixel Switches**

**Table 3. ABSOLUTE MAXIMUM RATINGS**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Battery Supply voltage (Note 1) | $V_{BB}$ | −0.3 | 60 | V |
| Low voltage supply (Note 2) | $V_{DD}$ | −0.3 | 3.6 | V |
| High voltage control IO pins (Note 3) | $I_{OHV60}$ | −0.3 | 60 | V |
| High voltage IO pins (Note 4) | $I_{OHV}$ | −0.3 | 68 | V |
| Medium voltage IO pins (Note 5) | $I_{OMV}$ | −0.3 | 6.5 | V |
| Medium voltage IO pins: M−LVDS (Note 6) | $I_{OMV\_MLVDS}$ | −1.8 | 4 | V |
| Low voltage IO pins (Note 7) | $I_{OLV}$ | −0.3 | 3.6 | V |
| Low voltage supply for switch control: V2 = C2P − C2N | $V_2$ | −0.3 | 3.6 | V |
| Switch differential voltage (Note 8) | $V_{SWxx\_DIFF}$ | −0.3 | 12 | V |
| Storage Temperature (Note 9) | $T_{strg}$ | −50 | 150 | °C |
| Electrostatic discharge on component level Human Body Model (Note 10) | $V_{ESD\_HBM}$ | −2 | +2 | kV |
| Electrostatic discharge on component level Charge Device Model (Note 10) | $V_{ESD\_CDM}$ | −500 | +500 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Absolute maximum rating for pins: VBB
2. Absolute maximum rating for pins: VDD
3. Absolute maximum rating for pins: RX, TST
4. Absolute maximum rating for pins: C2P, C2N, SWxy for x={4÷1} & y={3÷0}
5. Absolute maximum rating for pins: TX
6. Absolute maximum rating for pins: A, B
7. Absolute maximum rating for pins: TST1, ADC0/SDA, ADC1/SCL, ADC2/ADR
8. Absolute maximum rating for pins: SWx_(y+1) − SWxy for x={4÷1} & y={2÷0}
9. For limited time up to 100 hours. Otherwise the max storage temperature is 85°C.
10. This device series incorporates ESD protection and is qualified per AEC−Q100:
    ESD Human Body Model Classification level H1C in according to the AEC−Q100−002 Rev−E
    ESD Charge Device Model Classification C2b in according to the AEC−Q100−011 Rev−D
    Latch − up Current Maximum Rating: ≤ 100 mA in according to the AEC−Q100−004 Rev−D JEDEC−Class II

Operating ranges define the limits for functional operation and parametric characteristics of the device. A mission profile (Note 11) is a substantial part of the operation conditions; hence the Customer must contact **onsemi** in order to mutually agree in writing on the allowed missions profile(s) in the application.

**Table 4. RECOMMENDED OPERATING RANGES**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Battery supply voltage | $V_{BB}$ | 4.5 | | 40 | V |
| Switch differential voltage | $V_{SW\_DIFF}$ | 0 | | 10 | V |
| LED string voltage | $V_{STRING}$ | 0 | | 60 | V |
| Buck switch output current | $I_{SW}$ | | | 1.4 | A |
| PXN communication speed | $S_{PXN}$ | 125 | | 1000 | kbit |
| Ambient temperature | $T_A$ | −40 | | 125 | °C |
| Junction temperature range (Note 12) | $T_J$ | −40 | | 150 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.
11. The circuit functionality is not guaranteed outside the Operating junction temperature range. A mission profile describes the application specific conditions such as, but not limited to, the cumulative operating conditions over life time, the system power dissipation, the system's environmental conditions, the thermal design of the customer's system, the modes, in which the device is operated by the customer, etc.
12. The circuit functionality is not guaranteed outside the junction temperature range. Also please note that the device is verified on bench for operation up to 170 °C but the production test guarantees 150 °C only.

**Table 5. THERMAL RESISTANCE**

| Characteristic | Package | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal resistance junction to exposed pad (Note 13) | SSOP36−EP | Rthjp | | 3.5 | | °C/W |

13. Includes also typical solder thickness under the Exposed Pad (EP).

## ELECTRICAL CHARACTERISTICS

NOTE: All Min and Max parameters are guaranteed over full junction temperature ($T_{JP}$) range (−40 °C; 150 °C), unless otherwise specified.

### Table 6. CURRENT CONSUMPTION

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| The VBB current consumption | I_VBB | | | 19 | 25 | mA |
| The VBB current consumption UART only device | I_VBB_M−LVDS_OFF | M−LVDS off; OTP bit M−LVDS_OFF = '1' | | 6.5 | 10 | mA |

### Table 7. OSC20M: SYSTEM OSCILLATOR CLOCK

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Oscillator output frequency (trimmed) | OSC_CLK | | 18.2 | 20 | 21.8 | MHz |
| Oscillator duty cycle | OSC_DC | | 30 | 50 | 70 | % |

### Table 8. VDD: 3.45V LOW VOLTAGE ANALOG AND DIGITAL SUPPLY

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| VDD regulator output voltage | VDD | VBB > 4.5 V | 3.15 | 3.45 | 3.6 | V |
| VDD regulator current limitation | VDD_ILIM | VBB > 4.5 V | 40 | | 300 | mA |
| OUT_OFF_REG comparator voltage | V_OUT_OF_REG | | 2.7 | | 3.45 | V |
| VDD POR threshold, VDD rising | POR3V_H | | 2.7 | | 2.95 | V |
| VDD POR threshold, VDD falling | POR3V_L | | 2.5 | | 2.75 | V |
| VDD POR hysteresis | POR3V_HYST | | 0.1 | 0.2 | 0.3 | V |
| VBB POR threshold, VBB rising | POR_VBB_H | | 3.8 | | 4.3 | V |
| VBB POR threshold, VBB falling | POR_VBB_L | | 3.7 | | 4.2 | V |
| VBB POR hysteresis | POR_VBB_HST | | 0.05 | 0.1 | 0.25 | V |
| OTP UV comparator threshold (VBB pin) | OTP_UV | | 12.5 | | 15 | V |
| VBB supply during the OTP zapping | VBB_ZAP | | 15 | | 30 | V |
| VBB current limitation for OTP zapping | IBAT_ZAPP | | 85 | | | mA |

### Table 9. SWITCH CONTROL

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| V(C2) under voltage threshold, V(C2) rising | CCH_UVH | | 2.65 | 2.75 | 2.85 | V |
| V(C2) under voltage threshold, V(C2) falling | CCH_UVL | | 2.6 | 2.72 | 2.85 | V |
| Current from VBB to charge C2 capacitor | CCH_IBB | | 2 | | 15 | mA |
| Current limitation from VDD (during start−up) | CCH_ILIM_RST | | 6 | 12 | 20 | mA |
| Current limitation from VDD | CCH_ILIM | | 8 | 12 | 16 | mA |
| Voltage drop between VDD and V(C2) | CCH_VDROP | | | 120 | 270 | mV |
| V(C2) voltage after recharge CCH_V2 = VDD − CCH_VDROP | CCH_V2 | | | 3.33 | | V |
| Switch OFF time | SOF_TRISE | 5 mA, without decoupling capacitor | 1.5 | 1.6 | 2.5 | μs |
| Switch gate voltage detection threshold | SOF_VTH_A | At ambient temperature | 0.4 | 0.8 | 1.6 | V |
| Switch gate voltage detection threshold | SOF_VTH_C | At cold temperature | 0.9 | 1.3 | 1.7 | V |
| Switch gate voltage detection threshold | SOF_VTH_H | At hot temperature | 0.2 | 0.8 | 1.2 | V |
| Switch Short detection voltage threshold | SSH_VTH | | 0.35 | | 1 | V |
| Switch Overvoltage detection threshold | SOV_TH | | 10 | | 13.5 | V |

**Table 10. PIXEL SWITCHES**

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| RON from SWx3 to SWx0 pin (3 switches) | SW_3R | At ambient | | 0.43 | 1.1 | Ω |
| RON from SWxy to SWx(y−1) pin (1 switch) | SW_1R | At ambient | | 0.2 | 0.6 | Ω |
| Current from SWxy pin to GND (see Figure 9) | SW_IGND | | 40 | 53 | 70 | μA |

**Table 11. ADC FOR MEASURING VBB, VDD, VLED, TEMP, ADC$_X$**

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| ADC Resolution | ADC_RES | | | 8 | | Bits |
| Integral Non−linearity (INL) | ADC_INL | Best fitting straight line method | −1.5 | | +1.5 | LSB |
| Differential Non−linearity (DNL) | ADC_DNL | Best fitting straight line method | −2.0 | | +2.0 | LSB |
| Full path gain error | ADC_GE | VBB, VDD measurements | −3.25 | | 3.25 | % |
| Offset at output of ADC | ADC_OFFSET | VBB, VDD measurements | −2 | | 2 | LSB |
| Time for 1 SAR conversion | ADC_CONV | | 6.67 | 8 | 10 | μs |
| ADC full scale for VBB measurement | ADC_VBB | | 33.5 | 35 | 36.5 | V |
| ADC full scale for VDD measurement | ADC_VDD | | 3.87 | 4 | 4.13 | V |
| ADC full scale for VLED measurement | ADC_VLED | | 63.6 | 66.1 | 68.6 | V |
| ADC full scale for ADCx measurement | ADC_ADCx | | 1.175 | 1.205 | 1.235 | V |
| ADCx input current | I_ADCx | | 0.3 | 1 | 1.7 | μA |
| TSD threshold level | ADC_TSD | ADC measurement of junction temperature | 163 | 170 | 177 | °C |
| Accuracy of temperature meas at hot | ADC_TEMP_ACC_HOT | T = 155 °C | −7 | | 7 | °C |
| Accuracy of temperature meas at cold | ADC_TEMP_ACC_COLD | T = −40 °C | −15 | | 15 | °C |

**Table 12. GND LOSS DETECTION**

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| GND loss comparator threshold; both edges | GNDLOSS_THR | | 100 | 120 | 160 | mV |
| GND loss comparator delay; both falling and rising edge | GNDLOSS_DEL | | | 800 | 1200 | ns |

**Table 13. UART INTERFACE: RX, TX**

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High−level input voltage | RX_VIH | | 2 | | | V |
| Low−level input voltage | RX_VIL | | | | 0.8 | V |
| Input voltage hysteresis | RX_VIhyst | | 100 | 200 | 400 | mV |
| Input pull−down resistance | RX_RPULL | | 40 | | 160 | kΩ |
| High−level output voltage | TX_VOH | I$_{LOAD}$ = −3mA | 2.1 | | VDD or external pull−up voltage | V |
| Low−level output voltage | TX_VOL | I$_{LOAD}$ = 3mA | | | 0.4 | V |
| TX pin leakage current in HiZ | TX_ILEAK | | −1 | | 1 | μA |
| TX pin capacitance | TX_C | | | 5 | | pF |
| Propagation delay | TX_DL_50pF | C$_{LOAD}$ up to 50 pF | | | 40 | ns |
| Propagation delay | TX_DL_200pF | C$_{LOAD}$ up to 200 pF | | | 150 | ns |

**Table 14. M−LVDS INTERFACE: A, B**

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Differential output voltage magnitude | M−LVDS_TX_VAB | Rload_A−B = 49.9 Ω ±1%<br>Vtest = from −1 V to 3.4 V | 480 | | 650 | mV |
| Change in Differential output voltage magnitude between logic states | M−LVDS_TX _DVAB | Rload_A−B = 49.9 Ω ±1%<br>Vtest = from −1 V to 3.4 V | −50 | | 50 | mV |
| Steady state common mode output voltage | M−LVDS_TX _VOS | Rload_A−B = 49.9 Ω ±1% | 1 | 1.2 | 1.4 | V |
| Change in Steady state common mode output voltage between logic states | M−LVDS_TX _DVOS | Rload_A−B = 49.9 Ω ±1% | −50 | | 50 | mV |
| Peak−to−peak common−mode output voltage | M−LVDS_TX _VOSPP | Rload_A−B = 49.9 Ω ±1% | | | 150 | mV |
| Maximum steady−state open−circuit output voltage | M−LVDS_TX _VOC | Rload ≥ 1.62 kΩ | 1.9 | | 2.28 | V |
| Short−circuit output current magnitude | M−LVDS_TX _IOS | Vtest = from −1 V to 3.4 V | | | 43 | mA |
| Voltage overshoot, low−to−high level output | M−LVDS_TX _VPH | VSS = 2·VAB | | | 1.2 | VSS |
| Voltage overshoot, high−to−low level output | M−LVDS_TX _VPL | VSS = 2·VAB | −0.2 | | | VSS |
| Differential Output rise and fall times | M−LVDS_TX _TE | | | 5 | 12 | ns |
| Transmitter Propagation delay | M−LVDS_TX _TP | | 5 | 10 | 20 | ns |
| Positive−going Differential Input voltage Threshold for BUS common mode <0; 3.8> V | M−LVDS_RX_VITP | | | | 150 | mV |
| Positive−going Differential Input voltage Threshold for BUS common mode <−1.4; 0> V | M−LVDS_RX_VITP_NCMM | | | | 160 | mV |
| Negative−going Differential Input voltage Threshold for BUS common mode <0; 3.8> V | M−LVDS_RX _VITN | | 50 | | | mV |
| Negative−going Differential Input voltage Threshold for BUS common mode <−1.4; 0> V | M−LVDS_RX _VITN_NC̄MM | | 60 | | | mV |
| Receiver Propagation delay | M−LVDS_RX _TP | | 20 | 40 | 60 | ns |
| A or B pin capacitance | M−LVDS_C | | | 5 | | pF |
| Transceiver input current in high impedance state (range 1) | M−LVDS_IOZ_1 | 0 V ≤ (VA or VB) ≤ 2.4 V,<br>other output at 1.2 V,<br>transmitter in HiZ | −20 | | 20 | µA |
| Transceiver input current in high impedance state (range 2) | M−LVDS_IOZ_2 | −1.4 V ≤ (VA or VB) ≤ 0 V<br>or<br>2.4 V ≤ (VA or VB) ≤ 3.8 V,<br>other output at 1.2V,<br>transmitter in HiZ | −32 | | 32 | µA |

**Table 15. I2C INTERFACE: SDA, SCL**

| Characteristic | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| High−level input voltage | I2C_VIH | | 0.7 | | | VDD |
| Low−level input voltage | I2C_VIL | | | | 0.3 | VDD |
| Input voltage hysteresis | I2C_VIhyst | | 300 | | 700 | mV |
| Low−level output voltage | I2C_VOL | | | | 0.4 | V |
| High−level output voltage | I2C_VOH | $I_{LOAD}$ = −3 mA | | VDD−0.1 | | V |
| SDA or SCL pin capacitance | I2C_C | $I_{LOAD}$ = 3 mA | | 5 | | pF |
| SCL to SDA and SDA to SCL propagation delay, both edges | I2C_DL | | 5 | | 60 | ns |

## DETAILED OPERATING AND PIN DESCRIPTION

### SUPPLY CONCEPT IN GENERAL

Low operating voltages become more and more required due to the growing use of start stop systems. In order to respond to this necessity, the NCV78343 is designed to support power−up starting from VBB = 4.5 V.
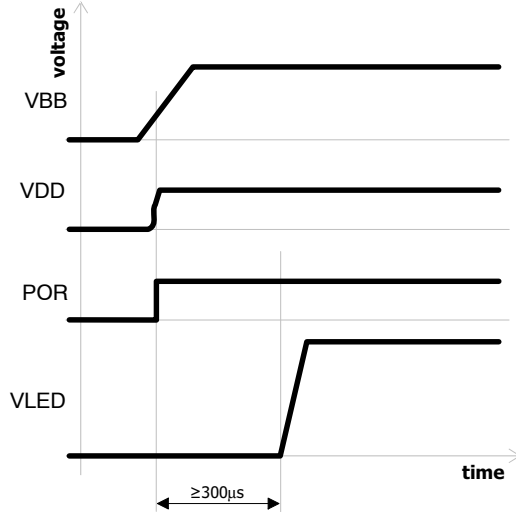


**Figure 10. Power−up Sequence**

A specific power−up and power−down sequences are shown in the Figure 20 and Figure 21.

There is no special circuit to disable switches in case of VBB power supply disconnection. The gate of the switch is discharged by SW−OFF circuit in case the VBB−LOW threshold is crossed. The gate of the switch is discharged by leakage currents when the supply is suddenly lost. Because of low leakage currents, the switch may stay enabled for a few seconds after power lost. Possible temperature rise speeds up opening the switch by higher leakage current.

### VDD Supply

The VDD supply is the low voltage digital and analog supply for the chip, which is powered from VBB. VDD is supplying the internal analog and digital circuits as well as external components like I2C EEPROM and resistor divider on ADC inputs. The POR−circuit is monitoring both the VBB and VDD voltages.

### VLED Supply

If the device is running but the LED current source is disconnected, the LEDs can light up because of the bias currents flowing through pins of the switches. Up to 180 μA (typical) from switch current source may cause the bottom−most LED to shine. If needed, resistors can be connected in parallel to the switches to avoid undesired LED lighting (typically 10 kΩ).

### INTERNAL CLOCK GENERATION

The clocks are fully internally generated without the need for any trimming by the user. The accuracy is guaranteed under all operating conditions and independent of external component selection.

### OSC20M Clock

The OSC20M clock is the system clock. All the internal timings as well as the internal PWM unit depend on OSC20M accuracy.

### Communication Clock

The internal clock is also used for oversampling of UART incoming frame and I2C EEPROM, so there is no need for any external clock.

### DIMMING CONTROLLER

Internal (built−in) dimming controller allows change of light intensity of individual LEDs in LED string by means of digital (PWM) dimming.

### Dimming Control Parameters

The dimming for all switches is controlled from 1 common 10−bit counter. The ON and OFF events are programmable per channel, each with a 10 bit counter value.

100% duty cycle is generated when ON time is set to min. value (0) and OFF time is set to max value (1023).

0% duty cycle is generated when ON time is equal to OFF time. When more than one 0% or 100% duty cycle is required, the TR (transition) slots must be used.

The dimming frequency is the DIMCLK frequency divided by 1024. The $T_{DIMCLK}$ is the duration of one PWM tick. The duration of one PWM period is $T_{PWM}$. The required time for one switch ON sequence is $T_{SW\_SEQ}$. The ratio of $T_{SW\_SEQ}$ and $T_{DIMCLK}$ results in number of PWM ticks required for one switch ON sequence. The number of slots available for each DIMCLK is 1024 divided by the ratio. The recommended time for TR slots and recommended step between each switch ON request is shown in Table 43. When the TR slot technique is used, the ON values should not be set within this period.

### Dimming Mode

The NCV78343 incorporates two modes of operation – ON/OFF dimming mode and direct mode.

- **ON/OFF mode** – the NCV78343 controls the dimming duty cycle and phase shift for each switch individually. The time of ON event is set by means of <ONx[9:0]> register and the time of OFF event is set by means of <OFFx[9:0]> register.
- **Direct mode** – in addition to ON/OFF dimming mode, the state of the switches can be controlled directly by means of <SWx> register.
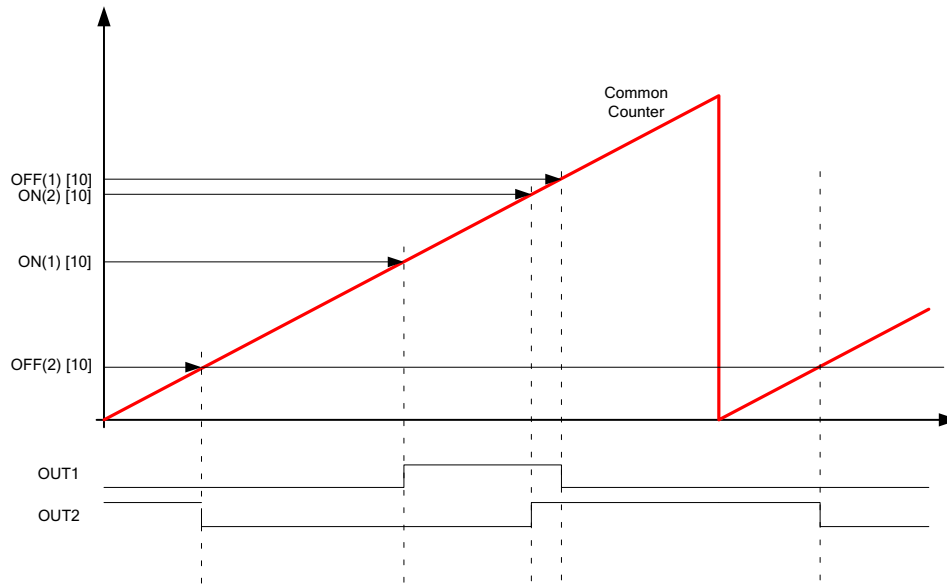
**Figure 11. Dimming Operation (dimming ON/OFF event)**

**Dimming Transition Vector Insertion**

Transition vectors are required in case of pattern changes (update of dimming settings) for avoiding multiple switching events at the same time and minimizing brightness error.

Fully closed switch (100% duty cycle) requires ON event equal to 0. It can happen that such switch ON event is required on more switches at the same time, which is not allowed. Therefore a transition slot technique is used for consecutive activation of those switches (which need to be changed to 100% duty cycle). When overlapping multiple switch ON events are invoked despite this, the <DIMERR> error is raised. When overlapping switch OFF events occur, the <DIMWARN> status bit is set and processing of this pattern continues. However, multiple switch OFF events may cause large LED string voltage changes.

Transition vector inserts additional transition either ON or OFF event at the beginning of next PWM period (in transition slots space). This helps to reduce brightness error significantly and the duty cycle is affected only in one period. The error is proportionate to duration of transition slot.

Pattern is updated when common PWM counter overflows and <MAPENA> = '1' (see Table 64) is set.

The NCV78343 contains 12 channels, so with unique settings of <TRx[3:0]> for each switch 12 different Transient Vector values are needed in the worst case ("0x0" to "0xB"). When <TRx[3:0]> = '0xC', '0xD', '0xE' or '0xF', the <TRx[3:0]> is ignored and transition vectors are not applied. In this case the switch status from previous PWM period is kept unchanged until next ON or OFF event into opposite direction.

**PWM dimming clock**

Selection of internal dimming clock is done by means of <DIMFREQ[4:0]> register, which shall be used to select dimming frequencies in range of 125 kHz to 1 MHz (see Table 43. PWM Frequency Settings).

**SWITCH CONFIGURATIONS**

The 12 integrated switches are typically organized as $12 \times 1$ switch of 1.4 A, but can be organized in $6 \times 2$ switches in parallel to offer $6 \times 1$ switch of 2.8 A. Examples of switch configurations are shown in Figure 12.

Selection of the switch configuration is done by <CONF_SEL[2:0]> register. Detailed information about switch configuration is available in Table 16.

**Table 16. SWITCH CONFIGURATIONS**

| CONF_SEL [2:0] | Conf. Code Name | Description |
|---|---|---|
| 000 | 1, 2, 3, 4 | $12 \times$ PWM channels |
| 001 | 1+2, 3, 4 | $9 \times$ PWM channels (PWM 1=2) |
| 010 | 1+2, 3+4 | $6 \times$ PWM channels (PWM 1=2 & 3=4) |
| 011 | 1, 2+3, 4 | $9 \times$ PWM channels (PWM 2=3) |
| 100 | 1, 2, 3+4 | $9 \times$ PWM channels (PWM 3=4) |
| 101 | 1+4, 2+3 | $6 \times$ PWM channels (PWM 1=4 & 2=3) |
| 110 | 1+4, 2, 3 | $9 \times$ PWM channels (PWM 1=4) |
| 111 | 1, 2, 3, 4. | Same as 0000, $12 \times$ PWM channels |

In case of configurations with 2× current, PWM signals of sections with higher index are controlled with PWM signals from lower index section. For example in case of configuration "101", the PWM signals of section 1 is controlling section 4; control signals of section 2 is controlling section 3.



**Figure 12. Example of Switch Configurations**

Parallel combination is used where the $I_{DR}$ current exceeds maximum switch current 1.4 A. This is not for use in redundant applications.

The following consequence must be taken into account when using parallel switches:

The OTP safe−state bits should be zapped to "0" to avoid sequentially switching ON which might cause that the higher current will flow through one switch.

**Analog Input**

The analog input AIN is an input channel that can be used for different types of measurements, like e.g. LED temperature or battery voltage. The converted voltage is calculated with the following formula:

$$V_{ADC_x} = ADC\_RES_{X_{[7:0]}} \cdot \frac{1.205}{255} \ [V] \qquad \text{(eq. 1)}$$

where
$ADC\_RES_X$ is saved in register 0x11

**OPEN, SHORT and FAIL Status Detection**



**Figure 13. OPEN, SHORT and FAIL Status Detection Timing**

Following the figure above, the OPEN and SHORT flags are detected only during the switch OFF state. The On/Off Failed flag detection is triggered by the transition between the switch ON and the switch OFF event. The SHORT and On/Off Failed status flags are cleared upon a successful read out of register 0x0F. Due to this behavior and the diagram above, the read status might alternate between the SHORT and On/Off Failed, following the duty cycle of the specific switch. When the buck current is disabled, the device reports SHORT status for all switches.



NOTE:    MAPENA DIRECT means writing into REG 0x00. MAPENA PWM means either writing into REG 0x0D or sending CF15.

**Figure 14. Normal Mode State Machine**

**Pixel Light Network**

The PXN is a proprietary network technology developed primarily for communication with and within the LED matrix head light system (see Figure 15).

The LED matrix head light system may incorporate a various number of sub−systems interconnected using PXN technology. The connection of such sub−system to a local network is realized using M−LVDS physical interface and a twisted−pair cable. Termination is required at both ends of the twisted−pair cable. Nominally, it is 100 Ω across the pair. Transmitter on the bus sees both termination resistors in parallel, thus the nominal bus load is actually 50 Ω.

The LED matrix head light system can be integrated into a superior system through an optional physical interface, e.g. differential low speed CAN. The choice of the external physical interface is application specific.

The PXN protocol for communication over PXN is based on UART communication standard, i.e. one start bit, 8 data bits (LSB first), one stop bit, no parity bit.

Rx pin is 5 V tolerant and has CMOS compatible threshold levels. External pull−up resistor is required on Tx pin.



**Figure 15. PXN Topology Inside LED Matrix Head Light System**

**Table 17. THE UART SIGNAL LEVELS TRANSFERRED TO M−LVDS BUS**

| UART RX Input Pin | M−LVDS Differential Voltage A−B | UART TX Output Pin |
|---|---|---|
| LOW | POSITIVE (A−B > 150 mV) | LOW |
| HIGH | NEGATIVE (A−B < 50 mV; in M−LVDS push−pull mode; valid for repeater−slave) | HIGH |

The table above must be taken into account when using only M−LVDS slaves cluster. The master MCU generates UART signal, which is connected to the M−LVDS transceiver, where the A and B pins are connected to the A and B pins on the devices. Since the M−LVDS signal is inverted to the UART signal, there must be placed an invertor on the Tx pin from the MCU to M−LVDS transceiver and another invertor on the Rx pin from the M−LVDS transceiver to the MCU.

**PXN Switch**

The PXN switch is responsible for PXN frame routing within a particular PXN node connected to network.

**PXN Media Access Layer**

The MAC layer is responsible for a PXN frame composition on a transmitting side, the PXN frame decomposition on a receiving side, a transmission of composed PXN frames, a reception of PXN frames and PXN network error detection and confinement.

**PXN Frame**

A message is transferred over PXN bus in a form of PXN frame, which is depicted in Figure 16. The PXN protocol for communication over PXN is based on UART communication standard, i.e. one start bit, 8 data bits (LSB first), one stop bit, no parity bit.

The PXN frame consists of a header and a response. The header is always transmitted by PXN master while the response can either be transmitted by master, in case of write frames or by slave, in case of read frames. The header and the response are separated by in−frame response space.

The header consists of a BREAK field (logic 0 for a certain time), a SYNC field (0x55 byte) and two protected identifiers PID1 and PID2. The response consists of an arbitrary number of DATA bytes within a range from 1 to 12 followed by CRC. The particular bytes are separated by inter−byte space. Minimal delay of 1 Tbit is required before starting new PXN frame. The minimum length for the BREAK field is 13 Tbits (52 μs for the default

communication speed 250 kbps). The BREAK field stop bit (BREAK field delimiter) is minimum 1 Tbit and maximum according to the selected watchdog time. If the device is not responding through the repeater−slave, the extended break (26 Tbits) can be required to recover communication to slave devices. Such case can occur when Read frame is addressed non assigned address. In case of only M−LVDS

slave cluster, the DE pin on the M−LVDS transceiver (e.g. NBA3N206S) must be set LOW within 1 Tbit after the Header part to allow device response.

The PXN protocol supports two frame types:
 − configuration frame
 − register bank frame



**Figure 16. PXN Frame**

### PXN Configuration Frame

The configuration PXN frame allows activation and monitoring of selected configuration service.

**Table 18. PXN CONFIGURATION FRAME**

| Byte | Name | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] | | | | |
| 2..13 | DATAx | DATA[7:0] 0 ..11 | | | | | | | |
| 3 | CRC | CRC[7:0] | | | | | | | |

PID1:

| P | odd parity bit |
|---|---|
| SA [4:0] | 5−bit slave node address |

PID2:

| P | odd parity bit |
|---|---|
| CSID[4:0] | 5−bit configuration service identifier |
| DATAx[7:0] | 8−bit data, from 1 up to 12 data bytes supported |
| CRC[7:0] | 8−bit CRC |

### PXN Register Bank Frame

The register bank PXN frame provides an access, both read or write to selected register(s) of internal register bank.

**Table 19. PXN REGISTER BANK FRAME**

| Byte | Name | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | FT[1:0] | | SA[4:0] | | | | |
| 1 | PID2 | P | BC[1:0] | | RBA[4:0] | | | | |
| 2..13 | DATAx | DATA[7:0] 0 ..11 | | | | | | | |
| 3 | CRC | CRC[7:0] | | | | | | | |

PID1:

| P | odd parity bit |
|---|---|

| FT [1:0] | 2−bit frame type: |
|---|---|
| | "00" − read frame |
| | "01" − write frame to address node only |
| | "10" − write frame to all nodes (broadcast) |
| SA [4:0] | 5−bit slave node address |

PID2:

| P | odd parity bit |
|---|---|
| BC[1:0] | 2−bit byte count |
| RBA[4:0] | 5−bit register bank address |
| DATAx[7:0] | 8−bit data, from 1 up to 12 data bytes supported |
| CRC[7:0] | 8−bit CRC |

### PXN Register Bank Frame Matched by Length

The PXN network supports devices with different logical organization of internal register bank. The following logical organizations of register bank are supported:

| TYPE1 | − up to 32x24 bits |
|---|---|
| TYPE2 | − up to 32x16 bits |
| TYPE3 | − up to 32x8 bits |

Each of types above has predefined number of data bytes for given PID2.BC parameter in case PID1.FT="10" (broadcast frame).

**Table 20. BROADCAST PXN FRAME DATA BYTE COUNT**

| PID2.BC[1:0] | Data Byte Count | | |
|---|---|---|---|
| | TYPE1 | TYPE2 | TYPE3 |
| 0x0 | 3 | 2 | 1 |
| 0x1 | 6 | 4 | 5 |
| 0x2 | 9 | 8 | 7 |
| 0x3 | 12 | 10 | 11 |

The NCV78343 supports only the TYPE1 register bank organization, since each register bank consists of 3 bytes.

This means that it is possible to read/write up to 4 registers in one frame, which can be for example used to write ON/OFF times for all 12 switches in only 3 PXN frames.

**PXN Error Detection**

The PXN network supports detection of these errors:
- frame error
- timeout error
- synchronization error
- local communication error
- global communication error

**PXN Application Layer**

List of supported configuration services:

**Table 21. CONFIGURATION SERVICES**

| Configuration Service | | Configuration Frame | | | |
|---|---|---|---|---|---|
| Name | Code | Name | CSID | Type | Description |
| Identification | 0 | CF0 | 0x00 | R | Slave Identification |
| Ext. EEPROM | 1 | CF1 | 0x01 | W | Write data to ext. I2C EEPROM |
| | | CF2 | 0x02 | W | Request data from ext. I2C EEPROM |
| | | CF3 | 0x03 | R | Read Data from ext. I2C EEPROM |
| Auto−addressing | 2 | CF4 | 0x04 | W | Enable/disable auto−addressing mode |
| | | CF5 | 0x05 | W | Assign address |
| | | CF6 | 0x06 | R | OP mode status |
| PXN mode | 3 | CF7 | 0x07 | W | Slave/repeater−slave PXN mode selection |
| | | CF8 | 0x08 | R | Read PXN mode status |
| OTP | 4 | CF9 | 0x09 | W | Write data to OTP |
| | | CF10 | 0x0A | W | Request data from OTP |
| | | CF11 | 0x0B | R | Read data from OTP |
| UART | 5 | CF12 | 0x0C | W | Set UART communication speed |
| System | 6 | CF13 | 0x0D | W | Switch to normal mode |
| | | CF14 | 0x0E | W | Reset system |
| | | CF15 | 0x0F | W | Trigger MAPENA and/or CNTRST |

List of supported register bank access:

**Table 22. REGISTER BANK ACCESS**

| Configuration Service | | Configuration Frame | | |
|---|---|---|---|---|
| Name | Code | Name | Access Type | Description |
| Read/Write | 0 | WF1 | Read | Write register bank |
| | | RF1 | Write | Read register bank |

**PXN Communication Modes**

The PXN node can operate in one of the two communication modes:
- slave mode
- repeater−slave mode

Depending on the mode selected, the PXN switch is configured to route the PXN frames the respective way. The repeater−slave device works as a bridge between UART bus and M−LVDS bus. It forwards frames from UART to M−LVDS and back from M−LVDS to UART when reading from a slave device.

*Addressing Options*

It is possible to set a device address in 3 different ways:
- Multi−level address pin
- Auto−addressing procedure
- OTP node address bits

Addressing using OTP memory is recommended for final application. Some of the other device parameters are saved in memory as well, which speeds up device setup after each power−on.

**Multi−level Address Pin**

The PXN node address can be determined by connecting ADC2/ADR input to a voltage divider. The voltage divider, represented by resistors R1 and R2 are supplied from regulated 3.3 V VDD supply. The voltage space is divided into 10 ranges where only 8 of them are associated with valid address. The corresponding thresholds are calculated as follows:

**Table 23. MULTI−LEVEL ADDRESS PIN**

| PXN | Resistor Divider | | ADC2/VDD | |
|---|---|---|---|---|
| Addr | R1 (kΩ) | R2 (kΩ) | min. (−) | max. (−) |
| 7 | 91 | 27 | 0.75 | 0.79 |
| 6 | 68 | 15 | 0.59 | 0.63 |
| 5 | 91 | 15 | 0.46 | 0.49 |
| 4 | 82 | 10 | 0.35 | 0.38 |
| 3 | 91 | 8.2 | 0.27 | 0.29 |
| 2 | 51 | 3.3 | 0.20 | 0.21 |
| 1 | 82 | 3.6 | 0.14 | 0.15 |
| 0 | 51 | 1.3 | 0.08 | 0.09 |

In case of valid address the node can process both the addressed and the broadcast frames. In case of invalid address the node can process the broadcast frames only.



**Figure 17. Voltage divided connected to ADC2/ADR Pin**

The Multi−level addressing procedure requires stable voltage level at ADC2/ADR pin in 200 μs after POR. If the application cannot ensure this time, please follow the

Multi−level addressing procedure with long time delay recommendation in Application notes. If the Multi−level addressing is successful, a device stays in the OTP config mode (see Figure 23).

### Auto−addressing Procedure

Regardless the node address assigned after the measurement of ADC2/ADR multi−level input, the auto−addressing procedure can still be invoked using the auto−address enable PXN frame. The auto−addressing is enabled/disabled on the PXN node upon receiving CF4 PXN configuration frame. The CF4 frame is accepted in the OTP_CONFIG mode only (see Table 53).

The PXN node address, when auto−addressing is enabled is assigned upon receiving CF5 PXN configuration frame. The CF5 frame is accepted in AUTO_ADDR mode only (see Table 54).

The auto−addressing procedure is described in the APPLICATION RELATED INFORMATION section.

### OTP Node Address

The OTP node address can be zapped by customer at EoL (End of Line) after the PXN node address was determined either by means of multi−level address pin measurement or by means of auto−addressing procedure. The value of OTP node address and OTP bank lock bit is obtained each time the PXN node is powered up and the custom OTP bank is read out. Loading of other device settings from OTP memory speeds up device setup after power−on. OTP memory zapping is necessary to fulfil ASIL B safety requirements.

### PXN Communication Speed

The PXN node can communicate at following speed:
− 125 kb/s
− 250 kb/s (default)
− 500 kb/s
− 1 Mb/s

Communication speed is changed upon receiving CF12 PXN communication frame in OTP_CONFIG, AUTO_ADDR and NORMAL modes only (see Table 61).

### OTP Bank − Custom Data

The custom OTP bank is typically zapped by customer at EOL and stored values are used for system operation customization.

**Table 24. OTP BANK**

| OTP# | OTP Name |
|---|---|
| 0 | **OTP lock bit** |
| 1 | OTP node address lock bit |
| 2 | OTP node address bit 0 |
| 3 | OTP node address bit 1 |
| 4 | OTP node address bit 2 |
| 5 | OTP node address bit 3 |
| 6 | OTP node address bit 4 |
| 7 | **Fail safe state lock bit** |
| 8 | Fail safe state of LEDs in string 1 |
| 9 | Fail safe state of LEDs in string 2 |
| 10 | Fail safe state of LEDs in string 3 |
| 11 | Fail safe state of LEDs in string 4 |
| 12 | **PXN lock bit** |
| 13 | Mode (slave/repeater−slave) |
| 14 | Communication speed bit 0 |
| 15 | Communication speed bit 1 |
| 16 | Global bit error detection disable |
| 17 | M−LVDS OFF |
| 18 | UART OFF |
| 19 | **EEPROM lock bit (write protect)** |
| 20 | CRC bit0 |
| 21 | CRC bit1 |
| 22 | CRC bit2 |
| 23 | CRC bit3 |
| 24 | CRC bit4 |
| 25 | CRC bit5 |
| 26 | CRC bit6 |

<OTP_LOCK_BIT> − custom OTP bank general lock bit. When zapped, any further zapping attempt of custom OTP bank is declined.

<OTP_NODE_ADDR_LOCK_BIT> − PXN node address lock bit. When zapped, any further zapping attempt of <OTP_NODE_ADDR> bits of custom OTP bank is declined.

<OTP_NODE_ADDR [4:0]> − 5−bit PXN node address. This address is taken into account only when the <OTP_NODE_ADDR_LOCK_BIT> is zapped.

<FAIL_SAFE_STATE_LOCK_BIT> − fail safe state of LED string lock bit. When zapped, any further zapping attempt of <FAIL_SAFE_STATE_LED_STRINGx> bits of custom OTP bank is declined.

<FAIL_SAFE_STATE_LED_STRINGx> − state of the LED string x, x={1,2,3,4}, in case one of the following conditions is detected:
● NORMAL mode is entered or
● Timeout error occurred

The bits set directly the switch state. The fail safe state is taken into account only when

<FAIL_SAFE_STATE_LOCK_BIT> is zapped.

<PXN_LOCK_BIT> − PXN settings lock bit. When zapped, any further zapping attempt of PXN settings related bits of custom OTP bank is declined.

<PXN_MODE> − PXN communication mode selection bit. Set '0' for slave mode and '1' for repeater−slave mode. The mode selection is taken into account only when the <PXN_LOCK_BIT> is set and the CRC is correct.

<PXN_COMMUNICATION_SPEED [1:0]> – 2−bit PXN communication speed selection bit. The communication speed selection is taken into account only when the <PXN_LOCK_BIT> is set and the CRC is correct.

**Table 25. PXN COMMUNICATION SPEED**

| COMMUNICATION_SPEED[1:0] OTP Setting | PXN Communication Speed [kb/s] |
|---|---|
| 0x0 | 125 |
| **0x1** | **250** |
| 0x2 | 500 |
| 0x3 | 1000 |

The default communication speed, when the <PXN_LOCK_BIT> is not zapped is 250 kbps.

<GLOBAL_BIT_ERR_DTC_DIS> – global bit error detection disable. In case the global bit error detection is enabled (<GLOBAL_BIT_ERR_DTC_DIS> is not zapped) the data transmitted on chip's TX output must be echoed back into chip's RX input. There are two ways to generate the TX echo. Either it can be ensured by a CAN transceiver connected between a chip and an MCU on UART bus or it can be generated by the MCU itself. When the echo is not present, chip stops transmitting and will wait for new incoming frame. When more than one device is present on the UART bus, the repeater−slave will always report <PXN_GLOBAL_COMM_ERR> bit when reading from another device on the UART bus. In case the global bit error detection is disabled, the reading from an address not assigned to a physical device will block the further operation of the repeater−slave device. Such device must be unplugged from a battery voltage in order to make it operational again. The global bit error detection is enabled by default.

The device configured to act as a PXN repeater−slave shall always have the global bit error detection enabled, i.e. <GLOBAL_BIT_ERR_DTC_DIS> shall be not zapped. The setting of <GLOBAL_BIT_ERR_DTC_DIS> bit does not affect the communication over M−LVDS bus. The <GLOBAL_BIT_ERR_DTC_DIS> bit is taken into account only when the <PXN_LOCK_BIT> is set and the CRC is correct.

<UART_OFF> – UART interface disable. The <UART_OFF> selection is taken into account only when the <PXN_LOCK_BIT> is set and the CRC is correct.

<M−LVDS_OFF> – M−LVDS interface disable. The <M−LVDS_OFF> selection is taken into account only when the <PXN_LOCK_BIT> is set and the CRC is correct. Unused M−LVDS transceiver can be disabled to reduce current consumption by 12.5 mA (typical).

<EEPROM_LOCK_BIT> – external EEPROM lock bit. The EEPROM lock bit acts as an EEPROM write protection. When zapped, any further write attempts to external EEPROM is declined.

**OTP Memory Zapping**

The OTP zapping process is one−time programming process during which the OTP memory is written. This process cannot be undone. The OTP zapping is possible only in the OTP config mode. To ensure correct OTP zapping, the VBB voltage must be in range of 16 to 30 V with the current capability at least 85 mA during the OTP zapping process. The OTP memory zapping should be done at the EoL to fulfil the ASIL B requirements.

External MCU can read content of OTP memory. To do this, device must first receive CF10 PXN configuration frame followed by CF11 PXN configuration frame. This process is similar to reading from external I2C EEPROM.

**Operating Modes**

The PXN node can operate in following modes:
- – OTP Config mode
- – Auto−addressing mode
- – Normal Direct mode
- – Normal PWM mode
- – Normal Fail−safe OTP mode
- – Normal Fail−safe OPEN mode
- – NO_CRC Direct mode
- – NO_CRC PWM mode
- – Fail−safe OTP mode
- – Fail−safe OPEN mode

OTP Config mode – the chip enters this mode under the following circumstances: when the OTPs are not zapped and the voltage divider at ADR pin is in a valid range, or the OTPs are zapped but the OTP CRC BANK2 is wrong, or after successful auto−addressing process. Please see the following flow diagram 'Flow chart after POR' in the Application notes.

Chip with non−zapped OTP memory starts with both UART and M−LVDS interfaces enabled. To determine which one will be used, there is a 60 ms timer (typical) that starts once device enters OTP Config mode. After timer elapses, chip reads state of UART RX pin to determine if UART bus should remain enabled (RX pulled high) or disabled (RX pulled low). During this period, M−LVDS devices might be unable to communicate if their UART RX pin is pulled low. Timer can be stopped before elapsing by leaving OTP Config mode, typically by receiving CF13.

Auto−addressing mode – when the chip receives CF4 (see Table 53) configuration frame.

Normal Direct/PWM mode – this is the normal working mode, the chip enters this mode after the POR when the OTPs are zapped and the CRC is correct. Direct means that the switches are controlled directly by writing to the register 0x00. The PWM means that the switches are controlled by the PWM by writing ON and OFF values and sending CF15 (see Table 64).

NO_CRC Direct/PWM mode – the device enters the NO_CRC mode after receiving CF13 (see Table 62) in the OTP Config mode. The functionality of NO_CRC Direct

and PWM modes is same as Normal Direct and Normal PWM modes. NO_CRC prefix means that the device detected invalid CRC in OTP memory bank 2 during power on, most likely because OTP memory is not written.

Please note that only device with written OTP memory achieves ASIL B safety rating.

Fail−safe OTP mode – when this fail−safe state is entered after watchdog timeout, OTP fail−safe data are loaded and applied on switches. Chip also enters this mode after DIMERR. To leave this mode, clear TIMEOUT or DIMERR flags set in register 0x10.

Fail−safe OPEN mode – this is the fail−safe state when the switches are automatically open under the following circumstances: TSD or CAP_UV or VBB_LOW appears. To leave this mode, please read out the register 0x10.

**EEPROM**

The external I2C EEPROM can be connected to SDO and SCL pins and supplied from the VDD net.

The PXN node writes data to EEPROM upon receiving CF1 PXN configuration frame (see Table 50). The PXN node reads data from EEPROM upon receiving CF2 PXN configuration frame (see Table 51). The EEPROM data are stored in the internal buffer.

The PXN node provides the data, previously read from the EEPROM and stored in the internal buffer upon receiving CF3 configuration frame (see table 52). The EEPROM address is valid for "1010" + <EESA> .

The write and read operations are shown in the application notes chapter (EEPROM write and read operations).

**Cyclic Redundancy Check**

All PXN frames are covered by an 8−bit CRC, where the polynomial is 0x83 (Koopman's notation; $x^8+x^2+x^1+1$) with 0xFF seed. The input bytes are bit swapped and LSB first. The CRC is calculated over PID1, PID2 and DATAx bytes.

The OTP bank 2 is covered by a 7−bit CRC, where the polynomial is 0x5B (Koopman's notation; $x^7+x^5+x^4+x^2+x^1+1$) with 0x7F seed. The input is MSB first. The CRC is calculated over bits 0−19.

The code examples for both CRCs are shown in the APPLICATION RELATED INFORMATION chapter.

## Table 26. PXN REGISTER BANK ADDRESS MAP

| Address | Access | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | BYTE2 (7..0) | | | | | | | | BYTE1 (7..0) | | | | | | | | BYTE0 (7..0) | | | | | | | |
| 0x0 | R/W | SERVICE=0x0 | – | – | – | – | – | – | – | – | – | – | – | SW12 | SW11 | SW10 | SW9 | SW8 | SW7 | SW6 | SW5 | SW4 | SW3 | SW2 | SW1 |
| | | SERVICE=0x1 | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | – | SW_SEL | | | |
| | | SERVICE=0x2 | | | | | | | | RESERVED_1 | | | | | | | | | | | | | | | |
| | | SERVICE=0x3 | | | | | | | | RESERVED_2 | | | | | | | | | | | | | | | |
| 0x1 | R/W | ON1 | | | | | | | | | | OFF1 | | | | | | | | | | TR1 | | | |
| 0x2 | R/W | ON2 | | | | | | | | | | OFF2 | | | | | | | | | | TR2 | | | |
| 0x3 | R/W | ON3 | | | | | | | | | | OFF3 | | | | | | | | | | TR3 | | | |
| 0x4 | R/W | ON4 | | | | | | | | | | OFF4 | | | | | | | | | | TR4 | | | |
| 0x5 | R/W | ON5 | | | | | | | | | | OFF5 | | | | | | | | | | TR5 | | | |
| 0x6 | R/W | ON6 | | | | | | | | | | OFF6 | | | | | | | | | | TR6 | | | |
| 0x7 | R/W | ON7 | | | | | | | | | | OFF7 | | | | | | | | | | TR7 | | | |
| 0x8 | R/W | ON8 | | | | | | | | | | OFF8 | | | | | | | | | | TR8 | | | |
| 0x9 | R/W | ON9 | | | | | | | | | | OFF9 | | | | | | | | | | TR9 | | | |
| 0xA | R/W | ON10 | | | | | | | | | | OFF10 | | | | | | | | | | TR10 | | | |
| 0xB | R/W | ON11 | | | | | | | | | | OFF11 | | | | | | | | | | TR11 | | | |
| 0xC | R/W | ON12 | | | | | | | | | | OFF12 | | | | | | | | | | TR12 | | | |
| 0xD | R/W | – | – | – | – | – | – | – | – | TW_CODE[7:0] | | | | | | | | – | – | – | – | ADC_SEL[1:0] | | CRC_CLR | MAP_ENA |
| 0xE | R/W | – | – | – | – | – | – | – | – | – | – | – | T1_CONF | – | – | – | – | DIMFREQ[4:0] | | | | | CONF_SEL[2:0] | | |
| 0xF | R | SW12.STATUS[1:0] | | SW11.STATUS[1:0] | | SW10.STATUS[1:0] | | SW9.STATUS[1:0] | | SW8.STATUS[1:0] | | SW7.STATUS[1:0] | | SW6.STATUS[1:0] | | SW5.STATUS[1:0] | | SW4.STATUS[1:0] | | SW3.STATUS[1:0] | | SW2.STATUS[1:0] | | SW1.STATUS[1:0] | |
| 0x10 | R | PXN_CRC_ERR_CNT[3:0] | | | | OTP_CRC_FAIL_BANK0 | OTP_CRC_FAIL_BANK2 | TIMEOUT | PXN_SYNC_ERR | PXN_FRAME_ERR | PXN_LOCAL_COMM_ERR | PXN_GLOBAL_COMM_ERR | MAP_ENA_STATUS | PWM_CNT_OVF | GND_LOSS | VBB_LOW | OTP_ZAP_UV | CAP_UV | HWR | 0 | DIM_ERR | DIM_WARN | GSW_ERR | TSD | TW |
| 0x11 | R | ADCX_RES[7:0] | | | | | | | | VDD_RES[7:0] | | | | | | | | TEMP_RES[7:0] | | | | | | | |
| 0x12 | R | TSD_CODE[7:0] | | | | | | | | VLED_RES[7:0] | | | | | | | | VBB_RES[7:0] | | | | | | | |

NOTE: Default value of all registers after POR is 0x00 if not specified explicitly.

**Table 27. REGISTER 0x00**

| Register 0x00 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x00 | Name | SW12 | SW11 | SW10 | SW9 | SW8 | SW7 | SW6 | SW5 | SW4 | SW3 | SW2 | SW1 |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x00 | Name | SERVICE[23:22] | | – | – | – | – | – | – | – | – | – | – |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

SERVICE[1:0] – specify the behavior of the last [21:0] bits:

"00" – Direct control – Direct control of all switches all together

"01" – OPEN clear request – De−activation of selected switch in on state due to OPEN fault previously detected

"10" – Reserved

"11" – Reserved

SW[11:0] – Direct control of the switches ON/OFF or OPEN clear request:

SERVICE = "00": direct control of the switches ON/OFF; valid SW[11:0], others are "0".

SERVICE = "01": OPEN clear request; Switch is chosen by valid SW_SEL[3:0] from "0001" to "1100" (Switch 1 to 12), others are "0".

**Table 28. REGISTER 0x01**

| Register 0x01 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x01 | Name | OFF1[11:4] | | | | | | | | TR1[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x01 | Name | ON1[23:14] | | | | | | | | | | OFF1[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON1[9:0] – 10−bit switch ON threshold.

OFF1[9:0] – 10−bit switch OFF threshold.

TR1[3:0] – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 29. REGISTER 0x02**

| Register 0x02 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x02 | Name | OFF2[11:4] | | | | | | | | TR2[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x02 | Name | ON2[23:14] | | | | | | | | | | OFF2[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON2[9:0] – 10−bit switch ON threshold.

OFF2[9:0] – 10−bit switch OFF threshold.

TR2[3:0] – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 30. REGISTER 0x03**

| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | **Register 0x03** | | | | | | | |
| 0x03 | Name | OFF3[11:4] | | | | | | | | TR3[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x03 | Name | ON3[23:14] | | | | | | | | | | OFF3[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON3[9:0] – 10−bit switch ON threshold.

OFF3[9:0] – 10−bit switch OFF threshold.

TR3[3:0] – Transition vector duration, it is prolonging the duration of  ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 31. REGISTER 0x04**

| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | **Register 0x04** | | | | | | | |
| 0x04 | Name | OFF4[11:4] | | | | | | | | TR4[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x04 | Name | ON4[23:14] | | | | | | | | | | OFF4[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON4[9:0] – 10−bit switch ON threshold.

OFF4[9:0] – 10−bit switch OFF threshold.

TR4[3:0] – Transition vector duration, it is prolonging the duration of  ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 32. REGISTER 0x05**

| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | **Register 0x05** | | | | | | | |
| 0x05 | Name | OFF5[11:4] | | | | | | | | TR5[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x05 | Name | ON5[23:14] | | | | | | | | | | OFF5[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON5[9:0] – 10−bit switch ON threshold.

OFF5[9:0] – 10−bit switch OFF threshold.

TR5[3:0] – Transition vector duration, it is prolonging the duration of  ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 33. REGISTER 0x06**

| Register 0x06 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x06 | Name | OFF6[11:4] | | | | | | | | TR6[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x06 | Name | ON6[23:14] | | | | | | | | | | OFF6[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

<u>ON6[9:0]</u> – 10−bit switch ON threshold.

<u>OFF6[9:0]</u> – 10−bit switch OFF threshold.

<u>TR6[3:0]</u> – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 34. REGISTER 0x07**

| Register 0x07 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x07 | Name | OFF7[11:4] | | | | | | | | TR7[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x07 | Name | ON7[23:14] | | | | | | | | | | OFF7[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

<u>ON7[9:0]</u> – 10−bit switch ON threshold.

<u>OFF7[9:0]</u> – 10−bit switch OFF threshold.

<u>TR7[3:0]</u> – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 35. REGISTER 0x08**

| Register 0x08 | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x08 | Name | OFF8[11:4] | | | | | | | | TR8[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x08 | Name | ON8[23:14] | | | | | | | | | | OFF8[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

<u>ON8[9:0]</u> – 10−bit switch ON threshold.

<u>OFF8[9:0]</u> – 10−bit switch OFF threshold.

<u>TR8[3:0]</u> – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 36. REGISTER 0x09**

| Register 0x09 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x09 | Name | OFF9[11:4] | | | | | | | | TR9[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x09 | Name | ON9[23:14] | | | | | | | | | | OFF9[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON9[9:0] – 10−bit switch ON threshold.

OFF9[9:0] – 10−bit switch OFF threshold.

TR9[3:0] – Transition vector duration, it is prolonging the duration of  ON resp. OFF value at the end of PWM period by $<TRx[3:0]> \times$ Time slot between switch activations.

**Table 37. REGISTER 0x0A**

| Register 0x0A | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0A | Name | OFF10[11:4] | | | | | | | | TR10[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x0A | Name | ON10[23:14] | | | | | | | | | | OFF10[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON10[9:0] – 10−bit switch ON threshold.

OFF10[9:0] – 10−bit switch OFF threshold.

TR10[3:0] – Transition vector duration, it is prolonging the duration of  ON resp. OFF value at the end of PWM period by $<TRx[3:0]> \times$ Time slot between switch activations.

**Table 38. REGISTER 0x0B**

| Register 0x0B | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0B | Name | OFF11[11:4] | | | | | | | | TR11[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x0B | Name | ON11[23:14] | | | | | | | | | | OFF11[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

ON11[9:0] – 10−bit switch ON threshold.

OFF11[9:0] – 10−bit switch OFF threshold.

TR11[3:0] – Transition vector duration, it is prolonging the duration of  ON resp. OFF value at the end of PWM period by $<TRx[3:0]> \times$ Time slot between switch activations.

**Table 39. REGISTER 0x0C**

| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Register 0x0C | | | | | | | | | | | |
| 0x0C | Name | OFF12[11:4] | | | | | | | | TR12[3:0] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x0C | Name | ON12[23:14] | | | | | | | | | | OFF12[13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

<u>ON12[9:0]</u> – 10−bit switch ON threshold.

<u>OFF12[9:0]</u> – 10−bit switch OFF threshold.

<u>TR12[3:0]</u> – Transition vector duration, it is prolonging the duration of ON resp. OFF value at the end of PWM period by <TRx[3:0]> × Time slot between switch activations.

**Table 40. REGISTER 0x0D**

| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Register 0x0D | | | | | | | | | | | |
| 0x0D | Name | TW_CODE[11:8] | | | | – | – | – | – | ADC_SEL[3:2] | | CRC_CLR | MAPENA |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x0D | Name | – | – | – | – | – | – | – | – | TW_CODE[15:12] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

<u>MAPENA</u> – Register bank map enable request. When MAPENA request is written '1' the internal mapena register bit is set. It remains set until PWM counter overflows. The internal mapena is cleared upon the PWM counter overflows. The <MAPENA> is always read as '0'.

<u>CRC_CLR</u> – <PXN_CRC_ERR_CNT[3:0]> clear request. When <CRC_CLR> bit is set to '1' the <PXN_CRC_ERR_CNT[3:0]> bits are cleared immediately. The <CRC_CLR> bit is always read as '0'.

<u>ADC_SEL[1:0]</u> – 2−bit ADC measurement channel selection for ADCx A/D conversion (see Table 11. ADC for measuring VBB, VDD, VLED, TEMP, ADCx). The measurement channel is selected according to the following table:

**Table 41. ADC MEASUREMENT CHANNEL SELECTION**

| ADC_SEL[1:0] | Measurement Channel |
|---|---|
| 0x0 | ADC0 |
| 0x1 | ADC1 |
| 0x2 | ADC2 |
| 0x3 | Reserved |

NOTE: The ADCx measurement result can be obtained by reading <ADCx_RES[7:0]> status bits. In case the <ADC_SEL[1:0]> bits are set to "11", the returned measured value is always "00000000".

<u>TW_CODE</u> – 8−bit thermal warning threshold. The default value is calculated as follows:

TW_CODE[7:0] = TSD_CODE[7:0] − 9

**Table 42. REGISTER 0x0E**

| Register 0x0E | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0E | Name | – | – | – | – | DIMFREQ[7:3] | | | | | CONF_SEL[2:0] | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x0E | Name | – | – | – | – | – | – | – | – | – | – | – | T1_CONF |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW | RW |

CONF_SEL[2:0] – Selects the switch configuration. NCV78343 supports the switch configurations listed in Table 16.

DIMFREQ[4:0] – Defines the DIMCLK frequency register, which shall be used to select dimming frequencies in range of 125 kHz to 1 MHz.

**Table 43. PWM FREQUENCY SETTING**

| DIMFREQ [4:0] | $f_{DIMCLK}$ [kHz] | $T_{DIMCLK}$ [μs] | $f_{PWM}$ [Hz] | $T_{PWM}$ [ms] | $T_{SW\_SEQ}$ [μs] | TR | SW SLOT | $T_{SW\_SEQ}/T_{DIMCLK}$ |
|---|---|---|---|---|---|---|---|---|
| 0 | 125.00 | 8.00 | 122.07 | 8.19 | 16 | 24 | 41 | 2 |
| 1 | 133.33 | 7.50 | 130.21 | 7.68 | 15 | 24 | 41 | 2 |
| 2 | 142.86 | 7.00 | 139.51 | 7.17 | 14 | 24 | 41 | 2 |
| 3 | 152.85 | 6.50 | 149.27 | 6.70 | 13 | 24 | 41 | 2 |
| 4 | 166.67 | 6.00 | 162.76 | 6.14 | 12 | 24 | 41 | 2 |
| 5 | 181.82 | 5.50 | 177.56 | 5.63 | 11 | 24 | 41 | 2 |
| 6 | 200.00 | 5.00 | 195.31 | 5.12 | 10 | 24 | 41 | 2 |
| 7 | 222.22 | 4.50 | 217.01 | 4.61 | 9 | 24 | 41 | 2 |
| 8 | 250.00 | 4.00 | 244.14 | 4.10 | 16 | 48 | 20 | 4 |
| 9 | 266.67 | 3.75 | 260.42 | 3.84 | 15 | 48 | 20 | 4 |
| 10 | 285.71 | 3.50 | 279.01 | 3.58 | 14 | 48 | 20 | 4 |
| 11 | 307.69 | 3.25 | 300.48 | 3.33 | 13 | 48 | 20 | 4 |
| 12 | 333.33 | 3.00 | 325.52 | 3.07 | 12 | 48 | 20 | 4 |
| 13 | 363.64 | 2.75 | 355.12 | 2.82 | 11 | 48 | 20 | 4 |
| 14 | 400.00 | 2.50 | 390.63 | 2.56 | 10 | 48 | 20 | 4 |
| 15 | 444.44 | 2.25 | 434.02 | 2.30 | 9 | 48 | 20 | 4 |
| 16 | 500.00 | 2.00 | 488.28 | 2.05 | 16 | 96 | 9 | 8 |
| 17 | 571.43 | 1.75 | 558.04 | 1.79 | 14 | 96 | 9 | 8 |
| 18 | 666.67 | 1.50 | 651.04 | 1.54 | 12 | 96 | 9 | 8 |
| 19 | 800.00 | 1.25 | 781.25 | 1.28 | 10 | 96 | 9 | 8 |
| 20 | 1000.00 | 1.00 | 976.56 | 1.02 | 16 | 192 | 4 | 16 |
| 21 .. 31 | 125.00 | 8.00 | 122.07 | 8.19 | 16 | 24 | 41 | 2 |

$T_{DIMCLK}$ – the duration of one dimming clock tick.
$T_{PWM}$ – the duration of 1024 dimming ticks.
$T_{SW\_SEQ}$ – the duration of one switch ON event.
$T_{SW\_SEQ}/T_{DIMCLK}$ – the number of clocks required for one switch ON event.
TR – the number of ticks for all transient vectors. This space should be reserved for TR when this technique is used. Calculated as $(T_{SW\_SEQ}/T_{DIMCLK})*12$.
SW SLOT – recommended distance (in ticks of dimming clock) between two switch ON events.

T1_CONF – The bit defines the switch ON time (switching slope), where the "1" means steeper slope. For better EMC results it is recommended to set this value to "0".

**Table 44. REGISTER 0x0F**

| Register 0x0F | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x0F | Name | SW6.STATUS [11:10] | | SW5.STATUS [9:8] | | SW4.STATUS [7:6] | | SW3.STATUS [5:4] | | SW2.STATUS [3:2] | | SW1.STATUS [1:0] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x0F | Name | SW12.STATUS [23:22] | | SW11.STATUS [21:20] | | SW10.STATUS [19:18] | | SW9.STATUS [17:16] | | SW1.STATUS [1:0] | | SW7.STATUS [13:12] | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |

SWx.STATUS[2] – Reflects status of internal SWx flags:
> "00" – On/Off OK
> "01" – On/Off Failed
> "10" – Open
> "11" – Short

The bit is cleared upon a successful readout over PXN (clear by read bit).

**Table 45. REGISTER 0x10**

| Register 0x10 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x10 | Name | PWM_CNT_OVF | GND_LOSS | VBB_LOW | OTP_ZAP_UV | CAP_UV | HWR | – | DIMERR | DIMWARN | GSWERR | TSD | TW |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x10 | Name | PXN_CRC_ERR_CNT[23:20] | | | | OTP_CRC_FAIL_BANK_0 | OTP_CRC_FAIL_BANK_2 | TIMEOUT | PXN_SYNC_ERR | PXN_FRAME_ERR | PXN_LOCAL_COMM_ERR | PXN_GLOBAL_COMM_ERR | MAPENA_STATUS |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |

TW – Thermal warning flag. <TW> flag is set when Tj above Thermal Warning Threshold is detected. The bit is cleared upon a successful readout over PXN.

TSD – Thermal shutdown flag. <TSD> flag is set when Tj above Thermal Shutdown Threshold is detected. When the flag is set, the device enters FAIL status mode and the switches are switched OFF.
The bit is cleared upon a successful readout over PXN.

GSWERR – Global switch error indicator. The bit is set high under the following conditions:
- at least one switch is shorted or
- at least one switch is open or
- ext. capacitor charging has failed

The bit is cleared upon a successful readout over PXN.

DIMWARN – Dimming warning indicator. The bit is set high in case of an overlapping switch OFF sequences are detected. The bit is cleared upon a successful readout over PXN (clear by read bit).

DIMERR - Dimming error indicator. The bit is set high in case an overlapping switch ON sequences are detected. When the flag is set, the device enters the FAIL status mode. The bit is cleared upon a successful readout over PXN (clear by read bit).

HWR – HWR flag is set after POR. The bit is cleared upon a successful readout over PXN (clear by read bit).

CAP_UV – Status bit indicating that charging process of external capacitor failed. When this bit is set, the <GSWERR> flag is set to '1' and the device enters the FAIL status mode and the switches are switched ON. The bit is cleared upon a successful readout over PXN (clear by read bit).

OTP_ZAP_UV – The bit is set if the battery voltage during OTP zapping is lower than 15 V. The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>VBB_LOW</u> − The bit is set if the battery voltage is lower than 4.5 V. The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>GND_LOSS</u> − The GND loss comparator detects Ground connection loss. The TST1 pin is used as reference ground. The TST1 pin is connected to ground on application PCB level (see Table 12. GND Loss Detection). The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>PWM_CNT_OVF</u> − When PWM counter overflows, flag is set to '1'. It should be used to detect that PWM control (PWM counter) is running/functional. The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>MAPENA_STATUS</u> - MAPENA request status. It corresponds to the state of internal MAPENA register bit.

<u>PXN_GLOBAL_COMM_ERR</u> − PXN global communication error. The flag is set in case of global communication error is detected and not disabled by "Global bit error detection DIS" in OTP bank (see Table 24. OTP Bank). For correct functionality it is mandatory to ensure an automatic echo from Tx to Rx. The PXN global communication error is detected under the following circumstance: REPEATER−SLAVE node, where the TX'' differs from RX''. The TX'' is monitored by PXN node in REPEATER−SLAVE mode through TX_ECHO_UART input.
The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>PXN_LOCAL_COMM_ERR</u> − PXN local communication error. The flag is set in case of local communication error detected. The PXN local communication error is detected under the following circumstance: SLAVE node, where the TX' differs from RX'. The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>PXN_FRAME_ERR</u> − PXN frame error. The flag is set whenever one of the following errors is detected:
- Parity error – the parity calculated over bits 0 .. 6 of either PID1 or PID2 is not matching the corresponding parity bit P
- CRC error – the CRC calculated over PID1, PID2 and all data bytes do not match the received CRC
- STOP BIT error – '0' received at the expected stop bit position

The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>PXN_SYNC_ERR</u> − The PXN synchronization error is detected in case the duration of eight synchronization field Tbits, when counted in 20 MHz domain is outside the following limits:

**Table 46. PXN SYNCHRONIZATION ERROR LIMITS**

| PXN Communication Speed [kb/s] | Eight_Tbits_min | Eight_Tbits_max |
|---|---|---|
| 125 | 1098 | 1484 |
| 250 | 549 | 742 |
| 500 | 274 | 371 |
| 1000 | 140 | 181 |

The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>TIMEOUT</u> − The PXN timeout error is detected in case neither MAPENA nor MAPENA_DIR is activated within a TIMEOUT period. The timeout error detection starts when the NORMAL mode is entered and either MAPENA or MAPENA_DIR is activated for the first time. When the flag is set, the device enters the FAIL status mode and LED's are switched ON/OFF following the OTP memory bits 8−11 in Table 24. OTP Bank. The reported OPMODE status is NORMAL_DIRECT mode. The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>OTP_CRC_FAIL_BANK2</u> – CRC over mirrored OTP BANK2 bit failure. The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>OTP_CRC_FAIL_BANK0</u> – CRC over mirrored OTP BANK0 bit failure. The device should not operate when this bit is set. The bit is cleared upon a successful readout over PXN (clear by read bit).

<u>PXN_CRC_ERR_CNT[3:0]</u> – 4−bit PXN frame CRC error counter. The counter is incremented each time a CRC error is detected on incoming PXN frame. Once a maximum number of errors is reached, the counter remains clamped at value of 15. The bit is cleared upon a successful write '1' to register < CRC_CLR>.

**Table 47. REGISTER 0x11**

| Register 0x11 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x11 | Name | VDD_RES[11:8] | | | | TEMP_RES[7:0] | | | | | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x11 | Name | ADCX_RES[23:16] | | | | | | | | VDD_RES[15:12] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |

TEMP_RES[7:0] – the TEMP measured value (read only bits).

VDD_RES[7:0] – the last VDD measured value (read only bits).

ADCX_RES[7:0] – the last value measured at selected ADC measurement channel (read only bits). In case the <ADC_SEL[1:0]> bits are set to "11" the returned measured value is always "00000000".

**Table 48. REGISTER 0x12**

| Register 0x12 | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Address | | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0x12 | Name | VLED_RES[11:8] | | | | VBB_RES[7:0] | | | | | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |
| Address | | Bit 23 | Bit 22 | Bit 21 | Bit 20 | Bit 19 | Bit 18 | Bit 17 | Bit 16 | Bit 15 | Bit 14 | Bit 13 | Bit 12 |
| 0x12 | Name | TSD_CODE[23:16] | | | | | | | | VLED_RES[15:12] | | | |
| | Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | Access | R | R | R | R | R | R | R | R | R | R | R | R |

VBB_RES[7:0] – the last VBB measured value (read only bits).

VLED_RES[7:0] – the last VLED measured value (read only bits). Because of the internal ESD structure, the minimum measured VLED voltage is VDD minus forward diode voltage Vf.

TSD_CODE[7:0] – thermal shutdown threshold (read only bits).

# CONFIGURATION FRAMES

**Table 49. CF0 – SLAVE IDENTIFICATION**

| Byte | Name | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x00 | | | | |
| 2 | DATA1 | DEV_ID[7:0] | | | | | | | |
| 3 | DATA2 | ANA_ID[7:0] | | | | | | | |
| 4 | DATA3 | DIG_ID[7:0] | | | | | | | |
| 5 | DATA4 | 0 | 0 | 0 | DLT_W[4:0] | | | | |
| 6 | DATA5 | DLT_X_AXS[7:0] | | | | | | | |
| 7 | DATA6 | DLT_Y_AXS[7:0] | | | | | | | |
| 8 | CRC | CRC[7:0] | | | | | | | |

DATA1

DEV_ID[7:0]             device ID, L343 = 1


DATA2

ANA_ID[7:0]             analog version ID, 35


DATA3

DIG_ID[7:0]             digital version ID, 1


DATA4

DLT_W[4:0]


DATA5

DLT_X_AXS[7:0]


DATA6

DLT_Y_AXS[7:0]


The DLT_W, DLT_X_AXS and DLT_Y_AXS parameters describe the wafer specifications.

**Table 50. CF1 − EEPROM WRITE DATA**

| Byte | Name | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x01 | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | EESA[2:0] | | |
| 3 | DATA2 | EEBA[7:0] | | | | | | | |
| 4 | DATA3 | BYTE0 @(EEBA+0)[7:0] | | | | | | | |
| 5 | DATA4 | BYTE1 @(EEBA+1)[7:0] | | | | | | | |
| 6 | DATA5 | BYTE2 @(EEBA+2)[7:0] | | | | | | | |
| 7 | DATA6 | BYTE3 @(EEBA+3)[7:0] | | | | | | | |
| 8 | DATA7 | BYTE4 @(EEBA+4)[7:0] | | | | | | | |
| 9 | DATA8 | BYTE5 @(EEBA+5)[7:0] | | | | | | | |
| 10 | DATA9 | BYTE6 @(EEBA+6)[7:0] | | | | | | | |
| 11 | DATA10 | BYTE7 @(EEBA+7)[7:0] | | | | | | | |
| 12 | CRC | CRC[7:0] | | | | | | | |

DATA1

B                      broadcast bit:

1 − broadcast frame
0 − addressed frame

EESA[2:0]              EEPROM slave address

DATA2

EEBA[7:0]              EEPROM byte address

DATA3 − DATA10

BYTEx[7:0]             bytes to be written

**Table 51. CF2 − EEPROM REQUEST DATA**

| Byte | Name | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x02 | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | EESA[2:0] | | |
| 3 | DATA2 | EEBA[7:0] | | | | | | | |
| 4 | CRC | CRC[7:0] | | | | | | | |

DATA1

B                      broadcast bit:

1 − broadcast frame
0 − addressed frame

EESA[2:0]              EEPROM slave address

DATA2

EEBA[7:0]              EEPROM byte address

**Table 52. CF3 − EEPROM READ DATA**

| Byte | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | | | **Contents** | | | | |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x03 | | | | |
| 2 | DATA1 | WP | EES[1:0] | | 0 | 0 | EESA[2:0] | | |
| 3 | DATA2 | EEBA[7:0] | | | | | | | |
| 4 | DATA3 | BYTE0 @(EEBA+0)[7:0] | | | | | | | |
| 5 | DATA4 | BYTE1 @(EEBA+1)[7:0] | | | | | | | |
| 6 | DATA5 | BYTE2 @(EEBA+2)[7:0] | | | | | | | |
| 7 | DATA6 | BYTE3 @(EEBA+3)[7:0] | | | | | | | |
| 8 | DATA7 | BYTE4 @(EEBA+4)[7:0] | | | | | | | |
| 9 | DATA8 | BYTE5 @(EEBA+5)[7:0] | | | | | | | |
| 10 | DATA9 | BYTE6 @(EEBA+6)[7:0] | | | | | | | |
| 11 | DATA10 | BYTE7 @(EEBA+7)[7:0] | | | | | | | |
| 12 | CRC | CRC[7:0] | | | | | | | |

DATA1

EESA[2:0]                    EEPROM slave address

EES[1:0]                     EEPROM status:
                             0x0 − EEPROM busy, access denied
                             0x1 − EEPROM busy, data transfer ongoing
                             0x2 − EEPROM ready, data transfer completed
                             0x3 − EEPROM ready, data transfer failed

WP                           EEPROM write protect status

DATA2

EEBA[7:0]                    EEPROM byte address

DATA3 − DATA10
BYTEx[7:0]                   read bytes

**Table 53. CF4 − ENABLE/DISABLE AUTO−ADDRESSING MODE**

| Byte | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | | | **Contents** | | | | |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x04 | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | 0 | 0 | AAC |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1

B                           broadcast bit:     1 − broadcast frame
                                               0 − addressed frame

AAC                         auto−addressing control bit:   1 − enable
                                                           0 − disable

The CF4 frame is accepted in the OTP_CONFIG mode only.

**Table 54. CF5 − ASSIGN ADDRESS**

| Byte | Name | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x05 | | | | |
| 2 | DATA1 | B | 0 | 0 | AA_ADR[4:0] | | | | |
| 3 | DATA2 | AA_THR[7:0] | | | | | | | |
| 4 | CRC | CRC[7:0] | | | | | | | |

DATA1
B                         broadcast bit:
                          1 − broadcast frame
                          0 − addressed frame


AA_ADR[4:0]               5−bit address to assign


DATA2
AA_THR[7:0]               8−bit auto−address threshold value


The CF5 frame is accepted in AUTO_ADDR mode only.


**Table 55. CF6 − OP MODE STATUS**

| Byte | Name | Contents | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x06 | | | | |
| 2 | DATA1 | PXN_FRAME_CNT[3:0] | | | | OPMODE[3:0] | | | |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1
PXN_FRAME_CNT[4:0]        PXN frame counter − 4−bit counter which is incremented each time any valid PXN frame
                         is processed. The counter overflows to 0 upon the increment.


OPMODE[3:0]              OP mode status:
                        0x0 − not valid            0x7 − normal fail−safe open mode
                        0x1 − OTP config mode      0xC − NO_CRC direct mode
                        0x2 − auto−addressing mode 0xD − NO_CRC pwm mode
                        0x4 − normal direct mode   0xE − fail safe OTP mode
                        0x5 − normal pwm mode      0xF − fail safe OPEN mode
                        0x6 − normal fail−safe otp mode

**Table 56. CF7 – SLAVE/REPEATER−SLAVE PXN MODE SELECTION**

| Byte | Name | Contents | | | | | | | |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x07 | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | 0 | 0 | PMC |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1

B　　　　　　　　　　　broadcast bit:
　　　　　　　　　　　　1 − broadcast frame
　　　　　　　　　　　　0 − addressed frame

PMC　　　　　　　　　　PXN mode control bit:
　　　　　　　　　　　　1 − repeater−slave mode
　　　　　　　　　　　　0 − slave mode

Overwrites device mode loaded from the OTP memory.

**Table 57. CF8 – READ PXN MODE STATUS**

| Byte | Name | Contents | | | | | | | |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x08 | | | | |
| 2 | DATA1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | PMS |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1

PMS　　　　　　　　　　PXN mode status bit:
　　　　　　　　　　　　1 − repeater−slave mode
　　　　　　　　　　　　0 − slave mode

**Table 58. CF9 − WRITE DATA TO OTP**

| Byte | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | **Contents** | | | | | | | |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x09 | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | 0 | OTPBS[1:0] | |
| 3 | DATA2 | BYTE0 @(OTPBA+0) | | | | | | | |
| 4 | DATA3 | BYTE1 @(OTPBA+1) | | | | | | | |
| 5 | DATA4 | BYTE2 @(OTPBA+2) | | | | | | | |
| 6 | DATA5 | BYTE3 @(OTPBA+3) | | | | | | | |
| 7 | DATA6 | 0x00 | | | | | | | |
| 8 | DATA7 | CRC[7:0] | | | | | | | |

DATA1

B            broadcast bit:
                        1 − broadcast frame
                        0 − addressed frame

OTPBS[1:0]            2−bit OTP bank selection
                        0x2 − custom OTP bank
                        0x0, 0x1, 0x3 − no bank selected

DATA2 − DATA6

BYTEx[7:0]            bytes to be written

The CF9 frame is accepted in OTP_CONFIG mode only.

**Table 59. CF10 − REQUEST DATA FROM OTP**

| Byte | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | **Contents** | | | | | | | |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x0A | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | 0 | OTPBS[1:0] | |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1

B            broadcast bit:
                        1 − broadcast frame
                        0 − addressed frame

OTPBS[1:0]            2−bit OTP bank selection:
                        0x2 − custom OTP bank
                        0x0, 0x1, 0x3 − no bank selected

**Table 60. CF11 – READ DATA FROM OTP**

| Byte | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
|      |      | **Contents** | | | | | | | |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x0B | | | | |
| 2 | DATA1 | LOCKB | OTPS[1:0] | | 0 | 0 | OTPBS[2:0] | | |
| 3 | DATA2 | BYTE0 @(OTPBA+0) | | | | | | | |
| 4 | DATA3 | BYTE1 @(OTPBA+1) | | | | | | | |
| 5 | DATA4 | BYTE2 @(OTPBA+2) | | | | | | | |
| 6 | DATA5 | BYTE3 @(OTPBA+3) | | | | | | | |
| 7 | DATA6 | BYTE4 @(OTPBA+4) | | | | | | | |
| 8 | CRC | CRC | | | | | | | |

DATA1

LOCKB
custom OTP bank general lock status bit:

1 − locked
0 − unlocked, further OTP programming possible

OTPS[1:0]
2−bit OTP status:

0x0 – idle, no data transfer ongoing
0x1 – busy, data transfer ongoing
0x2 – ready, data transfer OK
0x3 – ready, data transfer failed

OTPBS[1:0]
2−bit OTP bank selection:

0x2 – custom OTP bank
0x0 or
0x1 or
0x3 – no bank selected

DATA2 − DATA6

BYTEx[7:0]
read bytes

**Table 61. CF12 – COMMUNICATION SPEED**

| Byte | Name | Contents | | | | | | | |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x0C | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | 0 | CSPEED[1:0] | |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1

B                                    broadcast bit:

1 – broadcast frame
0 – addressed frame

CSPEED[1:0]                          communication speed:

0x0 – 125 kbps
0x1 – 250 kbps (default)
0x2 – 500 kbps
0x3 – 1000 kbps

Overwrites device communication speed loaded from the OTP memory.


**Table 62. CF13 – SWITCH TO NORMAL MODE**

| Byte | Name | Contents | | | | | | | |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x0D | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | 0 | 0 | NMD |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1

B                                    broadcast bit:

1 – broadcast frame
0 – addressed frame

NMD                                  request to enter NORMAL mode from OTP_CONFIG mode:

1 – go to NO_CRC or normal mode; according to the OTP bank 2 lock bit
0 – no effect

The CF13 frame is accepted in OTP_CONFIG mode only.

**Table 63. CF14 − RESET SYSTEM**

| Byte | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | \<Contents\> | | | | | | | |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x0E | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | 0 | 0 | 0 | SWRST |
| 3 | CRC | CRC | | | | | | | |

DATA1

B                          broadcast bit:
                           1 − broadcast frame
                           0 − addressed frame

SWRST                      software reset bit:
                           1 − perform software reset
                           0 − no effect

The CF14 frame is accepted in NORMAL mode only.


**Table 64. CF15 − TRIGGER MAPENA**

| Byte | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|------|------|-------|-------|-------|-------|-------|-------|-------|-------|
| | | \<Contents\> | | | | | | | |
| 0 | PID1 | P | 1 | 1 | SA[4:0] | | | | |
| 1 | PID2 | P | 0 | 0 | CSID[4:0] = 0x0F | | | | |
| 2 | DATA1 | B | 0 | 0 | 0 | WDT_SEL[1:0] | | 0 | MAPENA |
| 3 | CRC | CRC[7:0] | | | | | | | |

DATA1

B                          broadcast bit:
                           1 − broadcast frame
                           0 − addressed frame

MAPENA                     trigger MAPENA
                           1 − perform MAPENA
                           0 − no effect

WDT_SEL[1:0]               watchdog timeout selector; valid only with <MAPENA> = '1'
                           0x0 − 250 ms
                           0x1 − 150 ms
                           0x2 − 100 ms
                           0x3 − 60 ms

The NCV78343 offers a wide range of device−integrated diagnostic features. Their description follows.

### Thermal Warning and Shutdown

The junction temperature can be calculated from ADC code as follows:

$$T_j = \frac{ADC_{CODE} + 184}{TSD_{CODE} + 184} \cdot \left(TSD_{TEMPERATURE} + 273\right) - 273 \quad \text{(eq. 2)}$$

The <TSD_CODE> is trimmed in production to 170°C (TSD$_{TEMPERATURE}$). Typical value of <TSD_CODE> is 186 and exact trimmed value can be read from Register 0x12. The <TW> status bit is set high in case the measurement result is greater than or equal to TW_CODE[7:0] value. The <TSD> status bit is set high in case the measurement result is greater than or equal to TSD_CODE[7:0].

The TW and TSD status bits are cleared in case the <TEMP_RES> register value is smaller than both TSD_CODE and TW_CODE values and TW and TSD status bits are successfully read out over PXN.

### Overlapping switch ON/OFF events

Overlapping switch ON events is forbidden, the NCV78343 needs time slot between two switch ON events (see Table 43). Superior system has to ensure that overlapping switch ON events do not appear in patterns.

When overlapping switch ON events are despite this invoked, the NCV78343 incorporates protective feature, in which the <DIMERR> error is raised.

When overlapping switch OFF events occur, the <DIMWARN> status bit is set and processing of this pattern continues. However, it has to be taken into account, that overlapping switch OFF events can lead to large fluctuations of LED string voltage.

### Pixel Switches diagnostic

Embedded diagnostic covers a wide range of possible failure situations on switches. Each switch contains two comparators – short comparator and over voltage comparator. With the help of these two comparators a several fail situations can be detected and distinguished on each switch individually.

Overall status of switches errors are indicated by the Global Switch Error <GSWERR> status flag. Status of individual switches (whether a switch is ON or OFF) can be read in the Switch Status <SWx.STATUS> flag. The failure state of the individual switches (Short, Open) is indicated by corresponding status in <SW.STATUS[2:0]> register.

When the device operates in the PWM mode and a short is present, the device reports alternating On/Off Failed and SHORT status according to set ON/OFF dimming duration (see details in Figure 13).

### Dedicated OPEN clear request

When the OPEN state or overvoltage is detected, the switch is automatically closed and the status is shown in the SWx.STATUS register 0x0F. Further attempts to control this switch using PWM or DIRECT mode don't have any effect. The switch is released upon a successful OPEN clear request frame.

In direct mode, the released switch is updated upon a successful write to register 0x00 with service "00". In PWM mode, the released switch is updated according to the ON/OFF values.

### PWM_CNT_OVF

When PWM Counter overflows, <PWM_CNT_OVF> flag is set to '1'. It is clear by read flag. It should be used to detect that PWM control (PWM counter) is running/functional.

### CAP_UV

The <CAP_UV> status bit indicates that charging process of external capacitor failed. When this bit is set, the <GSWERR> flag is set to '1' and all switches are switched OFF. It is clear by read flag and the switches are set according to last successful write to the register 0x00.

### VBB_LOW

The <VBB_LOW> status bit indicates low battery voltage < 4.5 V (see Table 4). The bit is not detected when the battery voltage level is lower than 4.5 V during the start−up sequence.

### Power−on Reset

After a power−on a flag <HWR> in the register is set.

# APPLICATION RELATED INFORMATION

**PXN CRC Code Example**

```c
// Byte reverse
uint8_t l343_byte_reverse(uint8_t  b)
{
   b = (b & 0xF0) >> 4 | (b & 0x0F) << 4;
   b = (b & 0xCC) >> 2 | (b & 0x33) << 2;
   b = (b & 0xAA) >> 1 | (b & 0x55) << 1;
   return b;
}

// Calculate the PXN CRC
uint8_t l343_pxn_crc(uint8_t *data_bits, uint8_t length)
{
    uint8_t CRC8 = 0;

    for (uint8_t a=0; a<length; ++a)
    {
        CRC8 = CRC8 ^ data_bits[a];

        for (uint8_t i=0; i<8; ++i)
        {
            if (CRC8 & 0x80)
            {
                CRC8 = ((0x7F & CRC8) * 2) ^ 0x07;
            }
            else
            {
                CRC8 = CRC8 * 2;
            }
        }
    }

    return CRC8;
}

Function call example:
int main(void)
{
    // MAPENA as broadcast; SEED, PID1, PID2, DATA0; CRC = 0x28
    uint8_t data_bits[] = {0xFF, 0x61, 0x8F, 0x81};

    // Write to REG00; SEED, PID1, PID2, DATA0, DATA1, DATA2; CRC = 0x14
    // uint8_t data_bits[] = {0xFF, 0xA1, 0x80, 0x55, 0x05, 0x00};

    // Get the number of bytes
    int length = sizeof(data_bits)/sizeof(data_bits[0]);

    // Invert the input
    for (uint8_t a = 0; a<length; ++a) data_bits[a] = l343_byte_reverse(data_bits[a]);

    // Get the result
    uint8_t result = l343_pxn_crc(data_bits, length);
}
```

**Parity Bit Calculation**

```c
uint8_t l343_parity(uint8_t val)
{
    bool Par;

    Par = ((val>>0)&1) ^ ((val>>1)&1) ^ ((val>>2)&1) ^ ((val>>3)&1) ^ ((val>>4)&1) ^
    ((val>>5)&1) ^ ((val>>6)&1);
    Par = (Par ^ 1) & 1;

    return (uint8_t)Par;
}
```

**Go to NMD Frame (CF13)**

```c
int32_t l343_normal_mode(uint8_t addr)
{
    uint8_t p;
    uint8_t pdata[5];

    // SYNC
    pdata[0] = 0x55;

    // PID1
    uint8_t PID1 = 0;
    PID1 = 3<<5 | addr;
    p = l343_parity(PID1);
    pdata[1] = (p << 7) | PID1;

    // PID2
    uint8_t PID2 = 0;
    PID2 = 0x0D;
    p = l343_parity(PID2);
    pdata[2] = (p << 7) | PID2;

    // DATA bytes
    pdata[3] = 1;          // NMD


    uint8_t pdata_crc[4];

    // Invert the input
    for (uint8_t a = 0; a<4; ++a) pdata_crc[a] = l343_byte_reverse(pdata[a]);

    // Calculate the CRC
    pdata_crc[0] = 0xFF;
    uint8_t crc = l343_pxn_crc(pdata_crc, 4);

    pdata[4] = crc;

    // Send data
    return serial_pxn_set_data(pdata, 5);
}
```

**OTP Write Code Example**

```c
typedef struct OTP_t
{
        unsigned lb: 1;         // Lock bit
        unsigned na_lb: 1;      // Node Address Lock bit
        unsigned na: 5;         // Note Address
        unsigned fss_lb: 1;     // Fail Safe State Lock bit
        unsigned fss: 4;        // Fail Safe State of LEDs
        unsigned pxn_lb: 1;     // PXN Lock bit
        unsigned mode: 1;       // Mode
        unsigned cs: 2;         // Communication speed
        unsigned gbed: 1;       // Global bit error detection
        unsigned m_lvds_off: 1; // M-LVDS off
        unsigned uart_off: 1;   // UART off
        unsigned ee_lb: 1;      // EEPROM lock bit
        unsigned crc: 7;        // CRC
} OTP_t;

// Calculate the OTP CRC
uint8_t l343_otp_crc(uint8_t *data_bits, char length)
{
        uint8_t CRC7 = 0;

        for (uint8_t a = 0; a<length; ++a)
        {
                CRC7 = CRC7 ^ data_bits[a];

                for (uint8_t i = 0; i < 8; ++i)
                {
                        if (CRC7 & 0x80)
                        {
                                CRC7 = ((0x7F & CRC7) * 2) ^ (0x37 * 2);
                        }
                        else
                        {
                                CRC7 = (CRC7 * 2);
                        }
                }
        }

        return (CRC7 / 2);
}

int32_t l343_otp_zapping(OTP_t otp)
{
        uint8_t data_bits[4];
        data_bits[0] = 0x07;
        data_bits[1] = 0x0F<<4 | otp.ee_lb<<3 | otp.uart_off<<2 | otp.m_lvds_off<<1 | otp.gbed<<0;
        data_bits[2] = otp.cs<<6 | otp.mode<<5 | otp.pxn_lb<<4 | otp.fss<<0;
        data_bits[3] = otp.fss_lb<<7 | otp.na<<2 | otp.na_lb<<1 | otp.lb<<0;

        // Get the number of bytes
        int length = sizeof(data_bits)/sizeof(data_bits[0]);

        // Get the result
        otp.crc = l343_otp_crc(data_bits, length);

        // PXN OTP write frame
```

```
            uint8_t p;
            uint8_t pdata[10];

            // SYNC
            pdata[0] = 0x55;

            // PID1
            uint8_t PID1 = 0;
            PID1 = 3<<5 | otp.na;
            p = l343_parity(PID1);
            pdata[1] = (p << 7) | PID1;

            // PID2
            uint8_t PID2 = 0;
            PID2 = 0x09;
            p = l343_parity(PID2);
            pdata[2] = (p << 7) | PID2;


            // DATA bytes
            const uint32_t data = otp.lb |
                                  otp.na_lb << 1 |
                                  otp.na << 2 |
                                  otp.fss_lb << 7 |
                                  otp.fss << 8 |
                                  otp.pxn_lb << 12 |
                                  otp.mode << 13 |
                                  otp.cs << 14 |
                                  otp.gbed << 16 |
                                  otp.m_lvds_off << 17 |
                                  otp.uart_off << 18 |
                                  otp.ee_lb << 19 |
                                  otp.crc << 20;

            pdata[3] = 0x02;
            pdata[4] = ((data >> 0 ) & 0xFF);
            pdata[5] = ((data >> 8 ) & 0xFF);
            pdata[6] = ((data >> 16) & 0xFF);
            pdata[7] = ((data >> 24) & 0xFF);
            pdata[8] = 0x00;


            uint8_t pdata_crc[9];

            // Invert the input
            for (uint8_t a = 0; a<9; ++a) pdata_crc[a] = l343_byte_reverse(pdata[a]);

            // Calculate the CRC
            pdata_crc[0] = 0xFF;
            uint8_t crc = l343_pxn_crc(pdata_crc, 9);

            pdata[9] = crc;

            // Send data
            return serial_pxn_set_data(pdata, 10);
}
```

```
Function call example:
int main(void)
{
    // Zap the OTP
    //              lb    nalb   na    fss_lb fss   pxn_lb  mode  CS    GBED  lOff  uOff  eeLb  crc
    OTP_t otp = {0x01, 0x01, 0x01, 0x01, 0x0F, 0x01,  0x00, 0x01, 0x00, 0x00, 0x01, 0x00, 0x00};
    l343_otp_zapping(otp);
}
```

**Auto−addressing (AA) Process**

This example is valid for two devices, where the first one is in repeater−slave mode and the second one is in slave mode. The first device is connected to the MCU via UART and the second device is connected to the first device via M−LVDS.

The slave address (SA) for the first device will be set to '1' and the SA for the second device will be set to '7'.

The AA process combines benefits of current source and connected LED string. The application does not need any additional wires. When the device is connected to the LED string and the current source for this LED string is enabled, the voltage drop across the LED string will occur. The LED string voltage VLED is measured by the device. Thus the address may be assigned to specific device.

In general, the MCU sends a broadcast frame CF4 (see Table 53) to all node devices and the second broadcast frame CF5 (see Table 54) with the VLED threshold and new device address as parameters. Doing this, all devices on the node will be in AA mode and only the device with VLED higher than set threshold will assign new address.

For this example, the LED string voltage is 33 V (127 ADC code). The auto−addressing threshold will be set to 80.

1. Disable all buck outputs, thus the LEDs are not shining.
2. Enable buck output 1, so the LED string for the device 1 is shining.
3. Enable AA mode by sending CF4 as broadcast (B=1; AAC=1); see Table 53.
4. Assign the address for the device 1 by sending CF5 as broadcast (B=1; ADR=1; THR=80); see Table 54.
5. Disable buck output 1, so the LED string for the device 1 is not shining.
6. Disable the AA mode for the first device SA=1 by sending CF4 (B=0; AAC=0); see Table 53.
7. Force the normal mode for the first device SA=1 by sending CF13 (NMD=1); see Table 62.
8. Set the first device as repeater−slave SA=1 by sending CF7 (PMC=1); see Table 56.
9. Enable buck output 2, so the LED string for the device 2 is shining.
10. Enable AA mode by sending CF4 as broadcast (B=1; AAC=1); see Table 53.
11. Assign the address for the device 2 by sending CF5 as broadcast (B=1; ADR=7; THR=80); see Table 54.
12. Disable buck output 2, so the LED string for the device 2 is not shining.
13. Disable the AA mode for the second device SA=7 by sending CF4 (B=0; AAC=0); see Table 53.
14. Force the normal mode for the second device SA=7 by sending CF13 (NMD=1); see Table 62.

For multiple devices connected to the first one via M−LVDS, please repeat steps 9−14 with different ADR, THR, SA values.

**Dimming Control Patterns**

The simplest way to set ON, OFF and TR values is to keep the ON time at fixed value and calculate the OFF value according to the required duty. The following table (see Table 65) shows an example of fixed ON values. It is calculated for each switch 0−11 and for each DIMFREQ value 0−20.

The values are calculated as follows:

$$\text{TR\_SLOT} = 12 \times \text{T\_SW\_ON\_SEQ} \qquad \text{(eq. 3)}$$

$$\text{SW\_SLOT} = \frac{\dfrac{1024 - \text{TR\_SLOT}}{\text{T\_SW\_ON\_SEQ}}}{12} \qquad \text{(eq. 4)}$$

$$\text{ON\_VALUE} = \text{TR\_SLOT} + \text{SWITCH} \times \text{SW\_SLOT} \times \times \text{T\_SW\_ON\_SEQ} \qquad \text{(eq. 5)}$$

where

SWITCH goes from 0 to 11

T_SW_ON_SEQ is number of ticks required for one switch ON sequence

**Table 65. DIMMING CONTROL PATTERN ON VALUES**

| DIMFREQ | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| T_SW_ON_SEQ | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 8 | 8 | 8 | 8 | 16 |
| TR_SLOT | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 96 | 96 | 96 | 96 | 192 |
| SW_SLOT | 41 | 41 | 41 | 41 | 41 | 41 | 41 | 41 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 20 | 9 | 9 | 9 | 9 | 4 |
| SWITCH | ON values | | | | | | | | | | | | | | | | | | | | |
| 0 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 24 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 48 | 96 | 96 | 96 | 96 | 192 |
| 1 | 106 | 106 | 106 | 106 | 106 | 106 | 106 | 106 | 128 | 128 | 128 | 128 | 128 | 128 | 128 | 128 | 168 | 168 | 168 | 168 | 256 |
| 2 | 188 | 188 | 188 | 188 | 188 | 188 | 188 | 188 | 208 | 208 | 208 | 208 | 208 | 208 | 208 | 208 | 240 | 240 | 240 | 240 | 320 |
| 3 | 270 | 270 | 270 | 270 | 270 | 270 | 270 | 270 | 288 | 288 | 288 | 288 | 288 | 288 | 288 | 288 | 312 | 312 | 312 | 312 | 384 |
| 4 | 352 | 352 | 352 | 352 | 352 | 352 | 352 | 352 | 368 | 368 | 368 | 368 | 368 | 368 | 368 | 368 | 384 | 384 | 384 | 384 | 448 |
| 5 | 434 | 434 | 434 | 434 | 434 | 434 | 434 | 434 | 448 | 448 | 448 | 448 | 448 | 448 | 448 | 448 | 456 | 456 | 456 | 456 | 512 |
| 6 | 516 | 516 | 516 | 516 | 516 | 516 | 516 | 516 | 528 | 528 | 528 | 528 | 528 | 528 | 528 | 528 | 528 | 528 | 528 | 528 | 576 |
| 7 | 598 | 598 | 598 | 598 | 598 | 598 | 598 | 598 | 608 | 608 | 608 | 608 | 608 | 608 | 608 | 608 | 600 | 600 | 600 | 600 | 640 |
| 8 | 680 | 680 | 680 | 680 | 680 | 680 | 680 | 680 | 688 | 688 | 688 | 688 | 688 | 688 | 688 | 688 | 672 | 672 | 672 | 672 | 704 |
| 9 | 762 | 762 | 762 | 762 | 762 | 762 | 762 | 762 | 768 | 768 | 768 | 768 | 768 | 768 | 768 | 768 | 744 | 744 | 744 | 744 | 768 |
| 10 | 844 | 844 | 844 | 844 | 844 | 844 | 844 | 844 | 848 | 848 | 848 | 848 | 848 | 848 | 848 | 848 | 816 | 816 | 816 | 816 | 832 |
| 11 | 926 | 926 | 926 | 926 | 926 | 926 | 926 | 926 | 928 | 928 | 928 | 928 | 928 | 928 | 928 | 928 | 888 | 888 | 888 | 888 | 896 |

## Dimming Algorithm Code

```c
// Variables for dimming algorithm
static const uint8_t TR_SLOT[] = {24, 24, 24, 24, 24, 24, 24, 24, 48, 48, 48, 48, 48, 48, 48, 48, 96, 96, 96, 96, 192};
static const uint8_t SW_SLOT[] = {41, 41, 41, 41, 41, 41, 41, 41, 20, 20, 20, 20, 20, 20, 20, 20, 9, 9, 9, 9, 4};
static const uint8_t T_SW_SEQ_RATIO[] = {2, 2, 2, 2, 2, 2, 2, 2, 4, 4, 4, 4, 4, 4, 4, 4, 8, 8, 8, 8, 16};


bool l343_dimming(uint8_t dimfreq, uint16_t *DCs, uint16_t *onRet, uint16_t *offRet, uint16_t *trRet)
{
        const uint8_t LEDcount = 12;


        for (uint8_t i = 0; i<LEDcount; ++i)
        {
            if (DCs[i] > 1023) DCs[i] = 1023;


            // Input is brightness of LEDs, but the ON/OFF values are for switches, thus inverted
            DCs[i] = 1023 - DCs[i];
            trRet[i] = i;                        // set TR 0..11


            if (DCs[i] == 1023)                  // Fully ON 100% DUTY cycle, thus set dedicated values 0 and 1023
            {
                onRet[i] = 0;
                offRet[i] = 1023;
            }
            else
            {
                onRet[i] = TR_SLOT[dimfreq] + i*SW_SLOT[dimfreq]*T_SW_SEQ_RATIO[dimfreq];

                if (DCs[i] == 0)                 // Fully OFF 0% DUTY cycle, where OFF is equal to ON value
                {
                    offRet[i] = onRet[i];
                }
                else
                {
                    offRet[i] = (onRet[i] + DCs[i]) % 1024;
                }
            }

            DCs[i] = 1023 - DCs[i];       // Invert back to keep the values as they were
        }

        return true;
}



// Number of devices in a cluster
#define DEVICES  X                   // [1; 31]


#define REGISTERS  12                // number of registers to be written

```

```
// LED brightness; the length should be DEVICES*REGISTERS; or two-dimensional array might be used
uint16_t DC[DEVICES*REGISTERS];          // values are in a range of [0; 1023]
// uint16_t DC[DEVICES][REGISTERS];

// Drimfreq for each device
uint8_t dimfreq[DEVICES]

// Function call example:
// Send ON, OFF, TR values to all devices
void l343_send(uint16_t *DC)
{
        for (uint8_t dev = 0; dev<DEVICES; ++dev)
        {
            uint16_t ON[REGISTERS];
            uint16_t OFF[REGISTERS];
            uint16_t TR[REGISTERS];

            // Calculate the dimming values
            l343_dimming(dimfreq[dev], DC+REGISTERS*dev, ON, OFF, TR);
//          l343_dimming(dimfreq[dev], DC[dev], ON, OFF, TR);          // when two-dimensional array is used

            // Fill the registers values
            uint32_t reg[REGISTERS];

            for (uint8_t r = 0; r<REGISTERS; ++r)
            {
                reg[r] = (ON[r]<<14) | (OFF[r]<<4) | (TR[r]&0xF);
            }

            // 36 bytes need to be sent in 3 frames
            uint8_t RBA[3] = {1, 5, 9};

            for (uint8_t r = 0; r<3; ++r)
            {
                uint8_t p;
                uint8_t pdata[16];

                // SYNC
                pdata[0] = 0x55;

                // PID1
                uint8_t PID1 = 0;
                PID1 = 1<<5 | SA[dev];
                p = l343_parity(PID1);
                pdata[1] = p<<7 | 1<<5 | PID1;

                // PID2
                uint8_t PID2 = 0;
                PID2 = 3<<5 | (RBA[r]);
                p = l343_parity(PID2);
```

```
                    pdata[2] = p<<7 | PID2;


            // DATA bytes
            pdata[3] = reg[r*4+0]&0xFF;
            pdata[4] = (reg[r*4+0]>>8)&0xFF;
            pdata[5] = (reg[r*4+0]>>16)&0xFF;


            pdata[6] = reg[r*4+1]&0xFF;
            pdata[7] = (reg[r*4+1]>>8)&0xFF;
            pdata[8] = (reg[r*4+1]>>16)&0xFF;


            pdata[9] = reg[r*4+2]&0xFF;
            pdata[10] = (reg[r*4+2]>>8)&0xFF;
            pdata[11] = (reg[r*4+2]>>16)&0xFF;


            pdata[12] = reg[r*4+3]&0xFF;
            pdata[13] = (reg[r*4+3]>>8)&0xFF;
            pdata[14] = (reg[r*4+3]>>16)&0xFF;


            uint8_t pdata_crc[16];


            // Invert the input
            for (unsigned char a = 0; a<15; ++a) pdata_crc[a] = l343_byte_reverse(pdata[a]);


            // Calculate the CRC
            pdata_crc[0] = 0xFF;
            char crc = l343_pxn_crc(pdata_crc, 15);


            pdata[15] = crc;


            // Send data
            serial_pxn_set_data(2, pdata, 16, 11);
        }

    }

}
```

## OTP Read Data Interpretation

The table below shows an example of OTP read data and its interpretation in the OTP table (see Table 24).

| DATA1 | xC2 | 11000010 | OTPBS[2:0]=x02 | OTPS[1:0]=x02 | LOCKB=x01 |
|---|---|---|---|---|---|
| DATA2 | x87 | 10000111 | | | |
| DATA3 | x70 | 01110000 | | | |
| DATA4 | x30 | 00110000 | | | |
| DATA5 | x3D | 00111101 | | | |
| DATA6 | x00 | 00000000 | | | |

| 0 | 1 | 6 | 5 | 4 | 3 | 2 | 7 | 11 | 10 | 9 | 8 | 12 | 13 | 15 | 14 | 16 | 17 | 18 | 19 | 26 | 25 | 24 | 23 | 22 | 21 | 20 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| lb | Addr lb | NA [4:0] | | | | | FSS lb | FSS [3:0] | | | | PXN lb | Mode | CS [1:0] | | GBED DIS | LVDS OFF | UART OFF | EEPR lb | CRC[6:0] | | | | | | |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| | DATA2 | | | | | | | DATA3 | | | | | | | | DATA4 | | | | | | | DATA5 | | | |



**Figure 18. Read OTP Data Interpretation**

**Return to Normal Operation after Fail−Safe Mode**

Once a device detects one of the following status bits: TSD or CAP_UV or VBB_LOW or DIMERR or TIMEOUT, the device enters the fail−safe mode (see Operating Modes section). To leave this mode, the superior system shall read out the REG 0x10 (see Table 45) and/or handle the error if required.

The device enters FAIL−SAFE OTP mode when DIMERR or TIMEOUT appears. When TIMEOUT is set and this mode is entered, switches are set according to the OTP memory values. If the OTP memory is not zapped, the switches are switched OFF. Once the error status bit is cleared, the switches remain unchanged. When DIMERR is set and this mode is entered, switches operation is unaffected.

The device enters FAIL−SAFE OPEN mode when TSD or CAP_UV or VBB_LOW appears. In this mode, the switches are automatically switched OFF. Once the error status bit is cleared, the switches are set according to the values in REG 0x00 (see Table 27).

The TSD/CAP_UV/VBB_LOW group of bits (hardware fail) have higher priority to the DIMERR/TIMEOUT group of bits (application fail). When these two groups appear at the same time, the device enters the FAIL−SAFE OPEN mode.



Figure 19. FAIL−SAFE Modes

**Power Up and Down Sequences**



**Figure 20. Power−up Sequence with 10 nF at ADC2/ADR Pin**



**Figure 21. Power−down Sequence with 10 nF at ADC2/ADR Pin**

**Example Flow Chart Diagram for the Normal Operational Mode**



**Figure 22. Normal Operation Mode Flow Chart Diagram**

The main loop should consist of checking all status bits and handling them if necessary. Set a refresh rate for common headlamp lighting functions (e.g. High beam) as well as fulfill watchdog timeout. The MCU should calculate all ON/OFF/TR values within this time and send broadcast MAPENA (see Table 64) frame once the values are sent into devices.

**Flow Chart after POR**



**Figure 23. Flow Chart Diagram after POR**

The diagram above is an automatic flow after each POR. A device might end up in either CONFIG or NORMAL or NO_CRC mode according to zapped OTP bits.

A new device will end up in CONFIG mode, because OTP bits are not zapped. An address is set by either Auto−addressing process or by Multi−level addressing using a voltage divider or zapped in the OTP memory.

**Multi−level Addressing Procedure with Long Time Delay at ADC2/ADR Pin**

The following flow chart is valid for the repeater−slave and slaves cluster, where the repeater−slave communicates through CAN−PHY layer and slaves are connected via local M−LVDS bus.

Init

Send CF 13 as broadcast — Force the normal mode for the first device

Send CF 14 as broadcast — Reset the first device from NMD

The device read the ADC value again and set correct address

Set the PMC for the first device CF7 — Set the first device to repeater−slave mode

Send CF 13 as broadcast — Force the normal mode for other devices

Send CF 14 as broadcast — Reset the other devices from NMD

All devices have correct address

**Figure 24. Multi−level Addressing Procedure with Long Time Delay at ADC2/ADR Pin**

**EEPROM Write and Read Operations**



**Figure 25. EEPROM Write Operation**



**Figure 26. EEPROM Read Operation**

**ON Semiconductor®**

**SSOP36 EP**
CASE 940AB
ISSUE A

DATE 19 JAN 2016

SCALE 1:1

| △ | 0.20 | C | A–B |
4X

**D**

DETAIL B

**D**

36    19

**A**

**E1**

**E**

PIN 1
REFERENCE

1    18

**e**

**B**

36X
| △ | 0.25 | C |

36X **b**

| ⊕ | 0.25 Ⓜ | T | AⓈ | BⓈ |

**TOP VIEW**

**X**

X = A or B

**e/2**

**DETAIL B**

**H**

**A**    **A2**

| △ | 0.10 | C |
36X

**A1**

**C** SEATING PLANE

**SIDE VIEW**

NOTE 6

**h**

DETAIL A

**h**

**c**

**END VIEW**

**D2**

**E2**

**BOTTOM VIEW**

**M1**

GAUGE PLANE

**M**

**L2**

**C** SEATING PLANE

36X **L**

**DETAIL A**

**SOLDERING FOOTPRINT**

5.90

36X
1.06

4.10

10.76

1

0.50
PITCH

36X
0.36

DIMENSIONS: MILLIMETERS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THE b DIMENSION AT MMC.
4. DIMENSION b SHALL BE MEASURED BE-TWEEN 0.10 AND 0.25 FROM THE TIP.
5. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. DIMENSIONS D AND E1 SHALL BE DETERMINED AT DATUM H.
6. THIS CHAMFER FEATURE IS OPTIONAL. IF IT IS NOT PRESENT, A PIN ONE IDENTIFIER MUST BE LOACATED WITHIN THE INDICAT-ED AREA.

| DIM | MILLIMETERS | |
| | MIN | MAX |
| --- | --- | --- |
| A | --- | 2.65 |
| A1 | --- | 0.10 |
| A2 | 2.15 | 2.60 |
| b | 0.18 | 0.30 |
| c | 0.23 | 0.32 |
| D | 10.30 BSC | |
| D2 | 5.70 | 5.90 |
| E | 10.30 BSC | |
| E1 | 7.50 BSC | |
| E2 | 3.90 | 4.10 |
| e | 0.50 BSC | |
| h | 0.25 | 0.75 |
| L | 0.50 | 0.90 |
| L2 | 0.25 BSC | |
| M | 0° | 8° |
| M1 | 5° | 15° |

**GENERIC
MARKING DIAGRAM***

XXXXXXXXXX
XXXXXXXXXX
XXXXXXXXXX
AWLYYWWG

| XXXX | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb–Free Package |

*This information is generic. Please refer to device data sheet for actual part marking.

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## ADDITIONAL INFORMATION

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